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# BTS 5441G

## Smart High-Side Power Switch

## PROFET

## Four Channels, 25 mΩ

Automotive Power

Never stop thinking.

**Smart High-Side Power Switch**
**PROFET**

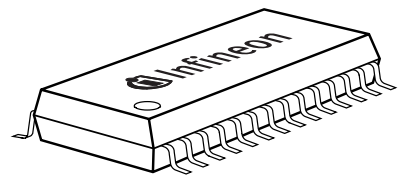
**BTS 5441G**

## Product Summary

**The BTS 5441G is a four channel high-side power switch in P-DSO-28-19 package providing embedded protective functions including ReverSave™.**

**The power transistor is built by a N-channel vertical power MOSFET with charge pump. The device is monolithically integrated in Smart SIPMOS technology.**

**P-DSO-28-19**




| | | |
|---|---|---|
| Operating voltage | $V_{bb(on)}$ | 4.5 .. 28 V |
| Over-voltage protection | $V_{bb(AZ)}$ | 41 V |
| On-State resistance | $R_{DS(ON)}$ | 25 mΩ |
| Nominal load current (one channel active) | $I_{L(nom)}$ | 5.6 A |
| Current limitation | $I_{L(LIM)}$ | 40 A |
| Current limitation repetitive | $I_{L(SCr)}$ | 9.5 A |
| Stand-by current for whole device with load | $I_{bb(OFF)}$ | 15 µA |

## Basic Features

- Very low standby current
- 3.3 V and 5 V compatible logic pins
- Improved electromagnetic compatibility (EMC)
- Stable behavior at under-voltage
- Logic ground independent from load ground
- Secure load turn-off while logic ground disconnected
- Optimized inverse current capability

| Type | Ordering Code | Package |
|---|---|---|
| BTS 5441G | Q67060-S6150 | P-DSO-28-19 |

## Protective Functions

- ReverSave™, channels switch on in case of reverse polarity
- Reverse battery protection without external components
- Short circuit protection
- Over-load protection
- Multi-step current limitation
- Thermal shutdown with restart
- Thermal restart at reduced current limitation
- Over-voltage protection without external resistor
- Loss of ground protection
- Electrostatic discharge protection (ESD)

## Diagnostic Functions

- Enable function for diagnosis pins (IS1 .. IS4)
- Proportional load current sense signal by current source
- Open load detection in ON-state by load current sense
- Open load detection in OFF-state by voltage source
- Feedback on over-temperature and current limitation in ON-state

## Applications

- µC compatible high-side power switch with diagnostic feedback for 12 V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

# 1 Overview

The BTS 5441G is a four channel high-side power switch (four times 25 mΩ) in P-DSO-28-19 package providing embedded protective functions including ReverSave.

ReverSave is a protection feature that causes the power transistors to switch on in case of reverse polarity. As a result, the power dissipation is reduced to almost forward condition.

The Enhanced IntelliSense pins IS1 to IS4 provide a sophisticated diagnostic feedback signal including current sense function and open load in off state. The diagnosis signals can be switched on and off by the sense enable pins SENA and SENB.

Integrated ground resistors as well as integrated resistors at each input pin (IN1, IN2, IN3, IN4, SEN) reduce external components to a minimum.

The power transistor is built by a N-channel vertical power MOSFET with charge pump. The inputs are ground referenced CMOS compatible. The device is built by two dual channel chips, each monolithically integrated in Smart SIPMOS technology.

## 1.1 Block Diagram

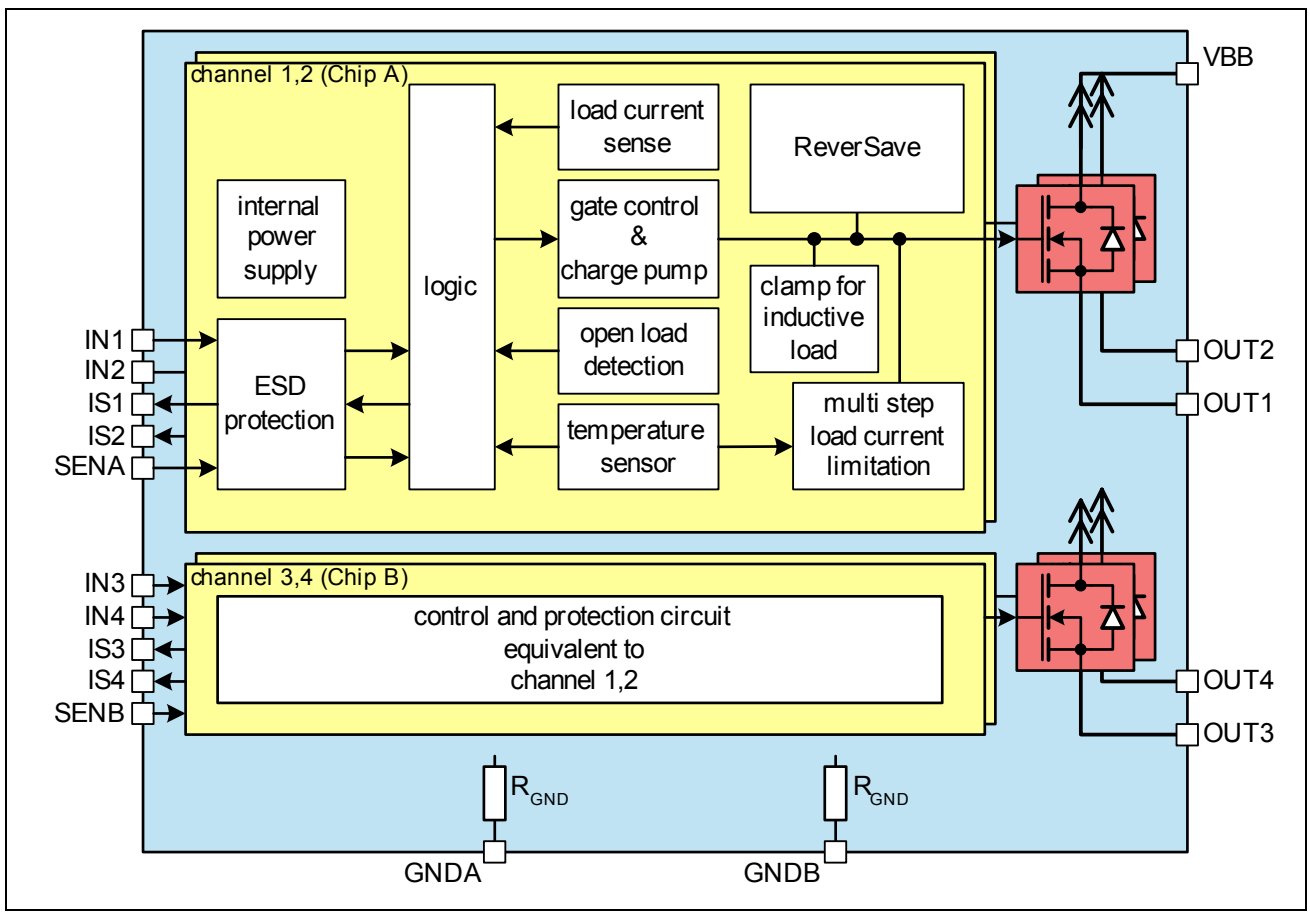



**Figure 1 Block Diagram**

## 1.2 Terms

Following figure shows all terms used in this data sheet.

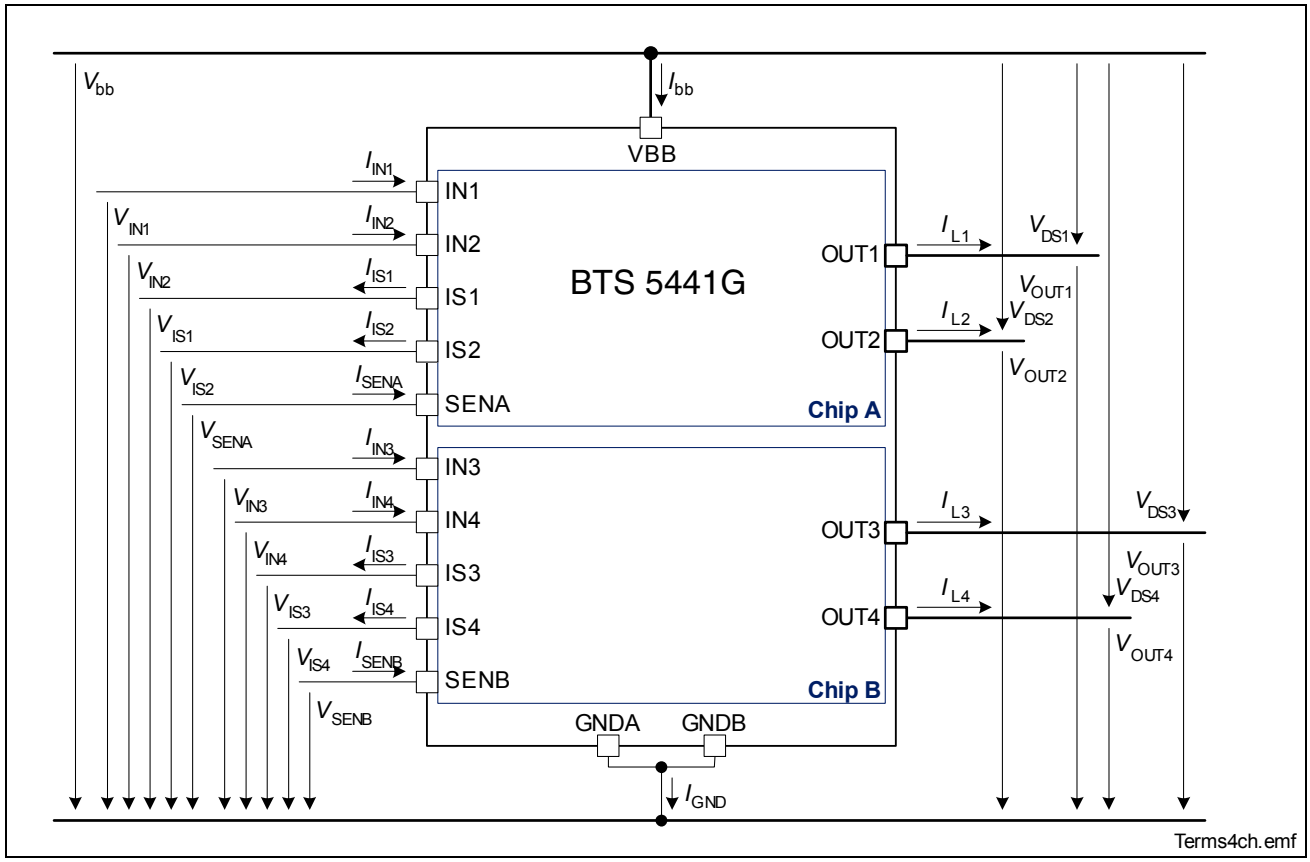



**Figure 2 Terms**

Channel related symbols without channel number are valid for each channel separately.

# 2 Pin Configuration

## 2.1 Pin Assignment BTS 5441G

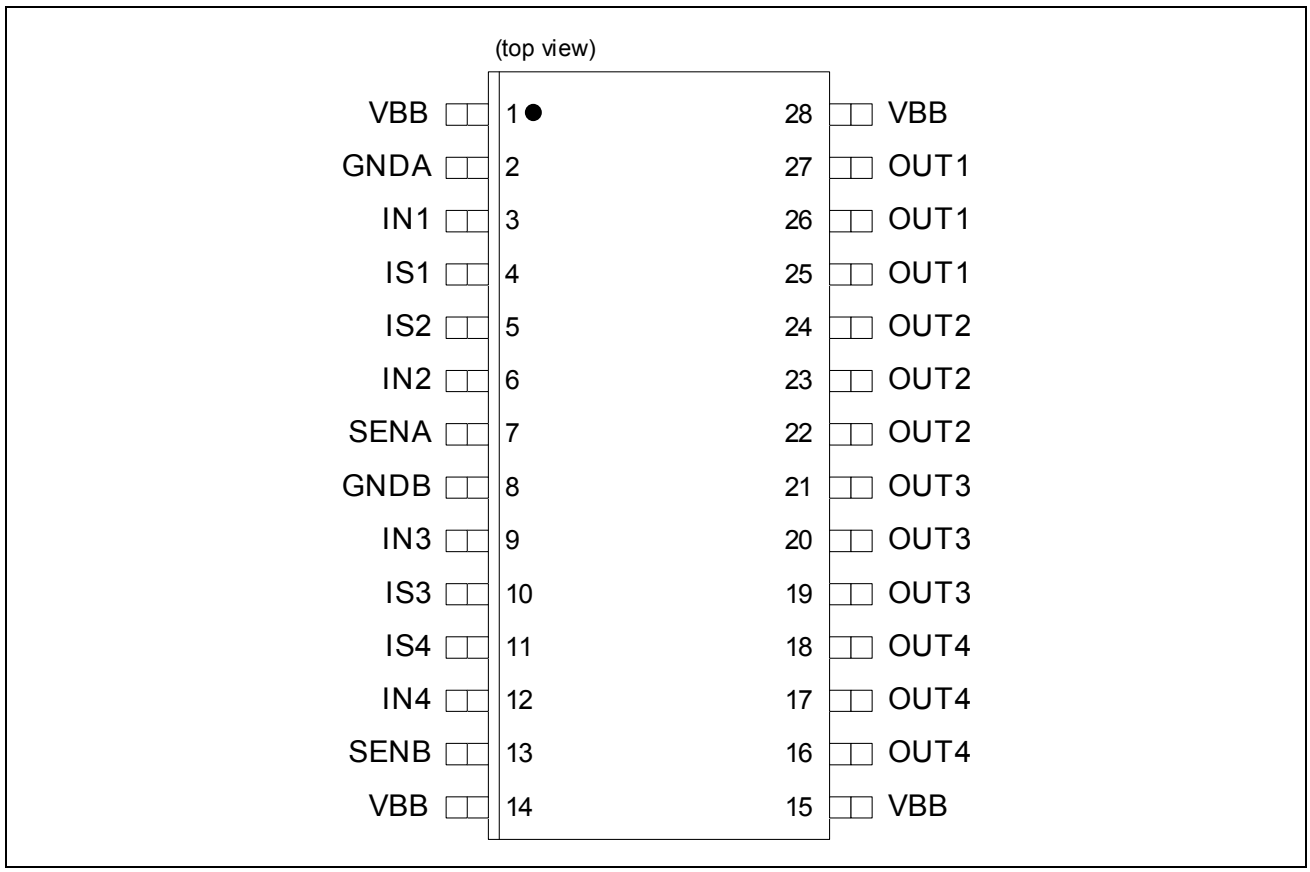



**Figure 3 Pin Configuration P-DSO-28-19**

## 2.2 Pin Definitions and Functions

| Pin | Symbol | I/O | Function |
|---|---|---|---|
| 3 | IN1 | I | Input signal for channel 1 |
| 6 | IN2 | I | Input signal for channel 2 |
| 9 | IN3 | I | Input signal for channel 3 |
| 12 | IN4 | I | Input signal for channel 4 |
| 4 | IS1 | O | Diagnosis output signal channel 1 |
| 5 | IS2 | O | Diagnosis output signal channel 2 |
| 10 | IS3 | O | Diagnosis output signal channel 3 |
| 11 | IS4 | O | Diagnosis output signal channel 4 |
| 7 | SENA | I | Sense Enable input for channel 1&2 |

| Pin | Symbol | I/O | Function |
|---|---|---|---|
| 13 | SENB | I | Sense Enable input for channel 3&4 |
| 25, 26, 27 | OUT1 | O | Protected high-side power output channel 1 |
| 22, 23, 24 | OUT2 | O | Protected high-side power output channel 2 |
| 19, 20, 21 | OUT3 | O | Protected high-side power output channel 3 |
| 16, 17, 18 | OUT4 | O | Protected high-side power output channel 4 |
| 2 | GNDA | - | Ground connection chip A |
| 8 | GNDB | - | Ground connection chip B |
| 1, 14, 15, 28 | VBB | - | Positive power supply for logic supply as well as output power supply |

# 3 Electrical Characteristics

## 3.1 Maximum Ratings

Stresses above the ones listed here may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

$T_j$ = 25 °C (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| **Supply Voltage** | | | | | | |
| 3.1.1 | Supply voltage | $V_{bb}$ | -16 | 28 | V | |
| 3.1.2 | Supply voltage for full short circuit protection (single pulse) ($T_j$ = -40°C .. 150°C) | $V_{bb(SC)}$ | 0 | 28 | V | $L$ = 8 µH<br>$R$ = 0.2 Ω [1] |
| 3.1.3 | Voltage at power transistor | $V_{DS}$ | - | 52 | V | |
| 3.1.4 | Supply Voltage for Load Dump protection | $V_{bb(LD)}$ | - | 53 | V | $R_I$ = 2 Ω [2]<br>$R_L$ = 6.8 Ω |
| **Power Stages** | | | | | | |
| 3.1.5 | Load current | $I_L$ | - | $I_{L(LIM)}$ | A | [3] |
| 3.1.6 | Maximum energy dissipation per channel (single pulse) | $E_{AS}$ | - | 0.26 | J | [4]<br>$I_{L(0)}$ = 5.5 A<br>$T_{j(0)}$ = 150°C |
| 3.1.7 | Total power dissipation (DC) for whole device | $P_{tot}$ | - | 2.0 | W | [5]<br>$T_a$ = 85 °C<br>$T_j \leq$ 150 °C |
| **Logic Pins** | | | | | | |
| 3.1.8 | Voltage at input pin | $V_{IN}$ | -5<br>-16 | 19 | V | <br>$t \leq$ 2 min |
| 3.1.9 | Current through input pin | $I_{IN}$ | -2.0<br>-8.0 | 2.0 | mA | <br>$t \leq$ 2 min |
| 3.1.10 | Voltage at sense enable pin | $V_{SEN}$ | -5<br>-16 | 19 | V | <br>$t \leq$ 2 min |
| 3.1.11 | Current through sense enable pin | $I_{SEN}$ | -2.0<br>-8.0 | 2.0 | mA | <br>$t \leq$ 2 min |
| 3.1.12 | Current through sense pin | $I_{IS}$ | -25 | 10 | mA | |

$T_j$ = 25 °C (unless otherwise specified)

| Pos. | Parameter | Symbol | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | min. | max. | | |
| **Temperatures** | | | | | | |
| 3.1.13 | Junction temperature | $T_j$ | -40 | 150 | °C | |
| 3.1.14 | Dynamic temperature increase while switching | $\Delta T_j$ | - | 60 | °C | |
| 3.1.15 | Storage temperature | $T_{stg}$ | -55 | 150 | °C | |
| **ESD Susceptibility** | | | | | | |
| 3.1.16 | ESD susceptibility HBM | $V_{ESD}$ | | | kV | according to EIA/JESD 22-A 114B |
| | IN, SEN | | -1 | 1 | | |
| | IS | | -2 | 2 | | |
| | OUT | | -4 | 4 | | |

1) R and L describe the complete circuit impedance including line, contact and generator impedances

2) Load Dump is specified in ISO 7637, $R_I$ is the internal resistance of the Load Dump pulse generator

3) Current limitation is a protection feature. Operation in current limitation is considered as “outside” normal operating range. Protection features are not designed for continuous repetitive operation.

4) Pulse shape represents inductive switch off: $I_L(t) = I_L(0) * (1 - t / t_{peak})$; $0 < t < t_{peak}$

5) Device mounted on PCB (50 mm x 50 mm x 1.5mm epoxy, FR4) with 6 $cm^2$ copper heatsinking area (one layer, 70 µm thick) for $V_{bb}$ connection. PCB is vertical without blown air.

# 4 Block Description and Electrical Characteristics

## 4.1 Power Stages

The power stages are built by a N-channel vertical power MOSFET (DMOS) with charge pump.

### 4.1.1 Output On-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature $T_j$. **Figure 4** shows these dependencies for the typical on-state resistance. The on-state resistance in reverse polarity mode is described in **Section 4.2.2**.

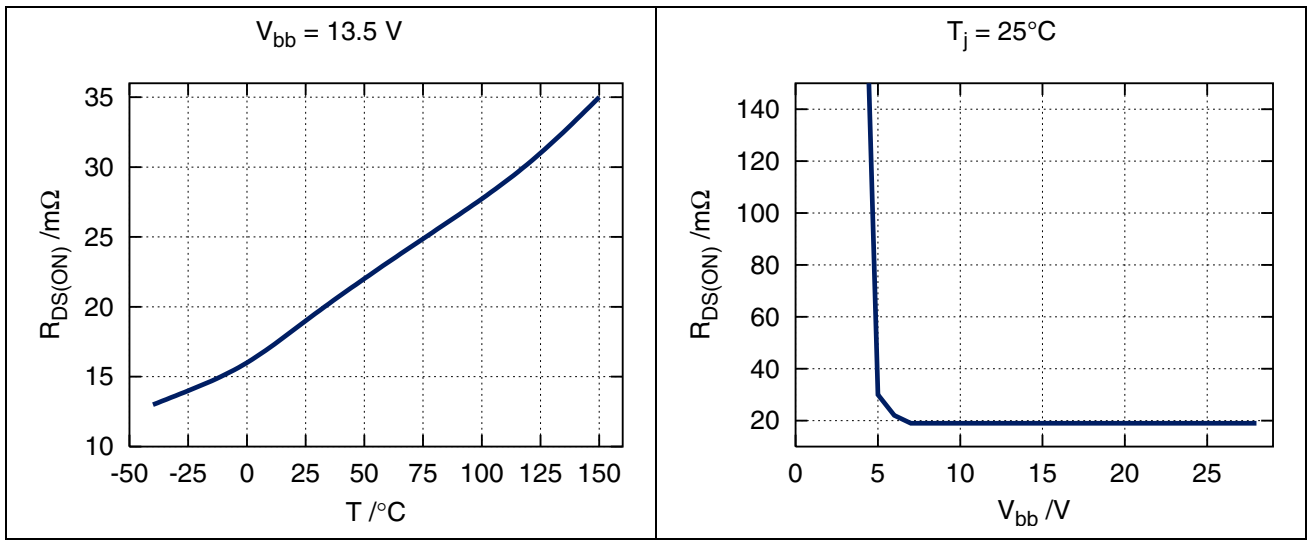



**Figure 4 Typical On-State Resistance**

### 4.1.2 Input Circuit

**Figure 5** shows the input circuit of the BTS 5441G. There is an integrated input resistor that makes external components obsolete. The current source to ground ensures that the device switches off in case of open input pin. The zener diode protects the input circuit against ESD pulses.

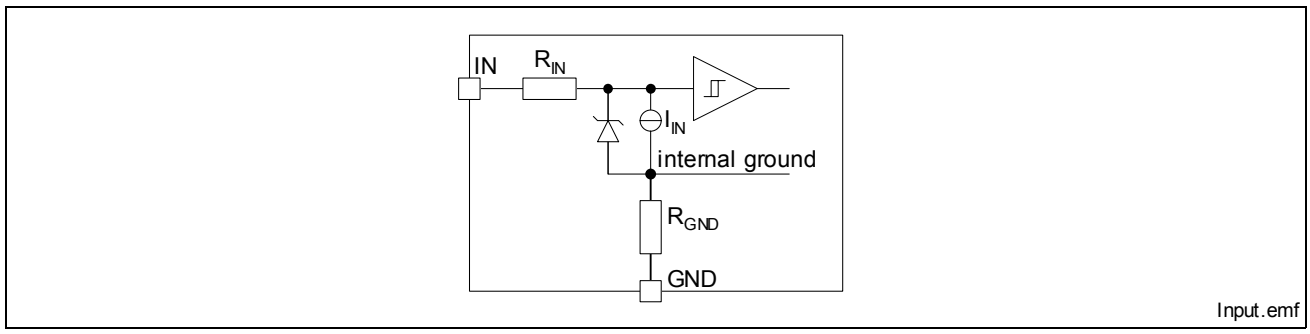



**Figure 5 Input Circuit (IN1 .. IN4)**

A high signal at the input pin causes the power DMOS to switch on with a dedicated slope, which is optimized in terms of EMC emission.

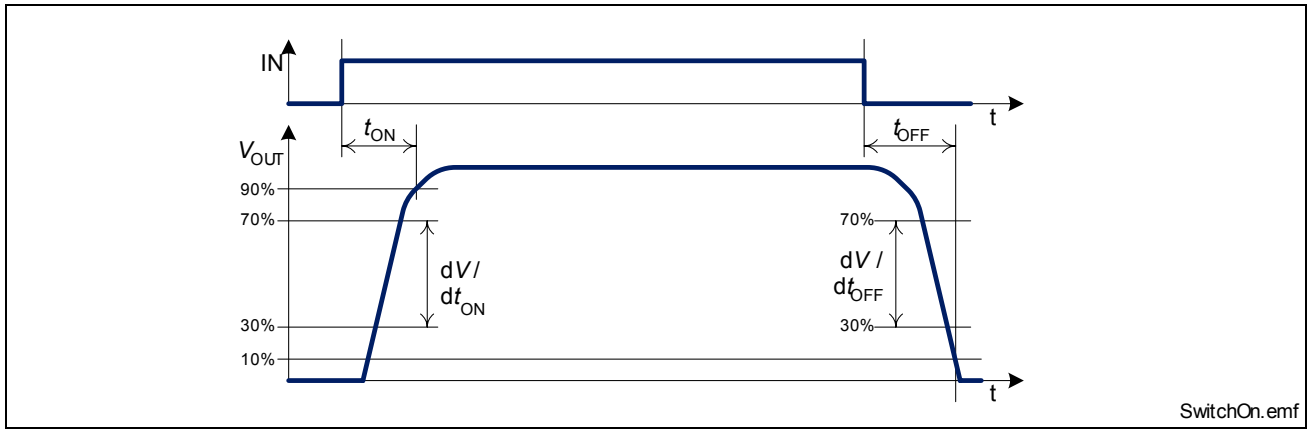



**Figure 6 Switching a Load (resistive)**

### 4.1.3 Inductive Output Clamp

When switching off inductive loads with high-side switches, the potential at pin OUT drops below ground potential, because the inductance intends to continue driving the current.

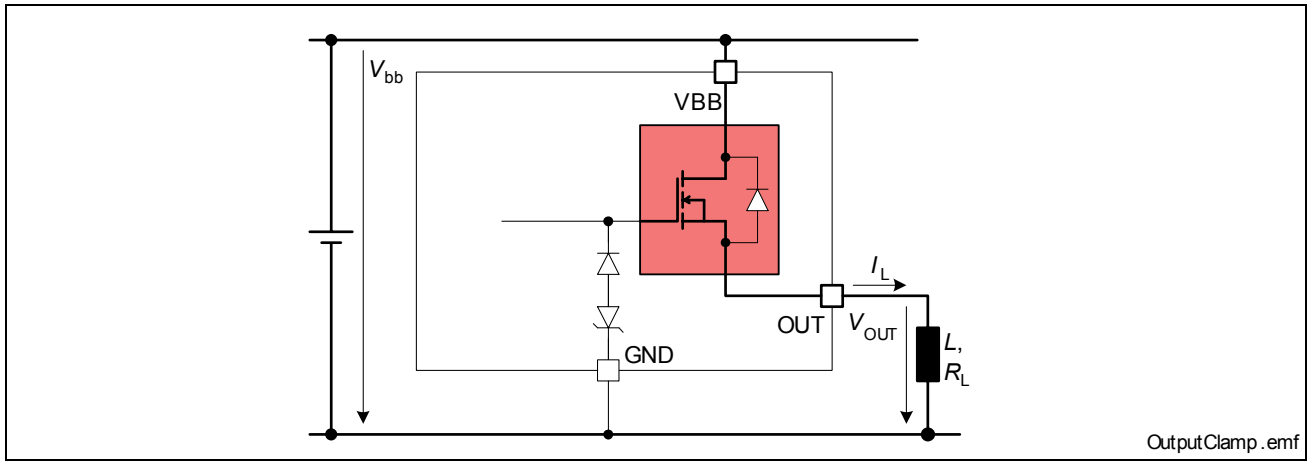



**Figure 7 Output Clamp (OUT1 .. OUT4)**

To prevent destruction of the device, there is a voltage clamp mechanism implemented that keeps that negative output voltage at a certain level ($V_{OUT(CL)}$). See **Figure 7** and **Figure 8** for details. Nevertheless, the maximum allowed load inductance is limited.

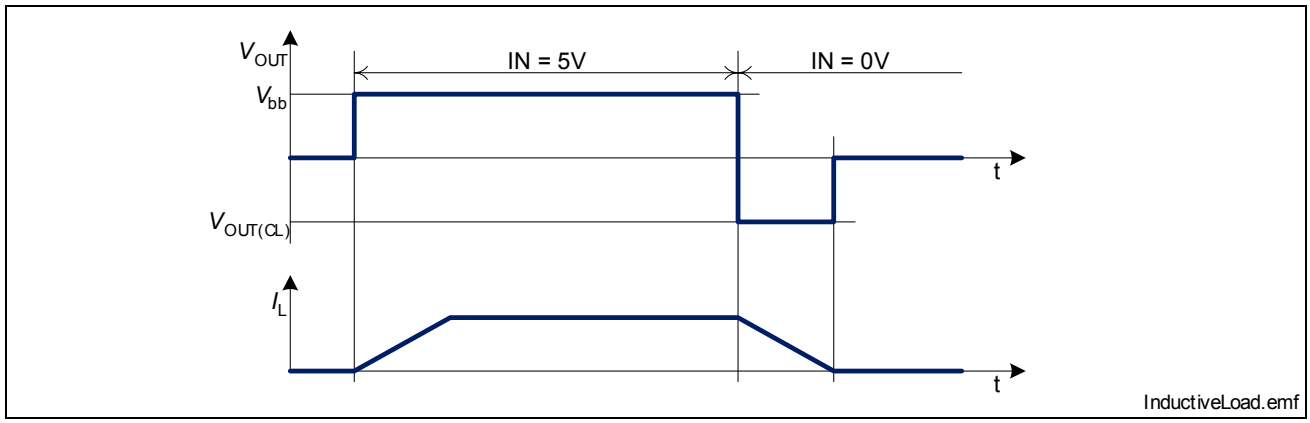



**Figure 8 Switching an Inductance**

## Maximum Load Inductance

While demagnetization of inductive loads, energy has to be dissipated in the BTS 5441G. This energy can be calculated with following equation:

$$E = (V_{bb} + |V_{OUT(CL)}|) \cdot \left[ \frac{|V_{OUT(CL)}|}{R_L} \cdot \ln\left(1 + \frac{R_L \cdot I_L}{|V_{OUT(CL)}|}\right) + I_L \right] \cdot \frac{L}{R_L}$$

Following equation simplifies under the assumption of $R_L = 0$:

$$E = \frac{1}{2} L I_L^2 \cdot \left(1 + \frac{V_{bb}}{|V_{OUT(CL)}|}\right)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See **Figure 9** for the maximum allowed energy dissipation.

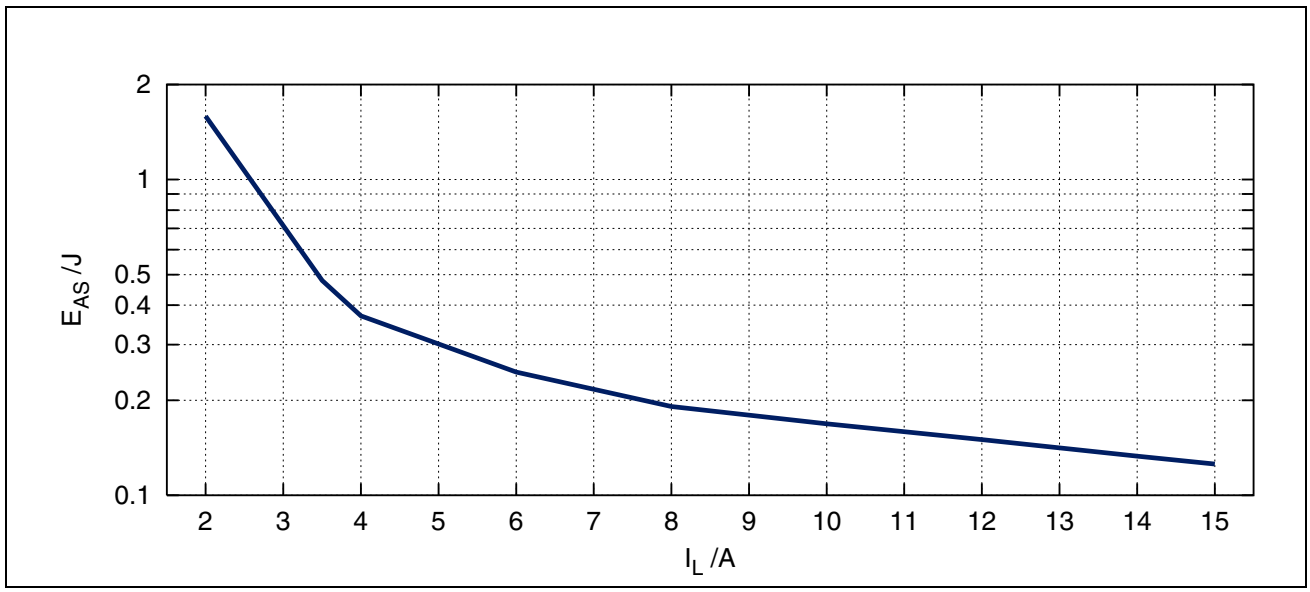



**Figure 9 Maximum energy dissipation single pulse, $T_{j,Start}$ = 150°C**

### 4.1.4 Electrical Characteristics

$V_{bb}$ = 9 V to 16 V, $T_j$ = -40 °C to +150 °C (unless otherwise specified)
typical values: $V_{bb}$ = 13.5 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **General** | | | | | | | |
| 4.1.1 | Operating voltage | $V_{bb}$ | 4.5 | | 28 | V | $V_{IN}$ = 4.5 V<br>$R_L$ = 12 Ω<br>$V_{DS}$ < 0.5 V |
| 4.1.2 | Operating current<br>one channel<br>all channels | $I_{GND}$ | | <br>1.5<br>5.6 | <br>4<br>16 | mA | $V_{IN}$ = 5 V |
| 4.1.3 | Stand-by current for whole device with load | $I_{bb(OFF)}$ | | <br><br><br>10 | <br><br><br>15<br>15<br>40 | µA | $V_{IN}$ = 0 V<br>$V_{SEN}$ = 0 V<br>$V_{OUT}$ < $V_{OUT(OL)}$<br>$T_j$ = 25°C<br>$T_j$ = 105°C [1]<br>$T_j$ = 150°C |
| **Output characteristics** | | | | | | | |
| 4.1.4 | On-State resistance per channel | $R_{DS(ON)}$ | | <br>19<br>35 | <br>25<br>48 | mΩ | $I_L$ = 5 A<br>$T_j$ = 25 °C<br>$T_j$ = 150 °C |
| 4.1.5 | Output voltage drop limitation at small load currents | $V_{DS(NL)}$ | | 40 | | mV | $I_L$ < 0.5 A |
| 4.1.6 | Nominal load current per channel<br>one channel active<br>four channels active | $I_{L(nom)}$ | <br>5.6<br>3.2 | | | A | $T_a$ = 85 °C<br>$T_j \leq$ 150 °C [2] [3] |
| 4.1.7 | Output clamp | $V_{OUT(CL)}$ | -17 | -14.5 | -12 | V | $I_L$ = 40 mA |
| 4.1.8 | Output leakage current per channel | $I_{L(OFF)}$ | | 1.5 | 8 | µA | $V_{IN}$ = 0 V |
| 4.1.9 | Inverse current capability | $-I_{L(inv)}$ | | 3 | | A | [1] |

$V_{bb}$ = 9 V to 16 V, $T_j$ = -40 °C to +150 °C (unless otherwise specified)
typical values: $V_{bb}$ = 13.5 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Thermal Resistance** | | | | | | | |
| 4.1.10 | Junction to case | $R_{thjc}$ | | | 30 | K/W | 1) |
| 4.1.11 | Junction to ambient<br>one channel active<br>all channels active | $R_{thja}$ | | <br>40<br>32 | | K/W | 1) 2) |
| **Input characteristics** | | | | | | | |
| 4.1.12 | Input resistance | $R_{IN}$ | 2.3 | 3.6 | 5.3 | kΩ | |
| 4.1.13 | L-input level | $V_{IN(L)}$ | -0.3 | | 1.0 | V | |
| 4.1.14 | H-input level | $V_{IN(H)}$ | 2.6 | | 17 | V | |
| 4.1.15 | Input hysteresis | $\Delta V_{IN}$ | | 0.4 | | V | 1) |
| 4.1.16 | L-input current | $I_{IN(L)}$ | 3 | | 75 | µA | $V_{IN}$ = 0.4 V |
| 4.1.17 | H-input current | $I_{IN(H)}$ | 10 | 38 | 75 | µA | $V_{IN}$ = 5 V |
| **Timings** | | | | | | | |
| 4.1.18 | Turn-on time to 90% $V_{bb}$ | $t_{ON}$ | | 120 | 250 | µs | $R_L$ = 12 Ω<br>$V_{bb}$ = 13.5 V |
| 4.1.19 | Turn-off time to 10% $V_{bb}$ | $t_{OFF}$ | | 135 | 250 | µs | $R_L$ = 12 Ω<br>$V_{bb}$ = 13.5 V |
| 4.1.20 | slew rate 30% to 70% $V_{bb}$ | $dV/dt_{ON}$ | 0.1 | 0.25 | 0.5 | V/µs | $R_L$ = 12 Ω<br>$V_{bb}$ = 13.5 V |
| 4.1.21 | slew rate 70% to 30% $V_{bb}$ | $-dV/dt_{OFF}$ | 0.1 | 0.25 | 0.5 | V/µs | $R_L$ = 12 Ω<br>$V_{bb}$ = 13.5 V |

1) Not subject to production test, specified by design

2) Device mounted on PCB (50 mm x 50 mm x 1.5mm epoxy, FR4) with 6 $cm^2$ copper heatsinking area (one layer, 70 µm thick) for $V_{bb}$ connection. PCB is vertical without blown air.

3) Not subject to production test, parameters are calculated from $R_{DS(ON)}$ and $R_{th}$

*Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing.*

## 4.2 Protection Functions

The device provides embedded protective functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are neither designed for continuous nor repetitive operation.

### 4.2.1 Over-Load Protection

The load current $I_{OUT}$ is limited by the device itself in case of over-load or short circuit to ground. There are two steps of current limitation which are selected automatically depending on the voltage $V_{DS}$ across the power DMOS. Please note that the voltage at the OUT pin is $V_{bb}$ - $V_{DS}$. Please refer to the following figure for details.

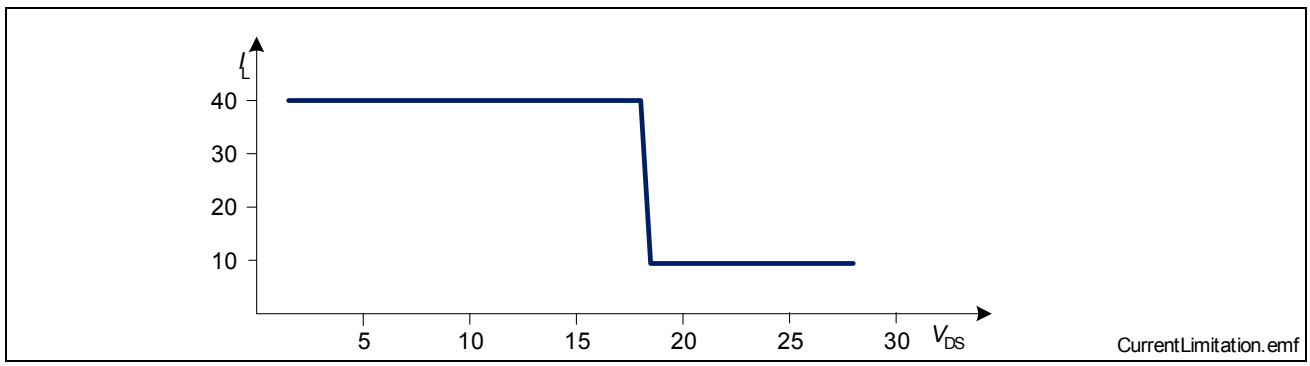



**Figure 10 Current Limitation (minimum values)**

Current limitation is realized by increasing the resistance of the device which leads to rapid temperature rise inside. A temperature sensor for each channel causes an over-heated channel to switch off to prevent destruction. After cooling down with thermal hysteresis, the channel switches on again. Please refer to **Figure 11** for details.

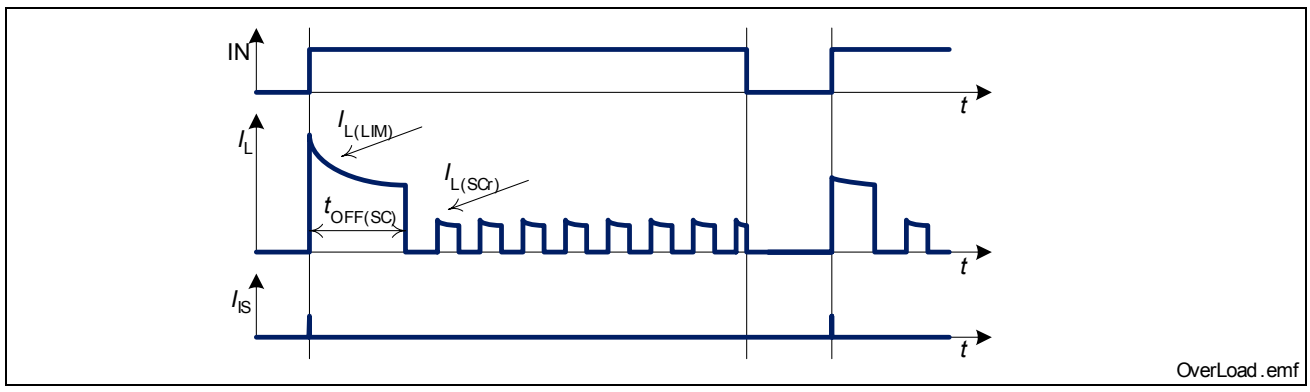



**Figure 11 Shut Down by Over-Temperature**

In short circuit condition, the load current is initially limited to $I_{L(LIM)}$. After thermal restart, the current limitation level is reduced to $I_{L(SCr)}$. The current limitation level is reset to $I_{L(LIM)}$ by switching off the device ($V_{IN}$ = 0 V).

### 4.2.2 Reverse Polarity Protection

The BTS 5441G is ReverSave. This means, no additional components are required to protect the device in reverse polarity mode. In case of reverse polarity, the device switches on the power transistor to almost forward condition, so the power dissipation is reduced. Additional power is dissipated by the integrated ground resistor. Use following formula for estimation of power dissipation $P_{diss(rev)}$ in reverse polarity mode.

$$P_{diss(rev)} = \left( R_{ON(rev)} \cdot \sum_{\text{all channels}} I_L^2 \right) + 2 \frac{V_{bb}^2}{R_{GND}}$$

The reverse current through the power transistors has to be limited by the connected loads. The current trough sense pins IS1 to IS4 has to be limited (please refer to maximum ratings on **Page 9**). The temperature protection is not active during reverse polarity.

### 4.2.3 Over-Voltage Protection

In addition to the output clamp for inductive loads as described in **Section 4.1.3**, there is a clamp mechanism for over-voltage protection. Because of the integrated ground resistor, over-voltage protection does not require external components.

As shown in **Figure 12**, in case of supply voltages greater than $V_{bb(AZ)}$, the power transistors switche on, and the voltage across logic part is clamped. As a result, the internal ground potential rises to $V_{bb}$ - $V_{bb(AZ)}$. Due to the ESD zener diodes, the potential at pin IN1, IN2 and SEN rises almost to that potential, depending on the impedance of the connected circuitry.

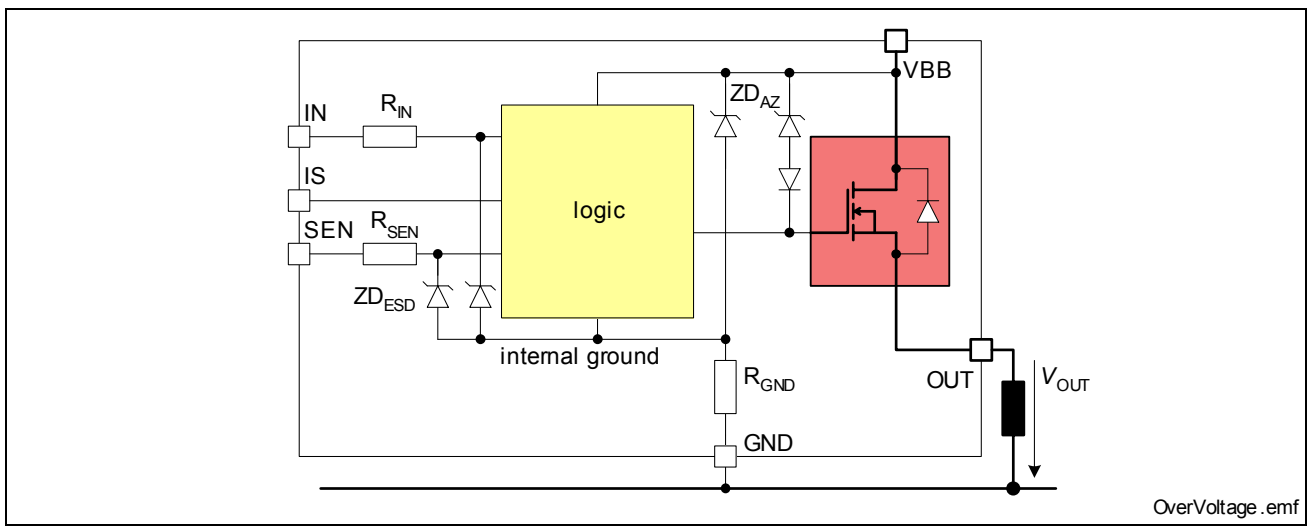



**Figure 12 Over-Voltage Protection**

### 4.2.4 Loss of Ground Protection

In case of complete loss of the device ground connections, but connected load ground, the BTS 5441G securely changes to or keeps in off state.

### 4.2.5 Electrical Characteristics

$V_{bb}$ = 9 V to 16 V, $T_j$ = -40 °C to +150 °C (unless otherwise specified)
typical values: $V_{bb}$ = 13.5 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Over-Load Protection** | | | | | | | |
| 4.2.1 | Load current limitation | $I_{L(LIM)}$ | 40 | | 55 | A | |
| 4.2.2 | Repetitive short circuit current limitation | $I_{L(SCr)}$ | | 9.5 | | A | $T_j = T_{j(SC)}$ 1) |
| 4.2.3 | Initial short circuit shut down time | $t_{OFF(SC)}$ | | 0.5 | | ms | $T_{jStart}$ = 25 °C 1) |
| 4.2.4 | Thermal shut down temperature | $T_{j(SC)}$ | 150 | 170 1) | | °C | |
| 4.2.5 | Thermal hysteresis | $\Delta T_j$ | | 7 | | K | 1) |
| **Reverse Battery** | | | | | | | |
| 4.2.6 | On-State resistance per channel in case of reverse polarity | $R_{ON(rev)}$ | | <br><br>30<br>50 | <br><br>35<br>70 | mΩ | $I_L$ = -3.5 A<br>$V_{bb}$ = -13.5 V<br>$T_j$ = 25 °C<br>$T_j$ = 150 °C |
| 4.2.7 | Reverse current through each GND pin | $-I_{GND}$ | | 70 | | mA | $V_{bb}$ = -13.5 V 1) |
| **Ground Circuit** | | | | | | | |
| 4.2.8 | Integrated Resistors in GND lines | $R_{GND}$ | 120 | 175 | 260 | Ω | |
| **Over-Voltage** | | | | | | | |
| 4.2.9 | Over-voltage protection | $V_{bb(AZ)}$ | 41 | 47 | 53 | V | $I_{bb}$ = 300 µA 2) |
| **Loss of GND** | | | | | | | |
| 4.2.10 | Output current while GND disconnected | $I_{L(GND)}$ | | | 1 | mA | $I_{IN}$ = 0 1) 3)<br>$I_{SEN}$ = 0<br>$I_{GND}$ = 0<br>$I_{IS}$ = 0 |

1) Not subject to production test, specified by design

2) Current is measured by ramping up $V_{bb}$ until test condition ($I_{bb}$) is reached

3) no connection at these pins

## 4.3 Diagnosis

For diagnosis purpose, the BTS 5441G provides an Enhanced IntelliSense signal at pins IS1 to IS4 that is enabled by pin SEN. The current sense signal $I_{IS}$, a proportional signal to the load current (ratio $k_{ILIS} = I_L / I_{IS}$), is provided as long as no failure mode occurs. In case of open load in OFF-state, the voltage $V_{IS(fault)}$ is fed to the diagnosis pin.

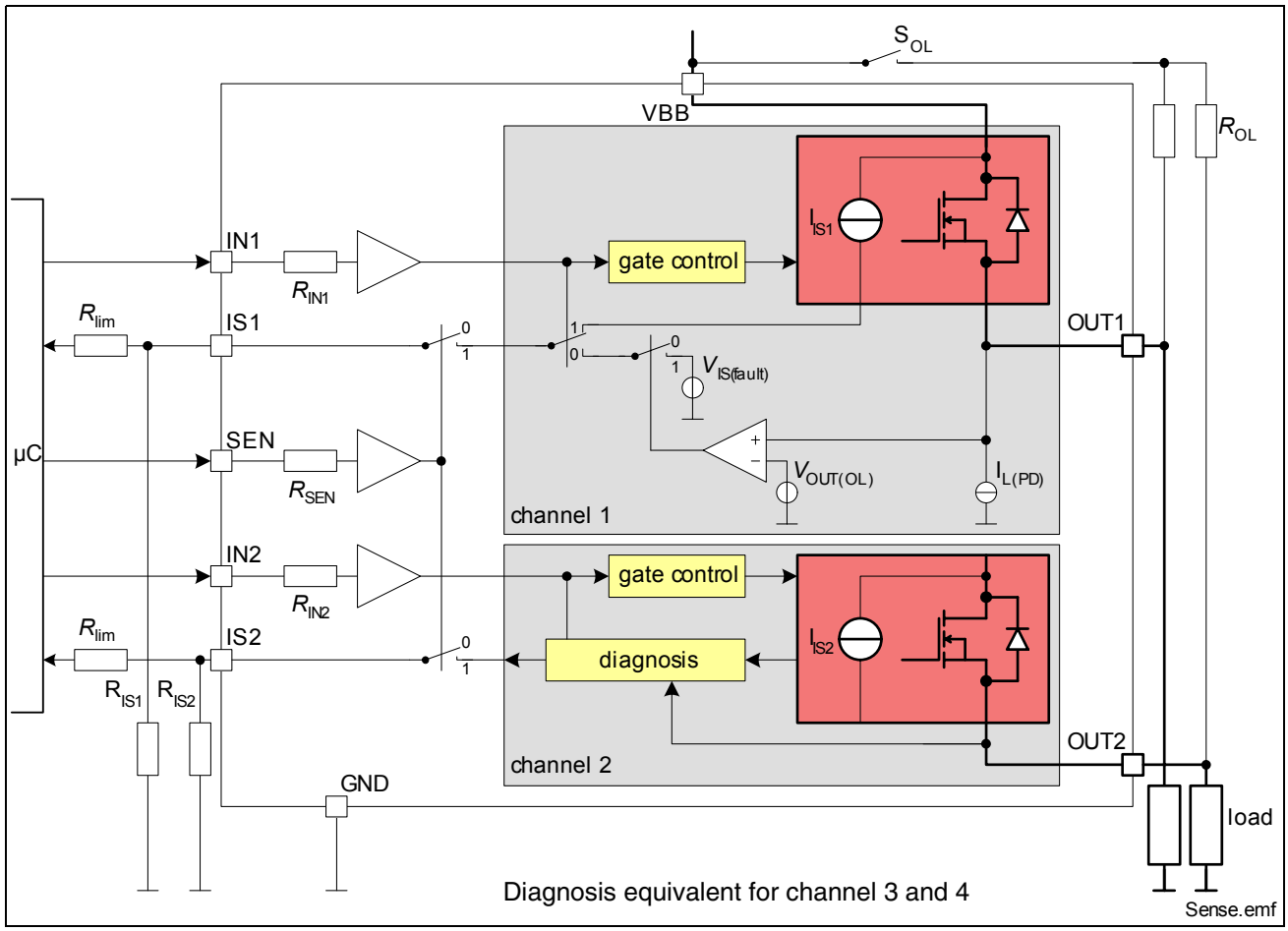



**Figure 13 Block Diagram: Diagnosis**

**Table 1 Truth Table**

| Operation Mode | Input Level | Output Level | Diagnostic Output | |
|---|---|---|---|---|
| | | | SEN = H | SEN = L |
| Normal Operation (OFF) | L | Z | Z | Z |
| Short Circuit to GND | | Z | Z | Z |
| Over-Temperature | | Z | Z | Z |
| Short Circuit to $V_{bb}$ | | $V_{bb}$ | $V_{IS} = V_{IS(fault)}$ | Z |
| Open Load | | < $V_{OUT(OL)}$<br>> $V_{OUT(OL)}$ | Z<br>$V_{IS} = V_{IS(fault)}$ | Z<br>Z |

**Table 1 Truth Table**

| Operation Mode | Input Level | Output Level | Diagnostic Output | |
|---|---|---|---|---|
| | | | SEN = H | SEN = L |
| Normal Operation (ON) | H | $\sim V_{bb}$ | $I_{IS} = I_L / k_{ILIS}$ | Z |
| Current Limitation | | $< V_{bb}$ | Z | Z |
| Short Circuit to GND | | ~GND | Z | Z |
| Over-Temperature | | Z | Z | Z |
| Short Circuit to $V_{bb}$ | | $V_{bb}$ | $I_{IS} < I_L / k_{ILIS}$ | Z |
| Open Load | | $\sim V_{bb}$ | Z | Z |

L = Low Level, H = High Level, Z = high impedance, potential depends on leakage currents and external circuit

### 4.3.1 ON-State Diagnosis

The standard diagnosis signal is a current sense signal proportional to the load current. The accuracy of the ratio ($k_{ILIS} = I_L / I_{IS}$) depends on the temperature. Please refer to **Figure 14** for details. Usually a resistor $R_{IS}$ is connected to the current sense pin. It is recommended to use sense resistors $R_{IS} > 500\ \Omega$. A typical value is 4.7 kΩ

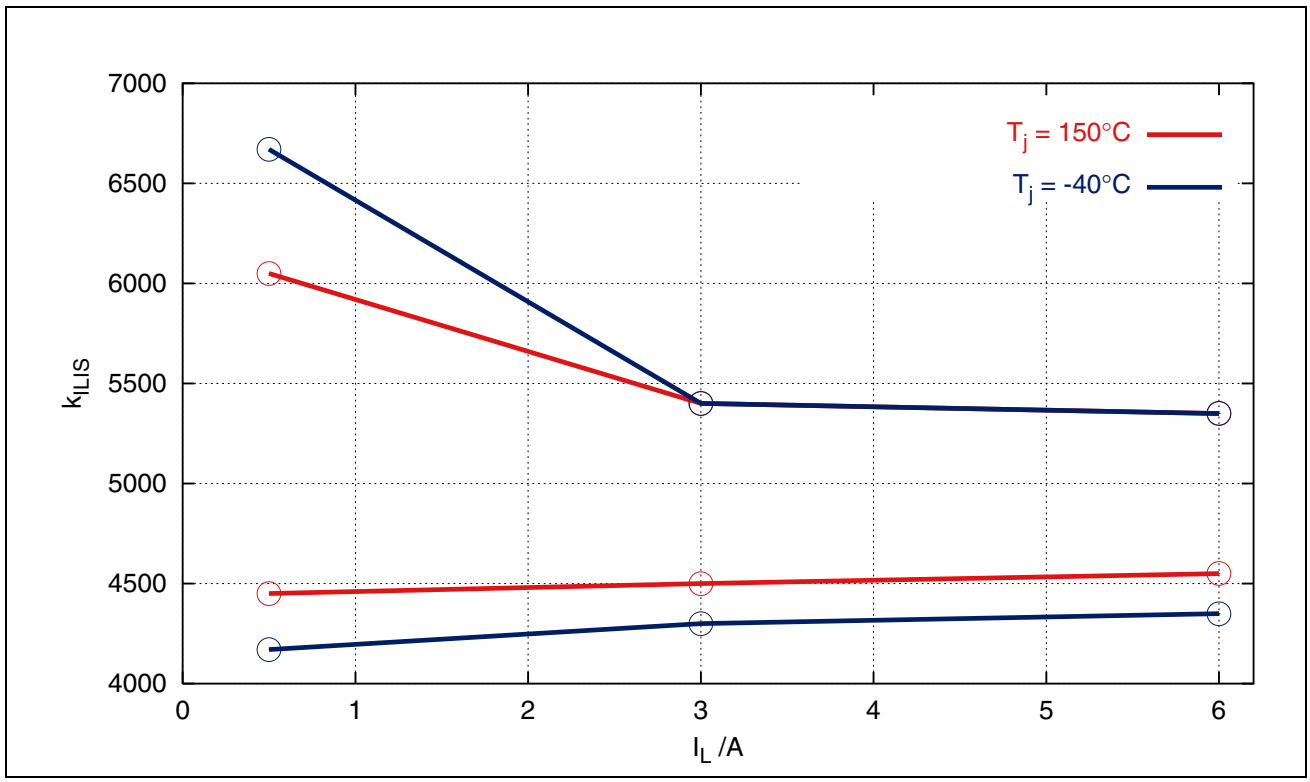



**Figure 14 Current sense ratio $k_{ILIS}$ [1)]**

1) The curves show the behavior based on characterization data. The marked points are guaranteed in this Data Sheet in **Section 4.3.4** (Position **4.3.7**).

In case of over-current as well as over-temperature, the current sense signal is switched off. As a result, one threshold is enough to distinguish between normal and faulty operation. Open load and over-load can be differentiated by switching off the channel and using open-load detection in off-state.

Details about timings between the diagnosis signal $I_{IS}$ and the output voltgage $V_{OUT}$ and the load current $I_L$ in ON-state can be found in **Figure 15**.

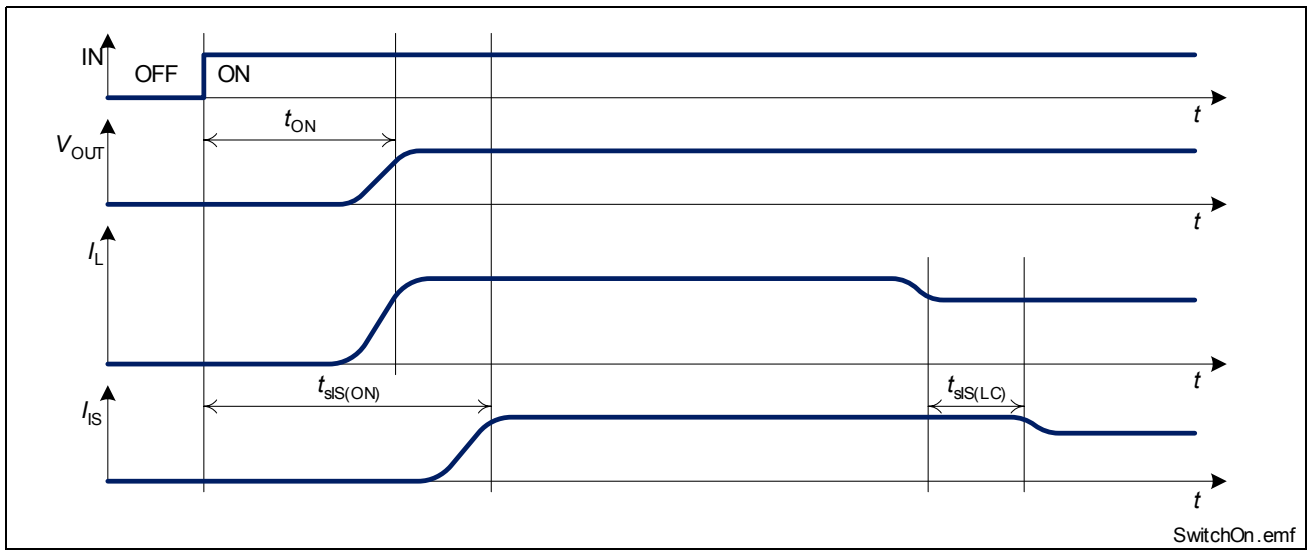



**Figure 15 Timing of Diagnosis Signal in ON-state**

### 4.3.2 OFF-State Diagnosis

Details about timings between the diagnosis signal $I_{IS}$ and the output voltgage $V_{OUT}$ and the load current $I_L$ in OFF-state can be found in **Figure 16**.

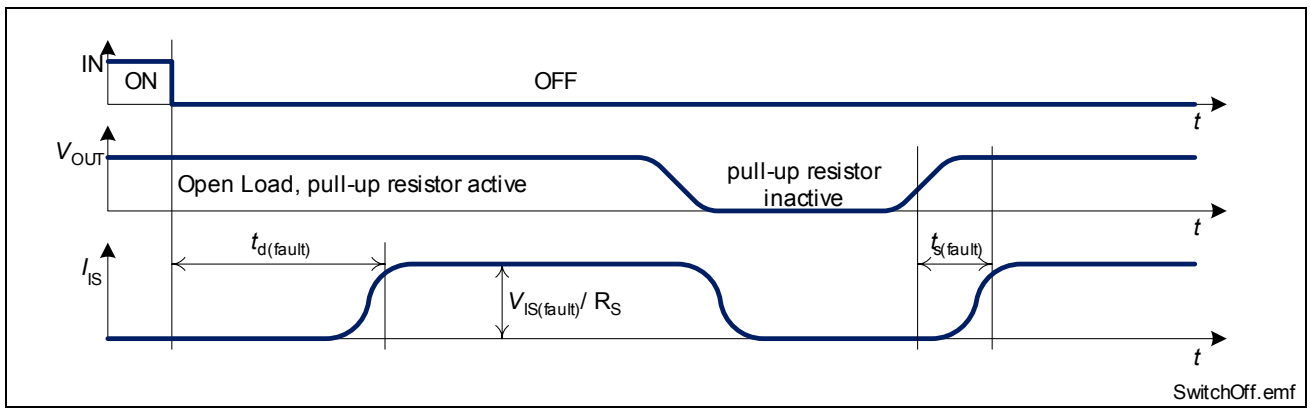



**Figure 16 Timing of Diagnosis Signal in OFF-state**

For open load diagnosis in off-state an external output pull-up resistor ($R_{OL}$) is necessary, because the integrated pull-down current $I_{L(PD)}$ causes secure suppression of the open load condition as long as no pull-up resistor is activated. For caluclation of

the pull-up resistor, the pull-down current $I_{L(PD)}$ and the open load threshold voltage $V_{OUT(OL)}$ has to be taken into account.

$$R_{OL} = \frac{V_{bb(min)} - V_{OUT(OL,max)}}{I_{L(PD,max)} + I_{leakage}}$$

$I_{leakage}$ defines the leakage current in the complete system e.g. caused by humidity. $V_{bb(min)}$ is the minimum supply voltage at which the open load diagnosis in off-state must be ensured.

To reduce the stand-by current of the system, an open load resistor switch ($S_{OL}$) is recommended.

### 4.3.3 Sense Enable Function

The diagnosis signals can be switched off by a low signal at sense enable pin (SEN). See **Figure 17** for details on the timing between SEN pin and diagnosis signal $I_{IS}$. Please note that the diagnosis is enabled, when no signal is provided at pin SEN.

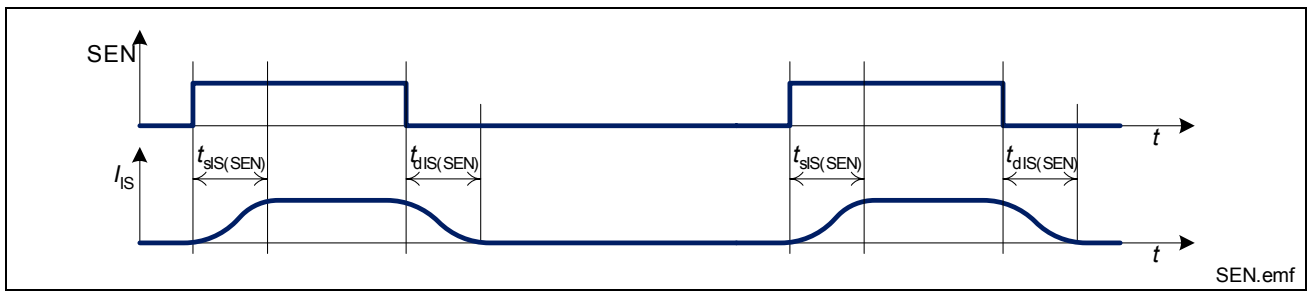



**Figure 17 Timing of Sense Enable Signal**

The SEN pin circuit is designed equal to the input pin. Please refer to **Figure 5** for details. The resistors $R_{lim}$ are recommended to limit the current through the sense pins IS1 to IS4 in case of reverse polarity and over-voltage.

The stand-by current of the BTS 5441G is minimized, when all input pins (IN1 and IN2 or IN3 and IN4) and the according sense enable pin (SENA or SENB) are on low level or left open and $V_{OUT} < V_{OUT(OL)}$. In case of open load in off-state ($V_{OUT} > V_{OUT(OL)}$ and $V_{IN}$ = 0 V), diagnosis tries to switch on automatically which causes an increase in supply current. To reduce the stand-by current to a minimum, the open load condition has to be suppressed by opening $S_{OL}$.

### 4.3.4 Electrical Characteristics

$V_{bb}$ = 9 V to 16 V, $T_j$ = -40 °C to +150 °C, $V_{SEN}$ = 5 V (unless otherwise specified)
typical values: $V_{bb}$ = 13.5 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| **Open Load at OFF state** | | | | | | | |
| 4.3.1 | Open load detection threshold voltage | $V_{OUT(OL)}$ | 2.0 | 3.2 | 4.4 | V | |
| 4.3.2 | Integrated output pull-down current | $-I_{L(PD)}$ | 200 | 300 | 400 | µA | $V_{OUT} > V_{OUT(OL)}$ |
| 4.3.3 | Sense signal in case of open load | $V_{IS(fault)}$ | 5.0 | 6.4 | 8 | V | $V_{IN}$ = 0 V<br>$V_{OUT} = V_{bb}$<br>$I_{IS}$ = 1 mA |
| 4.3.4 | Sense signal current limitation | $I_{IS(LIM)}$ | 4 | | | mA | $V_{IN}$ = 0 V<br>$V_{OUT} = V_{bb}$ |
| 4.3.5 | Sense signal invalid after negative input slope | $t_{d(fault)}$ | | | 1.2 | ms | $V_{IN}$ = 5 V to 0 V<br>$V_{OUT} = V_{bb}$ |
| 4.3.6 | Fault signal settling time | $t_{s(fault)}$ | | | 200 | µs | $V_{IN}$ = 0 V<br>$V_{OUT}$ = 0 V to > $V_{OUT(OL)}$<br>$I_{IS}$ = 1 mA |
| **Load Current Sense** | | | | | | | |
| 4.3.7 | Current sense ratio | $k_{ILIS}$ | | | | | $V_{IN}$ = 5 V |
| | $I_L$ = 0.5 A | | 4170 | 5420 | 6670 | | $T_j$ = -40 °C |
| | $I_L$ = 3.0 A | | 4300 | 4850 | 5400 | | |
| | $I_L$ = 6.0 A | | 4350 | 4850 | 5350 | | |
| | $I_L$ = 0.5 A | | 4450 | 5250 | 6050 | | $T_j$ = 150 °C |
| | $I_L$ = 3.0 A | | 4500 | 4950 | 5400 | | |
| | $I_L$ = 6.0 A | | 4550 | 4950 | 5350 | | |
| 4.3.8 | Current sense voltage limitation | $V_{IS(LIM)}$ | 5.0 | 6.3 | 7.5 | V | $I_{IS}$ = 0.5 mA<br>$I_L$ = 5 A |
| 4.3.9 | Current sense leakage/offset current | $I_{IS(LH)}$ | | | 5 | µA | $V_{IN}$ = 5 V<br>$I_L$ = 0 A |

$V_{bb}$ = 9 V to 16 V, $T_j$ = -40 °C to +150 °C, $V_{SEN}$ = 5 V (unless otherwise specified)
typical values: $V_{bb}$ = 13.5 V, $T_j$ = 25 °C

| Pos. | Parameter | Symbol | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | min. | typ. | max. | | |
| 4.3.10 | Current sense leakage, while diagnosis disabled | $I_{IS(dis)}$ | | | 2 | µA | $V_{SEN}$ = 0 V<br>$I_L$ = 5 A |
| 4.3.11 | Current sense settling time to $I_{IS}$ static ±10% after positive input slope | $t_{sIS(ON)}$ | | | 300 | µs | $V_{IN}$ = 0 V to 5 V<br>$I_L$ = 5 A [1] |
| 4.3.12 | Current sense settling time to $I_{IS}$ static ±10% after change of load current | $t_{sIS(LC)}$ | | | 50 | µs | $V_{IN}$ = 5 V<br>$I_L$ = 3 A to 5 A [1] |
| **Sense Enable** | | | | | | | |
| 4.3.13 | Input resistance | $R_{SEN}$ | 2.3 | 3.6 | 5.3 | kΩ | |
| 4.3.14 | L-input level | $V_{SEN(L)}$ | -0.3 | | 1.0 | V | |
| 4.3.15 | H-input level | $V_{SEN(H)}$ | 2.6 | | 17 | V | |
| 4.3.16 | L-input current | $I_{SEN(L)}$ | 3 | | 75 | µA | $V_{SEN}$ = 0.4 V |
| 4.3.17 | H-input current | $I_{SEN(H)}$ | 10 | 38 | 75 | µA | $V_{SEN}$ = 5 V |
| 4.3.18 | Current sense settling time | $t_{sIS(SEN)}$ | | 3 | 10 | µs | $V_{SEN}$ = 0 V to 5 V<br>$V_{IN}$ = 0 V<br>$V_{OUT} > V_{OUT(OL)}$ |
| 4.3.19 | Current sense deactivation time | $t_{dIS(SEN)}$ | | | 10 | µs | $V_{SEN}$ = 5 V to 0 V<br>$I_{IS}$ = 1 mA<br>$R_{IS}$ = 5 kΩ [1] |

[1] Not subject to production test, specified by design