Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

SPOC - BTS5572E

SPI Power Controller

Automotive Power

Never stop thinking

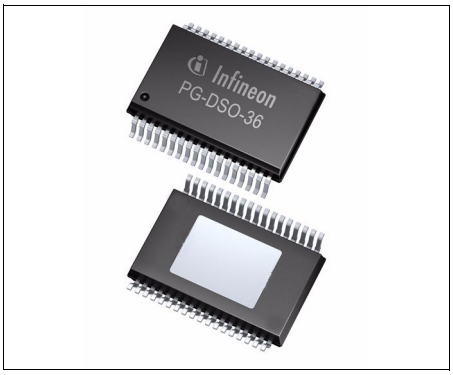
Table of Contents

SPI Power Controller **SPOC - BTS5572E**

for Advanced Light Control
with Integrated LED Mode

AEC Qualified RoHS

1 Overview



PG-DSO-36-36

Features

- 8 bit serial peripheral interface (daisy chain capable SPI) for control and diagnosis
- CMOS compatible parallel input pins for each channel provide direct PWM operation
- Selectable AND- / OR-combination for parallel inputs (PWM control)
- Very low stand-by current
- Enhanced electromagnetic compatibility (EMC) for bulbs as well as LED
- Stable behavior at under voltage
- Device ground independent from load ground
- Green Product (RoHS-Compliant)
- AEC Qualified

Description

The SPOC - BTS5572E is a five channel high-side smart power switch in PG-DSO-36-36 package providing embedded protective functions. It is specially designed to control standard exterior lighting in automotive applications. In order to use the same hardware, the device can be configured to bulb or LED mode. As a result, both load types are optimized in terms of switching and diagnosis behavior.

It is designed to drive lamps up to 3*27W + 2*10W.

Product Summary

Operating Voltage Power Switch	V_{BB}	5.5 … 28 V
Logic Supply Voltage	V_{DD}	3.8 … 5.5 V
Over Voltage Protection	$V_{BB(AZ,min)}$	40 V
Maximum Stand-By Current at 25 °C	$I_{BB(OFF)}$	3 µA
On-State Resistance at T_j = 150 °C channel 0, 1, 2 channel 3, 4	$R_{DS(ON,max)}$	 100 mΩ 260 mΩ
SPI Access Frequency	$f_{SCLK(max)}$	2 MHz

Type	Package	Marking
SPOC - BTS5572E	PG-DSO-36-36	BTS5572E

Configuration and status diagnosis are done via SPI. An 8 bit serial peripheral interface (SPI) is used. The SPI can be used in daisy chain configuration.

The device provides a current sense signal per channel that is multiplexed to the diagnosis pin IS. It can be enabled and disabled via SPI commands. An over load and over temperature flag is provided in the SPI diagnosis word. A multiplexed switch bypass monitor provides short-circuit to V_{BB} diagnosis.

In order to use the same hardware, channels OUT0, OUT1 and OUT2 can be configured to bulb or LED mode.

The SPOC - BTS5572E provides a fail-safe feature via a limp home input pin.

The power transistors are built by N-channel vertical power MOSFETs with charge pumps. The device is monolithically integrated in SMART technology.

Protective Functions

- Reverse battery protection with external components
- Short circuit protection
- Overload protection
- Multi step current limitation
- Thermal shutdown with latch and dynamic temperature sensor
- Overvoltage protection
- Loss of ground protection
- Electrostatic discharge protection (ESD)

Diagnostic Functions

- Multiplexed proportional load current sense signal (IS)
- Enable function for current sense signal configurable via SPI
- High accuracy of current sense signal at wide load current range
- Current sense ratio (k_{ILIS}) configurable for LEDs or bulbs
- Very fast diagnosis in LED mode (>2% duty cycle at 100 Hz)
- Feedback on over temperature and over load via SPI
- Multiplexed switch bypass monitor provides short circuit to V_{BB} detection

Application Specific Functions

- Fail-safe activation via LHI pin and control via input pins
- Load type configuration via SPI (bulbs or LEDs) for optimized load control

Applications

- High-side power switch for 12 V grounded loads in automotive applications
- Especially designed for standard exterior lighting like tail light, brake light, parking light, license plate light, indicators and equivalent LEDs
- Replaces electromechanical relays, fuses and discrete circuits

2 Block Diagram

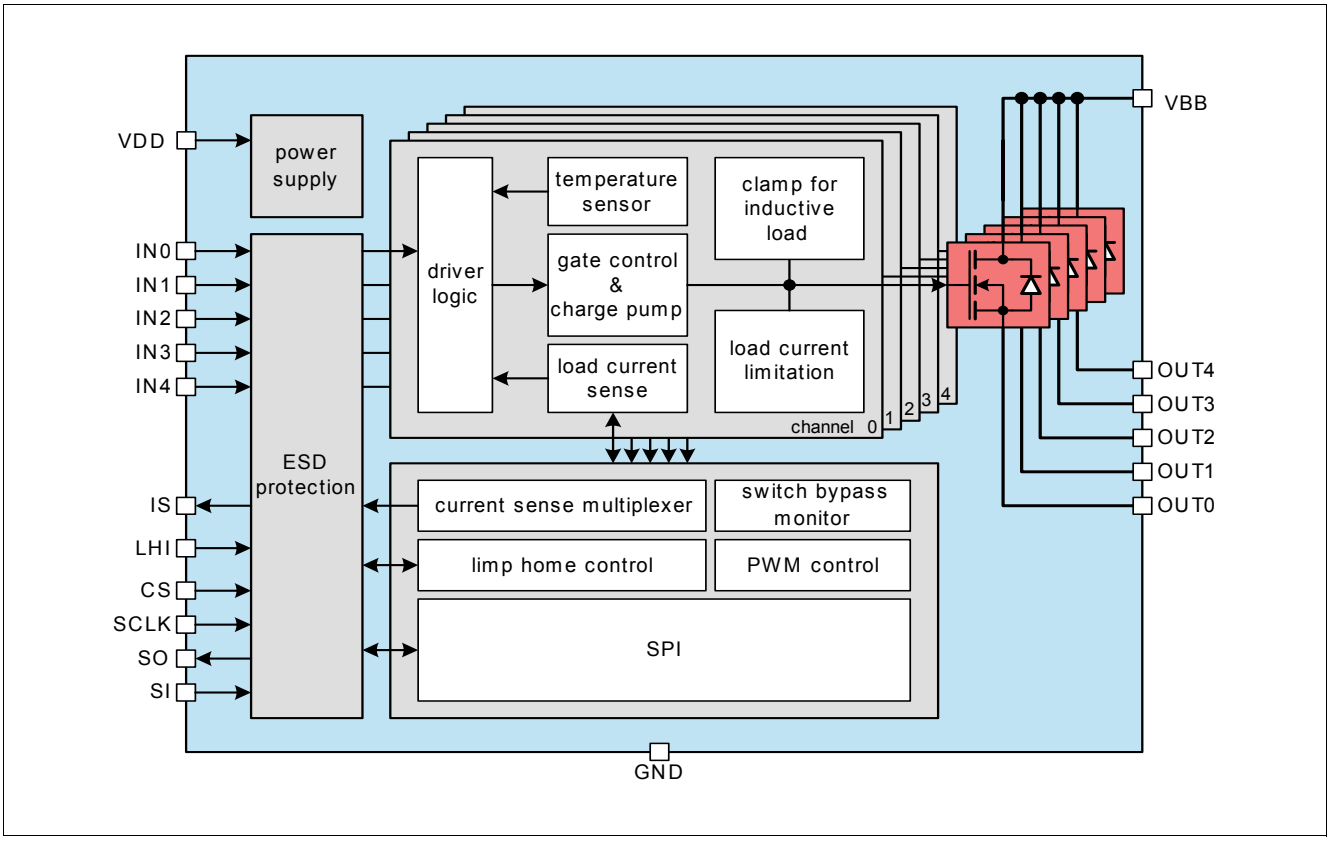


Figure 1 Block Diagram SPOC - BTS5572E

2.1 Terms

The following figure shows all terms used in this data sheet.

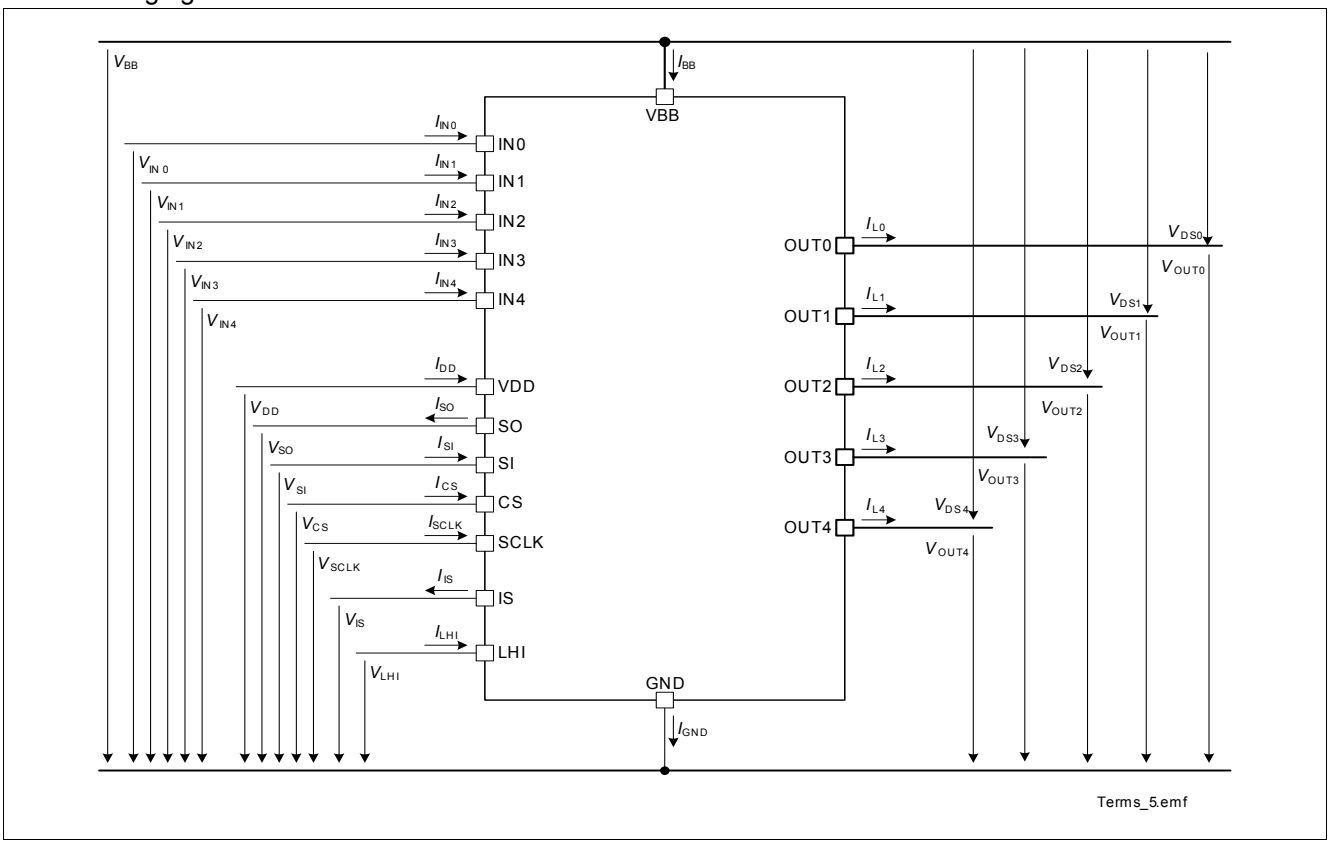


Figure 2 Terms

In all tables of electrical characteristics is valid: Channel related symbols without channel number are valid for each channel separately (e.g. V_{DS} specification is valid for V_{DS0} … V_{DS4}).

All SPI register bits are marked as follows: `ADDR.PARAMETER` (e.g. `HWCR.CTL`). In SPI register description, the values in bold letters (e.g. **0**) are default values.

3 Pin Configuration

3.1 Pin Assignment SPOC - BTS5572E

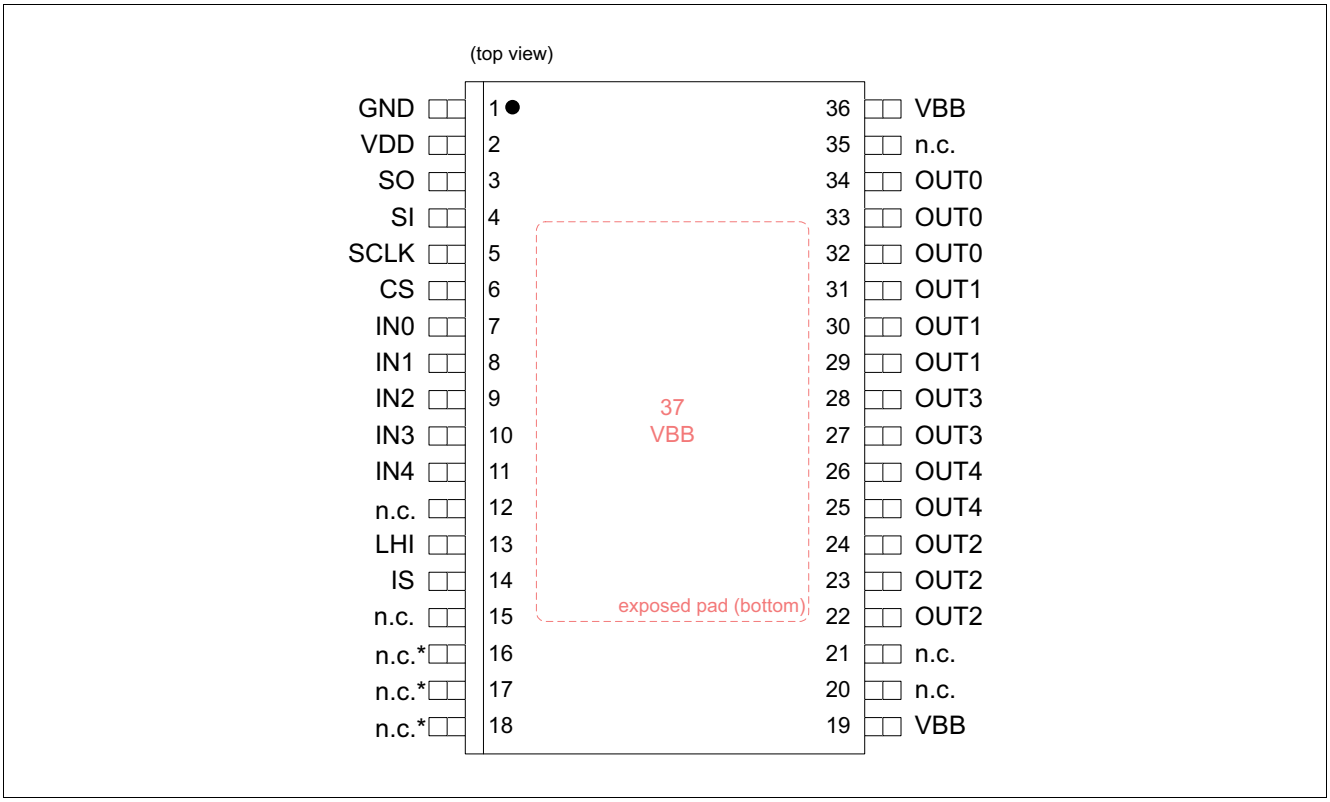


Figure 3 Pin Configuration PG-DSO-36-36

3.2 Pin Definitions and Functions

Pin	Symbol	I/O	Function
Power Supply Pins			
19, 36, 37 [1]	VBB	–	Positive power supply for high-side power switch
2	VDD	–	Logic supply (5 V)
1	GND	–	Ground connection
Parallel Input Pins (integrated pull-down, leave unused input pins unconnected)			
7	IN0	I	Input signal of channel 0
8	IN1	I	Input signal of channel 1
9	IN2	I	Input signal of channel 2
10	IN3	I	Input signal of channel 3
11	IN4	I	Input signal of channel 4
Power Output Pins			
32, 33, 34 [2]	OUT0	O	Protected high-side power output of channel 0
29, 30, 31 [2]	OUT1	O	Protected high-side power output of channel 1
22, 23, 24 [2]	OUT2	O	Protected high-side power output of channel 2
27,28 [2]	OUT3	O	Protected high-side power output of channel 3
25,26 [2]	OUT4	O	Protected high-side power output of channel 4
SPI & Diagnosis Pins			
6	CS	I	Chip select of SPI interface (low active), Integrated pull up
5	SCLK	I	Serial clock of SPI interface
4	SI	I	Serial input of SPI interface
3	SO	O	Serial output of SPI interface
14	IS	O	Diagnosis output signal
Limp Home Pin (integrated pull-down, leave unused limp home pin unconnected)			
13	LHI	I	Limp home activation signal; Active high
Not connected Pin			
12, 15, 20, 21, 35	n.c.	–	not connected, internally not bonded
16, 17, 18	n.c.*	–	not connected, internally not bonded, shorted together

1) The exposed pad (pin 37) has to be connected to the power supply with a low impedance connection. The exposed pad must be connected with a low thermal resistance.

2) All outputs pins of each channel have to be connected.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
Supply Voltage						
4.1.1	Power supply voltage	V_{BB}	-0.3	28	V	–
4.1.2	Logic supply voltage	V_{DD}	-0.3	5.5	V	–
4.1.3	Reverse polarity voltage according **Figure 21**	$-V_{bat(rev)}$	–	16	V	$T_{j(Start)}$ = 25 °C $t \leq$ 2 min. [2)]
4.1.4	Supply voltage for full short circuit protection (single pulse) ($T_{j(0)}$ = -40 °C … 150 °C)	$V_{BB(SC)}$	0	20	V	R_{ECU} = 20mΩ R_{Cable}= 16mΩ/m L_{Cable}= 1µH/m l = 0 or 5m [3)]
4.1.5	Voltage at power transistor	V_{DS}	–	40	V	–
4.1.6	Supply voltage for load dump protection	$V_{BB(LD)}$	–	40	V	R_I = 2 Ω [4)] t = 400ms
4.1.7	Current through ground pin	I_{GND}	-100	25	mA	$t \leq$ 2 min.
4.1.8	Current through V_{DD} pin	I_{DD}	-25	12	mA	$t \leq$ 2 min.
Power Stages						
4.1.9	Load current	I_L	$-I_{L(LIM)}$	$I_{L(LIM)}$	A	[5)]
Diagnosis Pin						
4.1.10	Current through sense pin IS	I_{IS}	-10	10	mA	$t \leq$ 2 min.
Input Pins						
4.1.11	Voltage at input pins	V_{IN}	-0.3	8.0	V	–
4.1.12	Current through input pins	I_{IN}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
SPI Pins						
4.1.13	Voltage at chip select pin	V_{CS}	-0.3	5.7	V	–
4.1.14	Current through chip select pin	I_{CS}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
4.1.15	Voltage at serial input pin	V_{SI}	-0.3	5.7	V	–
4.1.16	Current through serial input pin	I_{SI}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
4.1.17	Voltage at serial clock pin	V_{SCLK}	-0.3	5.7	V	–
4.1.18	Current through serial clock pin	I_{SCLK}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
4.1.19	Current through serial output pin SO	I_{SO}	-0.75 -2.0	0.75 2.0	mA	– $t \leq$ 2 min.
Limp Home Pin						
4.1.20	Voltage at limp home input pin	V_{LHI}	-0.3	8.0	V	–

Absolute Maximum Ratings (cont'd)[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground
(unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			min.	max.		
4.1.21	Current through limp home input pin	I_{LHI}	-0.75 -2.0	0.75 2.0	mA	– $t \leq 2$ min.
Temperatures						
4.1.22	Junction temperature	T_j	-40	150	°C	–
4.1.23	Dynamic temperature increase while switching	ΔT_j	–	60	K	–
4.1.24	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.25	ESD resistivity OUT pins vs. VBB other pins incl. OUT vs. GND	V_{ESD}	 -4 -2	 4 2	kV	HBM [6)] – –

1) Not subject to production test, specified by design.

2) Device mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

3) In accordance to AEC Q100-012 and AEC Q101-006.

4) R_I is the internal resistance of the load dump pulse generator.

5) Current limitation is a protection feature. Operation in current limitation is considered as "outside" normal operating range. Protection features are not designed for continuous repetitive operation.

6) ESD resistivity, HBM according to EIA/JESD 22-A 114B (1.5kΩ, 100pF).

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.2.1	Junction to Case [1)]	R_{thJC}	–	–	2	K/W	–
4.2.2	Junction to Ambient [1)]	R_{thJA}	–	22	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) Device mounted on a FR4 2s2p board according to Jedec JESD51-2,-5,-7 at natural convection; The product (chip+package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable, a thermal via array under the package contacted the first inner copper layer.

5 Power Supply

The SPOC - BTS5572E is supplied by two supply voltages V_{BB} and V_{DD}. The V_{BB} supply line is used by the power switches. The V_{DD} supply line is used by the SPI related circuitry and for driving the SO line. A capacitor between pins VDD and GND is recommended as shown in **Figure 21**.

There is a power-on reset function implemented for the V_{DD} logic power supply. After start-up of the logic power supply, all SPI registers are reset to their default values. The SPI interface including daisy chain function is active as soon as V_{DD} is provided in the specified range independent of V_{BB}. The first SPI transmission after a reset contains at pin SO the read information from register `OUT`, the transmission error bit `TER` is set.

5.1 Power Supply Modes

The following table shows all possible power supply modes for V_{BB}, V_{DD} and the pin LHI.

Power Supply Modes	Off	Off	SPI on	Reset	Off	Limp Home mode without SPI	Normal operation	Limp Home mode with SPI [1]
V_{BB}	0 V	0 V	0 V	0 V	13.5 V	13.5 V	13.5 V	13.5 V
V_{DD}	0 V	0 V	5 V	5 V	0 V	0 V	5 V	5 V
LHI	0 V	5 V	0 V	5 V	0 V	5 V	0 V	5 V
PROFET operating	–	–	–	–	–	✓	✓	✓
Limp home	–	–	–	–	–	✓	–	✓
SPI (logic)	–	–	✓	reset	reset	reset	✓	reset
Stand-by current	–	–	–	–	✓	–	✓[2]	–
Idle current	–	–	–	–	–	–	✓[3]	–
Diagnosis	–	–	–	–	–	–	✓	✓[4]

1) SPI read only.

2) When `DCR.MUX` = 111_b .

3) When all channels are in OFF-state and `DCR.MUX`!= 111_b.

4) Current sense disabled in limp home mode.

Stand-by mode is entered as soon as the current sense multiplexer (`DCR.MUX`) is in default (stand-by) position [1]. Additionally, all thermal latches are cleared automatically. As soon as stand-by mode is entered, register `HWCR.STB` is set. To wake-up the device, the current sense multiplexer (`DCR.MUX`) is programmed different to default (stand-by) position.

Idle mode parameters are valid, when all channels are switched off, but the current sense multiplexer is not in default position, and V_{DD} supply is available.

Limp home (LHI = high) will wake-up the device and is working without V_{DD} supply. As a result, all channels can be activated via the dedicated input pins.

1) Not affected by the inputs state

5.2 Reset

There are several reset triggers implemented in the device. They reset the SPI registers and errors flags to their default values. The power stages are not affected by the reset signals.

The first SPI transmission after any kind of reset contains at pin SO the read information from register `OUT`, the transmission error bit `TER` is set.

Power-On Reset

The power-on reset is released, when V_{DD} voltage level is higher than $V_{DD(min)}$. The SPI interface can be accessed after wake up time $t_{WU(PO)}$.

Reset Command

There is a reset command available to reset all register bits of the register bank and the diagnosis registers. As soon as `HWCR.RST` = 1, a reset is triggered equivalent to power-on reset. The SPI interface can be accessed after transfer delay time $t_{CS(td)}$.

Limp Home Mode

In Limp Home mode, the SPI write-registers are reset. Output OUTx will follow the input INx configuration only. For application example see **Figure 21**. The SPI interface is operating normally, so the limp home register bit LHI as well as the error flags can be read, but any write command will be ignored. To activate the Limp Home mode, LHI input pin voltage must be higher than $V_{LHI(H)}$.

5.3 Electrical Characteristics

Electrical Characteristics Power Supply

Unless otherwise specified: V_{BB} = 9 V to 16 V, V_{DD} = 3.8 V to 5.5 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, V_{DD} = 4.3 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
5.3.1	Operating voltage power switch	V_{BB}	5.5	–	28[1)]	V	–
5.3.2	Stand-by current for whole device with loads	$I_{BB(STB)}$	 – – –	 0.5 – –	 3 3 58	µA	V_{DD} = 0 V V_{LHI} = 0 V T_j = 25 °C $T_j \leq$ 85 °C [1)] T_j = 150 °C
5.3.3	Idle current for whole device with loads, all channels off.	$I_{BB(idle)}$	–	3	8	mA	V_{DD} = 5 V [2)] DCR.MUX = 110_B
5.3.4	Logic supply voltage	V_{DD}	3.8	–	5.5	V	–
5.3.5	Logic supply current	I_{DD}	–	55	120	µA	V_{CS} = 0 V f_{SCLK} = 0 Hz
5.3.6	Logic idle current	$I_{DD(idle)}$	–	20	50	µA	$V_{CS} = V_{DD}$ f_{SCLK} = 0 Hz Chip in Standby
5.3.7	Operating current for whole device	I_{GND}	–	12	25	mA	f_{SCLK} = 0 Hz
LHI Input Characteristics							
5.3.8	L-input level at pin LHI	$V_{LHI(L)}$	-0.3	–	1.0	V	–
5.3.9	H-input level at pin LHI	$V_{LHI(H)}$	2.6	–	5.5	V	–
5.3.10	L-input current through pin LHI	$I_{LHI(L)}$	3	–	85	µA	V_{LHI} = 0.4 V
5.3.11	H-input current through pin LHI	$I_{LHI(H)}$	7	30	85	µA	V_{LHI} = 5 V
Reset							
5.3.12	Power-On wake up time	$t_{WU(PO)}$			500	µs	[1)]

1) Not subject to production test, specified by design.

2) In case of OUT.5 = 1_b increased current consumption.

Note: Characteristics show the deviation of parameter at the given supply voltage and junction temperature. Typical values show the typical parameters expected from manufacturing at V_{BB} = 13.5 V, V_{DD} = 4.3 V and T_j = 25 °C.

5.4 Command Description

HWCR
Hardware Configuration Register

W/$\overline{R}$[1)]	RB[1)]	ADDR[1)]		3	2	1	0
read	**1**	**1**	**0**	**0**	**x**	**STB**	**CTL**
write	**1**	**1**	**0**	**0**	**0**	**RST**	**CTL**

1) W/$\overline{R}$ Write/Read, RB Register Bank, ADDR Address

Field	Bits	Type	Description
RST	1	w	**Reset Command** **0** Normal operation 1 Execute reset command
STB	1	r	**Stand-by** 0 Device is awake **1** Device is in stand-by mode

6 Power Stages

The high-side power stages are built by N-channel vertical power MOSFETs (DMOS) with charge pumps. There are five channels implemented in the device. Each channel can be switched on via an input pin or via SPI register `OUT`. Channels 0, 1 and 2 provides a load type configuration for bulbs or LEDs in register `PLCR`. The load type configuration is allowed to be changed in OFF-state only.

6.1 Output ON-State Resistance

The on-state resistance $R_{DS(ON)}$ depends on the supply voltage V_{BB} as well as on the junction temperature T_j. **Figure 4** shows those dependencies. The behavior in reverse polarity mode is described in **Section 11**.

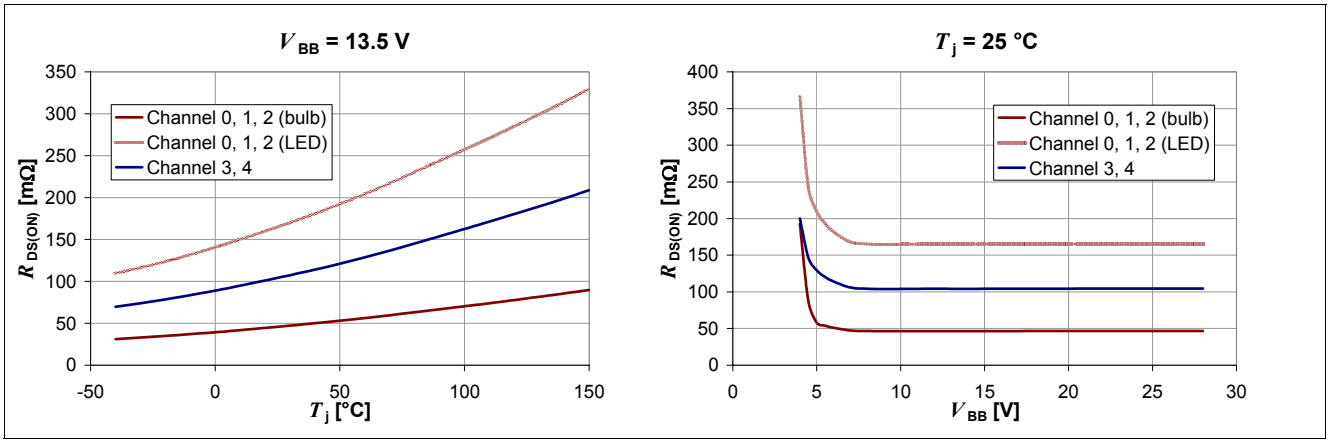


Figure 4 Typical On-State Resistance

6.2 Input Circuit

There are two ways of using the input pins in combination with the OUT register by programming the `HWCR.PWM` parameter.

- `PLCR.PWM` = 0: A channel is switched on either by the according `OUT` register bit or the input pin.
- `PLCR.PWM` = 1: A channel is switched on by the according `OUT` register bit only, when the input pin is high. In this configuration, a PWM signal can be given to the input pin and the channel is activated by the SPI register `OUT`.

Figure 5 shows the complete input switch matrix.

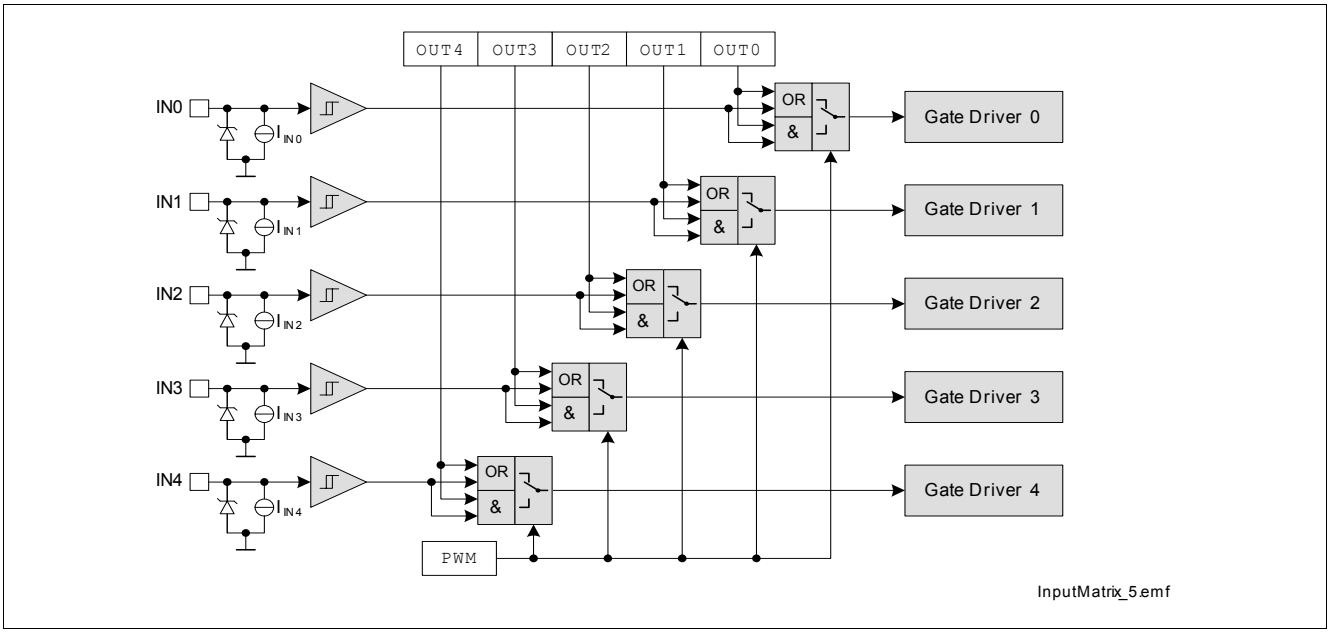


Figure 5 Input Switch Matrix

The current sink to ground ensures that the input signal is low in case of an open input pin. The zener diode protects the input circuit against ESD pulses.

6.3 Power Stage Output

The power stages are built to be used in high side configuration (**Figure 6**).

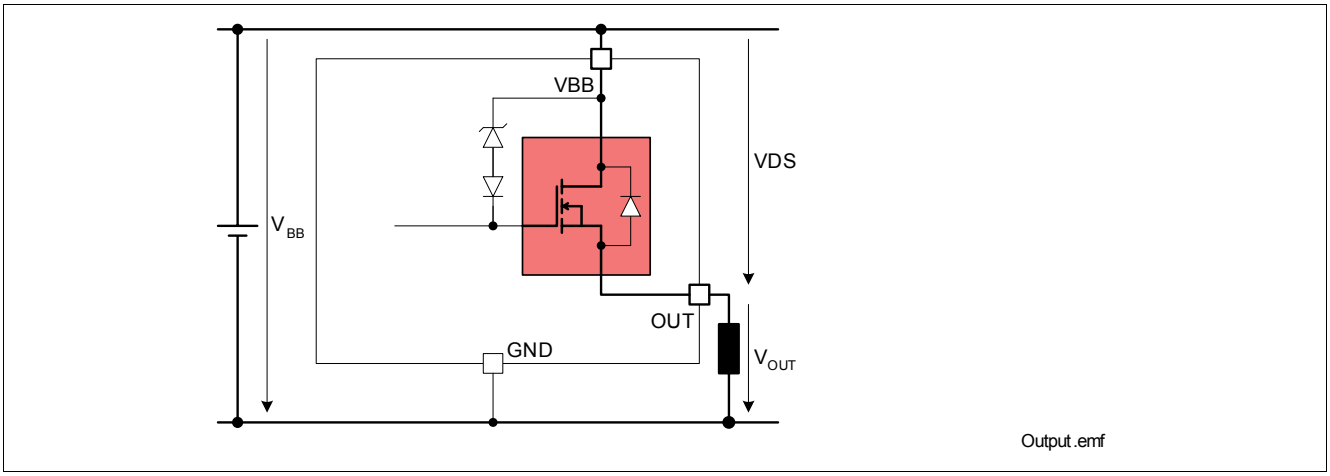


Figure 6 Power Stage Output

The power DMOS switches with a dedicated slope, which is optimized in terms of EMC emission.

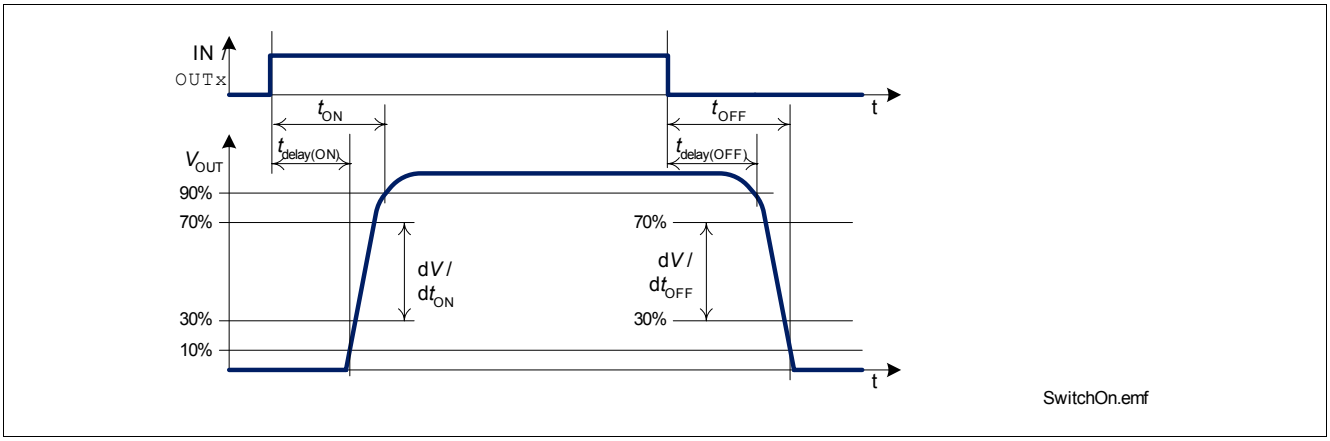


Figure 7 Switching a Load (resistive)

When switching off inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent avalanche of the device, there is a voltage clamp mechanism implemented which limits that negative output voltage to a certain level ($V_{DS(CL)}$). See **Figure 6** for details. The maximum allowed load inductance is limited.

6.4 Electrical Characteristics

Electrical Characteristics Power Stages

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Output Characteristics							
6.4.1	On-State resistance	$R_{DS(ON)}$				mΩ	
	channel 0, 1, 2						PLCR.LEDn = 0
			–	50	–		1) T_j = 25 °C / I_L = 2.6 A
			–	85	100		T_j = 150 °C / I_L = 2.6 A
							PLCR.LEDn = 1
			–	170	–		1) T_j = 25 °C / I_L = 0.6 A
			–	300	375		T_j = 150 °C / I_L = 0.6 A
	channel 3, 4		–	110	–		1) T_j = 25 °C / I_L = 1.3 A
			–	200	260		T_j = 150 °C / I_L = 1.3 A
6.4.2	Output voltage drop limitation at small load currents	$V_{DS(NL)}$				mV	
	channel 0, 1, 2						PLCR.LEDn = 0
			–	25	–		I_L = 35 mA
	channel 3, 4		–	25	–		I_L = 35 mA
6.4.3	Output clamp	$V_{DS(CL)}$	40	47	54	V	I_L = 20 mA 2)
6.4.4	Output leakage current per channel	$I_{L(OFF)}$				µA	V_{IN} = 0 V or floating
							OUT.OUTn = 0
	channel 0, 1, 2		–	0.1	10		stand-by
			–	–	40		idle
	channel 3, 4		–	0.1	8		stand-by
			–	–	40		idle
6.4.5	Inverse current capability per channel	$-I_{L(IC)}$				A	3)
	channel 0, 1, 2		–	2.5	–		–
	channel 3, 4		–	1.0	–		–
Input Characteristics							
6.4.6	L-input level	$V_{IN(L)}$	-0.3	–	1.0	V	–
6.4.7	H-input level	$V_{IN(H)}$	2.6	–	5.5	V	–
6.4.8	L-input current	$I_{IN(L)}$	3	25	75	µA	V_{IN} = 0.4 V
6.4.9	H-input current	$I_{IN(H)}$	10	40	75	µA	V_{IN} = 5 V

Electrical Characteristics Power Stages (cont'd)

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Timings							
6.4.10	Turn-ON delay to 10% V_{BB} (Logical propagation delay from input INx to output OUTx)	$t_{delay(ON)}$				µs	V_{BB} = 13.5 V [1]
	channel 0, 1, 2						PLCR.LEDn = 0
			–	35	–		R_L = 6.8 Ω
	channel 3, 4		–	20	–		R_L = 18 Ω
6.4.11	Turn-OFF delay to 90% V_{BB} (Logical propagation delay from input INx to output OUTx)	$t_{delay(OFF)}$				µs	V_{BB} = 13.5 V [1]
	channel 0, 1, 2						PLCR.LEDn = 0
			–	50	–		R_L = 6.8 Ω
	channel 3, 4		–	30	–		R_L = 18 Ω
6.4.12	Turn-ON time to 90% V_{BB}	t_{ON}				µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			–	–	250		R_L = 6.8 Ω
							PLCR.LEDn = 1
			–	–	100		R_L = 33 Ω
	channel 3, 4		–	–	150		R_L = 18 Ω
6.4.13	Turn-OFF time to 10% V_{BB}	t_{OFF}				µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			–	–	290		R_L = 6.8 Ω
							PLCR.LEDn = 1
			–	–	100		R_L = 33 Ω
	channel 3, 4		–	–	150		R_L = 18 Ω
6.4.14	Turn-ON slew rate 30% to 70% V_{BB}	dV/dt_{ON}				V/µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			0.1	0.2	0.5		R_L = 6.8 Ω
							PLCR.LEDn = 1
			0.1	0.75	1.9		R_L = 33 Ω
	channel 3, 4		0.1	0.45	0.9		R_L = 18 Ω

Electrical Characteristics Power Stages (cont'd)

Unless otherwise specified: V_{BB} = 9 V to 16 V, T_j = -40 °C to +150 °C
typical values: V_{BB} = 13.5 V, T_j = 25 °C

Pos.	Parameter	Symbol	Limit Values			Unit	Test Conditions
			min.	typ.	max.		
6.4.15	Turn-OFF slew rate 70% to 30% V_{BB}	$-\frac{dV}{dt_{OFF}}$				V/µs	V_{BB} = 13.5 V
	channel 0, 1, 2						PLCR.LEDn = 0
			0.1	0.2	0.5		R_L = 6.8 Ω
							PLCR.LEDn = 1
			0.1	0.75	1.9		R_L = 33 Ω
	channel 3, 4		0.1	0.5	0.9		R_L = 18 Ω

1) Not subject to production test, specified by design.

2) The voltage increase until the current is reached.

3) Not subject to production test, specified by design. In case of inverse current (V_{OUT} > V_{BB}), the error flag ERR in the standard diagnosis of the affected channel is cleared. The inverse current capability in ON-state and OFF-state is defined for T_j < $T_{j(SC)}$ and channel remains in same state (ON-state or OFF-state). Other channels can be affected (e.g. OUT latch due to junction temperature increase).

6.5 Command Description

OUT
Output Configuration Registers

W/$\overline{R}$	RB	5	4	3	2	1	0
read	**0**	**x**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**
write	**0**	**0**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**

Field	Bits	Type	Description
OUTn n = 4 to 0	n	rw	**Set Output Mode for Channel n** **0** Channel n is switched off 1 Channel n is switched on

Note: In case of `OUT.5 = 1`$_b$ *the device current consumption is increased.*

PLCR
PWM and LED-Mode Configuration Register

W/$\overline{R}$	RB	ADDR		3	2	1	0
read/write	**1**	**0**	**1**	**PWM**	**LED2**	**LED1**	**LED0**

Field	Bits	Type	Description
PWM	3	rw	**PWM Configuration** **0** Input signal OR-combined with according `OUT` register bit 1 Input signal AND-combined with according `OUT` register bit
LEDn n = 2 to 0	n	rw	**Set LED Mode for Channel n** **0** Channel n is in bulb mode 1 Channel n is in LED mode

7 Protection Functions

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

7.1 Over Load Protection

The load current I_L is limited by the device itself in case of over load or short circuit to ground. There are multiple steps of current limitation which are selected automatically depending on the voltage V_{DS} across the power DMOS. Please note that the voltage at the OUT pin is V_{BB} - V_{DS}. Please refer to following figures for details.

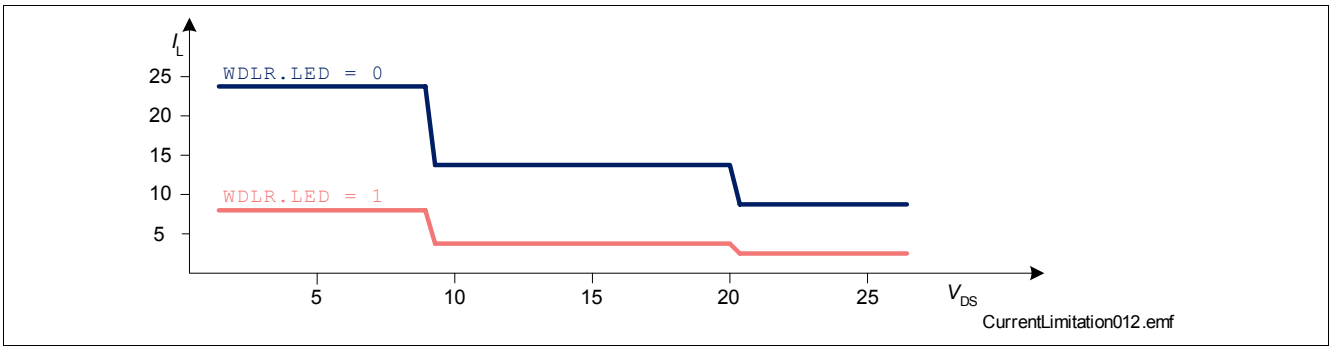


Figure 8 Current Limitation Channels 0, 1, 2 (minimum values)

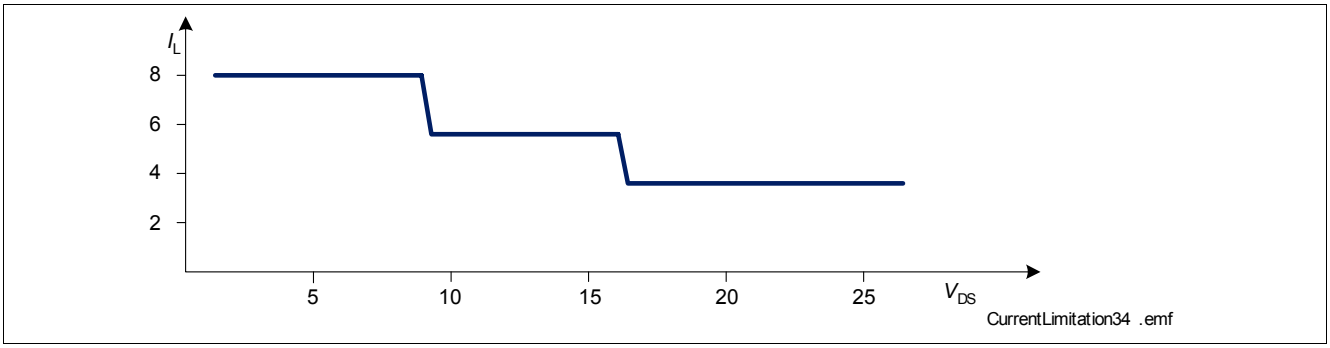


Figure 9 Current Limitation Channels 3, 4 (minimum values)

Current limitation to the value $I_{L(LIM)}$ is realized by increasing the resistance of the output channel, which leads to rapid temperature rise inside.

7.2 Over Temperature Protection

Each channel has its own temperature sensor. If the temperature at the channel exceeds the thermal shutdown temperature $T_{j(SC)}$, the channel will switch off and latch to prevent destruction (also in case of V_{DD} = 0V). In order to reactivate the channel, the temperature at the output must drop by at least the thermal hysteresis ΔT_j and the over temperature latch must be cleared by SPI command `HWCR.CTL` = 1. All over temperature latches are cleared by SPI command `HWCR.CTL` = 1.

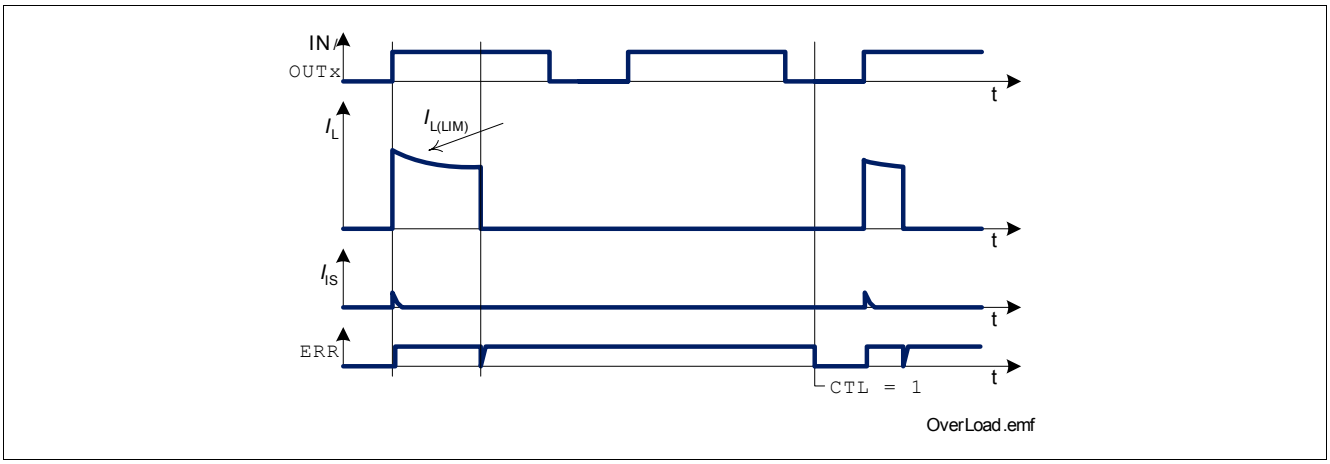


Figure 10 Shut Down by Over Temperature

Additionally, all channels have their own dynamic temperature sensors. The dynamic temperature sensor improves short circuit robustness by limiting sudden increases in the junction temperature. The dynamic temperature sensor turns off the channel if its sudden temperature increase exceeds the dynamic temperature sensor threshold $\Delta T_{j(SW)}$. Please refer to the following figure for details.

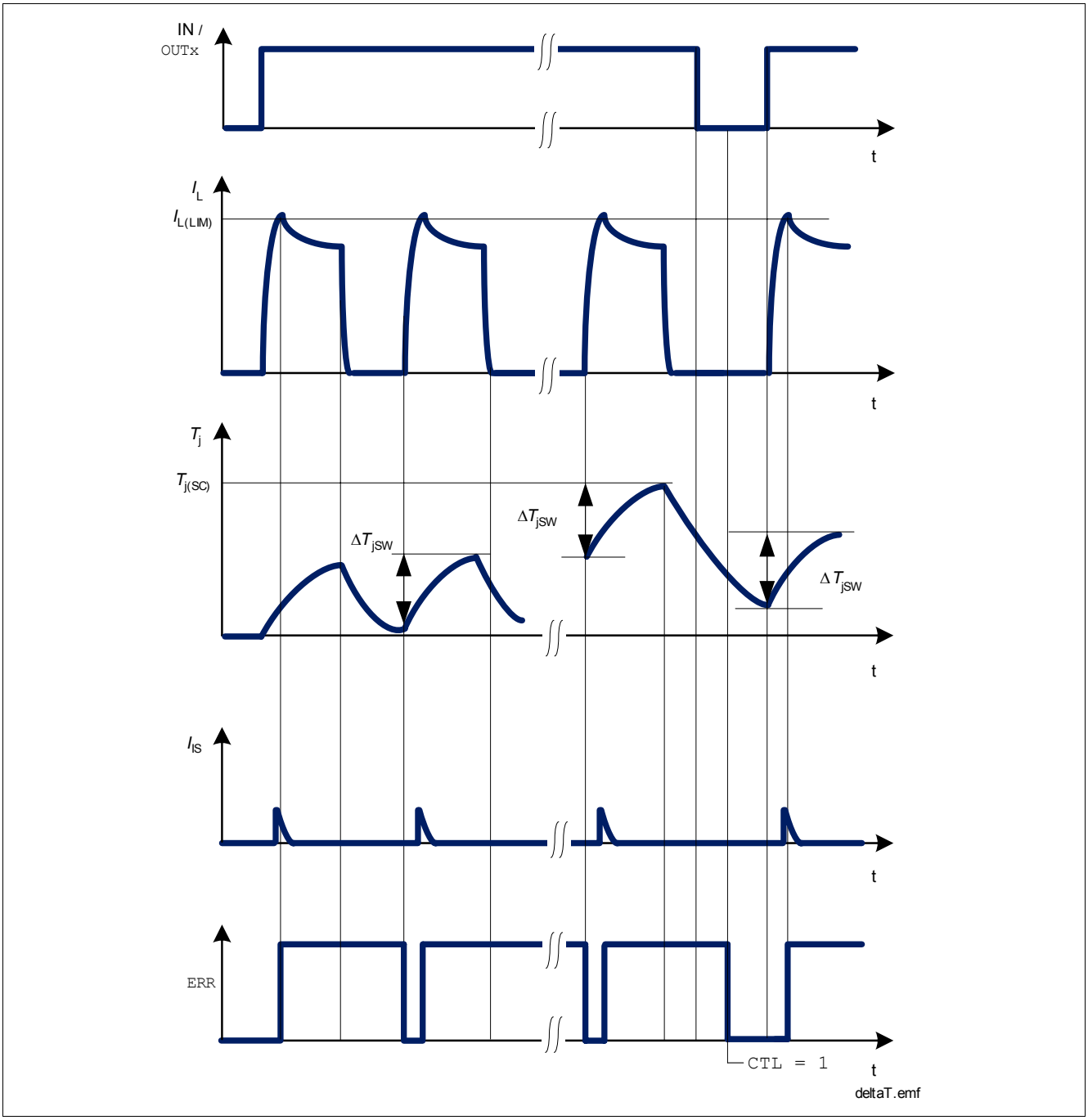


Figure 11 Dynamic Temperature Sensor Operations

The ERR-flag will be set during dynamic temperature sensor shut down. It can be reset by reading the ERR-flag. If the channel is still in dynamic temperature sensor shut down, the ERR-flag will be set again.

7.3 Reverse Polarity Protection

In reverse polarity mode, power dissipation is caused by the intrinsic body diode of each DMOS channel as well as each ESD diode of the logic pins. The reverse current through the channels has to be limited by the connected loads. The current through the ground pin, sense pin IS, the logic power supply pin V_{DD}, the SPI pins and the limp home input pin has to be limited as well (please refer to the maximum ratings listed on **Page 9**).

Note: No protection mechanism like temperature protection or current limitation is active during reverse polarity.

7.4 Over Voltage Protection

In addition to the output clamp for inductive loads as described in **Section 6.3**, there is a clamp mechanism available for over voltage protection. The current through the ground connection has to be limited during over voltage. Please note that in case of over voltage the pin GND might have a high voltage offset to the module ground.

7.5 Loss of Ground

In case of complete loss of the device ground connections, but connected load ground, the SPOC - BTS5572E securely changes to or stays in off-state.

7.6 Loss of V_{BB}

In case of loss of V_{BB} connection in on-state, all inductances of the loads have to be demagnetized through the ground connection or through an additional path from V_{BB} to ground. When a diode is used in the ground path for reverse polarity reason, the ground connection is not available for demagnetization. Then for example, a resistor can be placed in parallel to the diode or a suppressor diode can be used between V_{BB} and GND.