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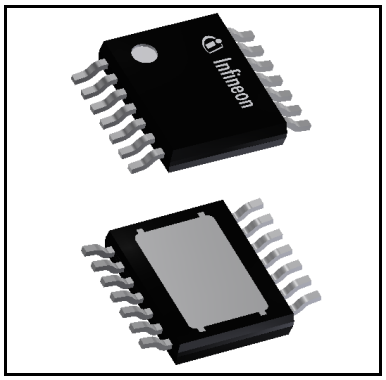
BTS7004-1EPP

High Current PROFET™ 12V **1x 4 mΩ**

Smart High-Side Power Switch

AEC Qualified RoHS

Package	PG-TSDSO-14-22
Marking	7004-1P



1 Overview

Potential Applications

- Suitable for driving 15 A resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Suitable for driving glow plug, heating loads, DC motor and for power distribution

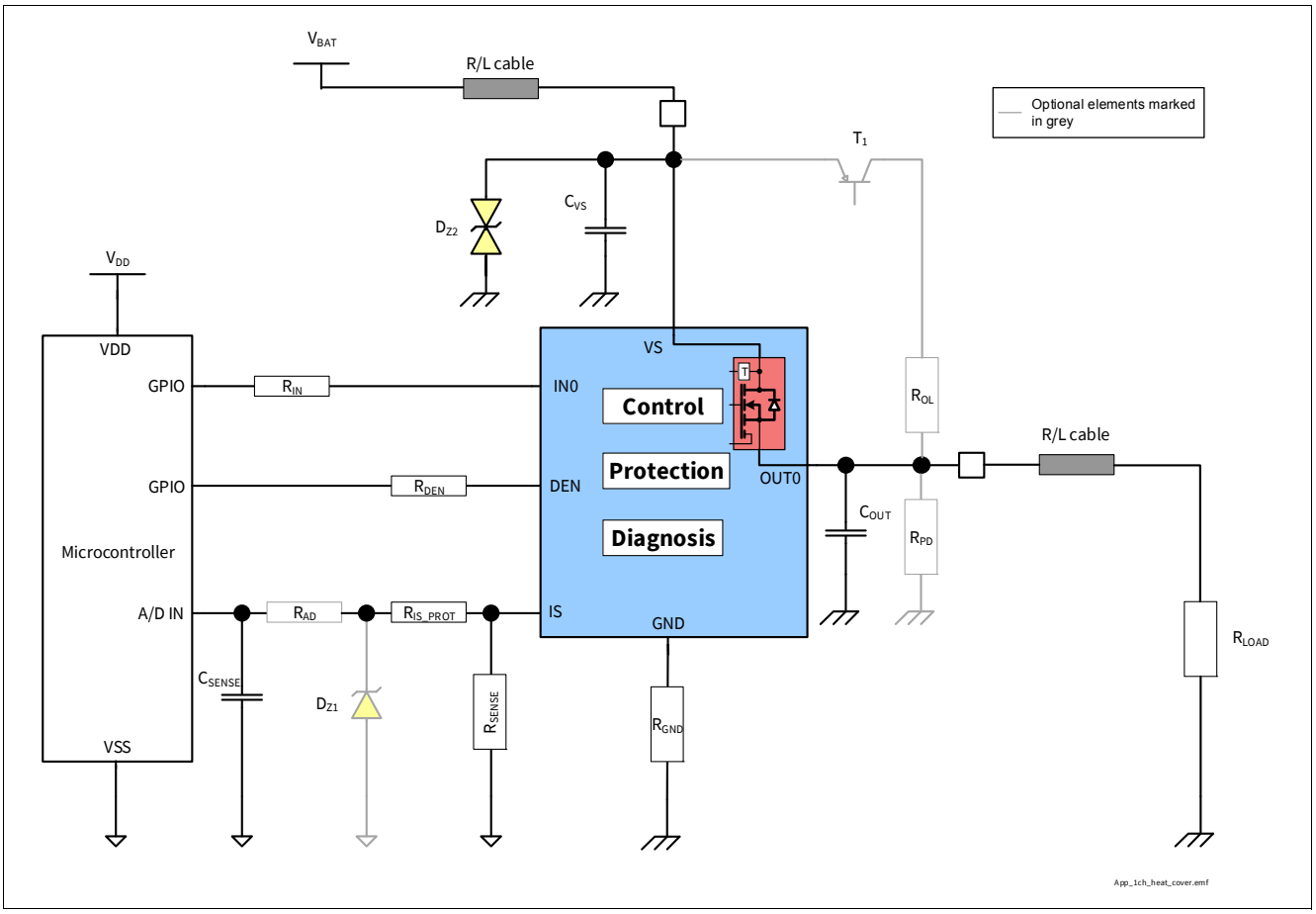


Figure 1 BTS7004-1EPP Application Diagram. Further information in Chapter 10

Overview

Basic Features

- High-Side Switch with Diagnosis and Embedded Protection
- Part of High Current PROFET™ 12V Family
- ReverSave™ for low power dissipation in Reverse Polarity
- Green Product (RoHS compliant)
- Qualified in accordance with AEC Q100 grade 1

Protection Features

- Absolute and dynamic temperature limitation with controlled reactivation
- Overcurrent protection (tripping) with Intelligent Latch
- Undervoltage shutdown
- Overvoltage protection with external components (as shown in **Figure 37**)

Diagnostic Features

- Proportional load current sense
- Open Load in ON and OFF state
- Short circuit to ground and battery

Description

The BTS7004-1EPP is a Smart High-Side Power Switch, providing protection functions and diagnosis.

Table 1 Product Summary

Parameter	Symbol	Values
Minimum Operating voltage	$V_{S(OP)}$	4.1 V
Minimum Operating voltage (cranking)	$V_{S(UV)}$	3.1 V
Maximum Operating voltage	V_S	28 V
Minimum Overvoltage protection (T_J = 25 °C)	$V_{DS(CLAMP)}$	35 V
Maximum current in OFF mode ($T_J \leq$ 85 °C)	$I_{VS(OFF)}$	0.5 µA
Maximum operative current	$I_{GND(ON\_D)}$	3 mA
Typical ON-state resistance (T_J = 25 °C)	$R_{DS(ON)\_25}$	4.4 mΩ
Maximum ON-state resistance (T_J = 150 °C)	$R_{DS(ON)}$	8 mΩ
Nominal load current (T_A = 85 °C)	$I_{L(NOM)}$	15 A
Minimum overload detection current	$I_{L(OVL0)\_-40}$	107 A
Typical current sense ratio at $I_L = I_{L(NOM)}$	k_{ILIS}	20000

2 Block Diagram and Terms

2.1 Block Diagram

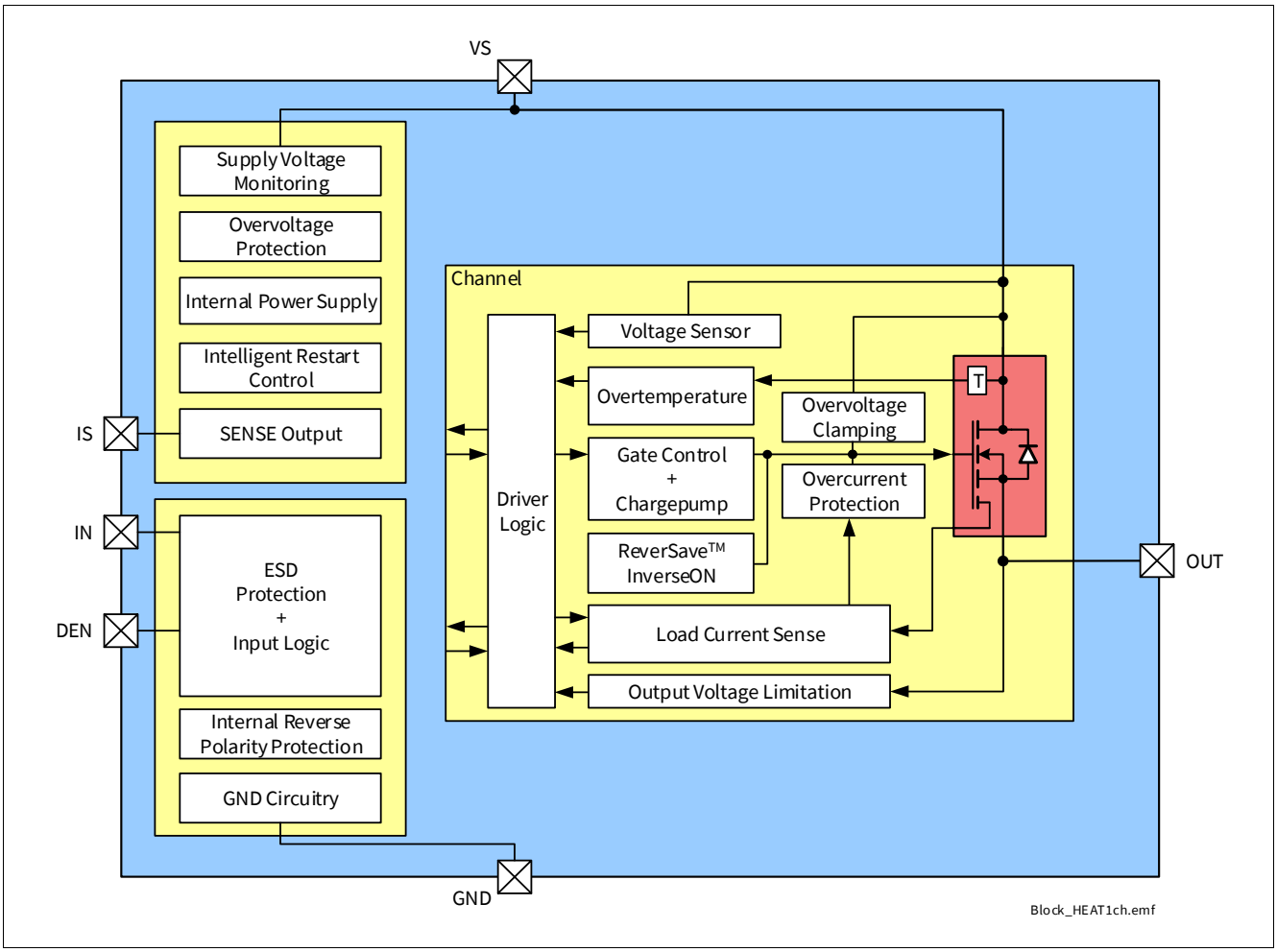


Figure 2 Block Diagram of BTS7004-1EPP

2.2 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

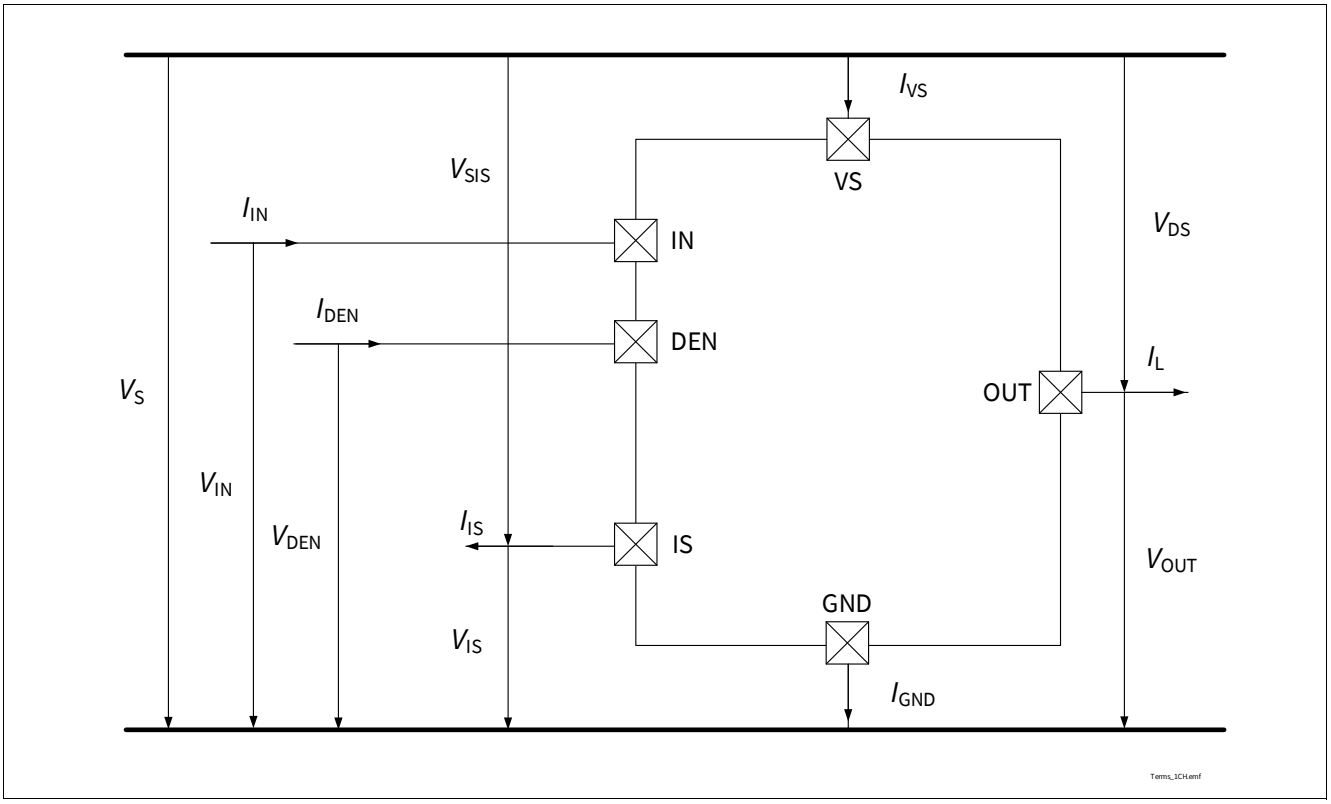


Figure 3 Voltage and Current Convention

3 Pin Configuration

3.1 Pin Assignment

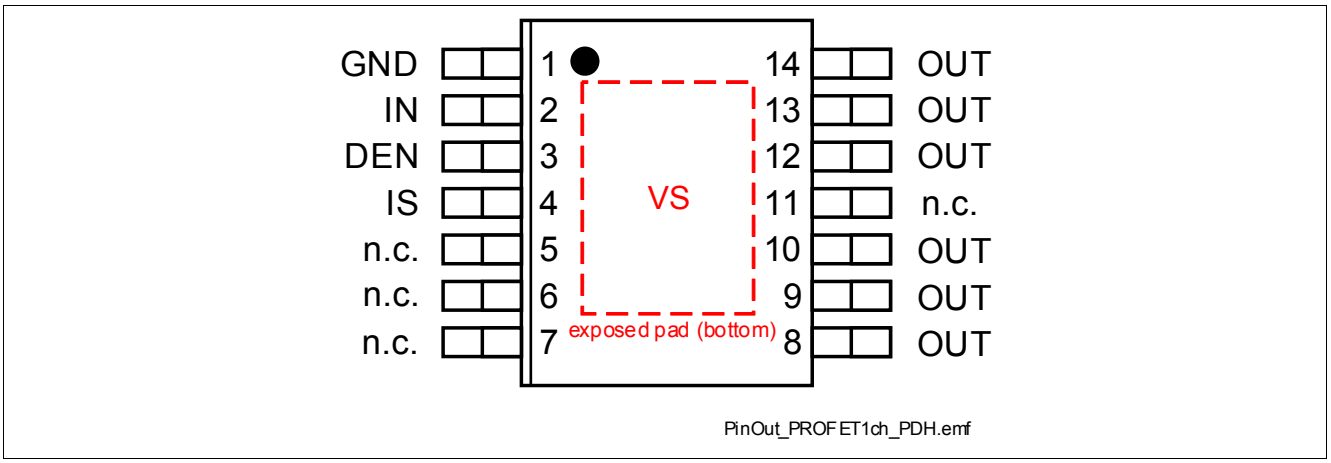


Figure 4 Pin Configuration

3.2 Pin Definitions and Functions

Table 2 Pin Definition

Pin	Symbol	Function
EP	VS (exposed pad)	**Supply Voltage** Battery voltage
1	GND	**Ground** Signal ground
2	IN	**Input Channel** Digital signal to switch ON the channel (“high” active) If not used: connect to GND pin or to module ground with resistor R_{IN} = 4.7 kΩ
3	DEN	**Diagnostic Enable** Digital signal to enable device diagnosis (“high” active) and to clear the protection latch of channel If not used: connect to GND pin or to module ground with resistor R_{DEN} = 4.7 kΩ
4	IS	**SENSE current output** Analog/digital signal for diagnosis If not used: left open
5-7, 11	n.c.	Not connected, internally not bonded
8-10, 12-14	OUT	**Output** Protected high-side power output channel[1)]

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

4 General Product Characteristics

4.1 Absolute Maximum Ratings - General

Table 3 Absolute Maximum Ratings[1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply pins							
Power Supply Voltage	V_S	-0.3	–	28	V	–	P_4.1.0.1
Load Dump Voltage	$V_{BAT(LD)}$	–	–	35	V	suppressed Load Dump acc. to ISO16750-2 (2010). R_i = 2 Ω	P_4.1.0.3
Supply Voltage for Short Circuit Protection	$V_{BAT(SC)}$	0	–	24	V	Setup acc. to AEC-Q100-012	P_4.1.0.25
Reverse Polarity Voltage	$-V_{BAT(REV)}$	–	–	16	V	$t \leq 2$ min T_A = +25 °C Setup as described in **Chapter 10**	P_4.1.0.5
Current through GND Pin	I_{GND}	-50	–	50	mA	R_{GND} according to **Chapter 10**	P_4.1.0.9
Logic & control pins (Digital Input = DI) DI = IN, DEN							
Current through DI Pin	I_{DI}	-1	–	2	mA	2)	P_4.1.0.14
Current through DI Pin Reverse Battery Condition	$I_{DI(REV)}$	-1	–	10	mA	2) $t \leq 2$ min	P_4.1.0.36
IS pin							
Voltage at IS Pin	V_{IS}	-1.5	–	V_S	V	I_{IS} = 10 µA	P_4.1.0.16
Current through IS Pin	I_{IS}	-25	–	$I_{IS(SAT),MAX}$	mA	–	P_4.1.0.18
Temperatures							
Junction Temperature	T_J	-40	–	150	°C	–	P_4.1.0.19
Storage Temperature	T_{STG}	-55	–	150	°C	–	P_4.1.0.20
ESD Susceptibility							

Table 3 Absolute Maximum Ratings[1)] (continued)

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD Susceptibility all Pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	HBM[3)]	P_4.1.0.21
ESD Susceptibility OUT vs GND and VS connected (HBM)	$V_{ESD(HBM)\_OUT}$	-4	–	4	kV	HBM[3)]	P_4.1.0.22
ESD Susceptibility all Pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	CDM[4)]	P_4.1.0.23
ESD Susceptibility Corner Pins (CDM) (pins 1, 7, 8, 14)	$V_{ESD(CDM)\_CRN}$	-750	–	750	V	CDM[4)]	P_4.1.0.24

1) Not subject to production test - specified by design.
2) Maximum V_{DI} to be considered for Latch-Up tests: 5.5 V.
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
4) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Absolute Maximum Ratings - Power Stages

4.2.1 Power Stage - 4 mΩ

Table 4 Absolute Maximum Ratings[1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum Energy Dissipation Single Pulse	E_{AS}	–	–	150	mJ	$I_L = 2^*I_{L(NOM)}$ $T_{J(0)}$ = 150 °C V_S = 28 V	P_4.2.11.1

Table 4 Absolute Maximum Ratings[1)] (continued)

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum Energy Dissipation Repetitive Pulse	E_{AR}	–	–	44	mJ	$I_L = I_{L(NOM)}$ $T_{J(0)}$ = 85 °C V_S = 13.5 V 1M cycles	P_4.2.11.4
Load Current	$\|I_L\|$	–	–	$I_{L(OVL0),MAX}$	A		P_4.2.11.3

1) Not subject to production test - specified by design.

4.3 Functional Range

Table 5 Functional Range - Supply Voltage and Temperature[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage Range for Normal Operation	$V_{S(NOR)}$	6	13.5	18	V	–	P_4.3.0.1
Lower Extended Supply Voltage Range for Operation	$V_{S(EXT,LOW)}$	3.1	–	6	V	2)3) (parameter deviations possible)	P_4.3.0.2
Upper Extended Supply Voltage Range for Operation	$V_{S(EXT,UP)}$	18	–	28	V	3) (parameter deviations possible)	P_4.3.0.3
Junction Temperature	T_J	-40	–	150	°C	–	P_4.3.0.5

1) Not subject to production test - specified by design.
2) In case of V_S voltage decreasing: $V_{S(EXT,LOW),MIN}$ = 3.1 V. In case of V_S voltage increasing: $V_{S(EXT,LOW),MIN}$ = 4.1 V.
3) Protection functions still operative.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics tables.

4.4 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 6 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Characterization Parameter Junction-Top	Ψ_{JTOP}	–	3	5	K/W	2)	P_4.4.0.1
Thermal Resistance Junction-to-Case	R_{thJC}	–	1.4	2.4	K/W	2) simulated at exposed pad	P_4.4.0.2
Thermal Resistance Junction-to-Ambient	R_{thJA}	–	31.8	–	K/W	2)	P_4.4.0.3

1) Not subject to production test - specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_A = 105°C, $P_{DISSIPATION}$ = 1 W.

4.4.1 PCB Setup

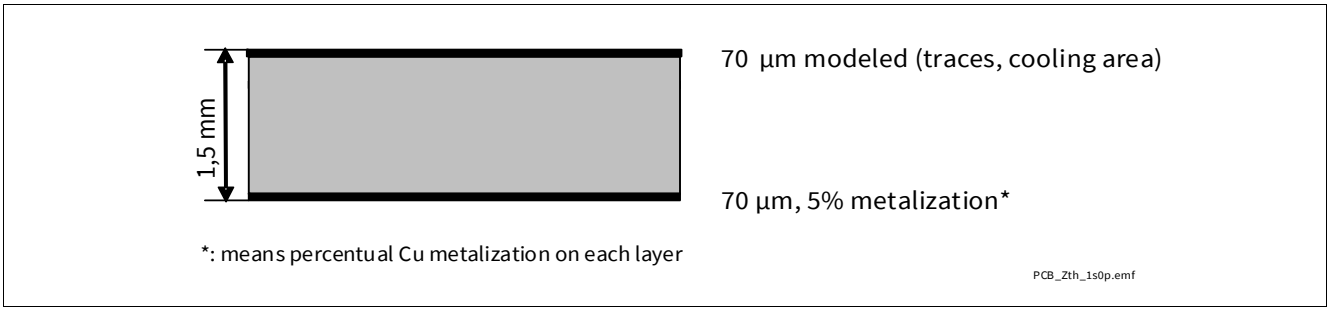


Figure 5 1s0p PCB Cross Section

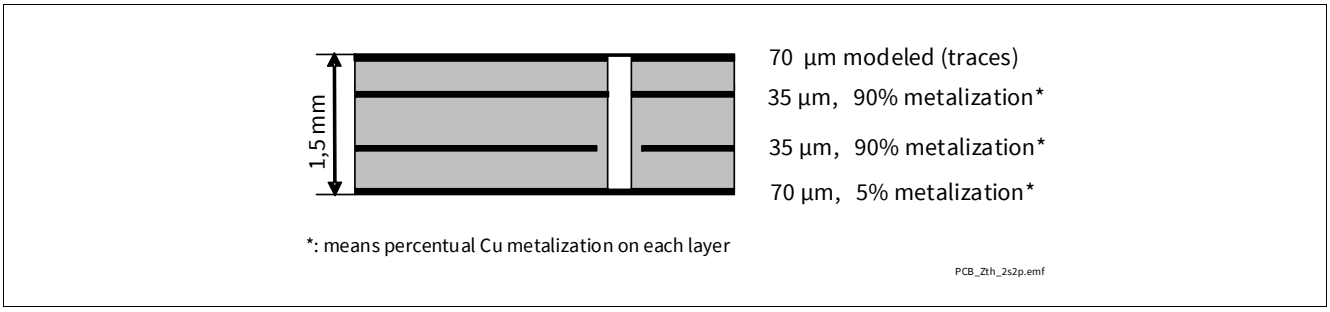


Figure 6 2s2p PCB Cross Section

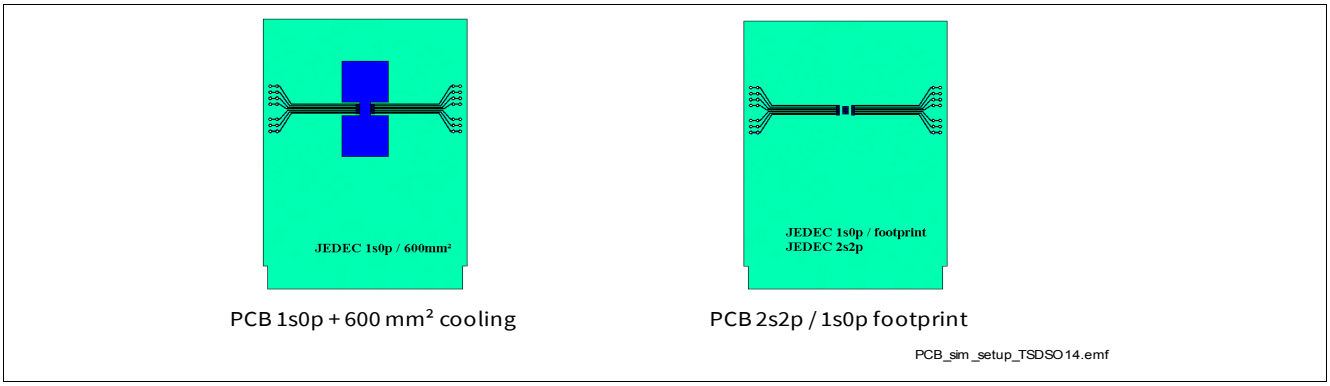


Figure 7 PCB setup for thermal simulations

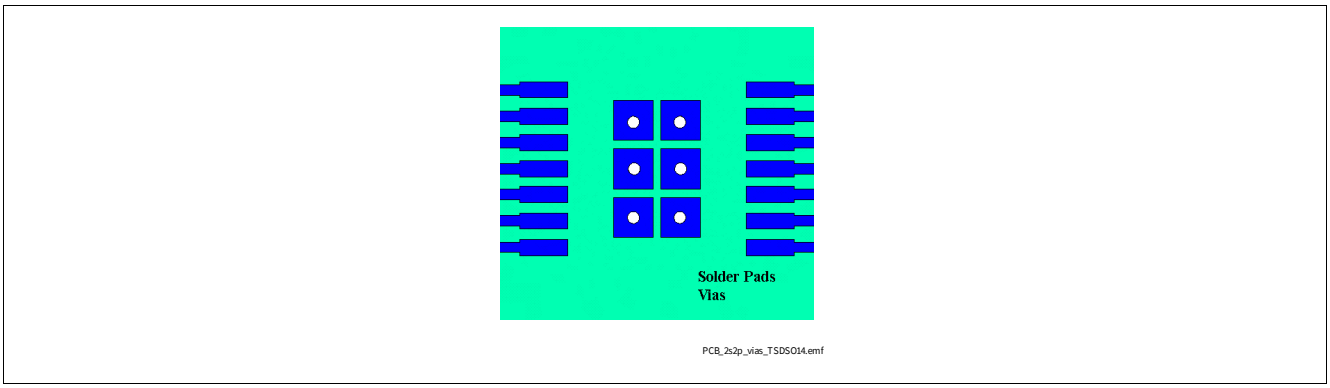


Figure 8 Thermal vias on PCB for 2s2p PCB setup

4.4.2 Thermal Impedance

Figure 9 Typical Thermal Impedance. PCB setup according Chapter 4.4.1

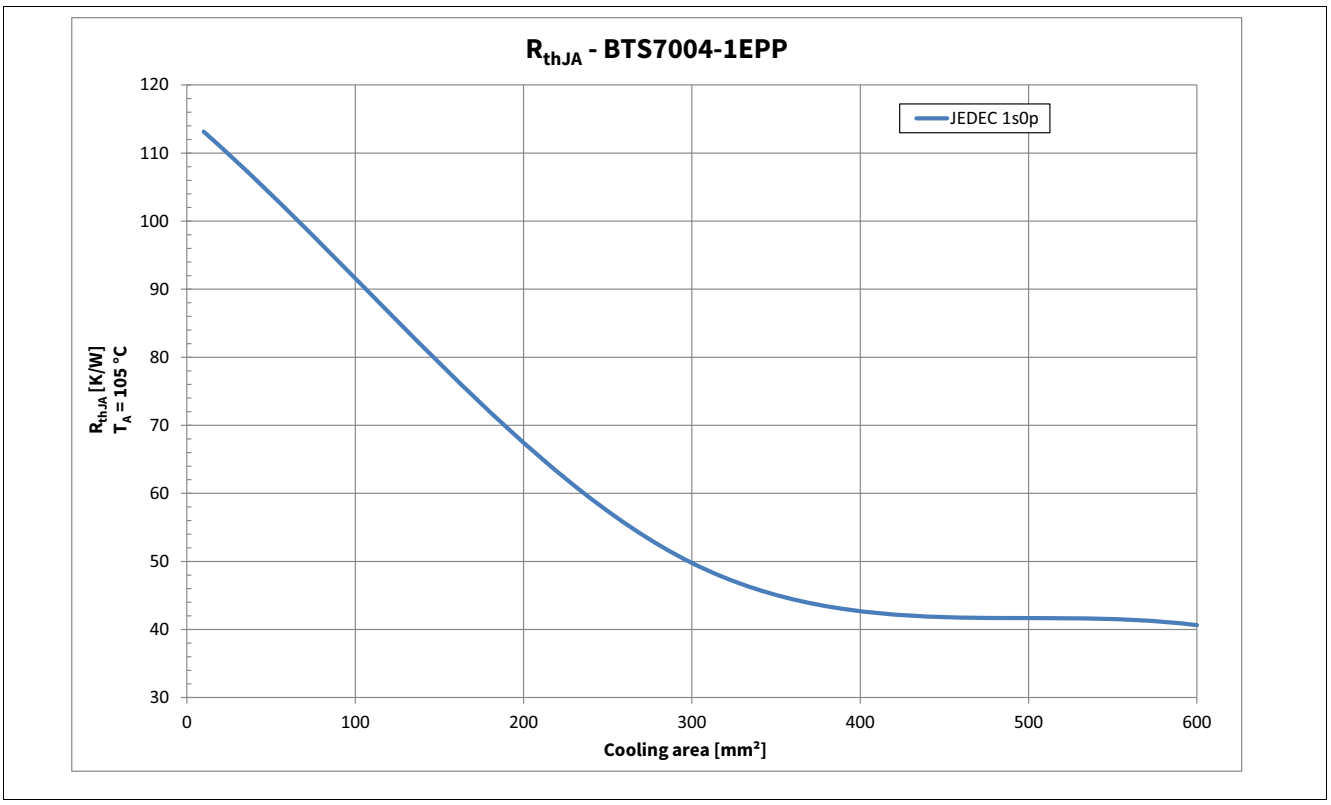


Figure 10 Thermal Resistance on 1s0p PCB with various cooling surfaces

5 Logic Pins

The device has 2 digital pins .

5.1 Input Pin (IN)

The input pin IN activates the output channel. The input circuitry is compatible with 3.3V and 5V microcontroller. The electrical equivalent of the input circuitry is shown in **Figure 11**. In case the pin is not used, it should be pulled to module GND or device GND pin via R_{IN} = 4.7 kΩ.

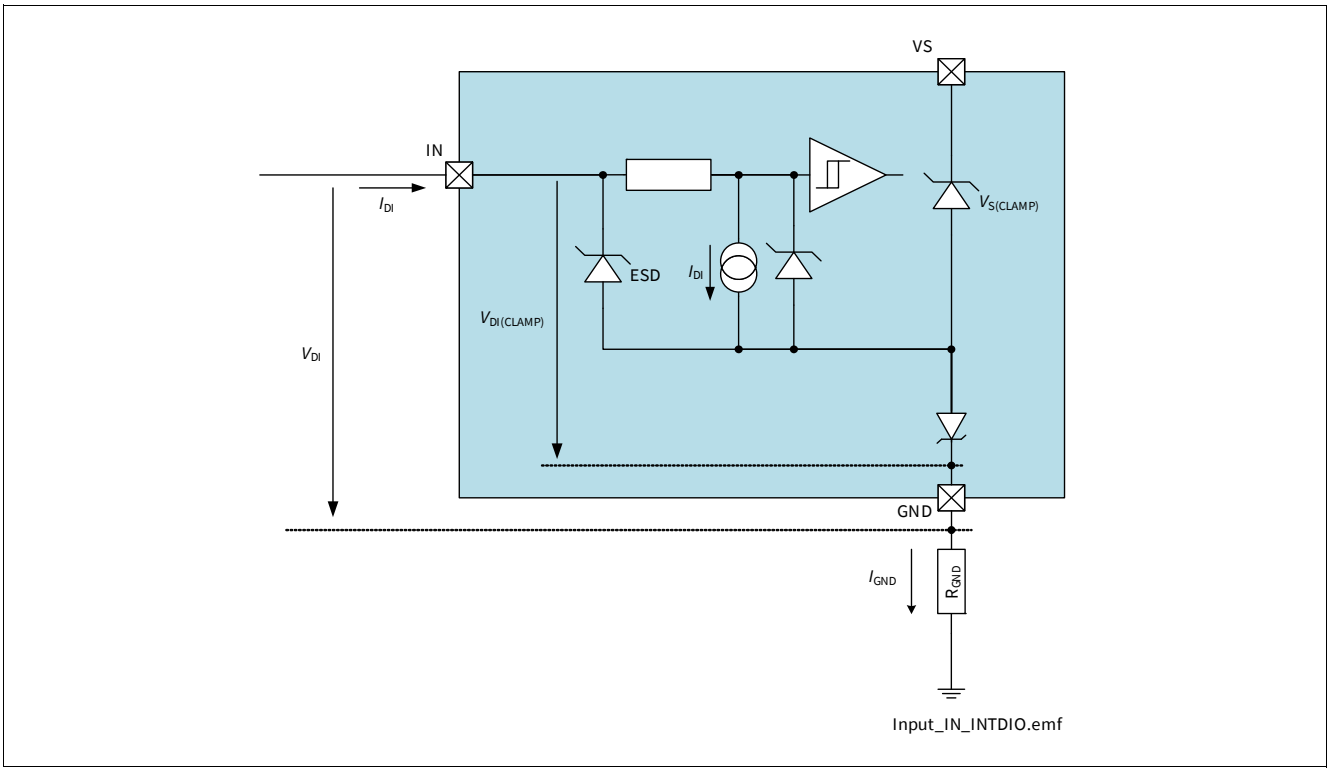


Figure 11 Input circuitry

The logic thresholds for “low” and “high” states are defined by parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in **Figure 12**. The voltage V_{IN} needed to ensure a “high” state is always higher than the voltage needed to ensure a “low” state.

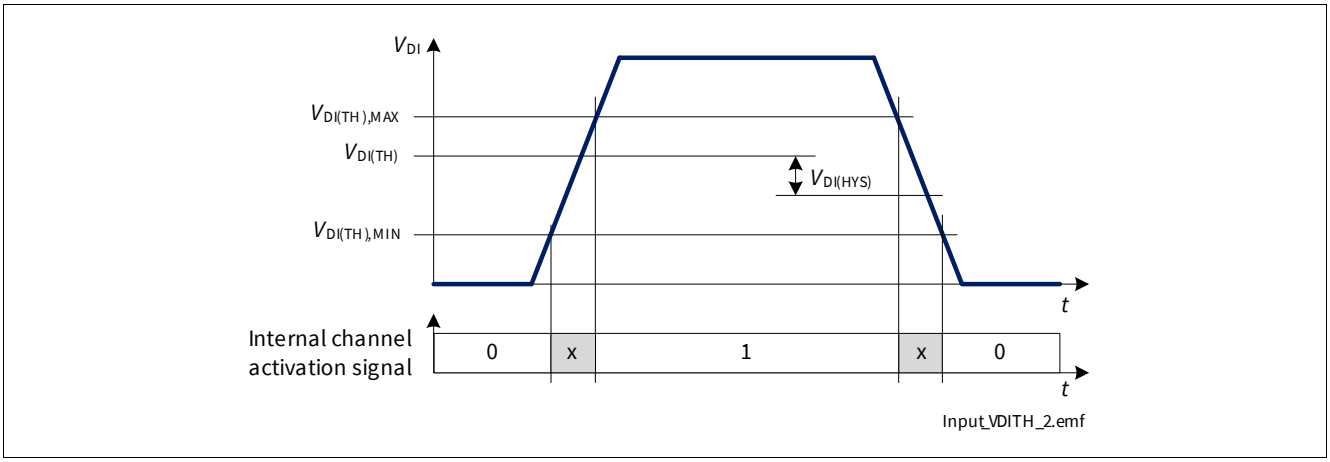


Figure 12 Input Threshold voltages and hysteresis

5.2 Diagnosis Pin

The Diagnosis Enable (DEN) pin controls the diagnosis circuitry and can be used to reset the latched protection (Protection circuitry not disabled by DEN). When DEN pin is set to “high”, the diagnosis is enabled (see **Chapter 9.2** for more details). When it is set to “low”, the diagnosis is disabled (IS pin is set to high impedance).

The transition from “high” to “low” of DEN pin clears the protection latch of the channel depending on the logic state of IN pin and DEN pulse length (see **Chapter 8.3** for more details). The internal structure of diagnosis pins is the same as the one of input pins. See **Figure 11** for more details.

5.3 Electrical Characteristics Logic Pins

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Digital Input (DI) pins = IN, DEN

Table 7 Electrical Characteristics: Logic Pins - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Digital Input Voltage Threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See **Figure 11** and **Figure 12**	P_5.4.0.1
Digital Input Clamping Voltage	$V_{DI(CLAMP1)}$	–	7	–	V	1) I_{DI} = 1 mA See **Figure 11** and **Figure 12**	P_5.4.0.2
Digital Input Clamping Voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	I_{DI} = 2 mA See **Figure 11** and **Figure 12**	P_5.4.0.3
Digital Input Hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	1) See **Figure 11** and **Figure 12**	P_5.4.0.4
Digital Input Current (“high”)	$I_{DI(H)}$	2	10	25	µA	V_{DI} = 2 V See **Figure 11** and **Figure 12**	P_5.4.0.5
Digital Input Current (“low”)	$I_{DI(L)}$	2	10	25	µA	V_{DI} = 0.8 V See **Figure 11** and **Figure 12**	P_5.4.0.6

1) Not subject to production test - specified by design.

6 Power Supply

The BTS7004-1EPP is supplied by V_S, which is used for the internal logic as well as supply for the power output stage. V_S has an undervoltage detection circuit, which prevents the activation of the power output stage and diagnosis in case the applied voltage is below the undervoltage threshold ($V_S < V_{S(OP)}$). During power up, the internal power on signal is set when supply voltage (V_S) exceeds the minimum operating voltage ($V_S > V_{S(OP)}$).

6.1 Operation Modes

BTS7004-1EPP has the following operation modes in case of $V_S > V_{S(OP)}$:

- OFF mode
- ON mode
- Diagnosis in ON mode
- Diagnosis in OFF mode
- Fault

The transition between operation modes is determined according to these variables:

- Logic level at IN pin
- Logic level at DEN pin
- Internal latch
- Sense current I_{IS} level

The truth table in case of $V_S > V_{S(OP)}$ is shown in **Table 8**. The behavior of BTS7004-1EPP as well as some parameters may change in dependence on the operation mode of the device.

There are three parameters describing each operation mode of BTS7004-1EPP:

- Status of the output channel
- Status of the diagnosis
- Current consumption at VS pin (measured by I_{VS} in OFF mode, I_{GND} in all other operative modes)

Table 8 Operation Mode truth table

IN	DEN	Internal latch	I_{IS}	Operative Mode	Comment
L	L	L	leakage	OFF	DMOS channel is OFF
L	L	H	leakage	OFF	DMOS channel is OFF
L	H	L	leakage	OFF_DIAG	Diagnostic in OFF-mode
			open load		Diagnostic in OFF-mode
L	H	H	fault		Diagnostic in OFF-mode
H	L	L	leakage	ON	DMOS channel is ON, no diagnostic
H	L	H	leakage	fault	DMOS channel is switched OFF due to failure
H	H	L	I_{IS}	ON_DIAG	DMOS channel is ON and diagnostic
H	H	H	fault	fault	DMOS channel is switched OFF due to failure

6.1.1 OFF mode

When BTS7004-1EPP is in OFF mode, the output channel is OFF. The current consumption is minimum (see parameter $I_{VS(OFF)}$). No Overtemperature, Overload protection mechanism and no diagnosis function is active when the device is in OFF mode.

6.1.2 ON mode

ON (IN = High; DEN = Low) mode is the normal operation mode of BTS7004-1EPP. Device current consumption is specified with $I_{GND(ON\_D)}$ + $I_{IS(OFF)}$ (measured at GND pin because the current at VS pin includes the load current). Overcurrent and Overtemperature protections are active. No diagnosis function is active.

6.1.3 OFF_Diag mode

The device is in OFF_Diag mode as long as DEN pin is set to “high” and IN pin is set to “low”. The output channel is OFF. If an open load case happens, an Open Load in OFF current $I_{IS(OLOFF)}$ may be present at IS pin. In such situation, the current consumption of the device is increased.

6.1.4 ON_Diag mode

The device is in normal ON mode with current sense function. I_{IS} or $I_{IS(FAULT)}$ will be present at IS pin. Device current consumption is specified with $I_{GND(ON\_D)}$. Depending on the load condition, either a fault current $I_{IS(FAULT)}$ or I_{IS} current may be present at IS pin.

6.1.5 Fault mode

The device is in Fault mode as soon as a protection event happens which affects that the device switches off due to its protection function. In Fault mode, a $I_{IS(FAULT)}$ signal is presenting at IS pin during the DEN signal is "high".

6.2 Undervoltage on V_S

Between $V_{S(OP)}$ and $V_{S(UV)}$ the undervoltage mechanism is triggered. If the device is operative (in ON mode) and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the internal logic switches OFF the output channel.

As soon as the supply voltage V_S is above the operative threshold $V_{S(OP)}$, the channel is switched ON again. The restart is delayed with a time $t_{DELAY(UV)}$ which protects the device in case the undervoltage condition is caused by a short circuit event (according to AEC-Q100-012), as shown in **Figure 13**.

If the device is in OFF mode and the input is set to “high”, the channel will be switched ON if $V_S > V_{S(OP)}$ without waiting for $t_{DELAY(UV)}$.

Power Supply

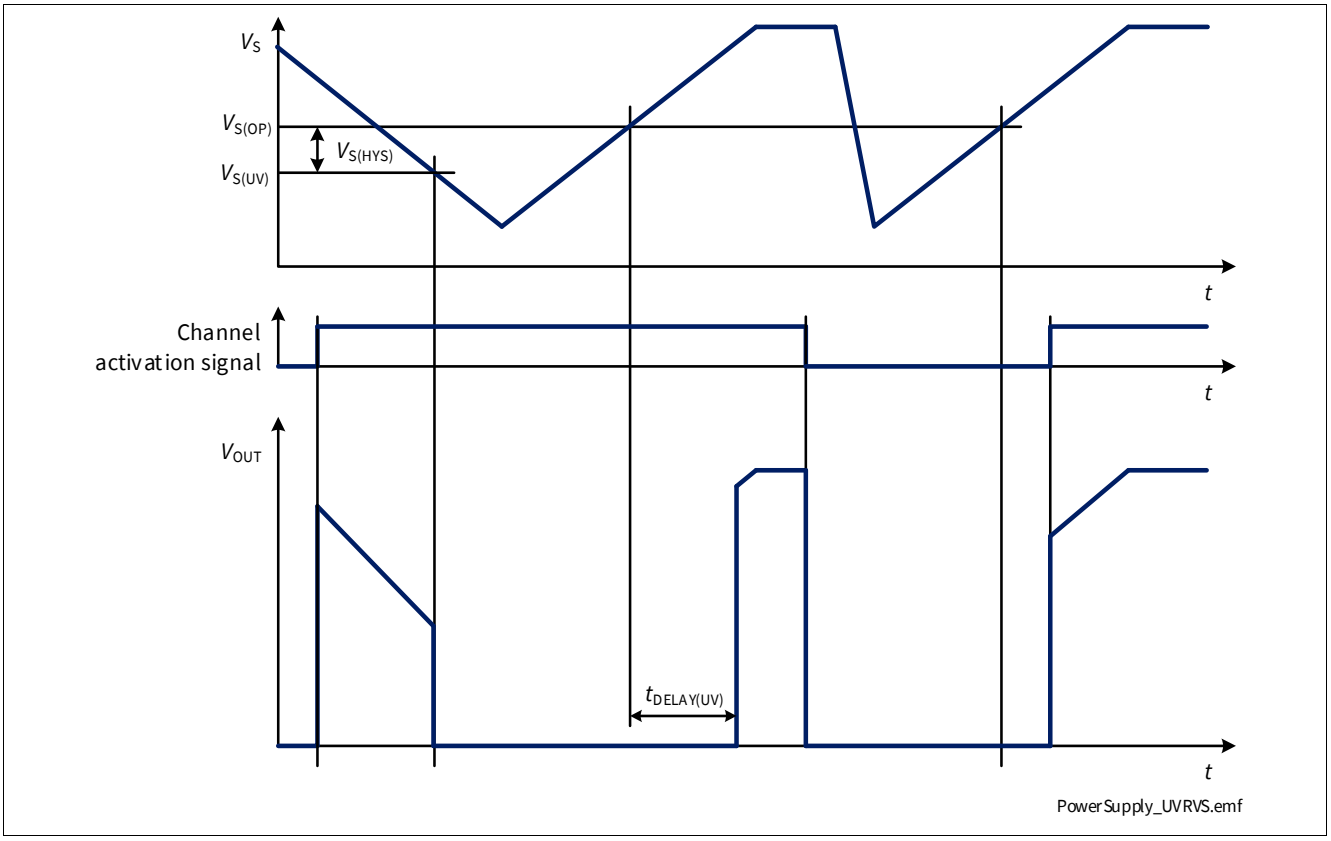


Figure 13 V_S undervoltage behavior

6.3 Electrical Characteristics Power Supply

V_S = 6 V to 18 V, T_J = -40 °C to +150 °C
Typical values: V_S = 13.5 V, T_J = 25 °C

Typical resistive load connected to the output for testing (unless otherwise specified):

R_L = 2.1 Ω

Table 9 Electrical Characteristics: Power Supply - General

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
VS pin							
Power Supply Undervoltage Shutdown	$V_{S(UV)}$	1.8	2.3	3.1	V	V_S decreasing IN = “high” From $V_{DS} \le 0.5$ V to $V_{DS} = V_S$ See **Figure 13**	P_6.4.0.1
Power Supply Minimum Operating Voltage	$V_{S(OP)}$	2.0	3.0	4.1	V	V_S increasing IN = “high” From $V_{DS} = V_S$ to $V_{DS} \le 0.5$ V See **Figure 13**	P_6.4.0.3
Power Supply Undervoltage Shutdown Hysteresis	$V_{S(HYS)}$	–	0.7	–	V	1) $V_{S(OP)} - V_{S(UV)}$ See **Figure 13**	P_6.4.0.6
Power Supply Undervoltage Recovery Time	$t_{DELAY(UV)}$	2.5	5	7.5	ms	$dV_S/dt \le 0.5$ V/µs $V_S \ge -1$ V See **Figure 13**	P_6.4.0.7
Breakdown Voltage between GND and VS Pins in Reverse Battery	$-V_{S(REV)}$	16	–	30	V	1) $I_{GND(REV)}$ = 7 mA T_J = 150 °C	P_6.4.0.9

1) Not subject to production test - specified by design.

6.4 Electrical Characteristics Power Supply - Product Specific

6.4.1 BTS7004-1EPP

Table 10 Electrical Characteristics: Power Supply BTS7004-1EPP

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Current Consumption in OFF Mode with Loads	$I_{VS(OFF)}$	–	0.01	0.5	µA	[1] V_S = 18 V V_{OUT} = 0 V IN = DEN = “low” $T_J \leq 85$ °C	P_6.5.21.1
Supply Current Consumption in OFF Mode with Loads	$I_{VS(OFF)}$	–	5	20	µA	V_S = 18 V V_{OUT} = 0 V IN = DEN = “low” T_J = 150 °C	P_6.5.21.2
Operating Current in ON_Diag Mode (Channel ON)	$I_{GND(ON\_D)}$	–	2	3	mA	V_S = 18 V IN = DEN = “high”	P_6.5.21.3
Operating Current in OFF_Diag Mode	$I_{GND(OFF\_D)}$	–	1.2	1.8	mA	V_S = 18 V IN = “low”; DEN = “high”	P_6.5.21.5

1) Not subject to production test - specified by design.

7 Power Stages

The high-side power stage is built using a N-channel vertical Power MOSFET with charge pump.

7.1 Output ON-State Resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature T_J. **Figure 14** shows the variation of $R_{DS(ON)}$ across the whole T_J range. The value “2” on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at T_J = 150 °C.

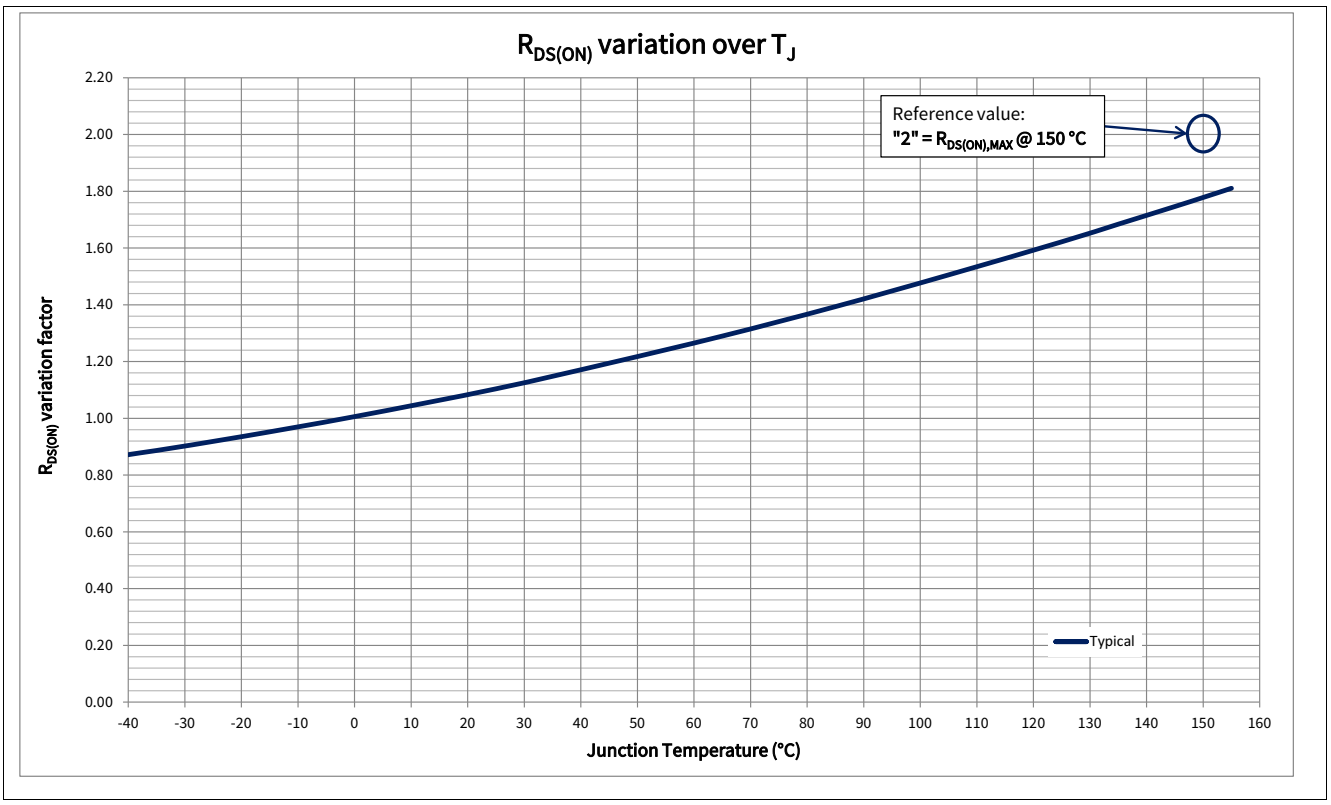


Figure 14 $R_{DS(ON)}$ variation factor

The behavior in Reverse Polarity is described in **Chapter 8.4.1**.

7.2 Switching loads

7.2.1 Switching Resistive Loads

When switching resistive loads, the switching times and slew rates shown in **Figure 15** can be considered. The switch energy values E_{ON} and E_{OFF} are proportional to load resistance and times t_{ON} and t_{OFF}.

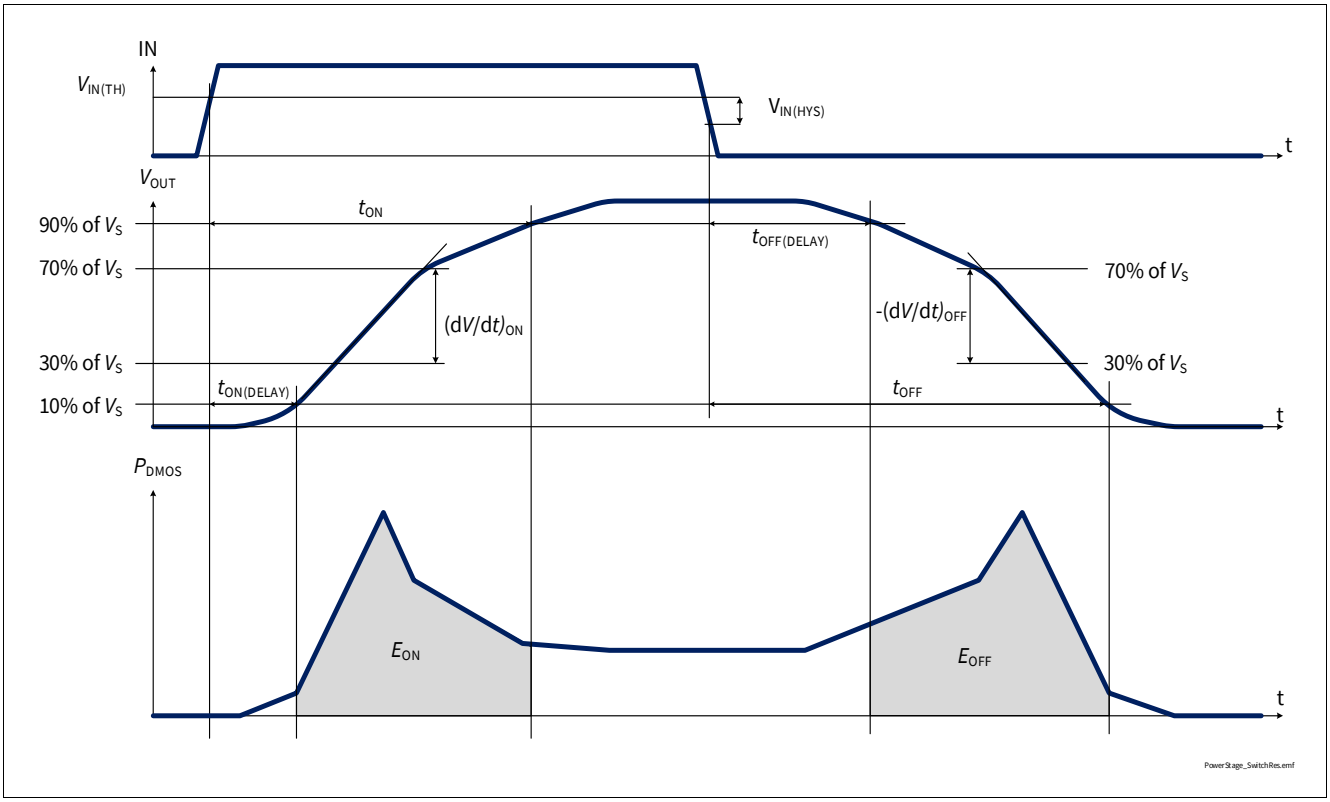


Figure 15 Switching a Resistive Load

7.2.2 Switching Inductive Loads

When switching OFF inductive loads with high-side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the negative output voltage so that $V_{DS} = V_{DS(CLAMP)}$. **Figure 16** shows a concept drawing of the implementation. The clamping structure is available in all operation modes listed in **Chapter 6.1**.

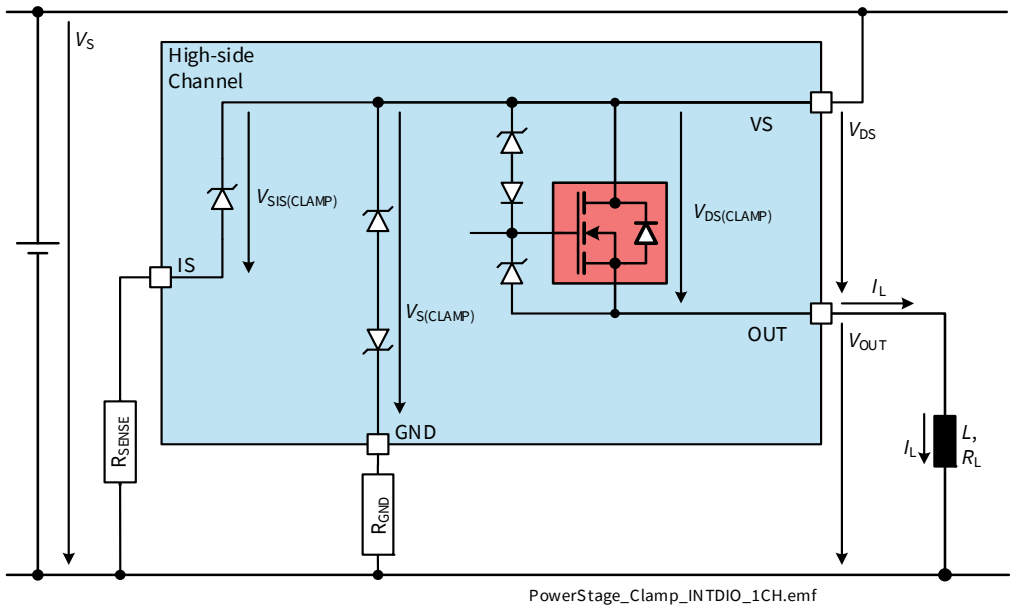


Figure 16 Output Clamp concept

During demagnetization of inductive loads, energy has to be dissipated in BTS7004-1EPP. The energy can be calculated with **Equation (7.1)**:

$$E = V_{DS(CLAMP)} \cdot \left[\frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}}\right) + I_L \right] \cdot \frac{L}{R_L} \quad (7.1)$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component. Please refer to **Chapter 4.2** for the maximum allowed values of E_{AS} (single pulse energy) and E_{AR} (repetitive energy).

7.2.3 Output Voltage Limitation

To increase the current sense accuracy, V_{DS} voltage is monitored. When the output current I_L decreases while the channel is diagnosed (DEN pin set to “high” - see **Figure 17**) bringing V_{DS} equal or lower than $V_{DS(SLC)}$, the output DMOS gate is partially discharged. This increases the output resistance so that $V_{DS} = V_{DS(SLC)}$ even for very small output currents. The V_{DS} increase allows the current sensing circuitry to work more efficiently, providing better k_{ILIS} accuracy for output current in the low range.

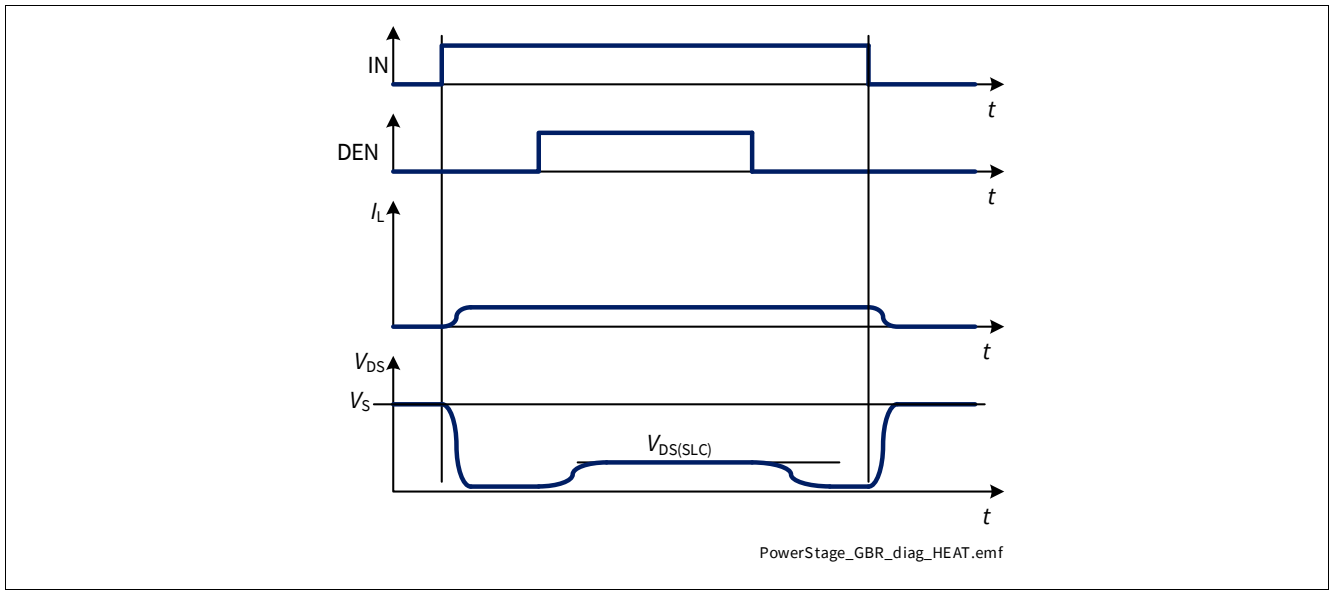


Figure 17 Output Voltage Limitation activation during diagnosis

7.3 Advanced Switching Characteristics

7.3.1 Inverse Current behavior

When $V_{OUT} > V_S$, a current I_{INV} flows into the power output transistor (see **Figure 18**). This condition is known as “Inverse Current”.

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses therefore an increase of overall device temperature. If the channel is in ON state, $R_{DS(INV)}$ can be expected and power dissipation in the output stage is comparable to normal operation in $R_{DS(ON)}$.

During Inverse Current condition, the channel remains in ON or OFF state as long as $|-I_L| < |-I_{L(INV)}|$.

With InverseON, it is possible to switch ON the channel during Inverse Current condition as long as $|-I_L| < |-I_{L(INV)}|$ (see **Figure 19**).

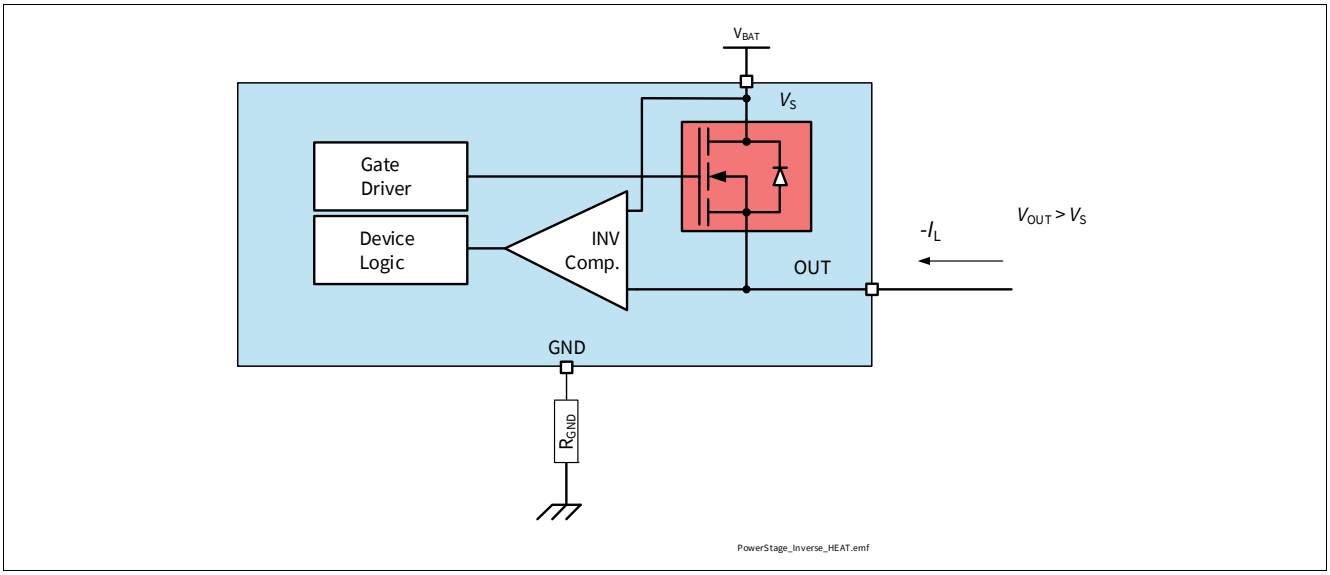


Figure 18 Inverse Current Circuitry

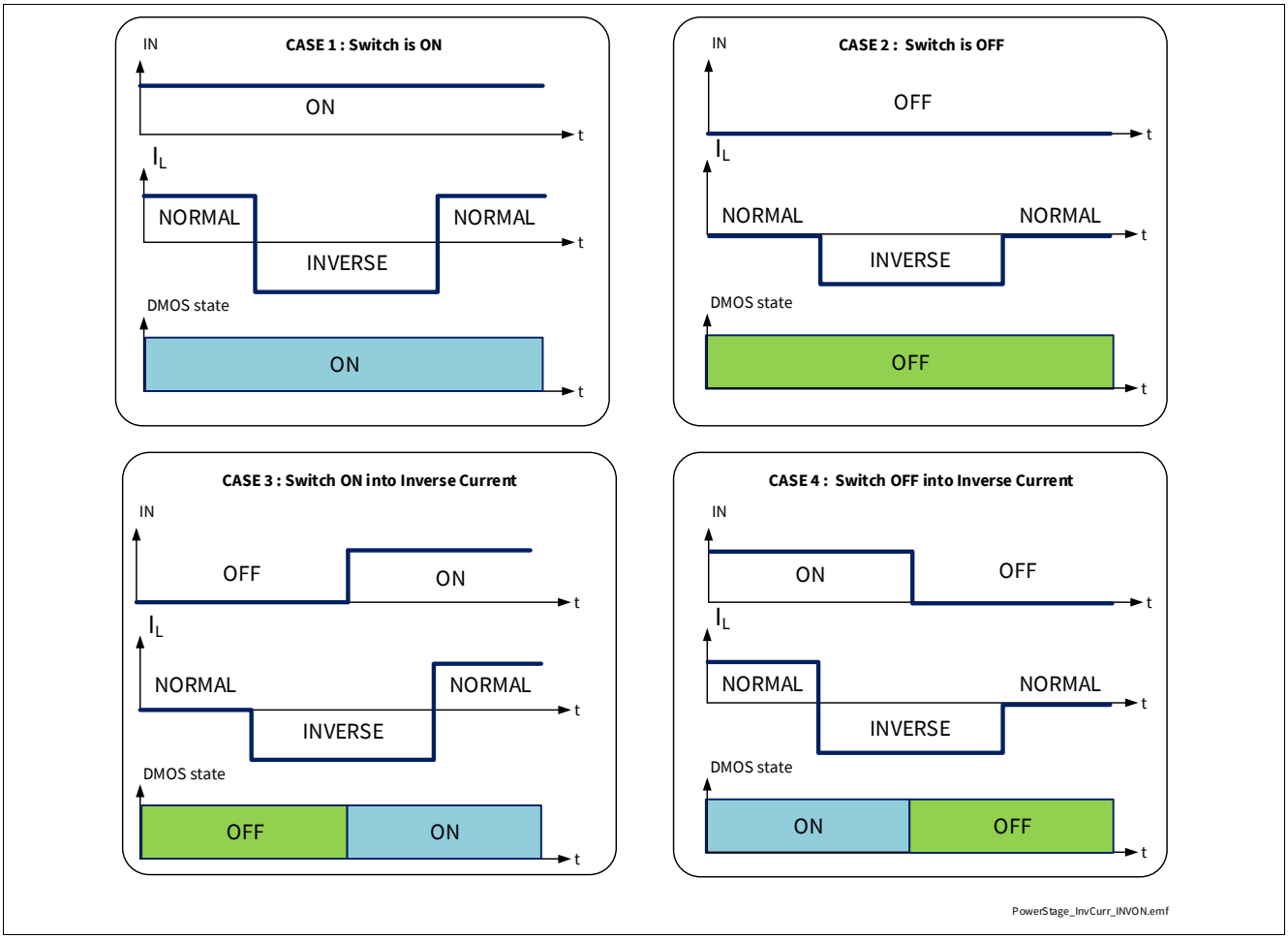


Figure 19 InverseON - Channel behavior in case of applied Inverse Current

Note: No protection mechanism like Overtemperature or Overload protection is active during applied Inverse Currents.

7.3.2 Cross Current robustness with H-Bridge configuration

When BTS7004-1EPP is used as high-side switch e.g. in a bridge configuration (therefore paired with a low-side switch as shown in **Figure 20**), the maximum slew rate applied to the output by the low-side switch must be lower than $|\,dV_{OUT}/dt\,|$. Otherwise the output stage may turn ON in linear mode (not in $R_{DS(ON)}$) while the low-side switch is commutating. This creates an unprotected overheating for the DMOS due to the cross-conduction current.

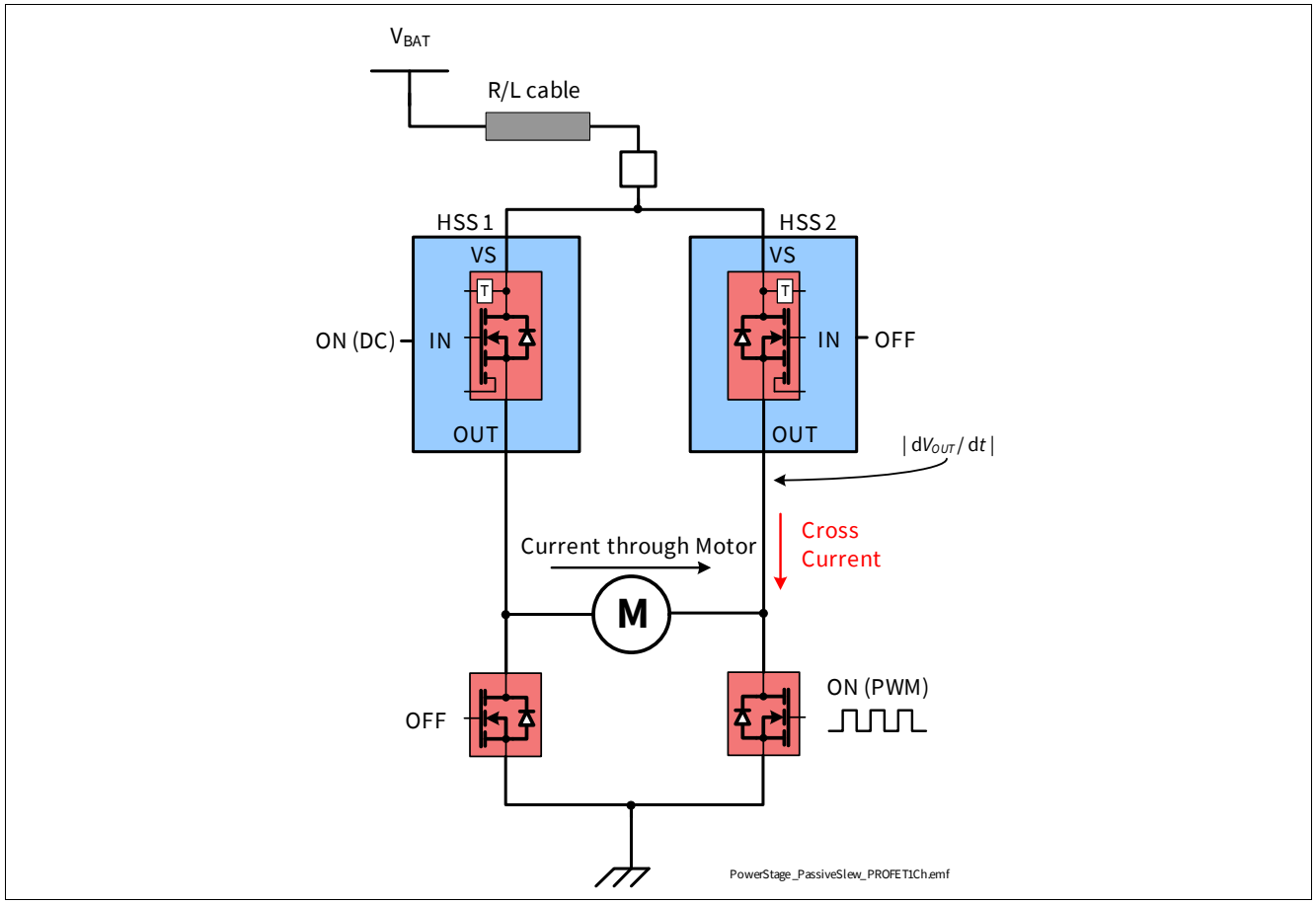


Figure 20 High-Side switch used in Bridge configuration