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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



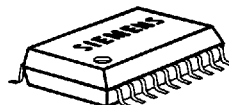
### Smart Two Channel Highside Power Switch

#### Product Summary

Overvoltage Protection	$V_{bb(AZ)}$	43	V
Operating voltage	$V_{bb(on)}$	5.0 ... 34	V
active channels:		one	two parallel
On-state resistance	$R_{ON}$	60	30
Nominal load current	$I_{L(NOM)}$	4.0	6.0
Current limitation	$I_{L(SC)}$	16	16

#### Features

- Overload protection
- Current limitation
- Short-circuit protection
- Thermal shutdown
- Overvoltage protection (including load dump)
- Fast demagnetization of inductive loads
- Reverse battery protection<sup>1)</sup>
- Undervoltage and overvoltage shutdown with auto-restart and hysteresis
- Open drain diagnostic output
- Open load detection in ON-state
- CMOS compatible input
- Loss of ground and loss of  $V_{bb}$  protection
- Electrostatic discharge (ESD) protection



#### Application

- $\mu$ C compatible power switch with diagnostic feedback for 12 V and 24 V DC grounded loads
- All types of resistive, inductive and capacitive loads
- Replaces electromechanical relays and discrete circuits

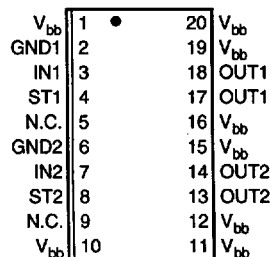
#### General Description

N channel vertical power FET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology. Fully protected by embedded protection functions.

#### Pin Definitions and Functions

Pin	Symbol	Function
1,10, 11,12, 15,16, 19,20	$V_{bb}$	<b>Positive power supply voltage.</b> Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
3	IN1	<b>Input 1,2,</b> activates channel 1,2 in case of logic high signal
7	IN2	
17,18	OUT1	<b>Output 1,2,</b> protected high-side power output of channel 1,2. Design the wiring for the max. short circuit current
13,14	OUT2	
4	ST1	<b>Diagnostic feedback 1,2</b> of channel 1,2, open drain, low on failure
8	ST2	
2	GND1	<b>Ground 1</b> of chip 1 (channel 1)
6	GND2	<b>Ground 2</b> of chip 2 (channel 2)
5,9	N.C.	<b>Not Connected</b>

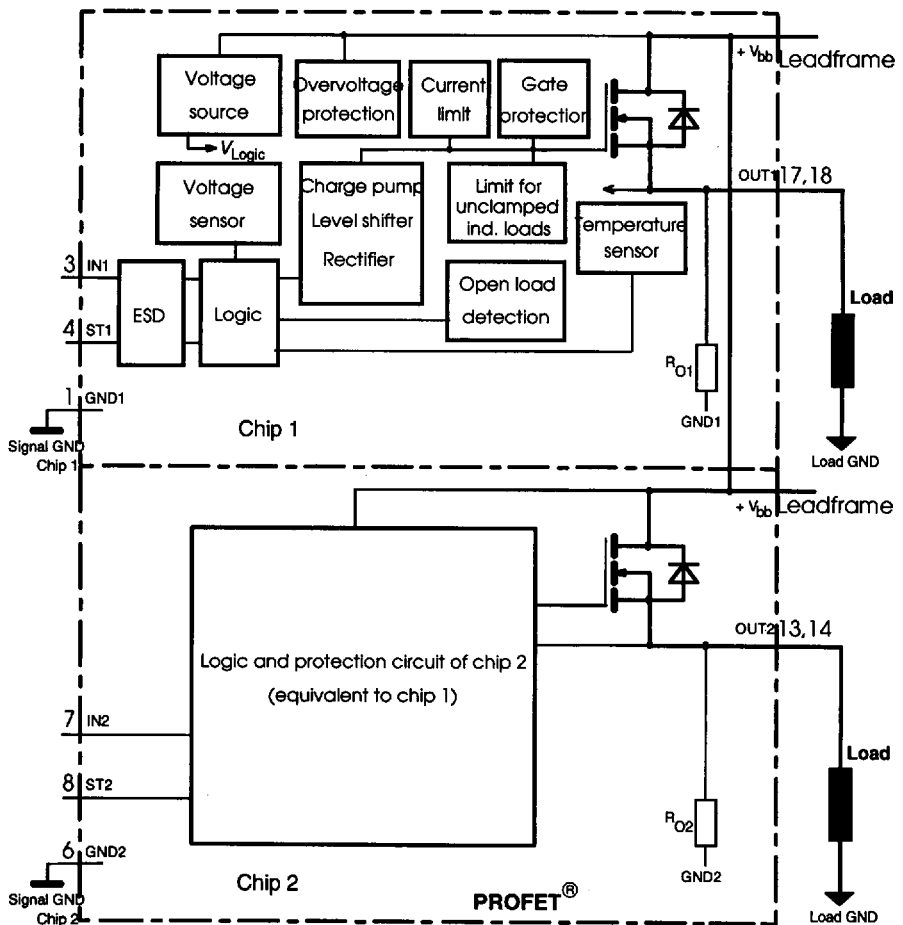
Pin configuration (top view)



1) With external current limit (e.g. resistor  $R_{GND}=150 \Omega$ ) in GND connection, resistor in series with ST connection, reverse load current limited by connected load.

### Block diagram

Two Channels; Open Load detection in on state;



Leadframe connected to pin 1, 10, 11, 12, 15, 16, 19, 20

**Maximum Ratings** at  $T_j = 25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 772)	$V_{bb}$	43	V
Supply voltage for full short circuit protection $T_{j,start} = -40 \dots +150^\circ\text{C}$	$V_{bb}$	34	V

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**Maximum Ratings** at  $T_j = 25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Values	Unit
Load current (Short-circuit current, see page 773)	$I_L$	self-limited	A
Load dump protection <sup>2)</sup> $V_{\text{LoadDump}} = U_A + V_s$ , $U_A = 13.5\text{ V}$ $R_i^3) = 2\ \Omega$ , $t_d = 200\text{ ms}$ ; $I_N = \text{low or high}$ , each channel loaded with $R_L = 3.4\ \Omega$ ,	$V_{\text{Load dump}}^4)$	60	V
Operating temperature range	$T_j$	-40 ... +150	$^\circ\text{C}$
Storage temperature range	$T_{\text{stg}}$	-55 ... +150	$^\circ\text{C}$
Power dissipation (DC) <sup>5)</sup> (all channels active)	$T_a = 25^\circ\text{C}$ : $T_a = 85^\circ\text{C}$ :	$P_{\text{tot}}$ 3.7 1.9	W
Inductive load switch-off energy dissipation, single pulse $V_{\text{bb}} = 12\text{ V}$ , $T_{j,\text{start}} = 150^\circ\text{C}^5)$ , $I_L = 4.0\text{ A}$ , $Z_L = 50\text{ m}\Omega$ one channel: $I_L = 6.0\text{ A}$ , $Z_L = 42\text{ m}\Omega$ two parallel channels: see diagrams on page 777 and page 778	$E_{\text{AS}}$	0.5 1.0	J
Electrostatic discharge capability (ESD) (Human Body Model)	$V_{\text{ESD}}$	1.0	kV
Input voltage (DC)	$V_{\text{IN}}$	-10 ... +16	V
Current through input pin (DC)	$I_{\text{IN}}$	$\pm 2.0$	mA
Current through status pin (DC) see internal circuit diagram page 776	$I_{\text{ST}}$	$\pm 5.0$	
Thermal resistance			
junction - soldering point <sup>5),6)</sup>	each channel: $R_{\text{thjs}}$	12	K/W
junction - ambient <sup>5)</sup>	one channel active: $R_{\text{thja}}$	41	
	all channels active:	34	

2) Supply voltages higher than  $V_{\text{bb(AZ)}}$  require an external current limit for the GND and status pins, e.g. with a 150  $\Omega$  resistor in the GND connection and a 15 k $\Omega$  resistor in series with the status pin. A resistor for input protection is integrated.

3)  $R_i$  = internal resistance of the load dump test pulse generator

4)  $V_{\text{Load dump}}$  is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

5) Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70 $\mu\text{m}$  thick) copper area for  $V_{\text{bb}}$  connection. PCB is vertical without blown air. See page 783

6) Soldering point: upper side of solder edge of device pin 15. See page 783

## Electrical Characteristics

Parameter and Conditions, each of the two channels at $T_j = 25^\circ\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

## Load Switching Capabilities and Characteristics

On-state resistance ( $V_{bb}$ to OUT) $I_L = 2\text{ A}$ each channel, $T_j = 25^\circ\text{C}$ : $T_j = 150^\circ\text{C}$ :  two parallel channels, $T_j = 25^\circ\text{C}$ :	$R_{ON}$	--	50 100	60 120	$\text{m}\Omega$
Nominal load current one channel active: two parallel channels active: Device on PCB <sup>5)</sup> , $T_a = 85^\circ\text{C}$ , $T_j \leq 150^\circ\text{C}$	$I_{L(NOM)}$	3.6 5.5	4.0 6.0	--	A
Output current while GND disconnected or pulled up; $V_{bb} = 30\text{ V}$ , $V_{IN} = 0$ , see diagram page 777	$I_{L(GNDhigh)}$	--	--	10	mA
Turn-on time to 90% $V_{OUT}$ : Turn-off time to 10% $V_{OUT}$ : $R_L = 12\ \Omega$ , $T_j = -40\dots+150^\circ\text{C}$	$t_{on}$ $t_{off}$	80 80	200 230	400 450	$\mu\text{s}$
Slew rate on 10 to 30% $V_{OUT}$ , $R_L = 12\ \Omega$ , $T_j = -40\dots+150^\circ\text{C}$ :	$dV/dt_{on}$	0.1	--	1	$\text{V}/\mu\text{s}$
Slew rate off 70 to 40% $V_{OUT}$ , $R_L = 12\ \Omega$ , $T_j = -40\dots+150^\circ\text{C}$ :	$-dV/dt_{off}$	0.1	--	1	$\text{V}/\mu\text{s}$

## Operating Parameters

Operating voltage <sup>7)</sup> $T_j = -40\dots+150^\circ\text{C}$ :	$V_{bb(on)}$	5.0	--	34	V
Undervoltage shutdown $T_j = -40\dots+150^\circ\text{C}$ :	$V_{bb(under)}$	3.5	--	5.0	V
Undervoltage restart $T_j = -40\dots+25^\circ\text{C}$ : $T_j = +150^\circ\text{C}$ :	$V_{bb(u\ rst)}$	--	--	5.0 7.0	V
Undervoltage restart of charge pump see diagram page 782 $T_j = -40\dots+150^\circ\text{C}$ :	$V_{bb(ucp)}$	--	5.6	7.0	V
Undervoltage hysteresis $\Delta V_{bb(under)} = V_{bb(u\ rst)} - V_{bb(under)}$	$\Delta V_{bb(under)}$	--	0.2	--	V
Overvoltage shutdown $T_j = -40\dots+150^\circ\text{C}$ :	$V_{bb(over)}$	34	--	43	V
Overvoltage restart $T_j = -40\dots+150^\circ\text{C}$ :	$V_{bb(o\ rst)}$	33	--	--	V
Overvoltage hysteresis $T_j = -40\dots+150^\circ\text{C}$ :	$\Delta V_{bb(over)}$	--	0.5	--	V
Overvoltage protection <sup>8)</sup> $T_j = -40\dots+150^\circ\text{C}$ : $I_{bb} = 40\text{ mA}$	$V_{bb(AZ)}$	42	47	--	V
Standby current, all channels off $T_j = 25^\circ\text{C}$ : $V_{IN} = 0$ $T_j = 150^\circ\text{C}$ :	$I_{bb(off)}$	--	20 29	50 56	$\mu\text{A}$
Leakage output current (included in $I_{bb(off)}$ ) $V_{IN} = 0$	$I_{L(off)}$	--	--	12	$\mu\text{A}$

7) At supply voltage increase up to  $V_{bb} = 5.6\text{ V}$  typ without charge pump,  $V_{OUT} = V_{bb} - 2\text{ V}$

8) see also  $V_{ON(CL)}$  in circuit diagram on page 776.

Parameter and Conditions, each of the two channels at $T_j = 25^\circ\text{C}$ , $V_{bb} = 12\text{V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	
Operating current <sup>9)</sup> , $V_{IN} = 5\text{V}$ , $T_j = -40\dots+150^\circ\text{C}$ $I_{GND} = I_{GND1} + I_{GND2}$ , one channel on: two channels on:	$I_{GND}$	--	1.8 3.6	3.5 7	mA

**Protection Functions**

Initial peak short circuit current limit, (see timing diagrams, page 780) each channel, $T_j = -40^\circ\text{C}$ : $T_j = 25^\circ\text{C}$ : $T_j = +150^\circ\text{C}$ : two parallel channels	$I_{L(SCp)}$	21 15 11	32 25 17	43 35 24	A
		twice the current of one channel			
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel two parallel channels (see timing diagrams, page 780)	$I_{L(SCr)}$	--	16 16	--	A
Initial short circuit shutdown time $T_{j,start} = -40^\circ\text{C}$ : $T_{j,start} = 25^\circ\text{C}$ : (see page 779 and timing diagrams on page 780)	$t_{off(SC)}$	--	5 4	--	ms
Output clamp (inductive load switch off) <sup>10)</sup> at $V_{ON(CL)} = V_{bb} - V_{OUT}$	$V_{ON(CL)}$	--	47	--	V
Thermal overload trip temperature	$T_{jt}$	150	--	--	$^\circ\text{C}$
Thermal hysteresis	$\Delta T_{jt}$	--	10	--	K

**Reverse Battery**

Reverse battery voltage <sup>11)</sup>	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ( $V_{out} > V_{bb}$ ) $I_L = -4.0\text{A}$ , $T_j = +150^\circ\text{C}$	$-V_{ON}$	--	610	--	mV

<sup>9)</sup> Add  $I_{ST}$ , if  $I_{ST} > 0$

<sup>10)</sup> If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest  $V_{ON(CL)}$



<sup>11)</sup> Requires a  $150\ \Omega$  resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Note that the power dissipation is higher compared to normal operating conditions due to the voltage drop across the intrinsic drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 771 and circuit page 776).

Parameter and Conditions, each of the two channels at $T_j = 25^\circ\text{C}$ , $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	max	

### Diagnostic Characteristics

Open load detection current, (on-condition) each channel, $T_j = -40^\circ\text{C}$ : $T_j = 25^\circ\text{C}$ : $T_j = 150^\circ\text{C}$ : two parallel channels	$I_{L(OL)}$	20 20 20	-- -- --	850 750 750	mA
		twice the current of one channel			
Open load detection voltage <sup>12)</sup> $T_j = -40..+150^\circ\text{C}$ :	$V_{OUT(OL)}$	2	3	4	V
Internal output pull down (OUT to GND), $V_{OUT} = 5\text{ V}$ $T_j = -40..+150^\circ\text{C}$ :	$R_O$	4	10	30	k $\Omega$

### Input and Status Feedback<sup>13)</sup>

Input resistance (see circuit page 776) $T_j = -40..+150^\circ\text{C}$ :	$R_i$	2.5	3.5	6	k $\Omega$
Input turn-on threshold voltage  $T_j = -40..+150^\circ\text{C}$ :	$V_{IN(T+)}$	1.7	--	3.5	V
Input turn-off threshold voltage  $T_j = -40..+150^\circ\text{C}$ :	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.5	--	V
Off state input current $T_j = -40..+150^\circ\text{C}$ : $V_{IN} = 0.4\text{ V}$ :	$I_{IN(off)}$	1	--	50	$\mu\text{A}$
On state input current $T_j = -40..+150^\circ\text{C}$ : $V_{IN} = 5\text{ V}$ :	$I_{IN(on)}$	20	50	90	$\mu\text{A}$
Delay time for status with open load after switch off (see timing diagrams, page 781), $T_j = -40..+150^\circ\text{C}$ :	$t_{d(ST-OL4)}$	100	520	1000	$\mu\text{s}$
Status invalid after positive input slope (open load) $T_j = -40..+150^\circ\text{C}$ :	$t_{d(ST)}$	--	250	600	$\mu\text{s}$
Status output (open drain) Zener limit voltage $T_j = -40..+150^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ : ST low voltage $T_j = -40..+25^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ : $T_j = +150^\circ\text{C}$ , $I_{ST} = +1.6\text{ mA}$ :	$V_{ST(high)}$ $V_{ST(low)}$	5.4 -- --	6.1 -- --	-- 0.4 0.6	V

<sup>12)</sup> External pull up resistor required for open load detection in off state.

<sup>13)</sup> If ground resistors  $R_{GND}$  are used, add the voltage drop across these resistors.

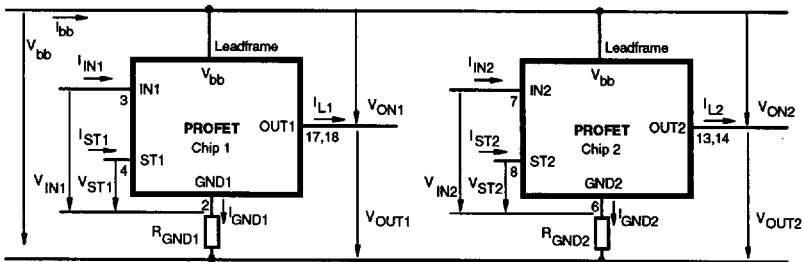
### Truth Table

Channel 1	Input 1	Output 1	Status 1
Channel 2	Input 2	Output 2	Status 2
	level	level	BTS 726L1
Normal operation	L	L	H
	H	H	H
Open load	L	Z	H (L <sup>14</sup> )
	H	H	L
Short circuit to V <sub>bb</sub>	L	H	L <sup>15</sup>
	H	H	H (L <sup>16</sup> )
Overtemperature	L	L	H
	H	L	L
Under-voltage	L	L	H
	H	L	H
Overvoltage	L	L	H
	H	L	H

L = "Low" Level      X = don't care      Z = high impedance, potential depends on external circuit  
 H = "High" Level      Status signal valid after the time delay shown in the timing diagrams

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

### Terms



Leadframe ( $V_{bb}$ ) is connected to pin 1,10,11,12,15,16,19,20

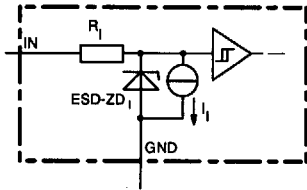
External  $R_{GND}$  optional; two resistors  $R_{GND1}$ ,  $R_{GND2} = 150 \Omega$  or a single resistor  $R_{GND} = 75 \Omega$  for reverse battery protection up to the max. operating voltage.

- 14) With external resistor between output and  $V_{bb}$
- 15) An external short of output to  $V_{bb}$  in the off state causes an internal current from output to ground. If  $R_{GND}$  is used, an offset voltage at the GND and ST pins will occur and the  $V_{ST\ low}$  signal may be erroneous.
- 16) Low resistance to  $V_{bb}$  may be detected by no-load-detection

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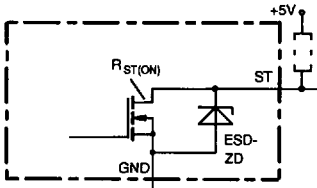


### Input circuit (ESD protection), IN1 or IN2



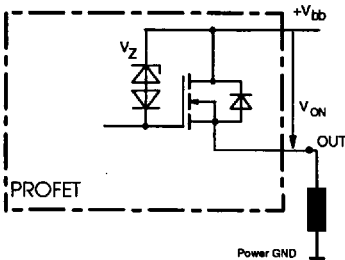
ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

### Status output, ST1 or ST2



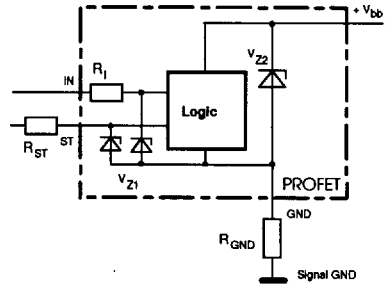
ESD-Zener diode: 6.1 V typ., max 5.0 mA;  $R_{ST(ON)} < 380 \Omega$  at 1.6 mA, ESD zener diodes are not to be used as voltage clamp at DC conditions. Operation in this mode may result in a drift of the zener voltage (increase of up to 1 V).

### Inductive and overvoltage output clamp, OUT1 or OUT2



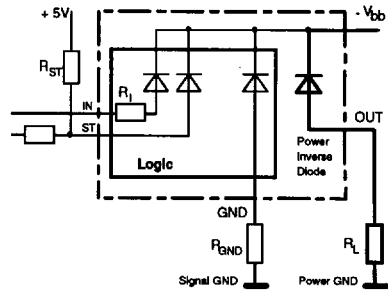
$V_{ON}$  clamped to  $V_{ON(CL)} = 47 \text{ V}$  typ.

### Overvoltage protection of logic part GND1 or GND2



$V_{Z1} = 6.1 \text{ V}$  typ.,  $V_{Z2} = 47 \text{ V}$  typ.,  $R_1 = 3.5 \text{ k}\Omega$  typ.,  $R_{GND} = 150 \Omega$ ,  $R_{ST} = 15 \text{ k}\Omega$  nominal.

### Reverse battery protection



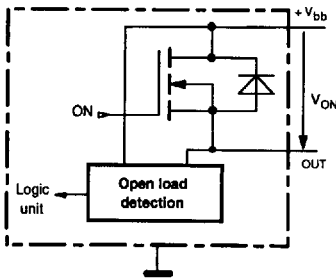
$R_{GND} = 150 \Omega$ ,  $R_1 = 3.5 \text{ k}\Omega$  typ.

Temperature protection is not active during inverse current operation.

### Open-load detection, OUT1 or OUT2

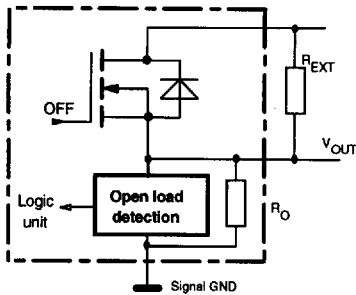
ON-state diagnostic condition:

$$V_{ON} < R_{ON} \cdot I_{L(OL)}; \text{IN high}$$

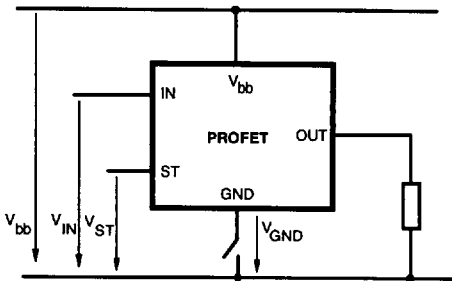


OFF-state diagnostic condition:

$$V_{OUT} > 3 \text{ V typ.}; \text{IN low}$$

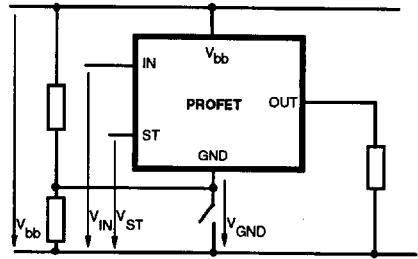


### GND disconnect



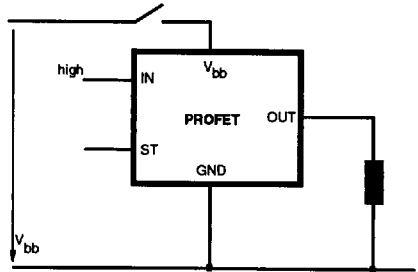
Any kind of load. In case of IN=high is  $V_{OUT} = V_{IN} - V_{IN(T+)}$ .  
Due to  $V_{GND} > 0$ , no  $V_{ST} = \text{low signal}$  available.

### GND disconnect with GND pull up



Any kind of load. If  $V_{GND} > V_{IN} - V_{IN(T+)}$  device stays off  
Due to  $V_{GND} > 0$ , no  $V_{ST} = \text{low signal}$  available.

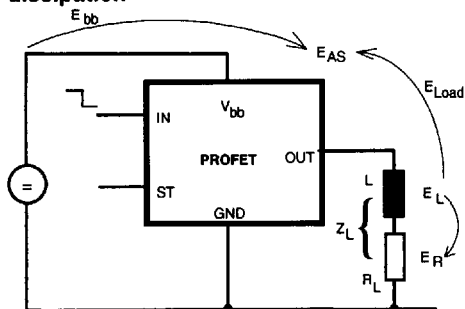
### Vbb disconnect with energized inductive load



For an inductive load current up to the limit defined by  $E_{AS}$   
(max. ratings see page 771 and diagram on page 778)  
each switch is protected against loss of  $V_{bb}$ .

Consider at your PCB layout that in the case of  $V_{bb}$  disconnection with energized inductive load the whole load current flows through the GND connection.

## Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = \frac{1}{2} \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

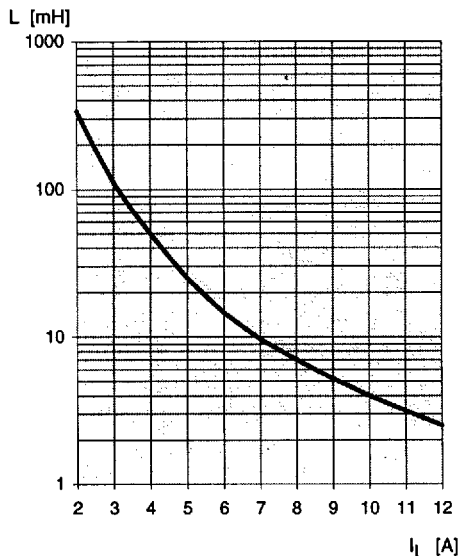
$$E_{AS} = E_{bb} + E_L \cdot E_R = \int V_{ON(CL)} \cdot i_L(t) dt,$$

with an approximate solution for  $R_L > 0 \Omega$ :

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left( 1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

### Maximum allowable load inductance for a single switch off (one channel)<sup>5)</sup>

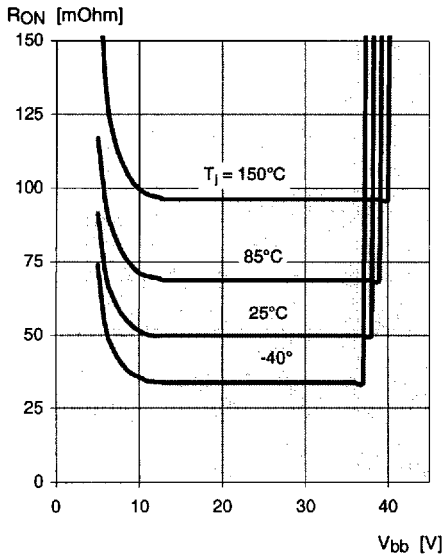
$L = f(I_L)$ ;  $T_{j,start} = 150^\circ\text{C}$ ,  $V_{bb} = 12\text{V}$ ,  $R_L = 0 \Omega$



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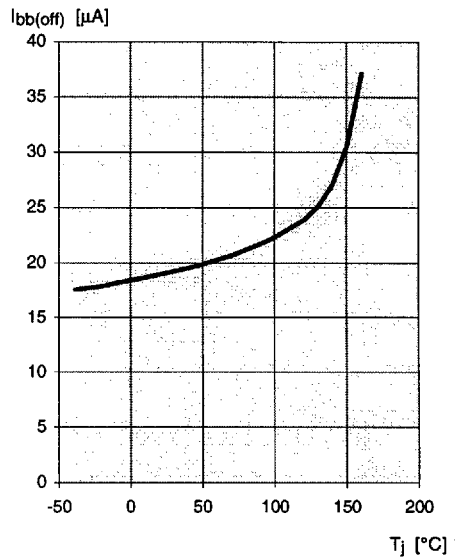
### Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j)$ ;  $I_L = 2\text{ A}$ ,  $I_N = \text{high}$



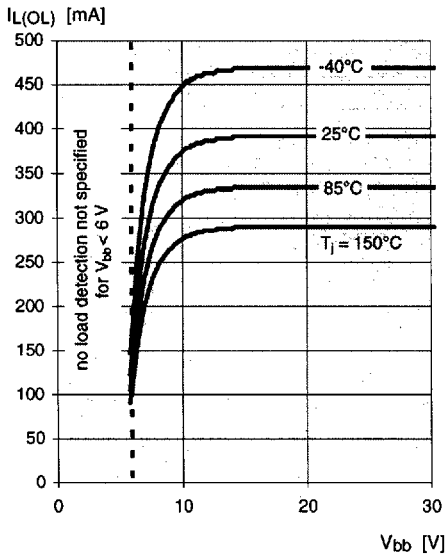
### Typ. standby current

$I_{bb(off)} = f(T_j)$ ;  $V_{bb} = 9 \dots 34\text{ V}$ ,  $I_{N1,2} = \text{low}$



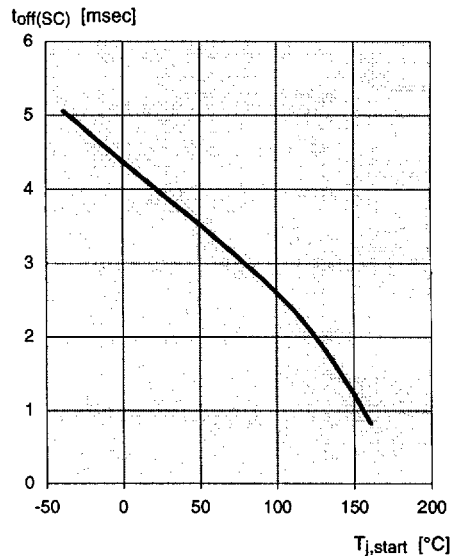
### Typ. open load detection current

$I_{L(OL)} = f(V_{bb}, T_j)$ ;  $I_N = \text{high}$



### Typ. initial short circuit shutdown time

$t_{off(SC)} = f(T_{j,start})$ ;  $V_{bb} = 12\text{ V}$

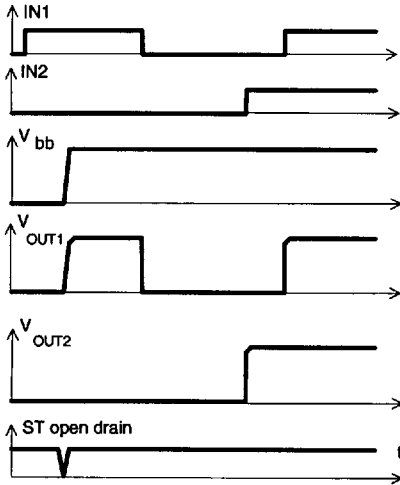


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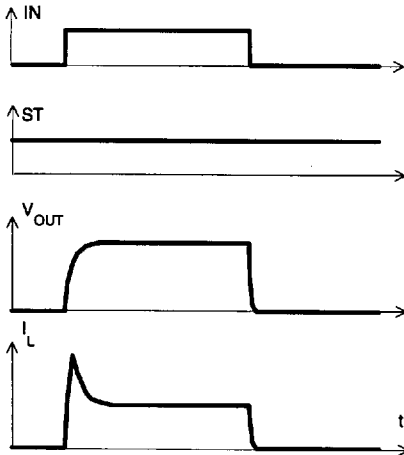
## Timing diagrams

Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

**Figure 1a:**  $V_{bb}$  turn on:

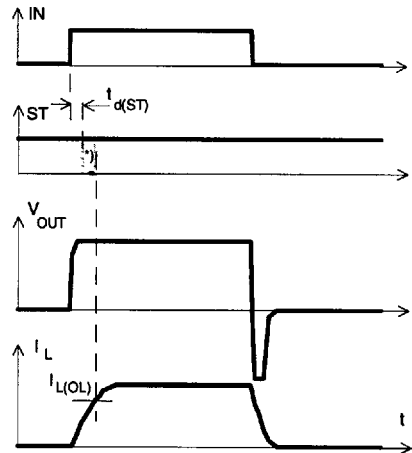


**Figure 2a:** Switching a lamp:



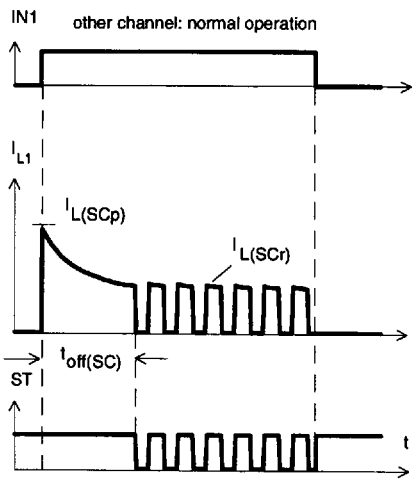
The initial peak current should be limited by the lamp and not by the initial short circuit current  $I_{L(SCp)} = 25$  A typ. of the device.

**Figure 2b:** Switching an inductive load



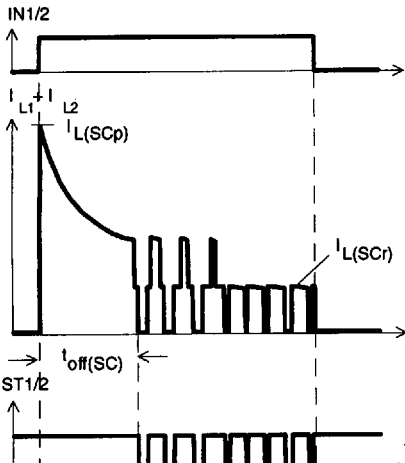
\*) if the time constant of load is too large, open-load-status may occur

**Figure 3a:** Turn on into short circuit:  
shut down by overtemperature, restart by cooling



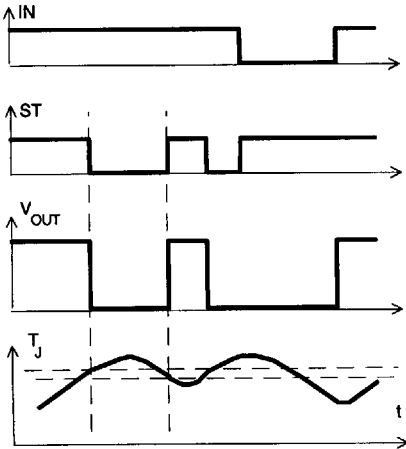
Heating up of the chip may require several milliseconds, depending on external conditions ( $t_{off(SC)}$  vs.  $T_{j,start}$  see page 779)

**Figure 3b:** Turn on into short circuit: shut down by overtemperature, restart by cooling (two parallel switched channels 1 and 2)

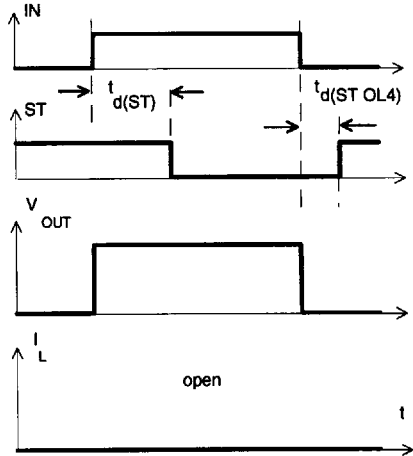


ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

**Figure 4a:** Overtemperature: Reset if  $T_j < T_{jt}$

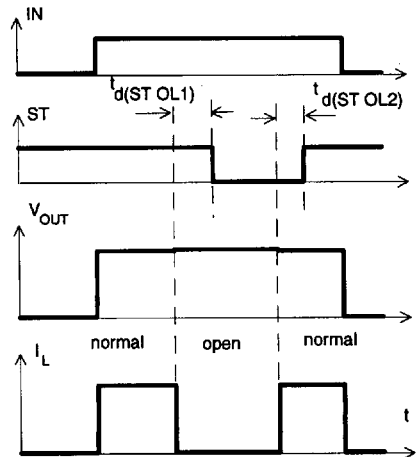


**Figure 5a:** Open load: detection in ON-state, turn on/off to open load



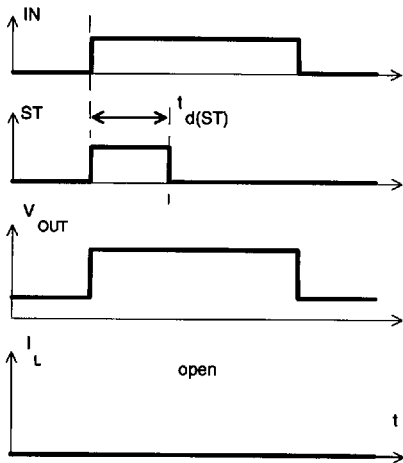
The status delay time  $t_d(STOL4)$  allows to distinguish between the failure modes "open load in ON-state" and "overtemperature".

**Figure 5b:** Open load: detection in ON-state, open load occurs in on-state

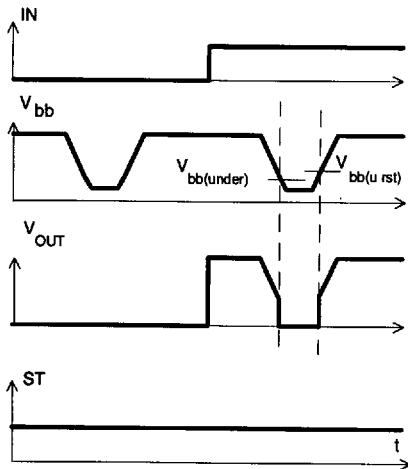


$t_{d(ST OL1)} = 20 \mu s$  typ.,  $t_{d(ST OL2)} = 10 \mu s$  typ

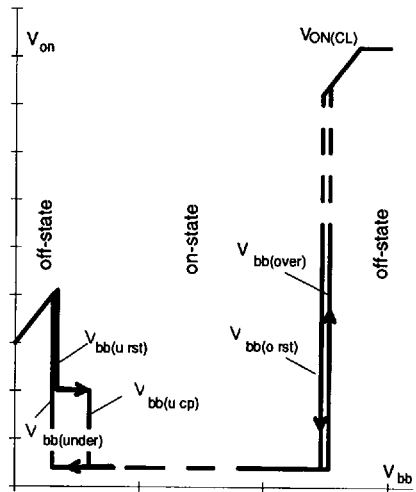
**Figure 5c:** Open load: detection in ON- and OFF-state (with  $R_{EXT}$ ), turn on/off to open load



**Figure 6a:** Undervoltage:

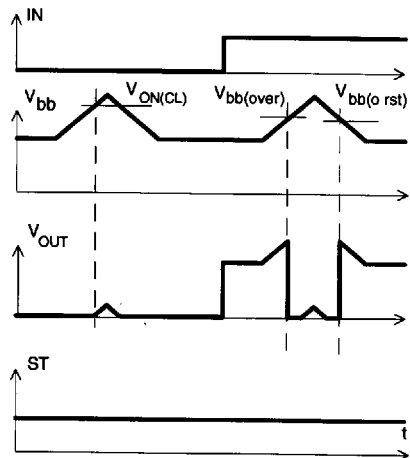


**Figure 6b:** Undervoltage restart of charge pump



IN = high, normal load conditions.  
Charge pump starts at  $V_{bb(u cp)} = 5.6 V$  typ.

**Figure 7a:** Overvoltage:

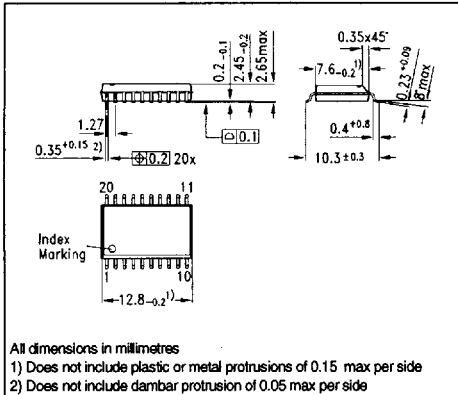


## Package and Ordering Code

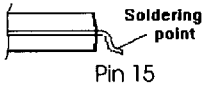
Standard P-DSO-20-9

Ordering Code

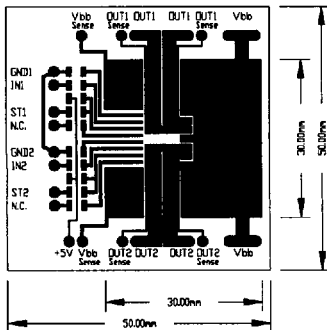
BTS726L1	Q67060-S7003-A2
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Definition of soldering point with temperature  $T_s$ :  
 upper side of solder edge of device pin 15.



Printed circuit board (FR4, 1.5mm thick, one layer  
 $70\mu\text{m}$ ,  $6\text{cm}^2$  active heatsink area) as a reference for  
 max. power dissipation  $P_{tot}$ , nominal load current  
 $I_{L(NOM)}$  and thermal resistance  $R_{thja}$



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