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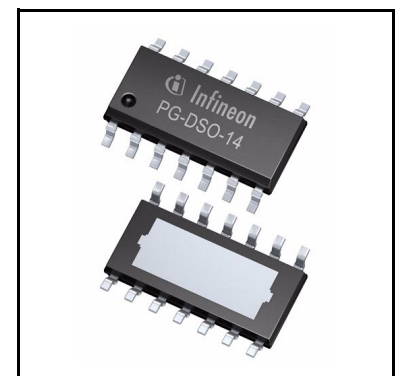
PROFET™+ 24V

BTT6030-2EKB

Smart High-Side Power Switch Dual Channel, 32 mΩ



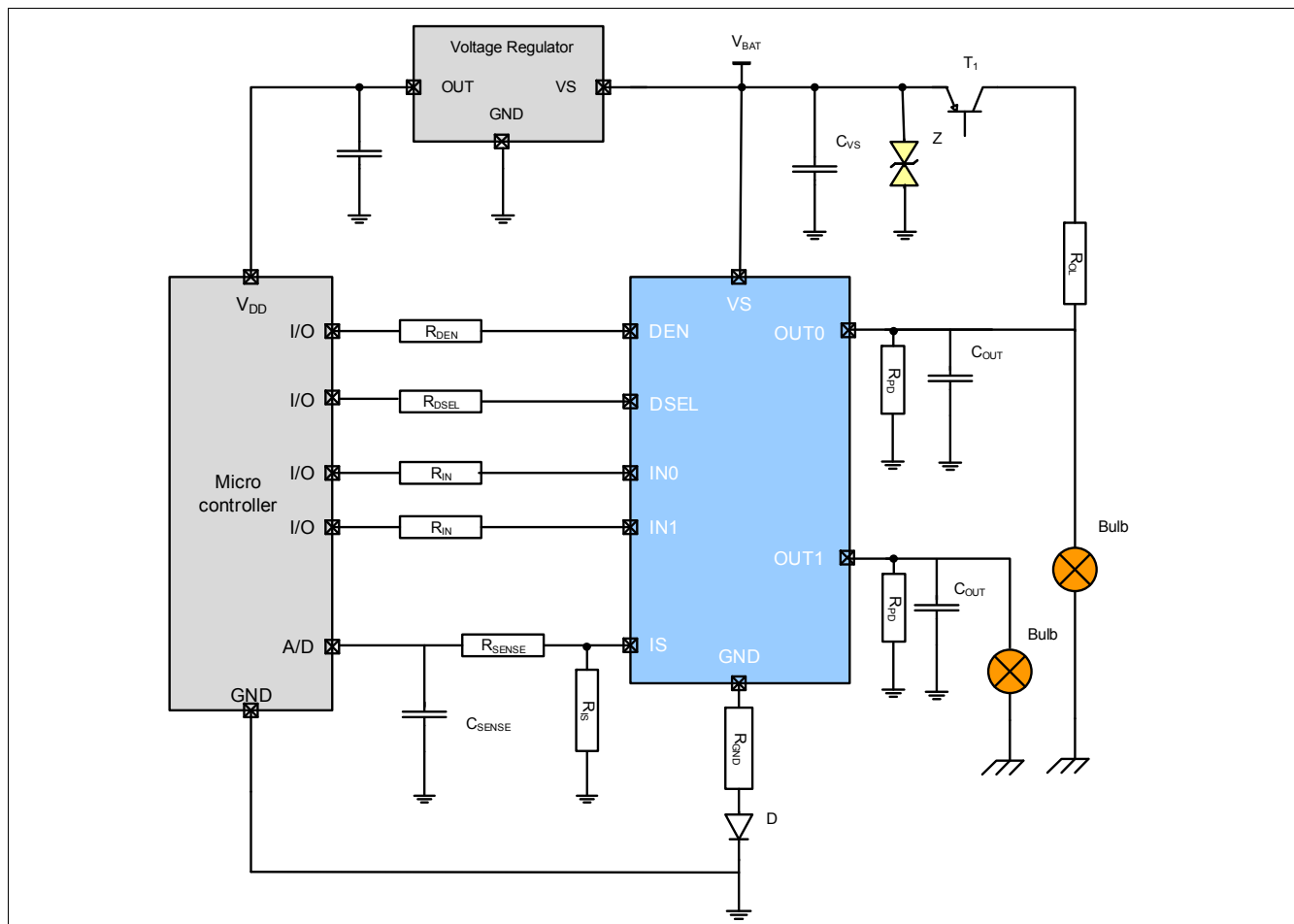
Package	PG-DSO-14-40 EP
Marking	BTT6030-2EKB



1 Overview

Application

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits
- Most suitable for loads with high inrush current, such as lamps
- Suitable for 24 V trucks + trailer and transportation systems



Application Diagram with BTT6030-2EKB

Overview

Basic Features

- Two channel device
- Very low stand-by current
- 3.3 V and 5 V compatible logic inputs
- Electrostatic discharge protection (ESD)
- Optimized electromagnetic compatibility
- Logic ground independent from load ground
- Very low power DMOS leakage current in OFF state
- Green product (RoHS compliant)
- AEC qualified

Description

The BTT6030-2EKB is a 32 mΩ dual channel Smart High-Side Power Switch, embedded in a PG-DSO-14-40 EP, Exposed Pad package, providing protective functions and diagnosis. The power transistor is built by an N-channel vertical power MOSFET with charge pump. The device is integrated in Smart6 HV technology. It is specially designed to drive lamps up to 2 * P21W 24V, as well as LEDs in the harsh automotive environment.

Table 1 Product Summary

Parameter	Symbol	Value
Operating voltage range	$V_{S(OP)}$	5 V ... 36 V
Maximum supply voltage	$V_{S(LD)}$	65 V
Maximum ON state resistance at $T_J = 150\text{ °C}$ per channel	$R_{DS(ON)}$	62 mΩ
Nominal load current (one channel active)	$I_{L(NOM)1}$	6 A
Nominal load current (both channels active)	$I_{L(NOM)2}$	4 A
Typical current sense ratio	k_{ILIS}	2240
Minimum current limitation	$I_{L5(SC)}$	40 A
Maximum standby current with load at $T_J = 25\text{ °C}$	$I_{S(OFF)}$	500 nA

Diagnostic Functions

- Proportional load current sense for both channels multiplexed
- Open load in ON and OFF
- Short circuit to battery and ground
- Overtemperature
- Stable diagnostic signal during short circuit
- Enhanced k_{ILIS} dependency with temperature and load current

Protection Functions

- Stable behavior during undervoltage
- Reverse polarity protection with external components
- Secure load turn-off during logic ground disconnect with external components
- Overtemperature protection with latch
- Overvoltage protection with external components
- Voltage dependent current limitation
- Enhanced short circuit protection for up to 40 m cables

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Block Diagram

2 Block Diagram

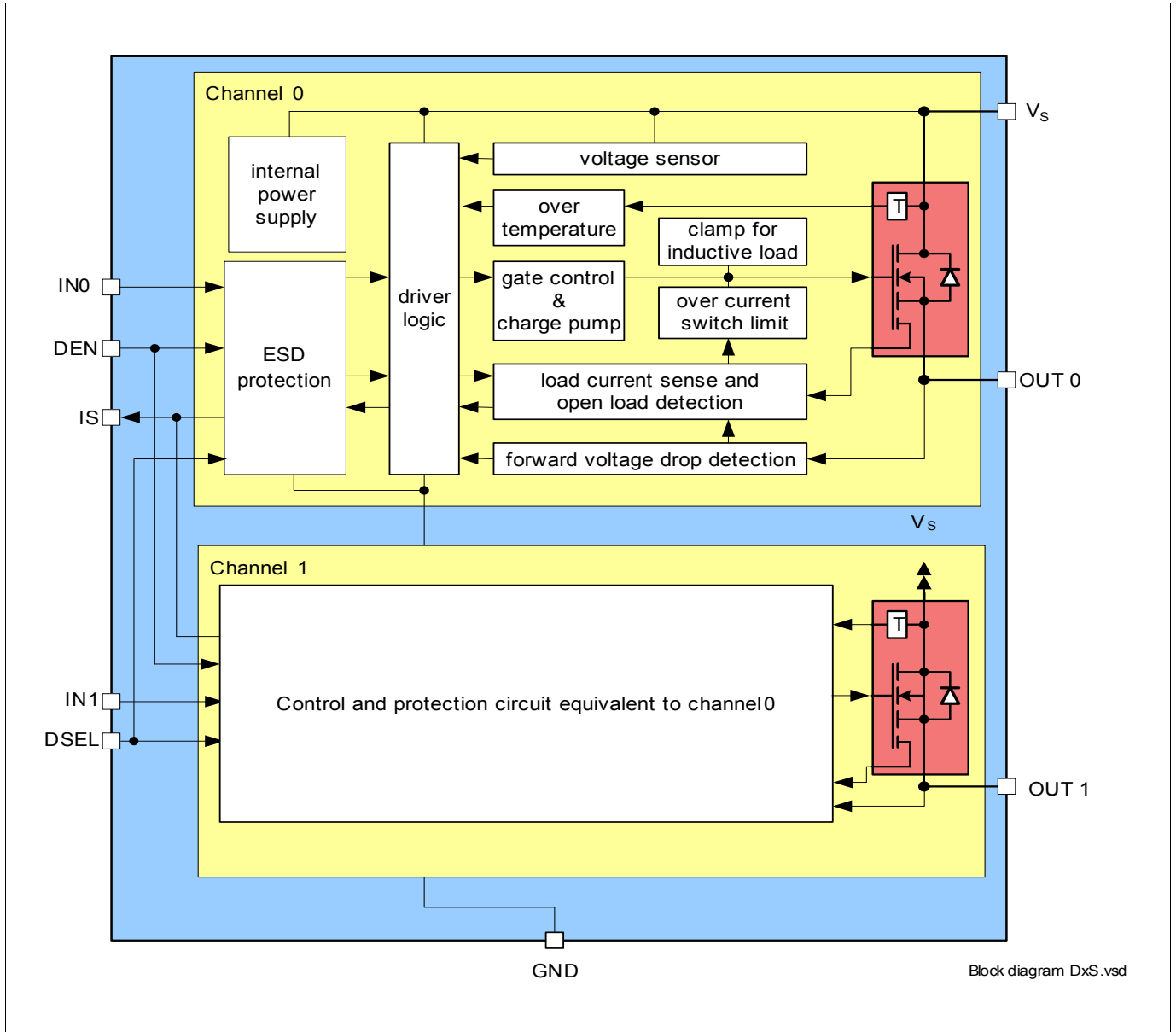


Figure 1 Block Diagram for the BTT6030-2EKB

Pin Configuration

3 Pin Configuration

3.1 Pin Assignment

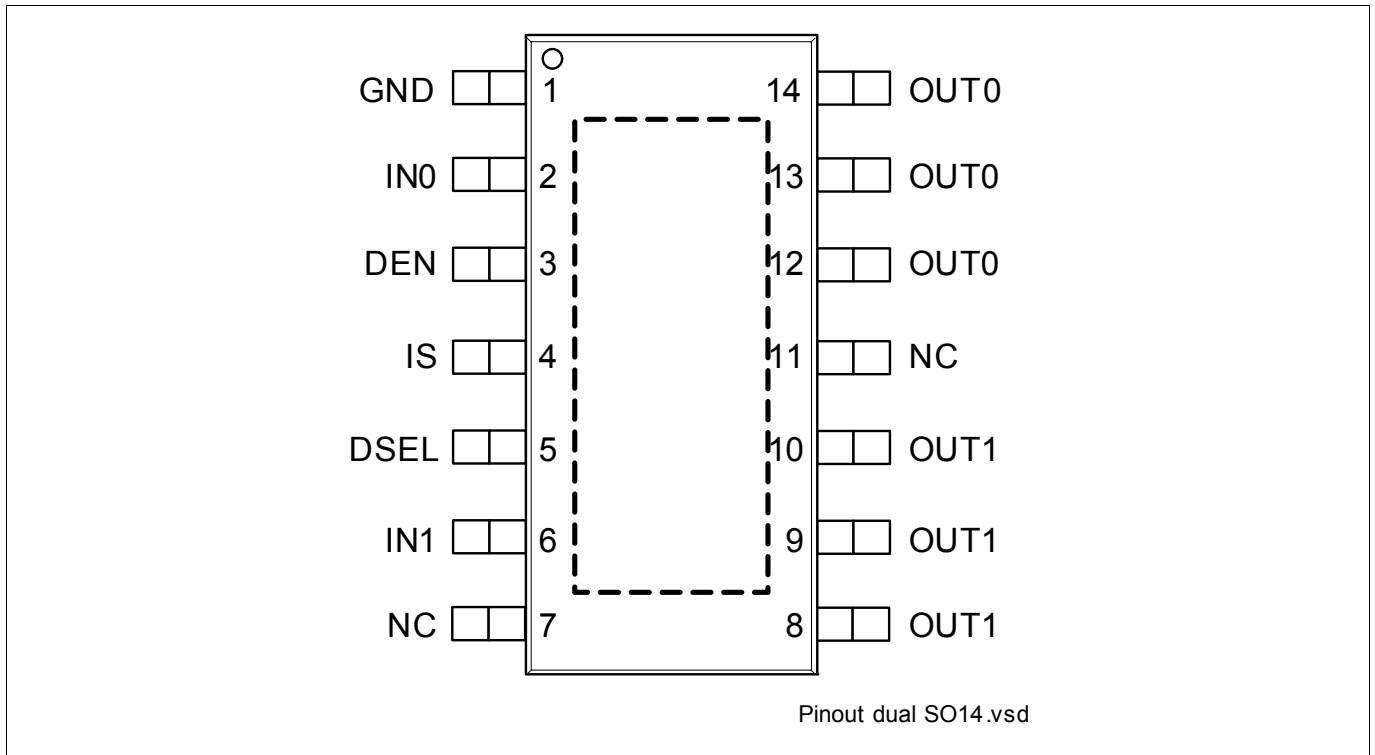


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Table 1 Pin Definition and Functions

Pin	Symbol	Function
1	GND	Ground ; Ground connection
2	IN0	Input channel 0 ; Input signal for channel 0 activation
3	DEN	Diagnostic ENable ; Digital signal to enable/disable the diagnosis of the device
4	IS	Sense ; Sense current of the selected channel
5	DSEL	Diagnostic SElection ; Digital signal to select the channel to be diagnosed
6	IN1	Input channel 1 ; Input signal for channel 1 activation
7, 11	NC	Not Connected ; No internal connection to the chip
8, 9, 10	OUT1	OUTput 1 ; Protected high side power output channel 1 ¹⁾
12, 13, 14	OUT0	OUTput 0 ; Protected high side power output channel 0 ¹⁾
Cooling Tab	V _S	Voltage Supply ; Battery voltage

1) All output pins of a given channel must be connected together on the PCB. All pins of an output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

Pin Configuration

3.3 Voltage and Current Definition

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

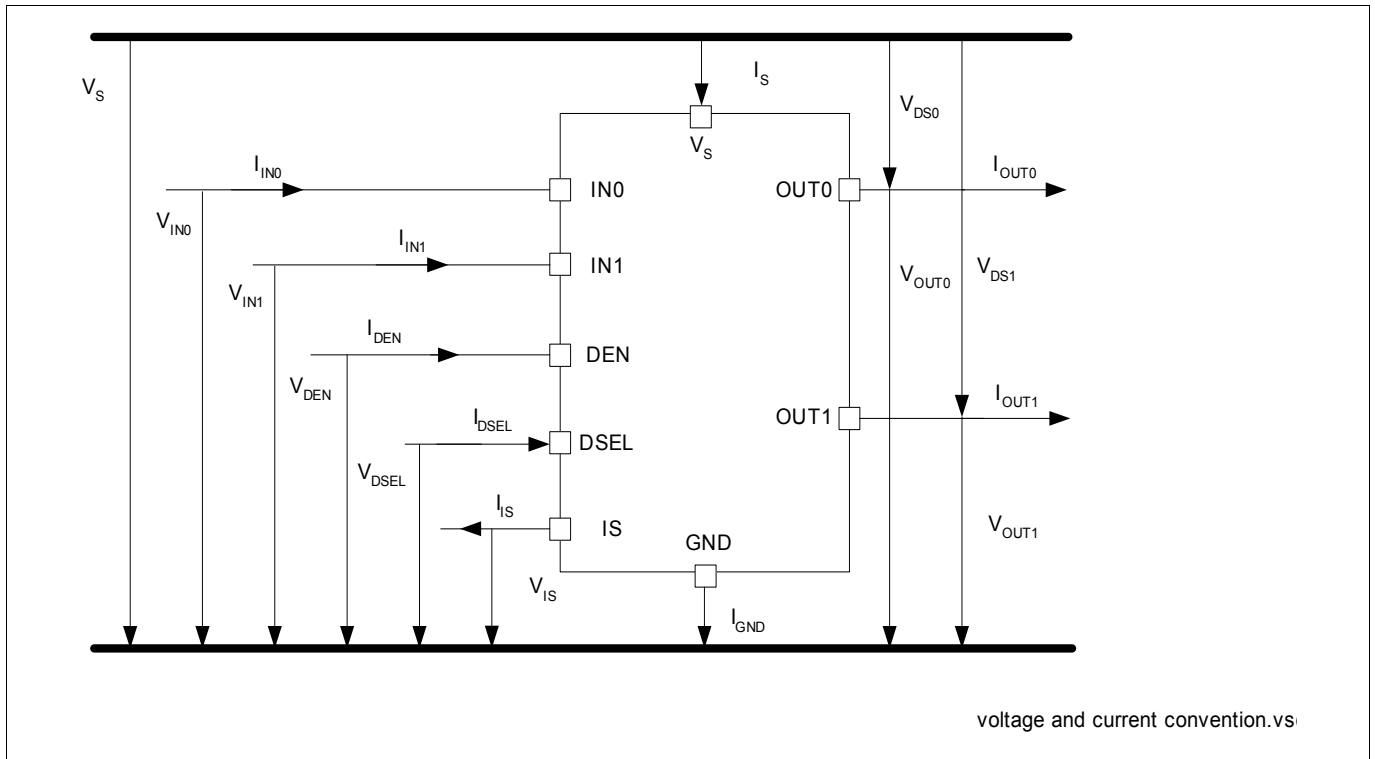


Figure 3 Voltage and Current Definition

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings ¹⁾

$T_J = -40\text{ °C}$ to $+150\text{ °C}$; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply voltage	V_S	-0.3	–	48	V	–	P_4.1.1
Reverse polarity voltage	$-V_{S(REV)}$	0	–	28	V	$t < 2\text{ min}$ $T_A = 25\text{ °C}$ $R_L \geq 12\ \Omega$ $Z_{GND} = \text{Diode} + 27\ \Omega$	P_4.1.2
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	36	V	$R_{supply} = 10\text{ m}\Omega$ $L_{supply} = 5\ \mu\text{H}$ $R_{Cable1} = 20\text{ m}\Omega$ $L_{Cable1} = 0\ \mu\text{H}$ $R_{Cable2} = 320\text{ m}\Omega$ $L_{Cable2} = 40\ \mu\text{H}$ See Chapter 6 and Figure 53	P_4.1.3
Supply voltage for Load dump protection	$V_{S(LD)}$	–	–	65	V	²⁾ $R_I = 2\ \Omega$ $R_L = 12\ \Omega$	P_4.1.12
Short Circuit Capability							
Permanent short circuit IN pin toggles	n_{RSC1}	–	–	100	k cycles	³⁾ $V_{Supply} = 28\text{ V}$	P_4.1.4
Input Pins							
Voltage at INPUT pins	V_{IN}	-0.3 –	–	6 7	V	– $t < 2\text{ min}$	P_4.1.13
Current through INPUT pins	I_{IN}	-2	–	2	mA	–	P_4.1.14
Voltage at DEN pin	V_{DEN}	-0.3 –	–	6 7	V	– $t < 2\text{ min}$	P_4.1.15
Current through DEN pin	I_{DEN}	-2	–	2	mA	–	P_4.1.16
Voltage at DSEL pin	V_{DSEL}	-0.3 –	–	6 7	V	– $t < 2\text{ min}$	P_4.1.17
Current through DSEL pin	I_{DSEL}	-2	–	2	mA	–	P_4.1.18
Sense Pin							
Voltage at IS pin	V_{IS}	-0.3	–	V_S	V	–	P_4.1.19
Current through IS pin	I_{IS}	-25	–	50	mA	–	P_4.1.20

General Product Characteristics

Table 2 Absolute Maximum Ratings (cont'd)¹⁾

$T_J = -40\text{ °C}$ to $+150\text{ °C}$; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Stage							
Load current	$ I_L $	–	–	$I_{L(LIM)}$	A	–	P_4.1.21
Power dissipation (DC)	P_{TOT}	–	–	2.0	W	$T_A = 85\text{ °C}$ $T_J < 150\text{ °C}$	P_4.1.22
Maximum energy dissipation Single pulse (one channel)	E_{AS}	–	–	85	mJ	$I_{L(0)} = 4\text{ A}$ $T_{J(0)} = 150\text{ °C}$ $V_S = 28\text{ V}$	P_4.1.23
Voltage at power transistor	V_{DS}	–	–	65	V	–	P_4.1.26
Currents							
Current through ground pin	I_{GND}	-20 -200	–	20 20	mA	– $t < 2\text{ min}$	P_4.1.27
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	P_4.1.28
Storage temperature	T_{STG}	-55	–	150	°C	–	P_4.1.30
ESD Susceptibility							
ESD susceptibility (all pins)	V_{ESD}	-2	–	2	kV	⁴⁾ HBM	P_4.1.31
ESD susceptibility OUT Pin vs. GND and V_S connected	V_{ESD}	-4	–	4	kV	⁴⁾ HBM	P_4.1.32
ESD susceptibility	V_{ESD}	-500	–	500	V	⁵⁾ CDM	P_4.1.33
ESD susceptibility pin (corner pins)	V_{ESD}	-750	–	750	V	⁵⁾ CDM	P_4.1.34

1) Not subject to production test. Specified by design.

2) $V_{S(LD)}$ is setup without the DUT connected to the generator per ISO 7637-1.

3) Threshold limit for short circuit failures : 100ppm. Please refer to the legal disclaimer for short circuit capability at the end of this document.

4) ESD susceptibility HBM according to ANSI/ESDA/JEDEC JS-001-2010

5) "CDM" ESDA STM5.3.1

Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

General Product Characteristics

4.2 Functional Range

Table 3 Functional Range $T_J = -40\text{ °C}$ to $+150\text{ °C}$; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Nominal operating voltage	V_{NOM}	8	28	36	V	–	P_4.2.1
Extended operating voltage	$V_{S(OP)}$	5	–	48	V	²⁾ $V_{IN} = 4.5\text{ V}$ $R_L = 12\ \Omega$ $V_{DS} < 0.5\text{ V}$ See Figure 15	P_4.2.2
Minimum functional supply voltage	$V_{S(OP_MIN)}$	3.8	4.3	5	V	¹⁾ $V_{IN} = 4.5\text{ V}$ $R_L = 12\ \Omega$ From $I_{OUT} = 0\text{ A}$ to $V_{DS} < 0.5\text{ V}$; See Figure 15 See Figure 29	P_4.2.3
Undervoltage shutdown	$V_{S(UV)}$	3	3.5	4.1	V	¹⁾ $V_{IN} = 4.5\text{ V}$ $V_{DEN} = 0\text{ V}$ $R_L = 12\ \Omega$ From $V_{DS} < 1\text{ V}$; to $I_{OUT} = 0\text{ A}$ See Figure 15 See Figure 30	P_4.2.4
Undervoltage shutdown hysteresis	$V_{S(UV_HYS)}$	–	850	–	mV	²⁾ –	P_4.2.13
Operating current One channel active	I_{GND_1}	–	5.5	9	mA	$V_{IN} = 5.5\text{ V}$ $V_{DEN} = 5.5\text{ V}$ Device in $R_{DS(ON)}$ $V_S = 36\text{ V}$ See Figure 31	P_4.2.5
Operating current All channels active	I_{GND_2}	–	9	12	mA	$V_{IN} = 5.5\text{ V}$ $V_{DEN} = 5.5\text{ V}$ Device in $R_{DS(ON)}$ $V_S = 36\text{ V}$ See Figure 32	P_4.2.6
Standby current for whole device with load	$I_{S(OFF)}$	–	0.1	0.5	μA	¹⁾ $V_S = 36\text{ V}$ $V_{OUT} = 0\text{ V}$ V_{IN} floating V_{DEN} floating $T_J \leq 85\text{ °C}$ See Figure 33	P_4.2.7

General Product Characteristics

Table 3 Functional Range (cont'd) $T_J = -40\text{ °C}$ to $+150\text{ °C}$; (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Maximum standby current for whole device with load	$I_{S(OFF_150)}$	–	6	15	μA	$V_S = 36\text{ V}$ $V_{OUT} = 0\text{ V}$ V_{IN} floating V_{DEN} floating $T_J = 150\text{ °C}$ See Figure 33	P_4.2.10
Standby current for whole device with load, diagnostic active	$I_{S(OFF_DEN)}$	–	0.6	–	mA	²⁾ $V_S = 36\text{ V}$ $V_{OUT} = 0\text{ V}$ V_{IN} floating $V_{DEN} = 5.5\text{ V}$	P_4.2.8

1) Test at $T_J = -40\text{ °C}$ only

2) Not subject to production test. Specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to soldering point	R_{thJS}	–	5	–	K/W	¹⁾	P_4.3.1
Junction to ambient Both channels active	R_{thJA}	–	29	–	K/W	^{1) 2)}	P_4.3.2

1) Not subject to production test. Specified by design.

2) Specified R_{thja} value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.4 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 μm Cu, 2 x 35 μm Cu). Where applicable, a thermal via array under the exposed pad contacts the first inner copper layer. Please refer to [Figure 4](#).

General Product Characteristics

4.3.1 PCB set up

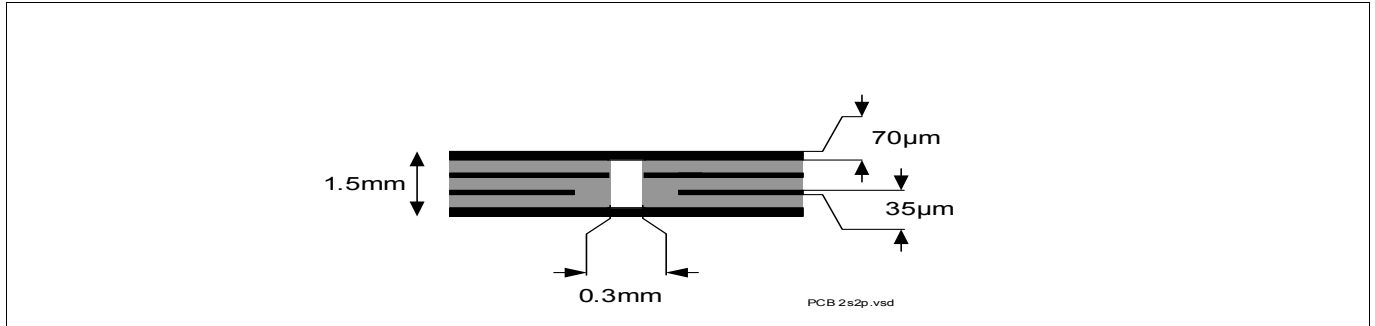


Figure 4 2s2p PCB Cross Section

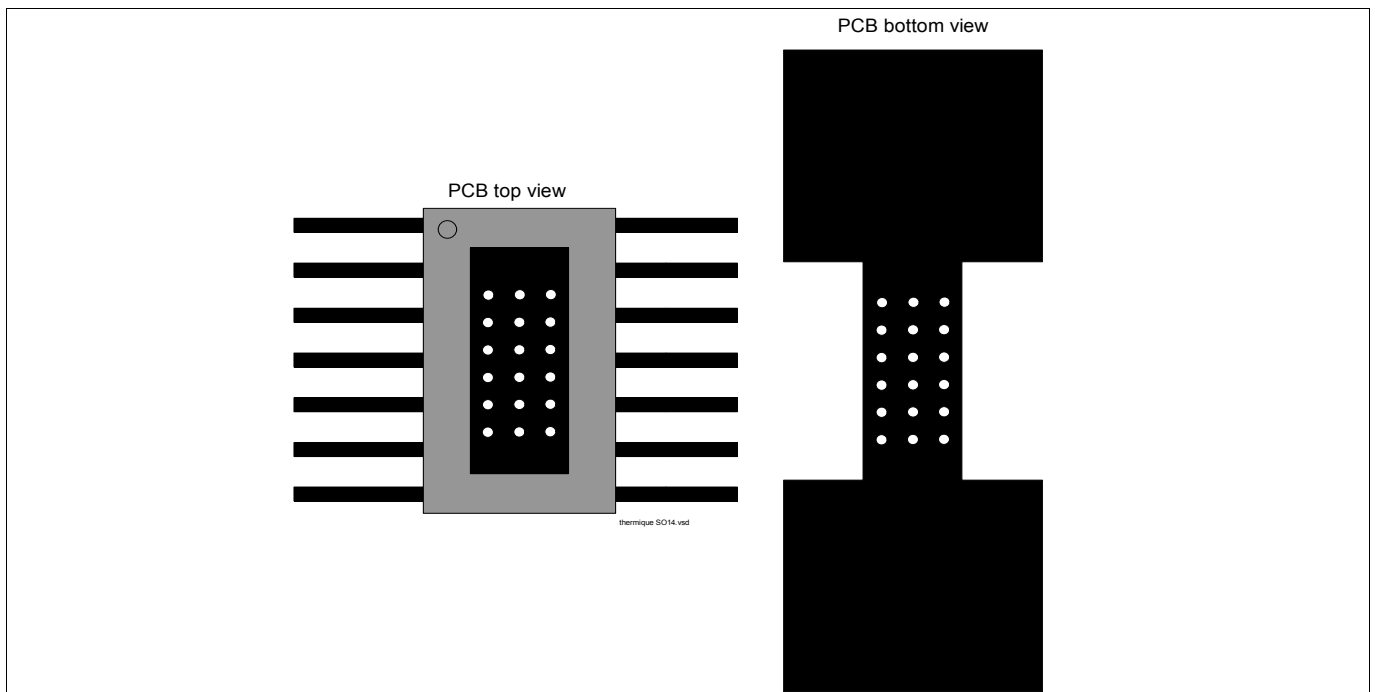


Figure 5 PC Board Top and Bottom View for Thermal Simulation with 600 mm² Cooling Area

General Product Characteristics

4.3.2 Thermal Impedance

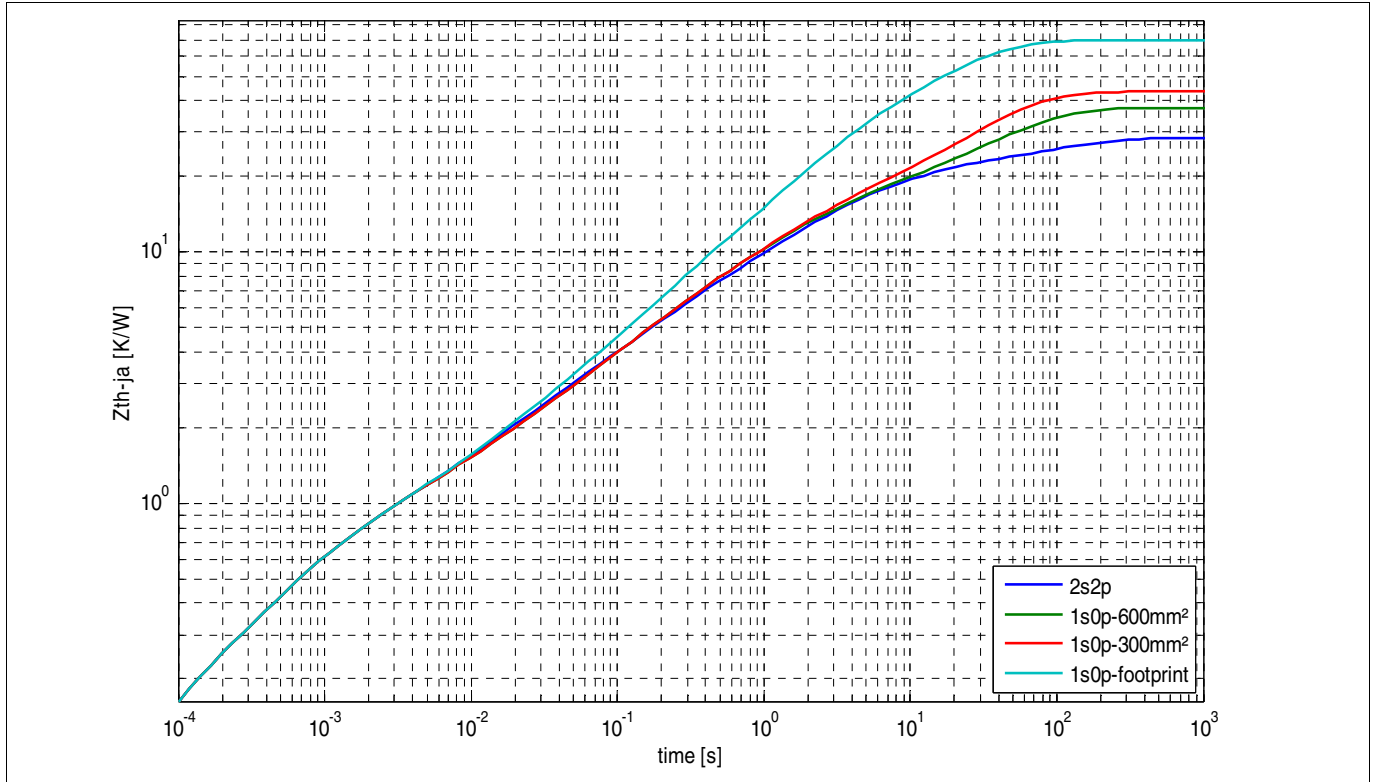


Figure 6 Typical Thermal Impedance. 2s2p set up according Figure 4

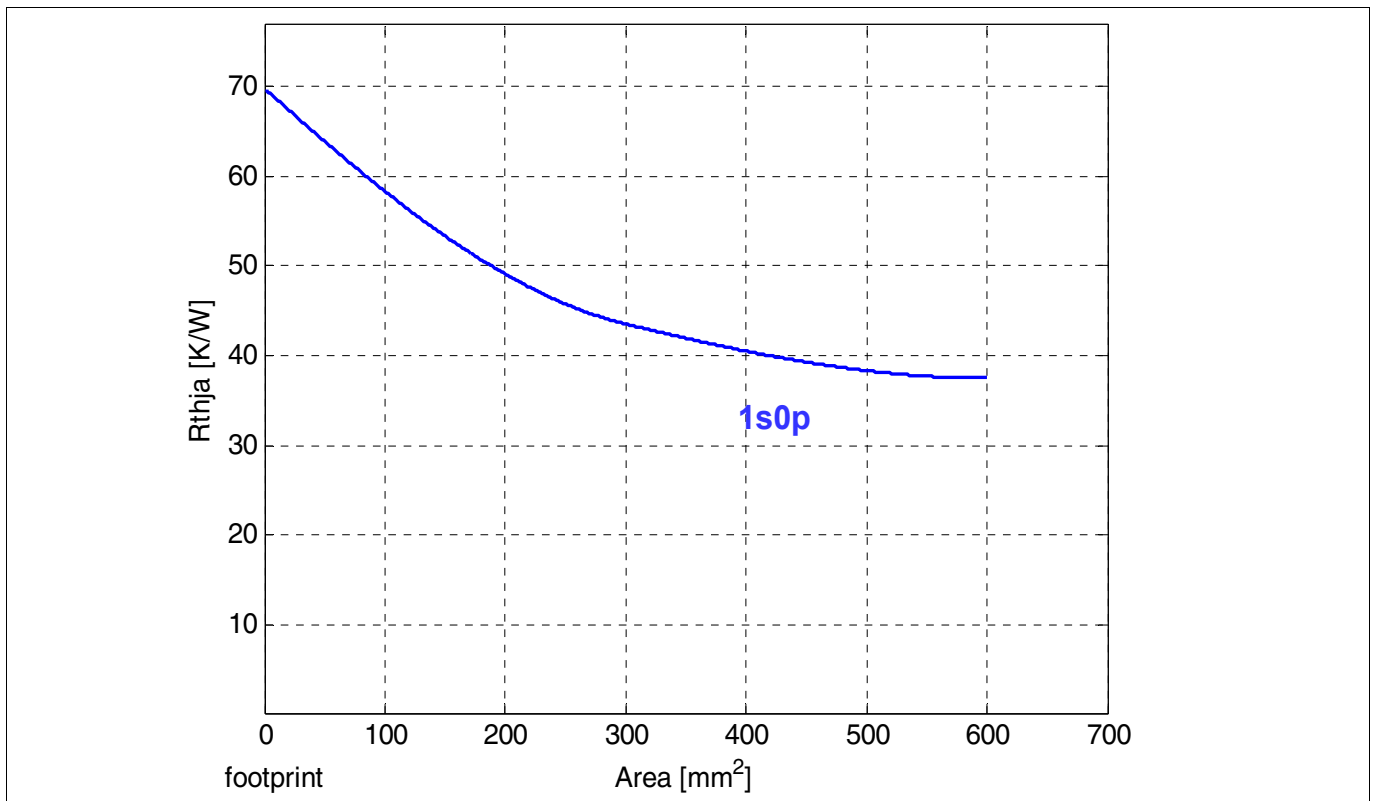


Figure 7 Typical Thermal Resistance. PCB set up 1s0p

Power Stage

5 Power Stage

The power stages are built using an N-channel vertical power MOSFET (DMOS) with charge pump.

5.1 Output ON-state Resistance

The ON-state resistance $R_{DS(ON)}$ depends on the supply voltage as well as the junction temperature T_J . **Figure 8** shows the dependencies in terms of temperature and supply voltage for the typical ON-state resistance. The behavior in reverse polarity is described in **Chapter 6.4**.

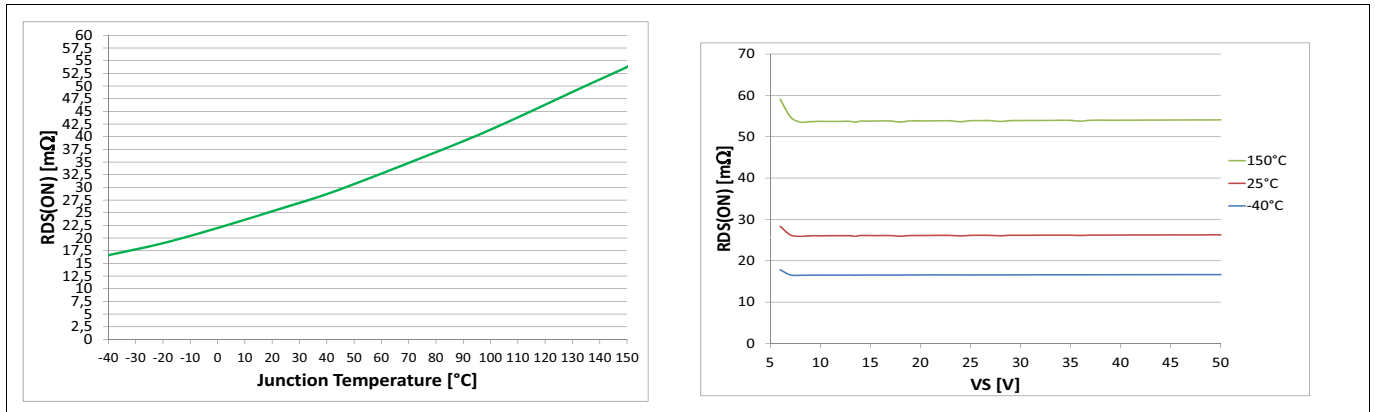


Figure 8 Typical ON-state Resistance

A high signal (see **Chapter 8**) at the input pin causes the power DMOS to switch ON with a dedicated slope, which is optimized in terms of EMC emission.

5.2 Turn ON/OFF Characteristics with Resistive Load

Figure 9 shows the typical timing when switching a resistive load.

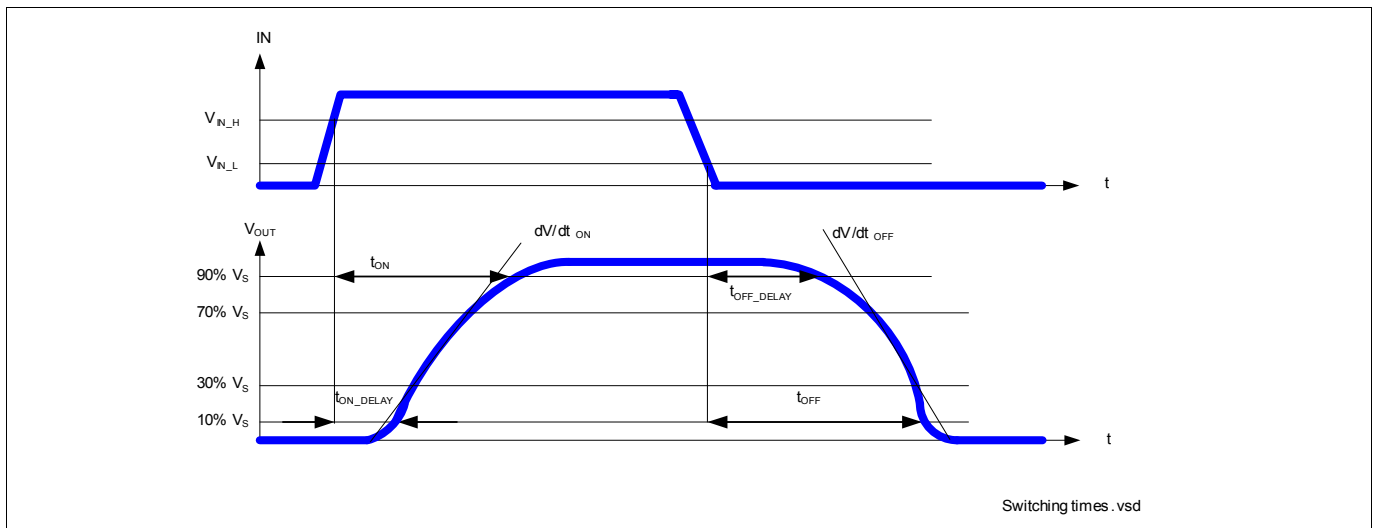


Figure 9 Switching a Resistive Load Timing

Power Stage

5.3 Inductive Load

5.3.1 Output Clamping

When switching OFF inductive loads with high side switches, the voltage V_{OUT} drops below ground potential, because the inductance intends to continue driving the current. To prevent the destruction of the device by avalanche due to high voltages, there is a voltage clamp mechanism $Z_{DS(AZ)}$ implemented that limits negative output voltage to a certain level ($V_S - V_{DS(AZ)}$). Please refer to [Figure 10](#) and [Figure 11](#) for details. Nevertheless, the maximum allowed load inductance is limited.

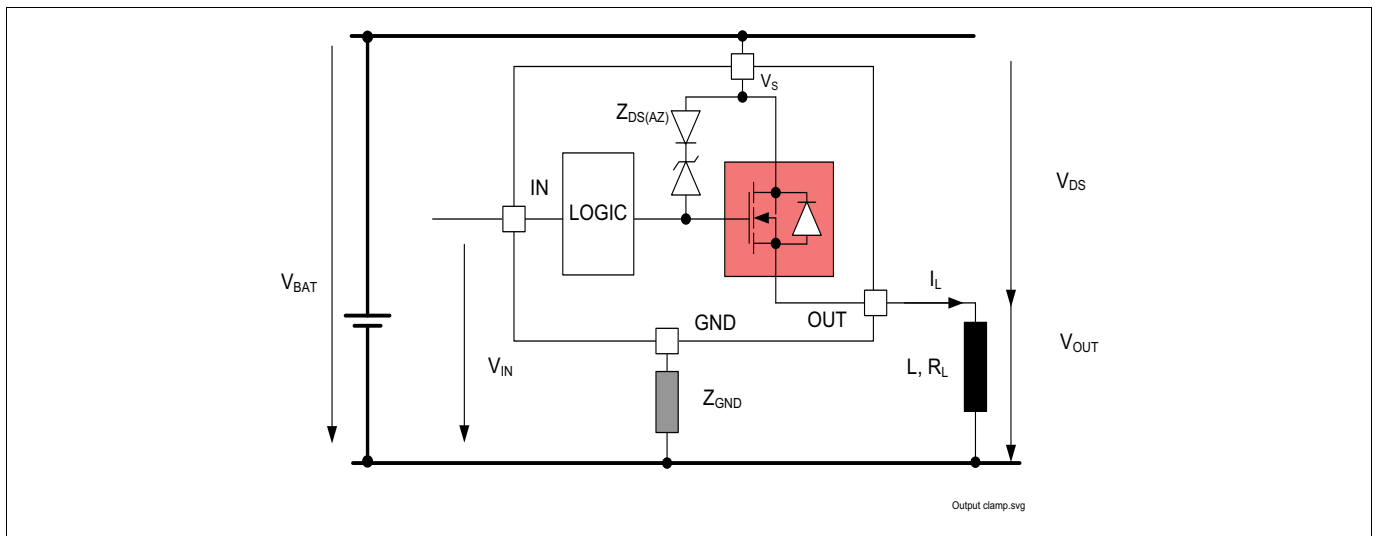


Figure 10 Output Clamp (OUT0 and OUT1)

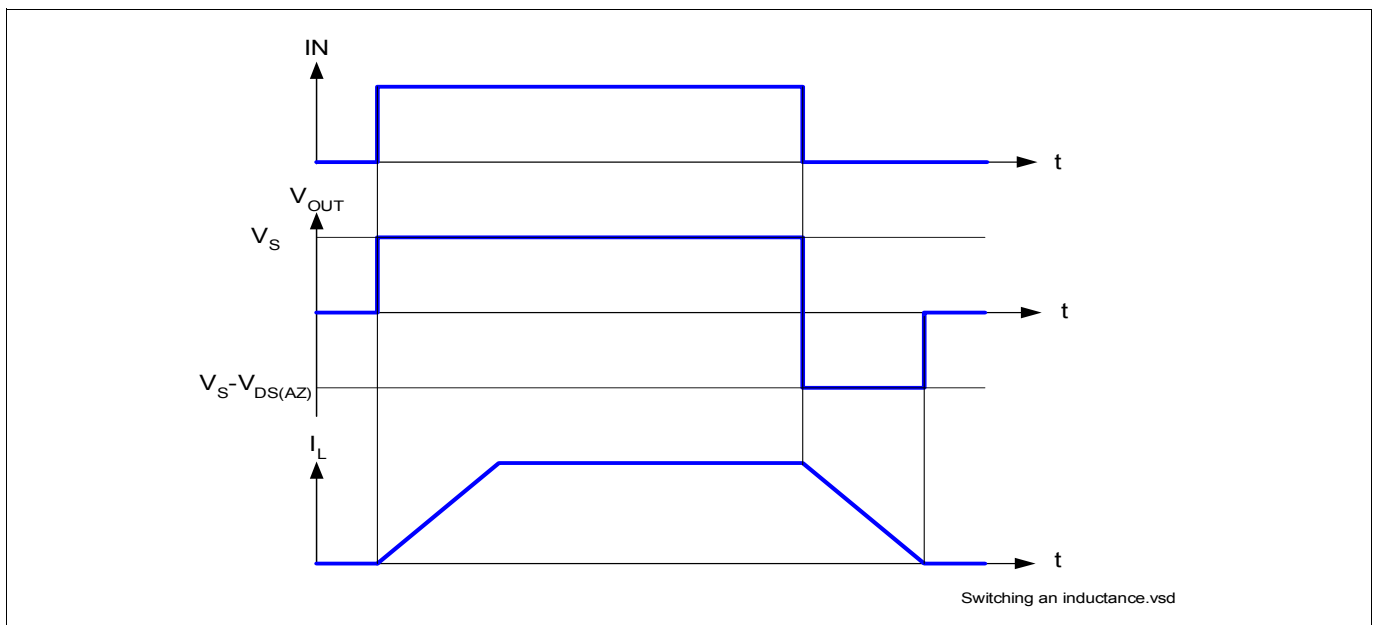


Figure 11 Switching an Inductive Load Timing

Power Stage

5.3.2 Maximum Load Inductance

During demagnetization of inductive loads, energy has to be dissipated in the BTT6030-2EKB. This energy can be calculated with following equation:

$$E = V_{DS(AZ)} \times \frac{L}{R_L} \times \left[\frac{V_S - V_{DS(AZ)}}{R_L} \times \ln\left(1 - \frac{R_L \times I_L}{V_S - V_{DS(AZ)}}\right) + I_L \right] \quad (5.1)$$

The following equation simplifies under the assumption of $R_L = 0 \Omega$.

$$E = \frac{1}{2} \times L \times I^2 \times \left(1 - \frac{V_S}{V_S - V_{DS(AZ)}}\right) \quad (5.2)$$

The energy, which is converted into heat, is limited by the thermal design of the component. See [Figure 12](#) for the maximum allowed energy dissipation as a function of the load current.

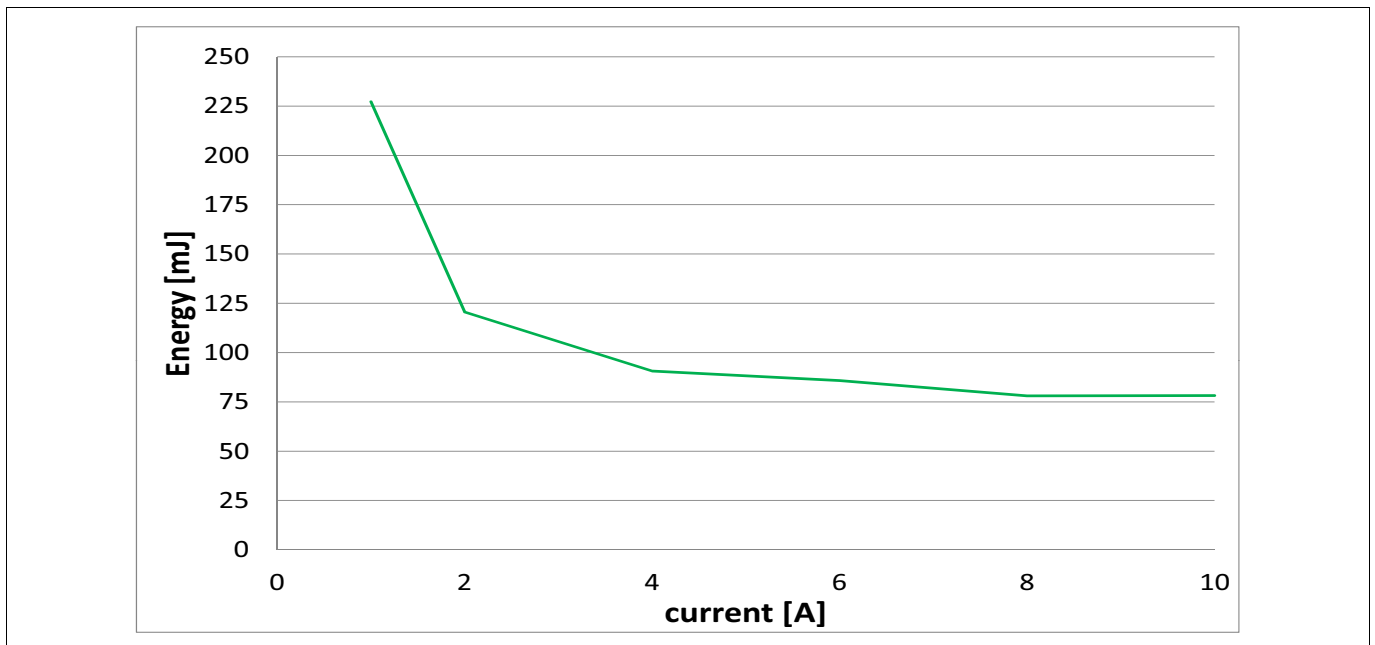


Figure 12 Maximum Energy Dissipation Single Pulse, $T_{J(0)} = 150 \text{ }^\circ\text{C}$; $V_S = 28 \text{ V}$

Power Stage

5.4 Inverse Current Capability

In case of inverse current, meaning a voltage V_{INV} at the OUTput higher than the supply voltage V_S , a current I_{INV} will flow from output to V_S pin via the body diode of the power transistor (please refer to [Figure 13](#)). The output stage follows the state of the IN pin, except if the IN pin goes from OFF to ON during inverse. In that particular case, the output stage is kept OFF until the inverse current disappears. Nevertheless, the current I_{INV} should not be higher than $I_{L(INV)}$. Otherwise, the second channel can be corrupted and erratic behavior can be observed. If the affected channel is OFF, the diagnostic will detect an open load at OFF. If the affected channel is ON, the diagnostic will detect open load at ON (the overtemperature signal is inhibited). At the appearance of V_{INV} , a parasitic diagnostic can be observed at the unaffected channel. After, the diagnosis is valid and reflects the output state. At V_{INV} vanishing, the diagnosis is valid and reflects the output state. During inverse current, no protection function are available.

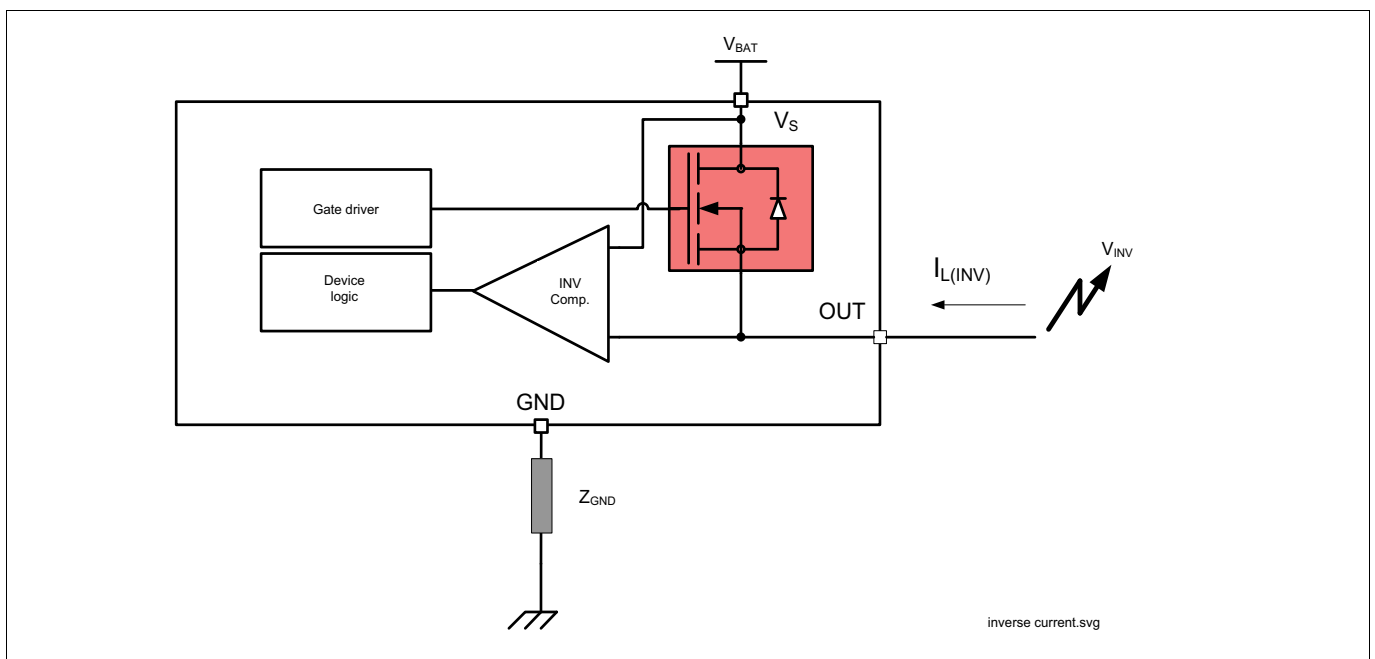


Figure 13 Inverse Current Circuitry

Power Stage

5.5 Electrical Characteristics Power Stage

Table 5 Electrical Characteristics: Power Stage

$V_S = 8\text{ V to }36\text{ V}$, $T_J = -40\text{ °C to }+150\text{ °C}$ (unless otherwise specified).
Typical values are given at $V_S = 28\text{ V}$, $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ON-state resistance per channel	$R_{DS(ON)_150}$	40	55	62	mΩ	$I_L = I_{L4} = 7\text{ A}$ $V_{IN} = 4.5\text{ V}$ $T_J = 150\text{ °C}$ See Figure 8	P_5.5.1
ON-state resistance per channel	$R_{DS(ON)_25}$	–	32	–	mΩ	¹⁾ $T_J = 25\text{ °C}$	P_5.5.21
Nominal load current One channel active	$I_{L(NOM)1}$	–	6	–	A	¹⁾ $T_A = 85\text{ °C}$ $T_J < 150\text{ °C}$	P_5.5.2
Nominal load current All channels active	$I_{L(NOM)2}$	–	4	–	A		P_5.5.3
Output voltage drop limitation at small load currents	$V_{DS(NL)}$	–	10	22	mV	$I_L = I_{L0} = 50\text{ mA}$ See Figure 34	P_5.5.4
Drain to source clamping voltage $V_{DS(AZ)} = (V_S - V_{OUT})$	$V_{DS(AZ)}$	66	70	75	V	$I_{DS} = 20\text{ mA}$ See Figure 11 See Figure 35	P_5.5.5
Output leakage current per channel; $T_J \leq 85\text{ °C}$	$I_{L(OFF)}$	–	0.05	0.5	μA	²⁾ V_{IN} floating $V_{OUT} = 0\text{ V}$ $T_J \leq 85\text{ °C}$	P_5.5.6
Output leakage current per channel; $T_J = 150\text{ °C}$	$I_{L(OFF)_150}$	–	2	10	μA	V_{IN} floating $V_{OUT} = 0\text{ V}$ $T_J = 150\text{ °C}$	P_5.5.8
Slew rate 30% to 70% V_S	$\Delta V/dt_{ON}$	0.3	0.8	1.4	V/μs	$R_L = 12\text{ Ω}$ $V_S = 28\text{ V}$ See Figure 9	P_5.5.11
Slew rate 70% to 30% V_S	$-\Delta V/dt_{OFF}$	0.3	0.8	1.4	V/μs	See Figure 36	P_5.5.12
Slew rate matching $dV/dt_{ON} - dV/dt_{OFF}$	$\Delta dV/dt$	-0.15	0	0.15	V/μs	See Figure 37 See Figure 38 See Figure 39	P_5.5.13
Turn-ON time to $V_{OUT} = 90\% V_S$	t_{ON}	20	50	150	μs	See Figure 40	P_5.5.14
Turn-OFF time to $V_{OUT} = 10\% V_S$	t_{OFF}	20	55	150	μs		P_5.5.15
Turn-ON / OFF matching $t_{OFF} - t_{ON}$	Δt_{SW}	-50	0	50	μs		P_5.5.16
Turn-ON time to $V_{OUT} = 10\% V_S$	t_{ON_delay}	–	30	70	μs		P_5.5.17
Turn-OFF time to $V_{OUT} = 90\% V_S$	t_{OFF_delay}	–	30	70	μs		P_5.5.18

Power Stage

Table 5 Electrical Characteristics: Power Stage (cont'd)

$V_S = 8\text{ V to }36\text{ V}$, $T_J = -40\text{ °C to }+150\text{ °C}$ (unless otherwise specified).

Typical values are given at $V_S = 28\text{ V}$, $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Switch ON energy	E_{ON}	–	0.6	–	mJ	¹⁾ $R_L = 12\ \Omega$ $V_{OUT} = 90\% V_S$ $V_S = 36\text{ V}$ See Figure 41	P_5.5.19
Switch OFF energy	E_{OFF}	–	0.8	–	mJ	¹⁾ $R_L = 12\ \Omega$ $V_{OUT} = 10\% V_S$ $V_S = 36\text{ V}$ See Figure 42	P_5.5.20

1) Not subject to production test, specified by design.

2) Test at $T_J = -40\text{ °C}$ only

6 Protection Functions

The device provides integrated protection functions. These functions are designed to prevent the destruction of the IC from fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are designed for neither continuous nor repetitive operation.

6.1 Loss of Ground Protection

In case of loss of the module ground and the load remains connected to ground, the device protects itself by automatically turning OFF (when it was previously ON) or remains OFF, regardless of the voltage applied on IN pins.

In case of loss of device ground, it's recommended to use input resistors between the microcontroller and the BTT6030-2EKB to ensure switching OFF of the channels.

In case of loss of module or device ground, a current ($I_{OUT(GND)}$) can flow out of the DMOS illustrated in [Figure 14](#). Z_{GND} is recommended to be a resistor in series to a diode.

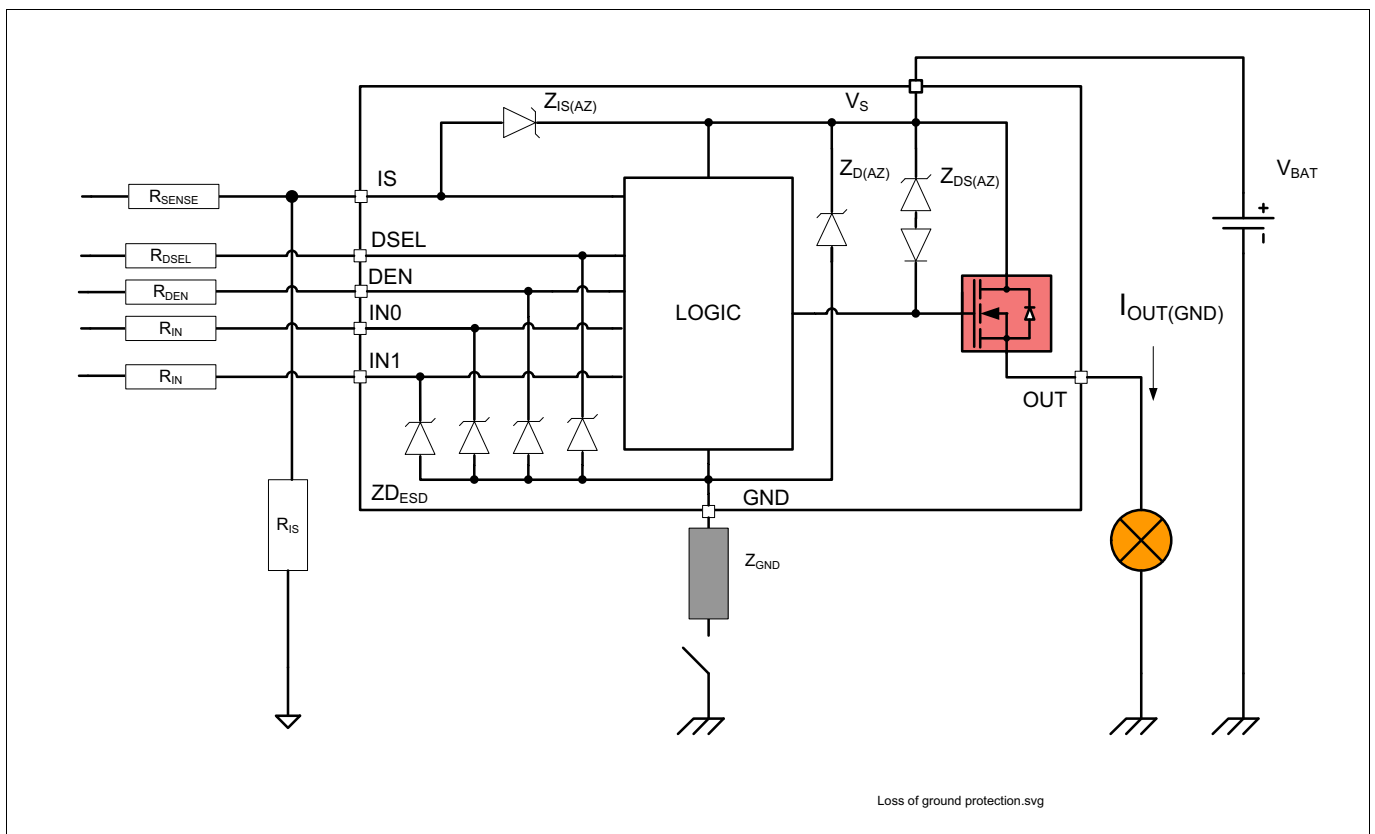


Figure 14 Loss of Ground Protection with External Components

6.2 Undervoltage Protection

Between $V_{S(UV)}$ and $V_{S(OP)}$, the undervoltage mechanism is triggered. $V_{S(OP)}$ represents the minimum voltage where the switching ON and OFF can take place. $V_{S(UV)}$ represents the minimum voltage the switch can hold ON. If the supply voltage is below the undervoltage mechanism $V_{S(UV)}$, the device is OFF (turns OFF). As soon as the supply voltage is above the undervoltage mechanism $V_{S(OP)}$, then the device can be switched ON. When the switch is ON, protection functions are operational. Nevertheless, the diagnosis is not guaranteed until V_S is in the V_{NOM} range. [Figure 15](#) illustrates the undervoltage mechanism.

Protection Functions

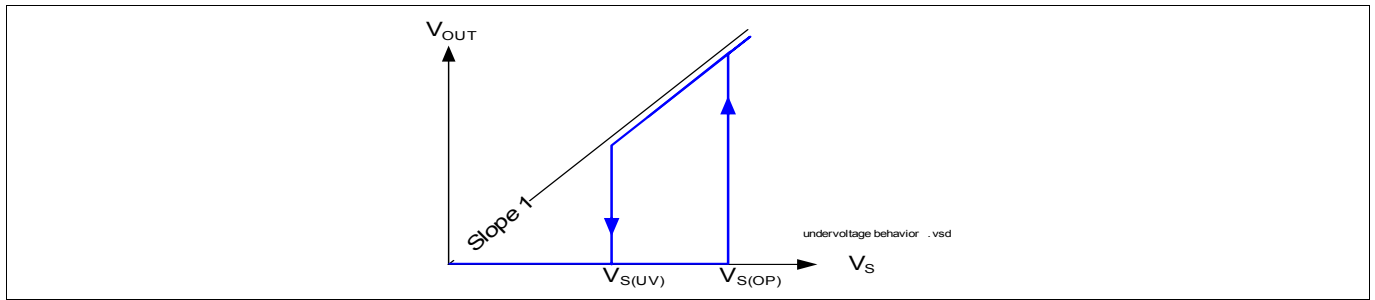


Figure 15 Undervoltage Behavior

6.3 Overvoltage Protection

There is an integrated clamp mechanism for overvoltage protection ($Z_{D(AZ)}$). To guarantee this mechanism operates properly in the application, the current in the Zener diode has to be limited by a ground resistor. **Figure 16** shows a typical application to withstand overvoltage issues. In case of supply voltage higher than $V_{S(AZ)}$, the power transistor switches ON and the voltage across the logic section is clamped. As a result, the internal ground potential rises to $V_S - V_{S(AZ)}$. Due to the ESD Zener diodes, the potential at pin IN and DEN rises almost to that potential, depending on the impedance of the connected circuitry. In the case the device was ON, prior to overvoltage, the BTT6030-2EKB remains ON. In the case the BTT6030-2EKB was OFF, prior to overvoltage, the power transistor can be activated. In the case the supply voltage is in above $V_{BAT(SC)}$ and below $V_{DS(AZ)}$, the output transistor is still operational and follows the input. If at least one channel is in the ON state, parameters are no longer guaranteed and lifetime is reduced compared to the nominal supply voltage range. This especially impacts the short circuit robustness, as well as the maximum energy E_{AS} capability.

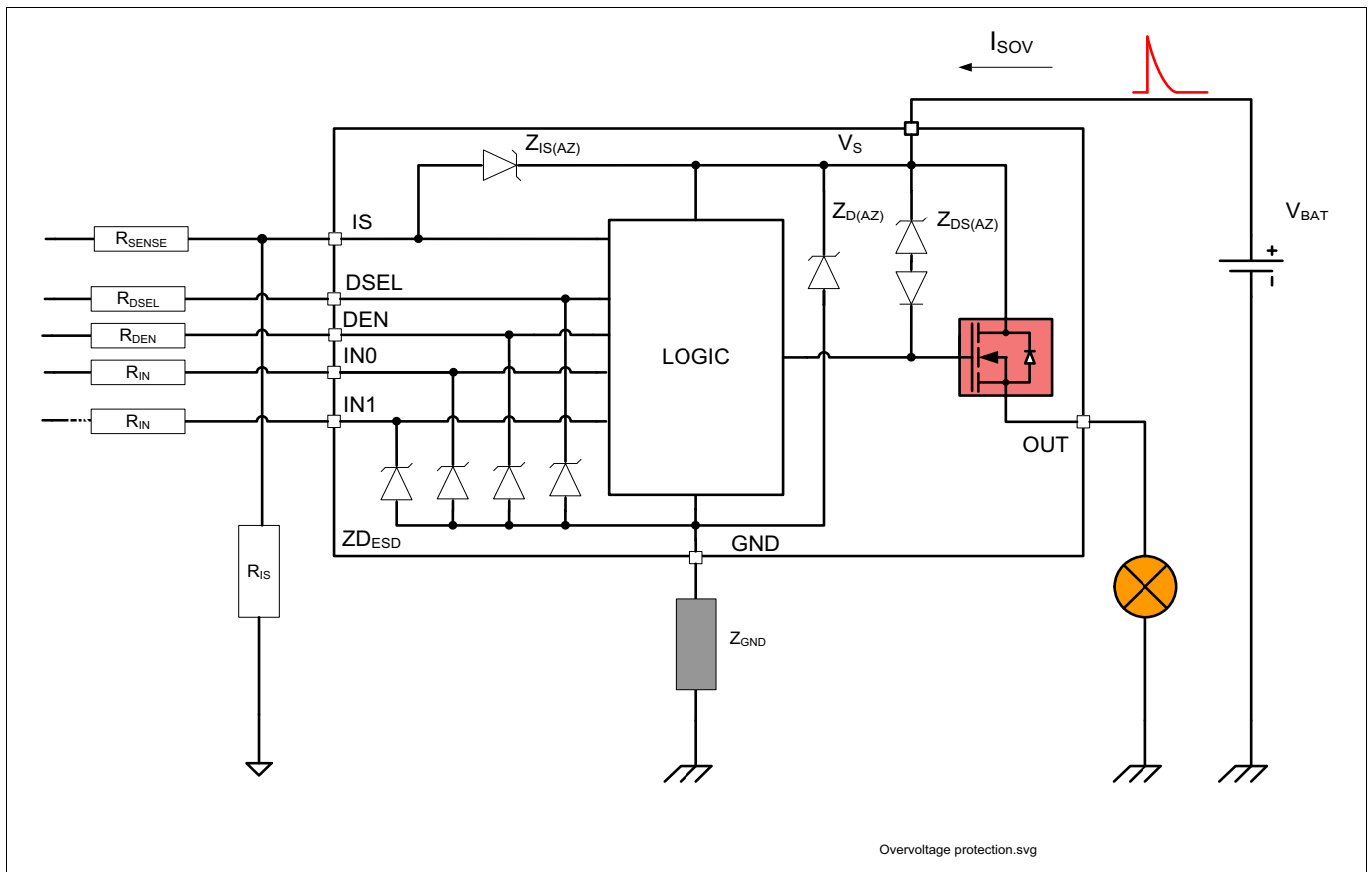


Figure 16 Overvoltage Protection with External Components

Protection Functions

6.4 Reverse Polarity Protection

In case of reverse polarity, the intrinsic body diodes of the power DMOS causes power dissipation. The current in this intrinsic body diode is limited by the load itself. Additionally, the current into the ground path and the logic pins has to be limited to the maximum current described in [Chapter 4.1](#) with an external resistor. [Figure 17](#) shows a typical application. R_{GND} resistor is used to limit the current in the Zener protection of the device. Resistors R_{DSEL} , R_{DEN} , and R_{IN} are used to limit the current in the logic of the device and in the ESD protection stage. R_{SENSE} is used to limit the current in the sense transistor which behaves as a diode. The recommended value for $R_{DEN} = R_{DSEL} = R_{IN} = R_{SENSE} = 10\text{ k}\Omega$. Z_{GND} is recommended to be a resistor in series to a diode.

During reverse polarity, no protection functions are available.

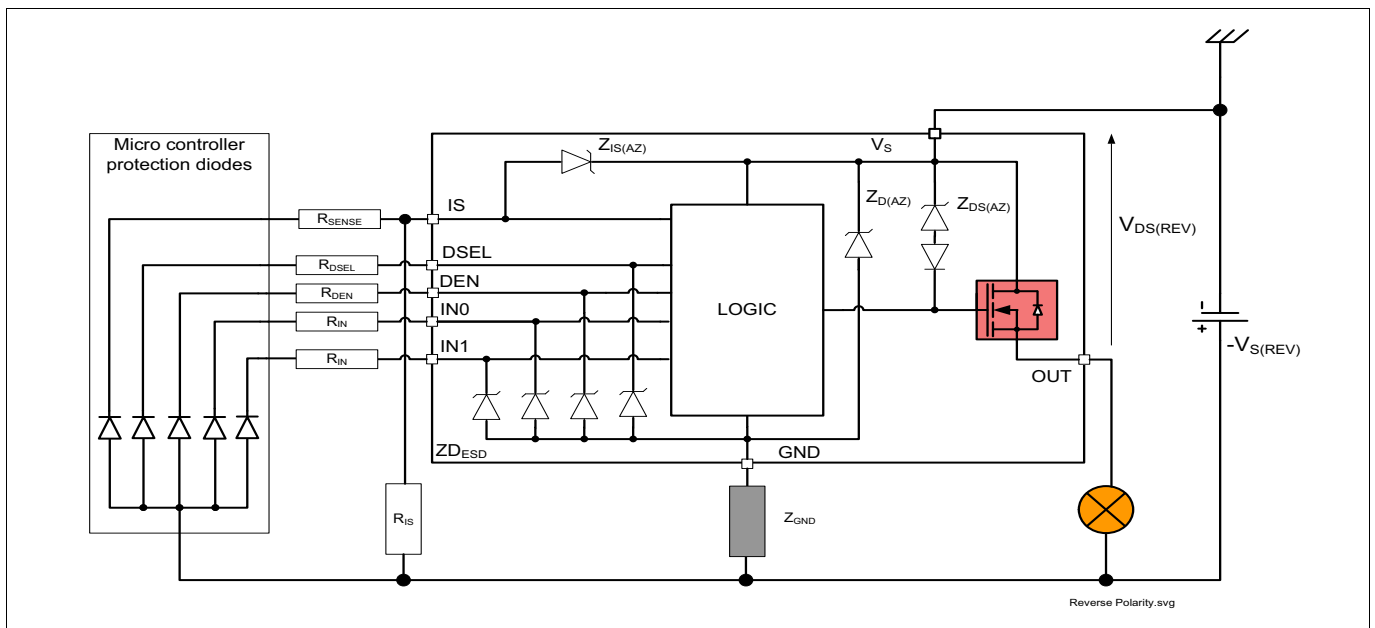


Figure 17 Reverse Polarity Protection with External Components

Protection Functions

6.5 Overload Protection

In case of overload, such as high inrush of cold lamp filament, or short circuit to ground, the BTT6030-2EKB offers several protection mechanisms.

6.5.1 Current Limitation

At first step, the instantaneous power in the switch is maintained at a safe value by limiting the current to the maximum current allowed in the switch $I_{L(SC)}$. During this time, the DMOS temperature is increasing, which affects the current flowing in the DMOS. The current limitation value is V_{DS} dependent. **Figure 18** shows the behavior of the current limitation as a function of the drain to source voltage.

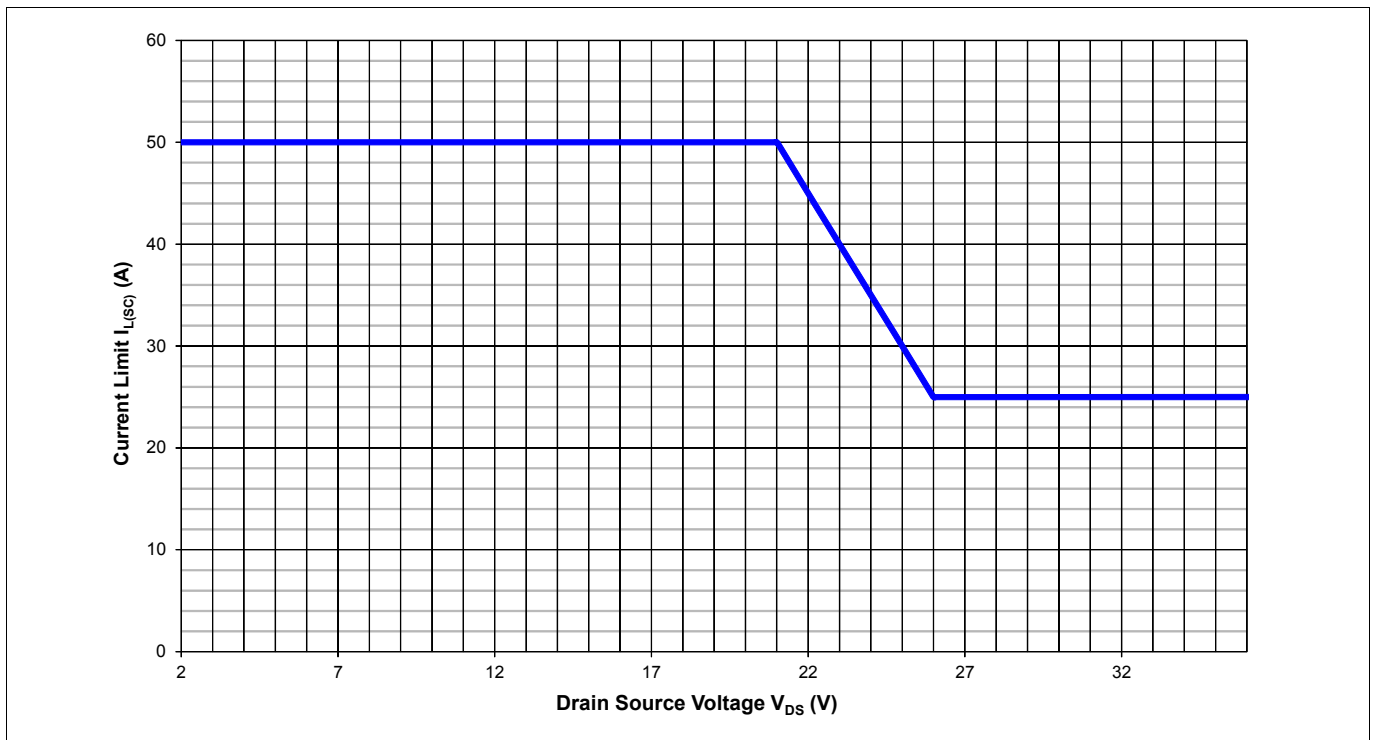


Figure 18 Current Limitation (typical behavior)

Protection Functions

6.5.2 Temperature Limitation in the Power DMOS

Each channel incorporates both an absolute ($T_{J(SC)}$) and a dynamic ($T_{J(SW)}$) temperature sensor. Activation of either sensor will cause an overheated channel to switch OFF to prevent destruction. Any protective switch OFF latches the output until the temperature has reached an acceptable value illustrated in **Figure 19**.

No retry strategy is implemented such that when the DMOS temperature has cooled down enough, the switch is switched ON again. Only the IN pin signal toggling can re-activate the power stage. (latch behavior).

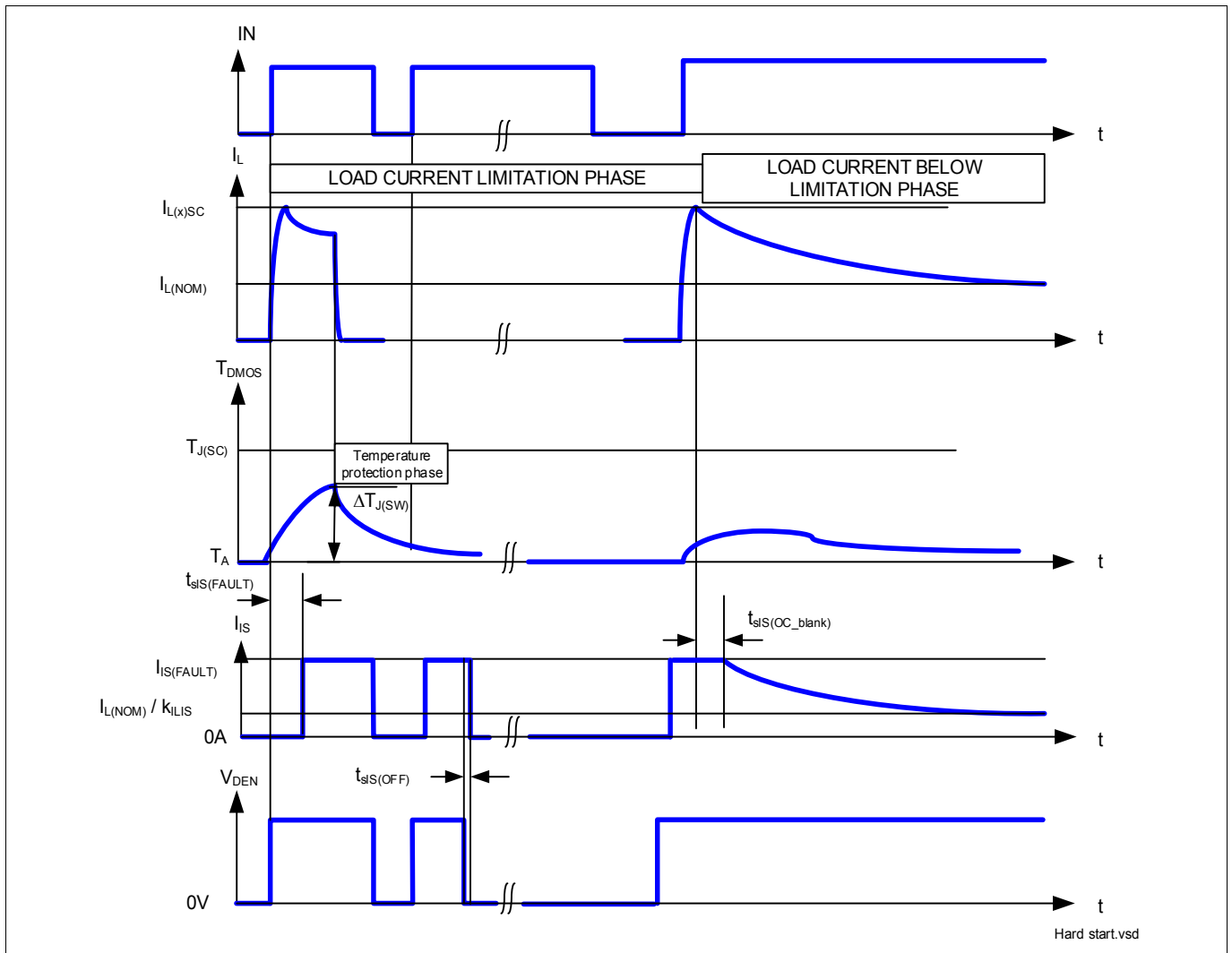


Figure 19 Overload Protection

Note: For better understanding, the time scale is not linear. The real timing of this drawing is application dependant and cannot be described.

Protection Functions

6.6 Electrical Characteristics for the Protection Functions

Table 6 Electrical Characteristics: Protection

$V_S = 8\text{ V to }36\text{ V}$, $T_J = -40\text{ °C to }+150\text{ °C}$ (unless otherwise specified).
Typical values are given at $V_S = 28\text{ V}$, $T_J = 25\text{ °C}$

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Loss of Ground							
Output leakage current while GND disconnected	$I_{\text{OUT(GND)}}$	–	0.1	–	mA	^{1) 2)} $V_S = 48\text{ V}$ See Figure 14	P_6.6.1
Reverse Polarity							
Drain source diode voltage during reverse polarity	$V_{\text{DS(REV)}}$	200	610	700	mV	$I_L = -4\text{ A}$ $T_J = 150\text{ °C}$ See Figure 17	P_6.6.2
Overvoltage							
Overvoltage protection	$V_{\text{S(AZ)}}$	65	70	75	V	$I_{\text{SOV}} = 5\text{ mA}$ See Figure 16	P_6.6.3
Overload Condition							
Load current limitation	$I_{\text{L5(SC)}}$	40	50	60	A	³⁾ $V_{\text{DS}} = 5\text{ V}$ See Figure 43	P_6.6.4
Load current limitation	$I_{\text{L28(SC)}}$	–	25	–	A	²⁾ $V_{\text{DS}} = 42\text{ V}$ See Figure 44	P_6.6.7
Dynamic temperature increase while switching	$\Delta T_{\text{J(SW)}}$	–	80	–	K	⁴⁾ See Figure 19	P_6.6.8
Thermal shutdown temperature	$T_{\text{J(SC)}}$	150	170 ⁴⁾	200 ⁴⁾	°C	⁵⁾ See Figure 19	P_6.6.10
Thermal shutdown hysteresis	$\Delta T_{\text{J(SC)}}$	–	30	–	K	^{5) 4)} See Figure 19	P_6.6.11

- 1) All pins are disconnected except V_S and OUT.
- 2) Not Subject to production test, specified by design
- 3) Test at $T_J = -40\text{ °C}$ only
- 4) Functional test only
- 5) Test at $T_J = +150\text{ °C}$ only