Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Capacitive Controller ICs

Capacitive Switch Controller ICs

BU21079F

General Description

BU21079F is a capacitive switch controller used for operating switches.
Low power consumption is achieved using the intermittent operation mode.
In addition to a regular simple switch, it supports matrix switches which are arranged in the matrix sensors. If external noise and temperature drift are detected, the automatic self-calibration is activated.

Features

- 8 capacitive sensor ports
- Supports matrix switches. Maximum of 16 switches.
- Automatic self-calibration
- Continued touch detection
- Sends an interrupt when there is a detected result of switch operation
- 2-wire serial bus interface
- 3.3V or 5.0V single power supply
- Built-in Power-On-Reset and Oscillator

Applications

- Electronic devices with multiple switches.
- Information appliances such as printers.
- AV appliances such as digital TV and HDD recorder.
- Notebook PC.
- Air-conditioner. Refrigerator. Electrical rice cooker.

Key Specifications

■ Input voltage range	3.0V to 5.5V
■ Operating temperature range	-25℃ to 85℃
■ Operating current	2.5mA (Typ)
■ Detect cycle	6msec (Typ)

Packages

BU21079F :

SOP16
10.00 ㎜×6.20 ㎜×1.71 ㎜

Typical Application Circuit

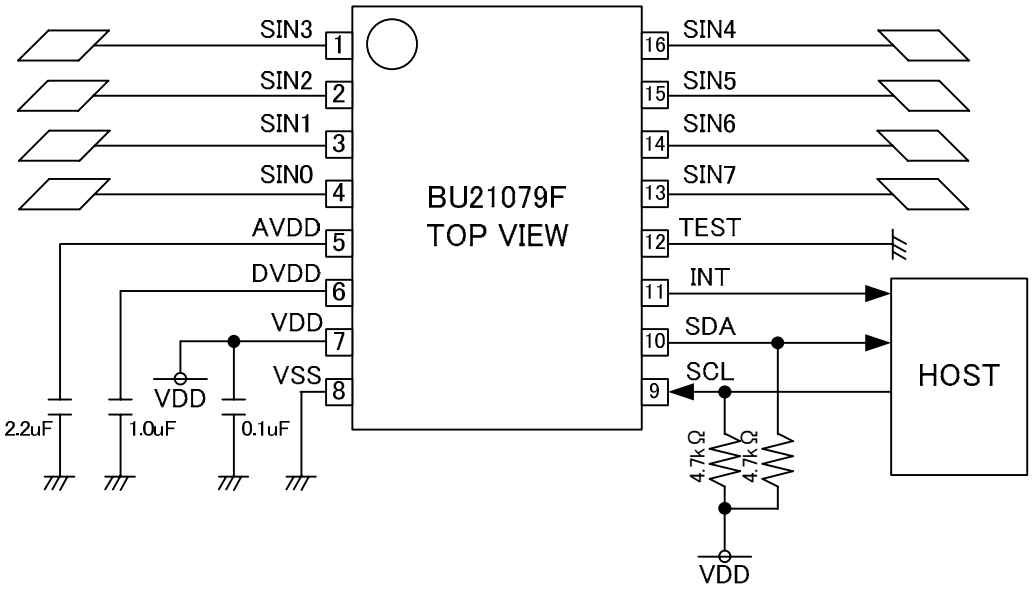


Figure 1. Typical Application Circuit

OVERVIEW

BU21079F is a capacitive sensor controller for switch operation.
BU21079F has the following blocks: AFE (Analog Front End) detecting capacitance, A/D converter, MPU, 2-wire serial bus interface compatible with I2C protocol, power-on-reset, and oscillator. It is operated with a 3.0V to 5.5V single power supply.

The results detected during switch operations (Touch/Release/Hold) are stored in a register. An interrupt is sent from INT port to the host when a register is updated during operations. If external noise and temperature drift are detected, automatic self-calibration is activated. When continuous monitoring of the host is unnecessary, the load of the host will be reduced.

Intermittent operation

When touch ON is detected, its operation shifts from intermittent operation to normal operation. When touch OFF is detected, its operation shifts from normal operation to intermittent operation, and the operating power is decreased. Sensing during intermittent operation is called “check sensing” and sensing during normal operation is called “normal sensing”.

Simple switch

One sensor is assigned to one switch. Each simple switch has the registers for the detected Touch/Release/Hold operations. Simple switches support multi-detect Touch/Release/Hold. It is possible to mask unused switches.

Matrix switches

The cross points of the sensors which are arranged in a matrix can be assigned to individual switches. Each matrix switch has registers for detected Touch/Release/Hold operations. Matrix switches do not support multi-detect Touch/Release/Hold. It is possible to mask unused matrix switches. BU21079F supports 16 matrix switches configured by 4x4 sensors.

Automatic self-calibration

BU21079F checks the status of the sensors based on the detected result. If external noise and temperature drift are detected, the automatic self-calibration is activated in order to get stable detection.

Host interface

BU21079F is slave device for the host device. 2-wire serial bus is compatible with I2C protocol.
Slave Address Is 0x5C.

Pin Configurations

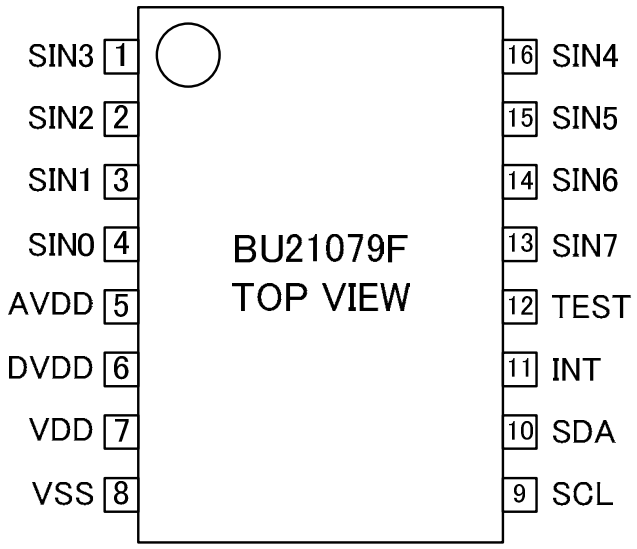


Figure 2. Pin configuration of BU21079F

Pin Descriptions

Pin Number	Pin Name	Type	Function	Note	Power	Initial condition	I/O Equivalence circuit
1	SIN3	Ain	Capacitive Touch Sensor 3		AVDD	Hi-Z	Fig.3
2	SIN2	Ain	Capacitive Touch Sensor 2		AVDD	Hi-Z	Fig.3
3	SIN1	Ain	Capacitive Touch Sensor 1		AVDD	Hi-Z	Fig.3
4	SIN0	Ain	Capacitive Touch Sensor 0		AVDD	Hi-Z	Fig.3
5	AVDD	Power	LDO output for analog blocks		—	—	—
6	DVDD	Power	LDO output for digital blocks		—	—	—
7	VDD	Power	Power		—	—	—
8	VSS	GND	Ground		—	—	—
9	SCL	In	Host I/F:SCL input pin		VDD	Hi-Z	Fig.4
10	SDA	InOut	Host I/F:SDA input/output pin		VDD	Hi-Z	Fig.4
11	INT	Out	Interrupt output	Interrupt “H”	VDD	L	Fig.4
12	TEST	In	Test input	Fix “L” at the normal operation	VDD	—	Fig.5
13	SIN7	Ain	Capacitive Touch Sensor 7		AVDD	Hi-Z	Fig.3
14	SIN6	Ain	Capacitive Touch Sensor 6		AVDD	Hi-Z	Fig.3
15	SIN5	Ain	Capacitive Touch Sensor 5		AVDD	Hi-Z	Fig.3
16	SIN4	Ain	Capacitive Touch Sensor 4		AVDD	Hi-Z	Fig.3

I/O Equivalent Circuits

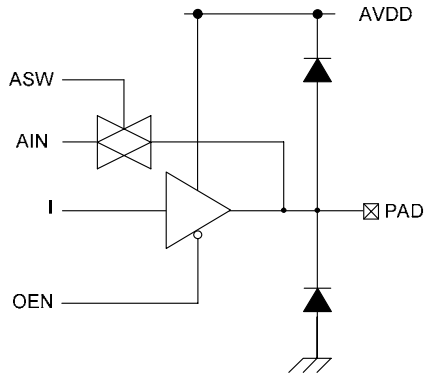


Figure 3. I/O equivalent circuit (a)

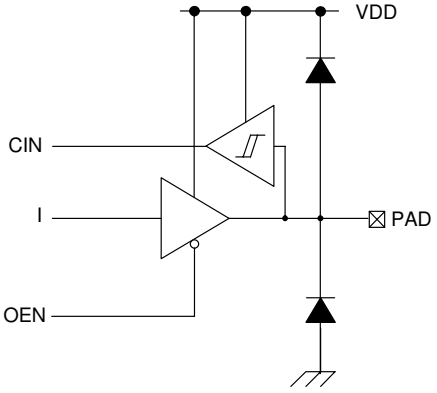


Figure 4. I/O equivalent circuit (b)

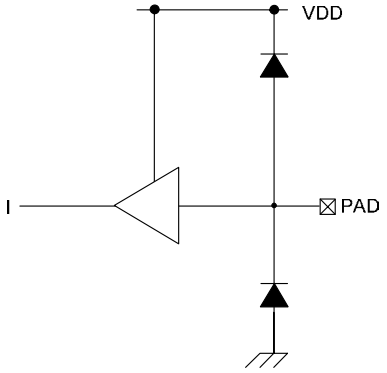


Figure 5. I/O equivalent circuit (c)

Block Diagram

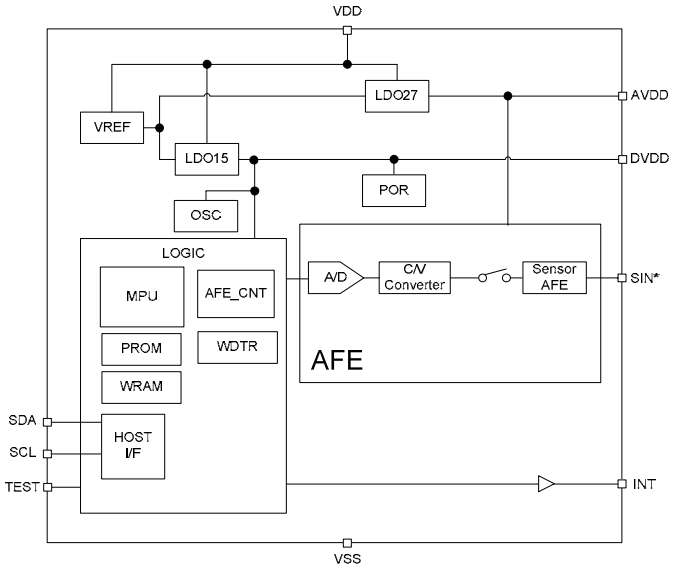


Figure 6. Block Diagram

Description of Blocks

Sensor AFE、C/V Converter
Converts capacitance from the sensors to voltage.

A/D
Converts the voltage from C/V Converter to digital.

LDO27
2.7V output LDO for Sensor AFE, C/V Converter and A/D.

LDO15
1.5V output LDO for OSC and digital blocks.

OSC
Ring oscillator used for the system clock.

POR
Power-On-Reset monitoring LDO15 for system reset.

MPU
Controls switch operations based on the sensing results and run Auto-calibration.
INT port informs the host that switch operations are detected.

PROM
Programmable ROM for the built-in MPU.

WRAM
Work RAM for the built-in MPU.

HOST I/F
2-wire serial bus interface compatible with I2C protocol.

AFE_CNT
Sequencer of Sensor AFE, C/V converter and A/D.

WDTR
Watchdog Timer Reset. It operates as the system resets. If MPU hangs-up, Watchdog Timer Reset can reset the IC.

Absolute Maximum Ratings (Ta = 25℃)

Parameter	Symbol	Rating	Unit
Power supply voltage	VDD	-0.5 to 7.0	V
Input voltage	V_{IN}	-0.5 to VDD + 0.3	V
Storage temperature range	T_{stg}	-55 to 125	℃
Permissible loss	P_d	0.30 *1	W
Maximum junction temperature	T_{jmax}	125	℃

*1 Derate by 3.00mW/℃ when operating above Ta =25℃. (IC only).
When mounted in a Rohm standard board (70mm x 70mm x 1.6t mm), Pd is 0.50W, and it reduces in 5.00mW/℃ over Ta=25℃.

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Power supply voltage	VDD	3.0 to 5.5	V
Operating temperature range	T_{opr}	-20 to 85	℃

Electrical Characteristics (Ta = 25℃ , VDD = 3.3V , VSS = 0V)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Input High voltage	V_{IH}	VDD x 0.7	-	VDD + 0.3	V	
Input Low voltage	V_{IL}	VSS - 0.3	-	VDD x 0.3	V	
Output High voltage	V_{OH}	VDD - 0.5	-	VDD	V	I_{OH} = -4mA
Output Low voltage	V_{OL}	VSS	-	VSS + 0.5	V	I_{OL} = 4mA
Oscillator clock frequency1	f_{OSC1}	45	50	55	MHz	
Oscillator clock frequency2	f_{OSC2}	51.2	64	76.8	KHz	
DVDD LDO output voltage	V_{DVDD}	1.35	1.50	1.65	V	
AVDD LDO output voltage	V_{AVDD}	2.61	2.71	2.81	V	
Full scan operating current	I_{DD}	-	2.5	-	mA	No load of sensors.
Intermittent operating current	I_{INT}		75		uA	Intermittent operation cycle 200m s

Register Map (OSC = 50MHz, unless otherwise noted.)
No accessing to the reserved areas is allowed

Group	Address	Name	R/W	Ini	7	6	5	4	3	2	1	0
Detect value	0x00	SIN_DATA0	R	0x00	SD_SIN0							
	0x01	SIN_DATA1	R	0x00	SD_SIN1							
	0x02	SIN_DATA2	R	0x00	SD_SIN2							
	0x03	SIN_DATA3	R	0x00	SD_SIN3							
	0x04	SIN_DATA4	R	0x00	SD_SIN4							
	0x05	SIN_DATA5	R	0x00	SD_SIN5							
	0x06	SIN_DATA6	R	0x00	SD_SIN6							
	0x07	SIN_DATA7	R	0x00	SD_SIN7							
	0x08	SIN_DATA8	R	0x00	SD_SIN8							
	0x09-0F	reserved	R	0x00	-							
Detect result	0x10	INTERRUPT	R	0x00	CONTDET	OFFDET	ONDET	PERCAL	WDT	ERCAL	CAL	INI
	0x11	SIN_STATE	R	0x00	SIN7_STAT	SIN6_STAT	SIN5_STAT	SIN4_STAT	SIN3_STAT	SIN2_STAT	SIN1_STAT	SIN0_STAT
	0x12	Reserved	R	0x00	-							
	0x13	DETECT_SW_ON	R	0x00	SW7_ON	SW6_ON	SW5_ON	SW4_ON	SW3_ON	SW2_ON	SW1_ON	SW0_ON
	0x14	DETECT_SLIDER_ON	R	0x00	SLIDER_ON	SLIDER_CNT						
	0x15	DETECT_MAT_ON	R	0x00	MAT_ON	-			KEY_ON			
	0x16	DETECT_SW_OFF	R	0x00	SW7_OFF	SW6_OFF	SW5_OFF	SW4_OFF	SW3_OFF	SW2_OFF	SW1_OFF	SW0_OFF
	0x17	DETECT_SLIDER_OFF	R	0x00	SLIDER_OFF	-						
	0x18	DETECT_MAT_OFF	R	0x00	MAT_OFF	-			KEY_OFF			
	0x19	DETECT_SW_CONT	R	0x00	SW7_CONT	SW6_CONT	SW5_CONT	SW4_CONT	SW3_CONT	SW2_CONT	SW1_CONT	SW0_CONT
	0x1A	Reserved	R	0x00	-							
	0x1B	DETECT_MAT_CONT	R	0x00	MAT_CONT	-			KEY_CONT			
	0x1C	STATE	R	0x00	E_CALIB	-	-	-	-	-	INTVL	CALIB
	0x1D	Reserved	R	0x00	-							
	0x1E	RACT	R	0x00	RACT							
	0x1F-84	Reserved	R	0x00	-							
Reset setting	0x85	SOFTRESET0	R/W	0x00	SRST[7:0]							
	0x86-89	Reserved	-	-	reserved							
	0x8A	SOFTRESET1	R/W	0x00	SRST[15:8]							
-	0x8B-BF	Reserved	-	-	reserved							
Sensor setting	0xC0	CFG_SIN_1_0	R/W	0x00	GA_SIN1		ON_SIN1		GA_SIN0		ON_SIN0	
	0xC1	CFG_SIN_3_2	R/W	0x00	GA_SIN3		ON_SIN3		GA_SIN2		ON_SIN2	
	0xC2	CFG_SIN_5_4	R/W	0x00	GA_SIN5		ON_SIN5		GA_SIN4		ON_SIN4	
	0xC3	CFG_SIN_7_6	R/W	0x00	GA_SIN7		ON_SIN7		GA_SIN6		ON_SIN6	
	0xC4	CFG_SIN_x_8	R/W	0x00	-		-		GA_SIN8		ON_SIN8	
	0xC5-C7	Reserved	R/W	0x00	-							
	0xC8	GAIN_1_0	R/W	0x00	GA1				GA0			
	0xC9	GAIN_x_2	R/W	0x00	-				GA2			
	0xCA	ON_TH0	R/W	0x00	ON0							
	0xCB	ON_TH1	R/W	0x00	ON1							
	0xCC	ON_TH2	R/W	0x00	ON2							
	0xCD	OFF_TH	R/W	0x00	-	OFF						
	0xCE	OVERSAMPLES	R/W	0x00	OST				-			
	0xCF	CONTTIMES	R/W	0x00	CONTSEL	-	CONT					

Register Map (OSC = 50MHz, unless otherwise specified).
Access to reserved areas is restricted.

Group	Address	Name	R/W	Ini	7	6	5	4	3	2	1	0
Mask setting	0xD0	MSK_DETECT_SW	R/W	0x00	MSK_SW7	MSK_SW6	MSK_SW5	MSK_SW4	MSK_SW3	MSK_SW2	MSK_SW1	MSK_SW0
	0xD1	Reserved	R/W	0x00	-							
	0xD2	MSK_DETECT_MAT0	R/W	0x00	MSK_KEYH	MSK_KEYG	MSK_KEYF	MSK_KEYE	MSK_KEYD	MSK_KEYC	MSK_KEYB	MSK_KEYA
	0xD3	MSK_DETECT_MAT1	R/W	0x00	MSK_KEYP	MSK_KEYO	MSK_KEYN	MSK_KEYM	MSK_KEYL	MSK_KEYK	MSK_KEYJ	MSK_KEYI
	0xD4-D8	Reserved	R/W	0x00	-							
	0xD9	EN_SLIDER	R/W	0x00	EN_SLID_SIN7	EN_SLID_SIN6	EN_SLID_SIN5	EN_SLID_SIN4	EN_SLID_SIN3	EN_SLID_SIN2	EN_SLID_SIN1	EN_SLID_SIN0
	0xDA	KEEP_SENS_NUM	R/W	0x00	KEEP_SENS_NUM							
	0xDB	UNIT_SENS_NUM	R/W	0x00	-				UNIT_SENS_NUM			
	0xDC	TH_SLEEP_H	R/W	0x00	TH_SLEEP[15:8]							
	0xDD	TH_SLEEP_L	R/W	0x00	TH_SLEEP[7:0]							
	0xDE	OUTPUT_OFFSET	R/W	0x00	OUTPUT_OFFSET							
	0xDF	MSK_INTERRUPT	R/W	0x00	-	-	-	MSK_PERCAL	MSK_WDT	MSK_ERCAL	MSK_CAL	-
Analog setting	0xE0	MODE_CONFIG0	R/W	0x00	-	-	FIX_BASE_CYC	FIX_SNS_CYC	-	SLID_LOOP	EN_DSLP	EN_SLP
	0xE1	MODE_CONFIG1	R/W	0x00	DIS_SIN8	-		PERCAL_DIS	RET_DIS	HOP_DIS	ERROR_DIS	DRIFT_DIS
	0xE2	EN_SIN	R/W	0x00	EN_SIN7	EN_SIN6	EN_SIN5	EN_SIN4	EN_SIN3	EN_SIN2	EN_SIN1	EN_SIN0
	0xE3	SENS_NUM	R/W	0x00	SENS_NUM							
	0xE4	SENS_RD_TIME	R/W	0x00	SENS_RD_TIME							
	0xE5	SENS_RST_TIME	R/W	0x00	SENS_RST_TIME							
	0xE6	SENS_IRST_TIME	R/W	0x00	SENS_IRST_TIME							
	0xE7	CHK_NUM	R/W	0x00	CHK_NUM							
	0xE8	CHK_RD_TIME	R/W	0x00	CHK_RD_TIME							
	0xE9	CHK_RST_TIME	R/W	0x00	CHK_RST_TIME							
	0xEA	CHK_IRST_TIME	R/W	0x00	CHK_IRST_TIME							
	0xEB	DIG_GAIN	R/W	0x00	CHK_DIG_GAIN				SENS_DIG_GAIN			
	0xEC	CHK_WAIT_TIME	R/W	0x00	CHK_WAIT_TIME							
	0xED	SENS_WAIT_TIME	R/W	0x00	SENS_WAIT_TIME							
	0xEE	CALIB_CONFIG0	R/W	0x00	RET_NUM							
	0xEF	CALIB_CONFIG1	R/W	0x00	PRECAL_PERIOD				DRIFT_SIN_NUM			
Control	0xF0	CLR_INT	R/W	0x00	-	-	-	C_PERCAL	C_WDT	C_ERCAL	C_CAL	C_INI
	0xF1	CLR_DETECT_SW_ON	R/W	0x00	C_SW7_ON	C_SW6_ON	C_SW5_ON	C_SW4_ON	C_SW3_ON	C_SW2_ON	C_SW1_ON	C_SW0_ON
	0xF2	Reserved	R/W	0x00	-							
	0xF3	CLR_DETECT_MAT_ON	R/W	0x00	C_MAT_ON	-	-	-	-	-	-	-
	0xF4	CLR_DETECT_SW_OFF	R/W	0x00	C_SW7_OFF	C_SW6_OFF	C_SW5_OFF	C_SW4_OFF	C_SW3_OFF	C_SW2_OFF	C_SW1_OFF	C_SW0_OFF
	0xF5	CLR_DETECT_SLIDER_OF	R/W	0x00	C_SLIDER_OFF	-	-	-	-	-	-	-
	0xF6	CLR_DETECT_MAT_OFF	R/W	0x00	C_MAT_OFF	-	-	-	-	-	-	-
	0xF7	CLR_DETECT_SW_CONT	R/W	0x00	C_SW7_CONT	C_SW6_CONT	C_SW5_CONT	C_SW4_CONT	C_SW3_CONT	C_SW2_CONT	C_SW1_CONT	C_SW0_CONT
	0xF8	Reserved	R/W	0x00	-							
	0xF9	CLR_DETECT_MAT_CONT	R/W	0x00	C_MAT_CONT	-	-	-	-	-	-	-
	0xFA-FD	Reserved	R/W	0x00	-							
	0xFE	WACT	R/W	0x00	WACT							
	0xFF	CONTROL	R/W	0x00	FRCRLS	CALOVF	-	CALMOD	-	CFG	CAL	ACT

【0x00-0x08 : Sensor Data】

Name: SIN_DATA
Address: 0x00-0x08
Description: This register shows the 8bit ADC values for each sensor.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	SD_SIN0[7]	SD_SIN0[6]	SD_SIN0[5]	SD_SIN0[4]	SD_SIN0[3]	SD_SIN0[2]	SD_SIN0[1]	SD_SIN0[0]
0x01	SD_SIN1[7]	SD_SIN1[6]	SD_SIN1[5]	SD_SIN1[4]	SD_SIN1[3]	SD_SIN1[2]	SD_SIN1[1]	SD_SIN1[0]
0x02	SD_SIN2[7]	SD_SIN2[6]	SD_SIN2[5]	SD_SIN2[4]	SD_SIN2[3]	SD_SIN2[2]	SD_SIN2[1]	SD_SIN2[0]
0x03	SD_SIN3[7]	SD_SIN3[6]	SD_SIN3[5]	SD_SIN3[4]	SD_SIN3[3]	SD_SIN3[2]	SD_SIN3[1]	SD_SIN3[0]
0x04	SD_SIN4[7]	SD_SIN4[6]	SD_SIN4[5]	SD_SIN4[4]	SD_SIN4[3]	SD_SIN4[2]	SD_SIN4[1]	SD_SIN4[0]
0x05	SD_SIN5[7]	SD_SIN5[6]	SD_SIN5[5]	SD_SIN5[4]	SD_SIN5[3]	SD_SIN5[2]	SD_SIN5[1]	SD_SIN5[0]
0x06	SD_SIN6[7]	SD_SIN6[6]	SD_SIN6[5]	SD_SIN6[4]	SD_SIN6[3]	SD_SIN6[2]	SD_SIN6[1]	SD_SIN6[0]
0x07	SD_SIN7[7]	SD_SIN7[6]	SD_SIN7[5]	SD_SIN7[4]	SD_SIN7[3]	SD_SIN7[2]	SD_SIN7[1]	SD_SIN7[0]
0x08	SD_SIN8[7]	SD_SIN8[6]	SD_SIN8[5]	SD_SIN8[4]	SD_SIN8[3]	SD_SIN8[2]	SD_SIN8[1]	SD_SIN8[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x10 : Interrupt factor】

Name: INTERRUPT
Address: 0x10
Description: This register shows the interrupt factors. Port INT outputs this register's OR operation.

INI : Initialization finish.
It is set at the time the initialization of the MPU is completed.
There is no corresponding mask register. The clear register is 0xF0 [0].
It is also set when initialization by WDT occurs.

CAL : Software-calibration finish.
It is set at the time the calibration is finished.
The corresponding mask register is 0xDF [1], and the clear register is 0xF0 [1].

ERCAL : Self-calibration finish.
It is set at the time the calibration is ended by an error. There are four errors in calibration (Drift calibration, Calib-error calibration, Hopping calibration, and Return calibration).The corresponding mask register is 0xDF [2] and the clear register is 0xF0[2].

WDT : Watch Dog Timer interrupt generation
It is WDT interruption generation time.
If WDT interrupt occurs again without clearing WDT, HW reset will start, all are initialized, and INIT interruption of 0x10 [0] is active (low).
The corresponding mask register is 0xDF [3], and the clear register is 0xF0 [3].
The clearance of the WDT counter by MPU is not performed other than the time of a sense.
Therefore, in the state of deep sleep (0xE0 [1] =0), a WDT interrupt occurs periodically.
* The initial state is deep sleep.

PERCAL : Periodic calibration finish.
It is set at the time the periodic calibration is completed.
The corresponding mask register is 0xDF [4], and the clear register is 0xF0 [4].

ONDET : Detection of switch-on.
The value of this register is '1 'when it detects "ON" switch operation. This register is cleared by clearing every bit of the "Detection Switch-On" register. (0x13, 0x15)

OFFDET : Detection of switch-off.
The value of this register is '1 'when it detects "OFF" switch operation. This register is cleared by clearing every bit of the "Detection Switch-Off" register.(0x16, 0x18)

CONTDET : Detection of continued touch.
The value of this register is '1 'when it detects a continued touch switch operation. This register is cleared by clearing every bit of the "Detection continued touch" register.(0x19, 0x1B)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x10	CONTDET	OFFDET	ONDET	PERCAL	WDT	ERCAL	CAL	INI
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x11 : Sensor State】

Name: SIN_STATE
Address: 0x11
Description: This register indicates the state of each sensor.
1 : Switch-on.(Register “SIN” > Register “ON”) 0 : switch-off. (Register “SIN” < Register “OFF”)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x11	SIN7_STAT	SIN6_STAT	SIN5_STAT	SIN4_STAT	SIN3_STAT	SIN2_STAT	SIN1_STAT	SIN0_STAT
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x13, 0x15 : Detection Switch-On】

Name: DETECT_ON
Address: 0x13, 0x15
Description: This register indicates the transition from Off state to On state of every switch.
Since SW 0-7 supports multiple presses, each switch has bit recognition. And the matrix key does not support multiple detection, so matrix switch is indicated by 1 bit for ON detection (MAT) and 4 bits (KEY switch). Logical OR of each SW and MAT will be ONDET interrupt source register.
1: Detect On. 0: No detect.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x13	SW7_ON	SW6_ON	SW5_ON	SW4_ON	SW3_ON	SW2_ON	SW1_ON	SW0_ON
0x15	MAT_ON	-	-	-	KEY_ON[3]	KEY_ON[2]	KEY_ON[1]	KEY_ON[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x14 : Detection slider On】

Name: DETECT_SLIDER_ON
Address: 0x14
Description: SLIDER_ON: The value of this register is “1” when SLIDER is detected.
1: Detect On. 0: No detect.
SLIDER_CNT[6:0] : The detected amount of movement is shown in 2’s complement. The amount of movement detected in order of SIN0→SIN1→SIN2→⋯→SIN7 is expressed by a positive value, and the amount of the movement detected in a reverse order is expressed by a negative value. The amount of the movement is 2 when center of gravity moves to the next sensor, and when center of gravity comes between 2 sensors, the amount of the movement is 1. It loops when the range where the detected amount of movement that can be shown is exceeded. The next of 63(0111111) become -64(1000000).

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x14	SLIDER_ON	SLIDER_ CNT[6]	SLIDER_ CNT[5]	SLIDER_ CNT[4]	SLIDER_ CNT[3]	SLIDER_ CNT[2]	SLIDER_ CNT[1]	SLIDER_ CNT[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x16, 0x18 : Detection Switch-Off】

Name: DETECT_OFF
Address: 0x16, 0x18
Description: This register indicates the transition from On state to Off state of every switch.
Since SW 0-7 supports multiple presses, each switch has bit recognition. And the matrix key does not support multiple detection, so matrix switch is indicated by 1 bit for ON detection (MAT) and 4 bits (KEY switch). Logical OR of each SW and MAT will be OFFDET interrupt source register.
1 : Detect Off. 0 : No detect.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x16	SW7_OFF	SW6_OFF	SW5_OFF	SW4_OFF	SW3_OFF	SW2_OFF	SW1_OFF	SW0_OFF
0x18	MAT_OFF	-	-	-	KEY _OFF[3]	KEY_OFF[2]	KEY _OFF[1]	KEY _OFF[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x17 : Detection slider Off】

Name: DETECT_SLIDER_OFF
Address: 0x17
Description: It is set when IC detects that the slider is in the off state. It is necessary to clear this flag to detect. The corresponding clear register is 0xF5 [7]. 1 : Detect Off. 0 : No detect.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x17	SLIDER_OFF	-	-	-	-	-	-	-
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x19, 0x1B : Detection continued touch】

Name: DETECT_CONT
Address: 0x19, 0x1B
Description: This register indicates the detection of continued touch for every switch.
Since SW 0-7 supports multiple presses, each switch has bit recognition. And the matrix key does not support multiple detection, so matrix switch is indicated by 1 bit for ON detection (MAT) and 4 bits(KEY switch). Logical OR of each SW and MAT will be CONTDET interrupt source register.
1 : Detect continued touch. 0 : No detect.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x19	SW7_CONT	SW6_CONT	SW5_CONT	SW4_CONT	SW3_CONT	SW2_CONT	SW1_CONT	SW0_CONT
0x1B	MAT_CONT	-	-	-	KEY_CONT[3]	KEY_CONT[2]	KEY_CONT[1]	KEY_CONT[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x1C : State of IC】

Name: STATE
Address: 0x1C
Description: This register indicates the state of IC.

CALIB : Indicates whether the IC is in calibration or not.
1: In calibration 0: Not in calibration
INTVL : Indicates whether the IC is in Intermittent Operation or not.
1: Intermittent Operation 0: Not in Intermittent Operation
E_CALIB : When the calibration fails for three consecutive times, it is set.
1: Calibration Error 0: No Error

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1C	E_CALIB	-	-	-	-	-	INTVL	CALIB
R/W	R	-	-	-	-	-	R	R
Initial val.	0	-	-	-	-	-	0	0

【0x1E : Read register for operation check of MPU】

Name: RACT
Address: 0x1E
Description: This register is a read register for operational check of the IC. The value written to the write register for operation check (Address is 0xFE) is copied to this register. If the write value and the read value is equal, MPU and I/F are operating normally.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x1E	RACT[7]	RACT[6]	RACT[5]	RACT[4]	RACT[3]	RACT[2]	RACT[1]	RACT[0]
R/W	R	R	R	R	R	R	R	R
Initial val.	0	0	0	0	0	0	0	0

【0x85, 0x8A : Software Reset】

Name: SRST
Address: 0x85, 0x8A
Description: These registers are used for hardware reset. If register 0x85=55h and register 0x8A=AAh, then a hardware reset will be done.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x85	SRST[7]	SRST[6]	SRST[5]	SRST[4]	SRST[3]	SRST[2]	SRST[1]	SRST[0]
0x8A	SRST[15]	SRST[14]	SRST[13]	SRST[12]	SRST[11]	SRST[10]	SRST[9]	SRST[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xC0 – 0xC4 : Select a setting for Gain and Threshold for "Off→On"】

Name: CFG_SIN
Address: 0xC0 – 0xC4
Description: You can set 3 values for gain and set 3 values for threshold to the "Off → On" registers of this IC.
These registers are used to select a setting for gain and threshold for every sensor. There are three available settings.

Gain : GA_SIN*[1:0] = 0x0 : Select GA0.
0x1 : Select GA1.
0x2 : Select GA2.
0x3 : Select GA0.

Threshold : ON_SIN*[1:0] = 0x0 : Select ON0.
0x1 : Select ON1.
0x2 : Select ON2.
0x3 : Select ON0.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC0	GA_SIN1[1]	GA_SIN1[0]	ON_SIN1[1]	ON_SIN1[0]	GA_SIN0[1]	GA_SIN0[0]	ON_SIN0[1]	ON_SIN0[0]
0xC1	GA_SIN3[1]	GA_SIN3[0]	ON_SIN3[1]	ON_SIN3[0]	GA_SIN2[1]	GA_SIN2[0]	ON_SIN2[1]	ON_SIN2[0]
0xC2	GA_SIN5[1]	GA_SIN5[0]	ON_SIN5[1]	ON_SIN5[0]	GA_SIN4[1]	GA_SIN4[0]	ON_SIN4[1]	ON_SIN4[0]
0xC3	GA_SIN7[1]	GA_SIN7[0]	ON_SIN7[1]	ON_SIN7[0]	GA_SIN6[1]	GA_SIN6[0]	ON_SIN6[1]	ON_SIN6[0]
0xC4	-	-	-	-	GA_SIN8[1]	GA_SIN8[0]	ON_SIN8[1]	ON_SIN8[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xC8 – 0xC9 : Value of GAIN】

Name: GA0、GA1、GA2
Address: 0xC8 – 0xC9
Description: This register is used for setting the gain of AFE. The smaller the value of GA, the higher the gain will be. You can set 3 values for gain. These values are assigned to each sensor by register GA_SIN including CFG_SIN.
The settable range : 0x1 ≦ GA ≦ 0xF

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xC8	GA1[3]	GA1[2]	GA1[1]	GA1[0]	GA0[3]	GA0[2]	GA0[1]	GA0[0]
0xC9	-	-	-	-	GA2[3]	GA2[2]	GA2[1]	GA2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xCA – 0xCC : Value of the threshold for "Off → On"】

Name: ON0、ON1、ON2
Address: 0xCA – 0xCC
Description: These registers are used for setting the threshold of the "Off → On" operation. You can set 3 values for threshold. If the 8bit ADC value of each sensor (register SENS_DATA) is larger than this value, then the "Off → On" operation of the sensor is valid. These values are assigned to each sensor by register GA_SIN including ON_SIN.
The settable range : 0x00 < OFF < ON < 0xFF

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCA	ON0[7]	ON0[6]	ON0[5]	ON0[4]	ON0[3]	ON0[2]	ON0[1]	ON0[0]
0xCB	ON1[7]	ON1[6]	ON1[5]	ON1[4]	ON1[3]	ON1[2]	ON1[1]	ON1[0]
0xCC	ON2[7]	ON2[6]	ON2[5]	ON2[4]	ON2[3]	ON2[2]	ON2[1]	ON2[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xCD : Value of the threshold for "On → Off"】

Name: OFF
Address: 0xCD
Description: This register is used for setting the threshold for "On → Off" operation. If the 8bit ADC value of each sensor (register SENS_DATA) is smaller than this value, then the "On → Off" operation of the sensor is enabled.
The setting range : 0x00 < OFF < ON < 0xFF

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCD	-	OFF [6]	OFF [5]	OFF [4]	OFF [3]	OFF [2]	OFF [1]	OFF [0]
R/W	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	-	0	0	0	0	0	0	0

【0xCE :Chattering cancel】

Name: OVERSAMPLES
Address: 0xCE
Description: OST[3:0] : This register has the number of times of over sampling for canceling chattering in the "ON" or "OFF" operation.
The continuous button level of over sampling frequency + three times or less is disregarded.
If the register value is 0, then the number of times of over sampling is 1.
Sampling rate : About 6msec.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCE	OST[3]	OST[2]	OST[1]	OST[0]	-	-	-	-
R/W	R/W	R/W	R/W	R/W	-	-	-	-
Initial val.	0	0	0	0	-	-	-	-

【0xCF :Long press】

Name: CONTTIMES
Address: 0xCF
Description: CONTSEL : The output pattern of an interrupt generated after recognizing long press is set up.

1 : Every continuous touch period.
0 : First detect only.

CONT[5:0] : Continuous touch period is about 0.036 [sec] x CONT.
If the setting value is 0x0, continuous touch function is invalid.
(0.036sec ≦ Continuous touch period ≦2.3sec)

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xCF	CONTSEL	-	CONT[5]	CONT[4]	CONT[3]	CONT[2]	CONT[1]	CONT[0]
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	-	0	0	0	0	0	0

【0xD0, 0xD2, 0xD3 : Mask switch operation】

Name: MSK_SW_KEY
Address: 0xD0, 0xD2, 0xD3
Description: This register is used for masking the operation of each matrix switches and each simple switches. The masked switches are excluded from the interrupt factor. It is prohibited to assign one sensor to both matrix switch and a simple switch. Unused switches must be masked.
1 : Masked. 0 : Unmasked.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD0	MSK_SW7	MSK_SW6	MSK_SW5	MSK_SW4	MSK_SW3	MSK_SW2	MSK_SW1	MSK_SW0
0xD2	MSK_KEYH	MSK_KEYG	MSK_KEYF	MSK_KEYE	MSK_KEYD	MSK_KEYC	MSK_KEYB	MSK_KEYA
0xD3	MSK_KEYP	MSK_KEYO	MSK_KEYN	MSK_KEYM	MSK_KEYL	MSK_KEYK	MSK_KEYJ	MSK_KEYI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xD9 : Slider】

Name: EN_SLIDER
Address: 0xD9
Description: EN_SLID_SIN [7:0]: It is used for enabling a sensor for a slider.
The sensor by which 1 was set is enabled as a slider. The order is SIN0, 1, 2, 3, 4, 5, 6, and 7, and the disabled sensor is skipped. For example, when only SIN1, 2, 5, and 6 are enabled, the order is SIN1, 2, 5, 6. Moreover, when SLIDER_LOOP (0xE0 2) is enabled, SIN7 and SIN0 are processed as a consecutive sensor. When touch is detected in any of the sensors operating in intermittent mode, all enabled sensors start sensing.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xD9	EN_SLID_SIN7	EN_SLID_SIN6	EN_SLID_SIN5	EN_SLID_SIN4	EN_SLID_SIN3	EN_SLID_SIN2	EN_SLID_SIN1	EN_SLID_SIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xDA : Keep intermittent sensing】

Name: KEEP_SENS_NUM
Address: 0xDA
Description: KEEP_SENS_NUM[7:0] : This is used for setting how long sensing operates from last intermittent operation.
It works only in the intermittent operation.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDA	KEEP_SENS_NUM[7]	KEEP_SENS_NUM[6]	KEEP_SENS_NUM[5]	KEEP_SENS_NUM[4]	KEEP_SENS_NUM[3]	KEEP_SENS_NUM[2]	KEEP_SENS_NUM[1]	KEEP_SENS_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xDB : Frequency of normal sensing during check sensing】

Name: UNIT_SENS_NUM
Address: 0xDB
Description: UNIT_SENS_NUM[3:0] : It is used to set the number of times normal sensing is done during check sensing for intermittent return. It works only in the intermittent operation. The number of times normal sensing is done is equal to the set value + 1.
For example, when 3 is set up, it becomes check -> Normal -> Normal -> Normal -> Normal -> check -> Normal -> Normal --.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDB	-	-	-	-	UNIT_SENS_NUM[3]	UNIT_SENS_NUM[2]	UNIT_SENS_NUM[1]	UNIT_SENS_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xDC : Intermittent operation return threshold setting 】

Name: TH_SLEEP_H
Address: 0xDC
Description: TH_SLEEP[15:8] : It is the upper 8 bits of the return threshold value from intermittent operation to normal operation. The lower 8 bits is register 0xDD. When the result of check sensing shifts from the median and more than this threshold value, that sensor is returned from intermittent operation and normal sensing operates.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDC	TH_SLEEP[15]	TH_SLEEP[14]	TH_SLEEP[13]	TH_SLEEP[12]	TH_SLEEP[11]	TH_SLEEP[10]	TH_SLEEP[9]	TH_SLEEP[8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xDD : Intermittent sensing return threshold setting 】

Name: TH_SLEEP_L
Address: 0xDD
Description: TH_SLEEP[7:0] : It is the lower 8 bits of the return threshold value from intermittent operation to normal operation. Please refer to register 0xDC.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDD	TH_SLEEP[7]	TH_SLEEP[6]	TH_SLEEP[5]	TH_SLEEP[4]	TH_SLEEP[3]	TH_SLEEP[2]	TH_SLEEP[1]	TH_SLEEP[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xDE : Sensor value offset setting 】

Name: OUTPUT_OFFSET
Address: 0xDE
Description: OUTPUT_OFFSET[7:0] : The offset added to the sensor value output to SD_SIN0-SD_SIN8(0x00-0x08) is set. When the calibration is completed, these sensor values reach the value of about 0.Therefore, it is shown as 0, and doesn't acquire an accurate value when swinging to negative. When offset is added, monitoring data at the minus side and acquiring an accurate value becomes possible.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDE	OUTPUT_ OFFSET[7]	OUTPUT_ OFFSET[6]	OUTPUT_ OFFSET[5]	OUTPUT_ OFFSET[4]	OUTPUT_ OFFSET[3]	OUTPUT_ OFFSET[2]	OUTPUT_ OFFSET[1]	OUTPUT_ OFFSET[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xDF : Mask interrupt】

Name: MSK_INTERRUPT
Address: 0xDF
Description: This register is for masking the interrupt factor. The masked interrupt factor is not shown on the register "Interrupt factor (address 0x10)", so it does not affect the output port INT.
1 : Masked. 0 : Unmasked.

MSK_CAL : Mask for Software-calibration finish.
This bit is used for masking the interrupt of Software-calibration finish (the bit CAL in the register INTERRUPT(address 0x10)).

MSK_ERCAL : Mask for Self-calibration finish.
This bit is used for masking the interrupt of Self-calibration finish (the bit ERCAL in the register INTERRUPT(address 0x10)).

MSK_WDT : Mask for watch dog timer.
This bit is used for masking the interrupt of initialization by WDT.
WDT of register interrupt factor (address 0x10) is masked.

MSK_PERCAL : Mask for Periodic calibration finish.
This bit is used for masking the interrupt of Periodic calibration finish (the bit PERCAL in the register INTERRUPT(address 0x10)).

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xDF	-	-	-	MSK_PERCAL	MSK_WDT-	MSK_ERCAL	MSK_CAL	-
R/W	-	-	-	R/W	R/W	R/W	R/W	-
Initial val.	-	-	-	0	-0	0	0	-

【0xE0 : Operation mode setting0】

Name: MODE_CONFIG0
Address: 0xE0
Description: FIX_BASE_CYC : Sensing frequency is changed at the time of calibration failure, and returns the error occurrence time. The noise measure function is disabled.
FIX_SNS_CYC : The noise measures function to change the frequency of sensing to each sensing is invalidated.
SLID_LOOP : Process which treats CH recognized as a slider like a sensor continuous like SIN6->SIN7->SIN0 and SIN1 ->SIN0 ->SIN7 is enabled.
EN_DSLP : The main clock is stopped when the main clock is not necessary while intermittent is operating and the operating current is lowered.
EN_SLP : Intermittent operation is activated and the operating current is lowered.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	-	-	FIX_BASE _CYC	FIX_SNS _CYC	-	SLID_LOOP	EN_DSLP	EN_SLP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE1 : Operation mode setting1】

Name: MODE_CONFIG1
Address: 0xE1
Description: DIS_SIN8: Disables SIN8 for noise detection. Since sensing is not done when it is disabled, the operating current decreases.
RERCAL_DIS : Disables regular calibration.
RET_DIS : Disables return calibration. 1: disable function.
HOP_DIS : Disables hopping calibration. 1: disable function.
ERROR_DIS : Disables error calibration. 1: disable function.
DRIFT_DIS : Disables drift calibration. 1: disable function.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE1	DIS_SIN8	-	-	RERCAL_DIS	RET_DIS	HOP_DIS	ERROR_DIS	DRIFT_DIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE2 : Effective sensor setting 】

Name: EN_SIN
Address: 0xE2
Description: EN_SIN[7:0]: Enables sensors
The sensor by which 1 was set is enabled. Sensing is done only when the sensor is enabled. Disabling unnecessary sensors can lower current consumption.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE2	EN_SIN[7]	EN_SIN[6]	EN_SIN[5]	EN_SIN[4]	EN_SIN[3]	EN_SIN[2]	EN_SIN[1]	EN_SIN[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE3 : Data compare frequency setting】

Name: SENS_NUM
Address: 0xE3
Description: SENS_NUM[7:0] : The number of times data comparison is performed during 1 time of sensing .
Increasing the value also increases the accuracy but time and its current consumption also increases.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE3	SENS_NUM[7]	SENS_NUM[6]	SENS_NUM[5]	SENS_NUM[4]	SENS_NUM[3]	SENS_NUM[2]	SENS_NUM[1]	SENS_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE4 : Normal sensing timing setting 1 】

Name: SENS_RD_TIME
Address: 0xE4
Description: SENS_RD_TIME [7:0] : Comparator initial waiting time at normal sensing.
The time of one normal sensing increases by increasing the value.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE4	SENS_RD_TIME[7]	SENS_RD_TIME[6]	SENS_RD_TIME[5]	SENS_RD_TIME[4]	SENS_RD_TIME[3]	SENS_RD_TIME[2]	SENS_RD_TIME[1]	SENS_RD_TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE5 : Normal sensing timing setting 2 】

Name: SENS_RST_TIME
Address: 0xE5
Description: SENS_RST_TIME [7:0] : Setting of normal sensing at impressed time.
The time of normal sensing increases by increasing the value.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE5	SENS_RST_TIME[7]	SENS_RST_TIME[6]	SENS_RST_TIME[5]	SENS_RST_TIME[4]	SENS_RST_TIME[3]	SENS_RST_TIME[2]	SENS_RST_TIME[1]	SENS_RST_TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE6 : Normal sensing timing setting 3 】

Name: SENS_IRST_TIME
Address: 0xE6
Description: SENS_IRST_TIME [7:0] : Setting of normal sensing at initial impressed time.
The time of normal sensing increases by increasing the value.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE6	SENS_IRST_TIME[7]	SENS_IRST_TIME[6]	SENS_IRST_TIME[5]	SENS_IRST_TIME[4]	SENS_IRST_TIME[3]	SENS_IRST_TIME[2]	SENS_IRST_TIME[1]	SENS_IRST_TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE7 : Datacompare frequency setting at check sensing】

Name: CHK_NUM
Address: 0xE7
Description: CHK_NUM[7:0] : Frequency of data comparison by check sensing and one time of calibration sensing. Increasing the value also increases the accuracy but sensing time and its current consumption also increases.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE7	CHK_NUM[7]	CHK_NUM[6]	CHK_NUM[5]	CHK_NUM[4]	CHK_NUM[3]	CHK_NUM[2]	CHK_NUM[1]	CHK_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE8 : Check sensing timing setting1 】

Name: CHK_RD_TIME
Address: 0xE8
Description: CHK_RD_TIME [7:0] :Setting of comparator initial waiting time for check sensing and calibration sensing. Increasing the value also increases the time for one sensing.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE8	CHK_RD_TIME[7]	CHK_RD_TIME[6]	CHK_RD_TIME[5]	CHK_RD_TIME[4]	CHK_RD_TIME[3]	CHK_RD_TIME[2]	CHK_RD_TIME[1]	CHK_RD_TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xE9 : Check sensing timing setting 2 】

Name: CHK_RST_TIME
Address: 0xE8
Description: CHK_RST_TIME [7:0] : Setup time setting for check sensing and calibration sensing.
Increasing the value also increases the time for one sensing.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE9	CHK_RST_TIME[7]	CHK_RST_TIME[6]	CHK_RST_TIME[5]	CHK_RST_TIME[4]	CHK_RST_TIME[3]	CHK_RST_TIME[2]	CHK_RST_TIME[1]	CHK_RST_TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEA : Check sensing timing setting 3 】

Name: CHK_IRST_TIME
Address: 0xEA
Description: CHK_IRST_TIME [7:0] : Setup time setting for check sensing and calibration sensing. The value also increases the time for one sensing.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEA	CHK_IRST_TIME[7]	CHK_IRST_TIME[6]	CHK_IRST_TIME[5]	CHK_IRST_TIME[4]	CHK_IRST_TIME[3]	CHK_IRST_TIME[2]	CHK_IRST_TIME[1]	CHK_IRST_TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEB : Digital gain setting 】

Name: DIG_GAIN
Address: 0xEB
Description: CHK_DIG_GAIN [3:0]: The digital gain result at the time of check sensing and calibration sensing is shifted to the right only by the set value. The sensor value obtained with 0x00-0x08 is the value after the digital gain is applied.
SENS_DIG_GAIN [3:0]: Digital gain at the time of normal sensing
The result is shifted to the right only by the set value.
Moreover, the sensor value obtained with 0x00-0x08 is the value after the digital gain is applied.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEB	CHK_DIG_GAIN[3]	CHK_DIG_GAIN[2]	CHK_DIG_GAIN[1]	CHK_DIG_GAIN[0]	SENS_DIG_GAIN[3]	SENS_DIG_GAIN[2]	SENS_DIG_GAIN[1]	SENS_DIG_GAIN[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEC : Setting at intermittent operation time 】

Name: CHK_WAIT_TIME
Address: 0xEC
Description: CHK_WAIT_TIME [7:0] : It decides the execution interval between the check sensing and the next check sensing. Corresponds to check intervals when all sensors are judged OFF through touch judgement of check sensing. Check interval = (set value + 1) X 4 ms
When ON judgment is done, the check sensing interval is decided by the sensing execution interval.
Intermittent sensing is applied only when it is enabled.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xEC	CHK_WAIT TIME[7]	CHK_WAIT TIME[6]	CHK_WAIT TIME[5]	CHK_WAIT TIME[4]	CHK_WAIT TIME[3]	CHK_WAIT TIME[2]	CHK_WAIT TIME[1]	CHK_WAIT TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xED : Setting at normal sensing waiting time 】

Name: SENS_WAIT_TIME
Address: 0xED
Description: SENS_WAIT_TIME [7:0] : Waiting time until the next sensing starts.
Normal sensing interval = set value x 4 ms
When 0 is set, the next sensing starts after the MPU calculation ends.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	SENS_WAIT _TIME[7]	SENS_WAIT _TIME[6]	SENS_WAIT _TIME[5]	SENS_WAIT _TIME[4]	SENS_WAIT _TIME[3]	SENS_WAIT _TIME[2]	SENS_WAIT _TIME[1]	SENS_WAIT _TIME[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEE : Calibration setting 0 】

Name: CALIB_CONFIG0
Address: 0xEE
Description: RET_NUM[7:0] : Frequency setting for Calibration
The return calibration starts when the sensing that touch detection is not performed and it is operated continuously more than the setting value after returning from intermittent operation to normal operation.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	RET_NUM[7]	RET_NUM[6]	RET_NUM[5]	RET_NUM[4]	RET_NUM[3]	RET_NUM[2]	RET_NUM[1]	RET_NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xEF : Calibration setting 1 】

Name: CALIB_CONFIG1
Address: 0xEF
Description: PRECAL_PERIOD [7:4]: Setting at cyclic calibration execution intervals
When either of the next conditions is filled, a cyclic calibration is executed.
Sleep function disabled and (setting value +1) x 500 >= the number of sensing
Sleep function enabled and (setting value +1) x 50 >= the number of check sensing
DRIFT_SIM_NUM[3:0]: Number of drift calibration detection sensor channels
When the drift detected with the sensor channel is more than this setting value, the drift calibration is activated.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xE0	PRECAL_ PERIOD [7]	PRECAL_ PERIOD [6]	PRECAL_ PERIOD [5]	PRECAL_ PERIOD [4]	DRIFT_SIM_ NUM[3]	DRIFT_SIM_ NUM[2]	DRIFT_SIM_ NUM[1]	DRIFT_SIM_ NUM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF0 : Clear interrupt】

Name: CLR_INTERRUPT
Address: 0xF0
Description: Clear Interrupt Register
C_INI : Clear Interrupt of Initialization finish.
Clears the INI interrupt by writing ‘0’ in this register.
C_CAL : Clear Interrupt of Software-calibration finish.
Clears the CAL interrupt by writing ‘0’ in this register.
C_ERCAL : Clear Interrupt of Self-calibration finish.
Clears the ERCAL interrupt by writing ‘0’ in this register.
C_WDT : '0' is set when clearing the bit WDT of the interrupt factor register.
C_PERCAL : Clear Interrupt of Periodic calibration finish.
Clears the PERCAL interrupt by writing ‘0’ in this register.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF0	-	-	-	C_PERCAL	C_WDT	C_ERCAL	C_CAL	C_INI
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Initial val.	-	-	-	0	0	0	0	0

【0xF1, 0xF3 : Clear Switch-ON】

Name: CLR_DETECT_ON
Address: 0xF1, 0xF3
Description: DETECT_ON Clear Register. Clear the DETECT_ON by writing ‘0’ in these registers. If you write ‘1’, the operation is disabled. SW 0-15 has individual clear bit because SW 0-15 supports multiple presses. The matrix key’s DETECT_ON clear bit is 1bit for MAT because the matrix key does not support multiple press.
1 : Invalid. 0 :Clear.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF1	C_SW7_ON	C_SW6_ON	C_SW5_ON	C_SW4_ON	C_SW3_ON	C_SW2_ON	C_SW1_ON	C_SW0_ON
0xF3	C_MAT_ON	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF4, 0xF6 : Clear Switch-OFF】

Name: CLR_DETECT_OFF
Address: 0xF4, 0xF6
Description: DETECT_OFF Clear Register. Clears the DETECT_OFF by writing '0' in these registers. If you write '1', the operation is disabled. SW 0-7 has individual clear bit because SW 0-7 supports multiple press. The matrix key's DETECT_OFF clear bit is 1bit for MAT because the matrix key does not support multiple press.
1 : Invalid. 0 :Clear.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF4	C_SW7_OFF	C_SW6_OFF	C_SW5_OFF	C_SW4_OFF	C_SW3_OFF	C_SW2_OFF	C_SW1_OFF	C_SW0_OFF
0xF6	C_MAT_OFF	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF5 : Slider Off recognition clear 】

Name: CLR_DETECT_SLIDER_OFF
Address: 0xF5
Description: C_SLIDER_OFF: Clear Slider off detection flag
SLIDER_OFF (0x17 7) is cleared by writing 0. The next slider is not detected until this flag is cleared.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF4	C_SLIDER_OFF	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xF7-0xF9 : Clear continuous touch】

Name: CLR_DETECT_CONT
Address: 0xF7-0xF9
Description: DETECT_CONT Clear Register. Clears the DETECT_CONT by writing '0' in these registers. If you write '1', the operation is disabled. SW 0-7 has individual clear bit because SW 0-7 supports multiple press. The matrix key's DETECT_CONT clear bit is 1bit for MAT because the matrix key does not support multiple press.
1 : Invalid. 0 :Clear.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xF7	C_SW7_CONT	C_SW6_CONT	C_SW5_CONT	C_SW4_CONT	C_SW3_CONT	C_SW2_CONT	C_SW1_CONT	C_SW0_CONT
0xF9	C_MAT_CONT	-	-	-	-	-	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xFE : Write register for operation check of MPU】

Name: WACT
Address: 0xFE
Description: This register is a write register for operational check of the IC. The value written to this register is copied to the register for operation check (Address is 0x1E). If the write value with the read value is equal then the MPU and I/F are operating normally.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFE	WACT[7]	WACT[6]	WACT[5]	WACT[4]	WACT[3]	WACT[2]	WACT[1]	WACT[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial val.	0	0	0	0	0	0	0	0

【0xFF : AFE control】

Name: CNT
Address: 0xFF
Description: This register is for controlling AFE.

ACT : Scan Enable :

This bit is the scan enable for sensors. 1:Normal Scan Enable. 0:Normal Scan Disable.

CAL : Act Software-calibration :

The calibration is operated by setting '1'.

CFG : Enable Configuration Value :

Writing '1' to this bit renew the values of Sensor Configuration (Address 0xC0-0xCF), Mask Configuration except for 0xDF(Address 0xD0-0xDE), Analog setting Configuration (Address 0xE0-0xEF), FRCRLS and CALOVF. Also It affect the IC's operation.

CALMOD : Select Software-calibration mode :

0: All sensors are the targets for software-calibration. If some sensor has the value more than the threshold for "Off→On", the sensors are changed to OFF, and DETECT_OFF registers are enabled. (default)
1: Sensors with value more than the threshold for "Off→On are not included"

CALOVF : Select Self-calibration mode detected overflow :

When the periodic calibration is active, it selects whether to activate self-calibration or not to activate in the case that the sensor values are over the dynamic range of included ADC.
0: Deactivate self-calibration (default) 1: Activate self-calibration.

FRCRLS : Select Force OFF at continued touch :

When the continued touch is active, select whether to activate force OFF or not in the case that the max value after detect continued touch minus the current sensor value is more than the threshold for "Off→On".
0: Deactivate force OFF(default) 1:Activate force OFF.
The continued touch sensor is changed to OFF, and DETECT_OFF register is enabled.

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0xFF	FRCRLS	CALOVF	-	CALMOD	-	CFG	CAL	ACT
R/W	R/W	R/W	-	R/W	-	R/W	R/W	R/W
Initial val.	0	0	-	0	-	0	0	0

Timing Charts

●Host interface

2-wire serial bus.
Compatible with I2C protocol.
Supports slave mode only.
Slave Address = 0x5C
Supports Standard-mode (data transfer rate is 100 kbit/s) and Fast-mode (data transfer rate is 400 kbit/s).
Supports sequential read.

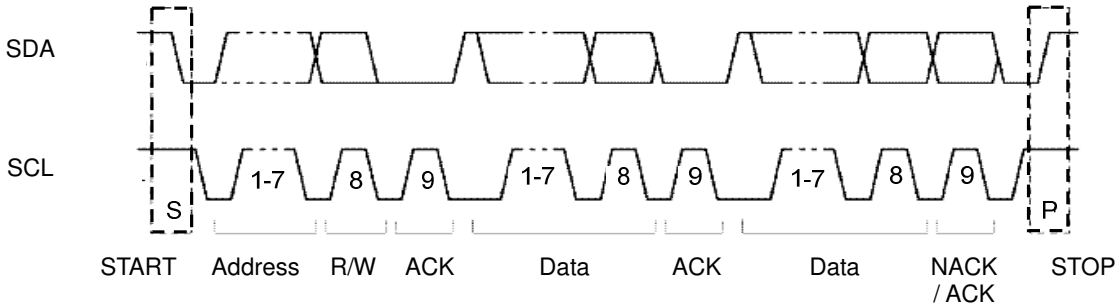


Fig 7. 2-wire serial bus data format

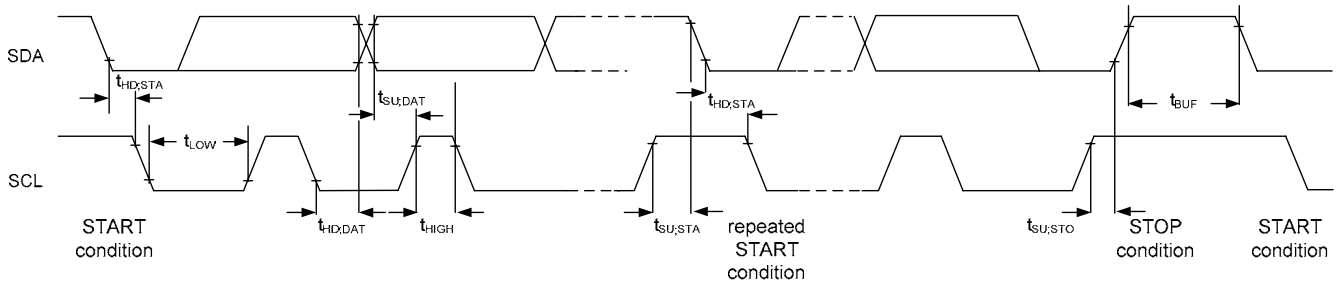
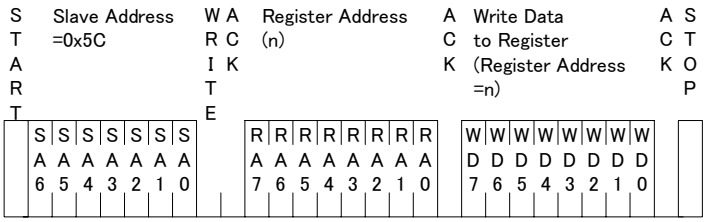


Fig 8. 2-wire serial bus timing chart

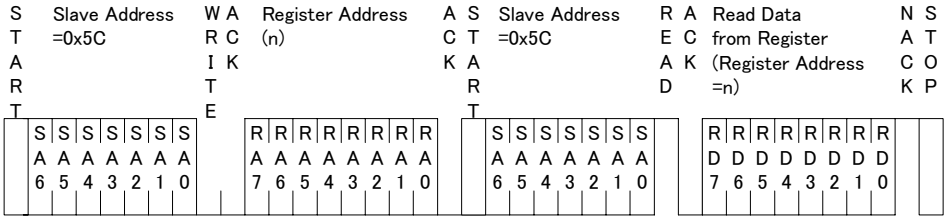
Parameter	Symbol	Standard-mode		Fast-mode		Unit
		MIN	MAX	MIN	MAX	
Hold time (repeated) START condition	f_{SCL}	0	100	0	400	kHz
LOW period of the SCL clock	$t_{HD;STA}$	4.0	-	0.6	-	µsec
HIGH period of the SCL clock	t_{LOW}	4.7	-	1.3	-	µsec
Data hold time	t_{HIGH}	4.0	-	0.6	-	µsec
Data set-up time	$t_{HD;DAT}$	0.1	3.45	0.1	0.9	µsec
Set-up time for a repeated START condition	$t_{SU;DAT}$	0.25	-	0.1	-	µsec
Set-up time for STOP condition	$t_{SU;STA}$	4.7	-	0.6	-	µsec
Bus free time between a STOP and START condition	$t_{SU;STO}$	4.0	-	0.6	-	µsec
Hold time (repeated) START condition	t_{BUF}	4.7	-	1.3	-	µsec

●Byte Write



SA : Slave Address
RA : Register Address
RD : Read Data
WD : Write Data

●Random Read



●Sequential Read

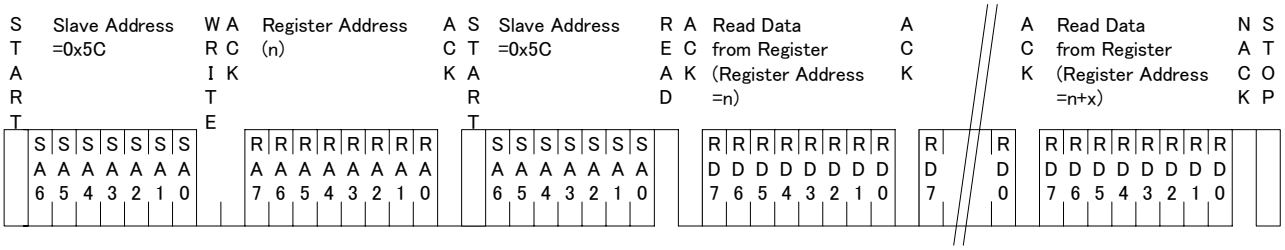


Figure 9. 2-wire serial bus protocol

Scan rate

After scanning each sensor in time series, MPU converts the detected results to switch operations. One scan rate is about 6msec at typical.

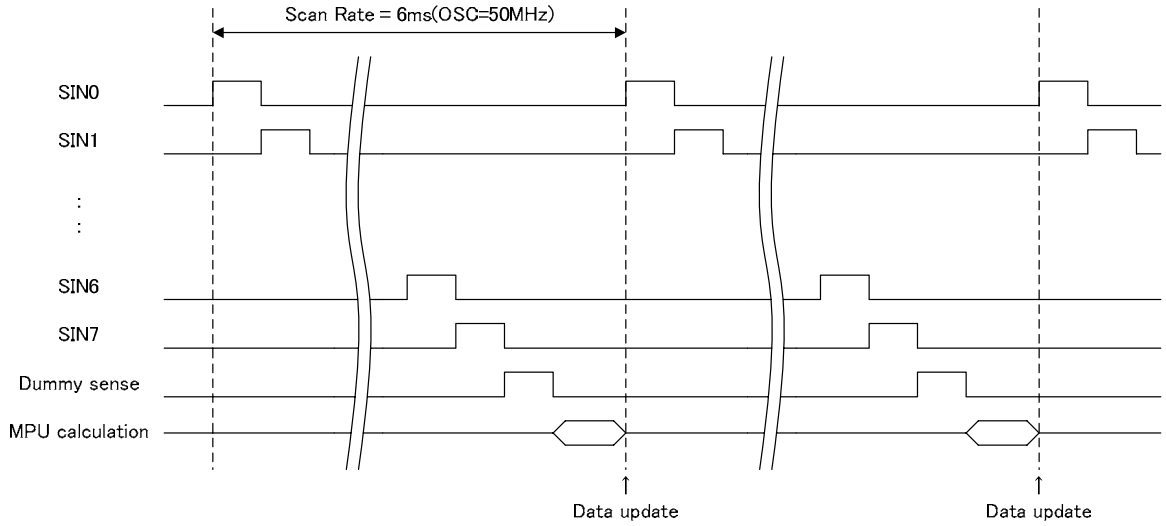


Figure 10. Timing chart of scan rate

Power on sequence

The power supply pin is only VDD. Because AVDD and DVDD are generated by a built-in LDO, there is no need for an external supply. The internal reference voltage is started up by the VDD supply, and DVDD starts up continuously. Power-on reset is released when DVDD reaches the required voltage.

Recommended value of external capacitors

C_1	0.1μF	VDD decoupling capacitor
C_2	1.0μF	DVDD decoupling capacitor
C_3	2.2μF	AVDD decoupling capacitor

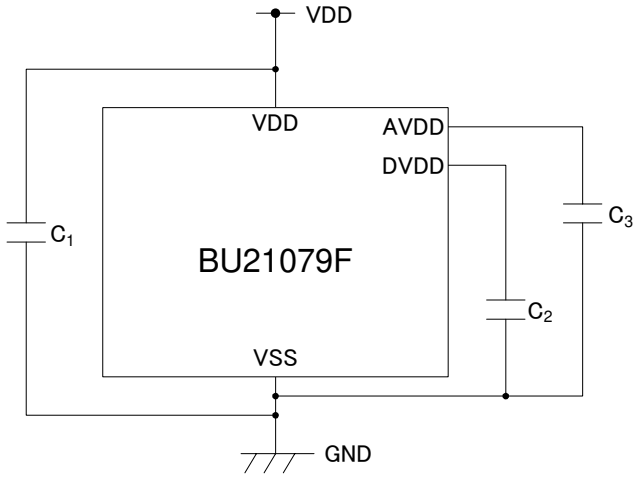


Figure 11. Arrangement of external decoupling capacitors

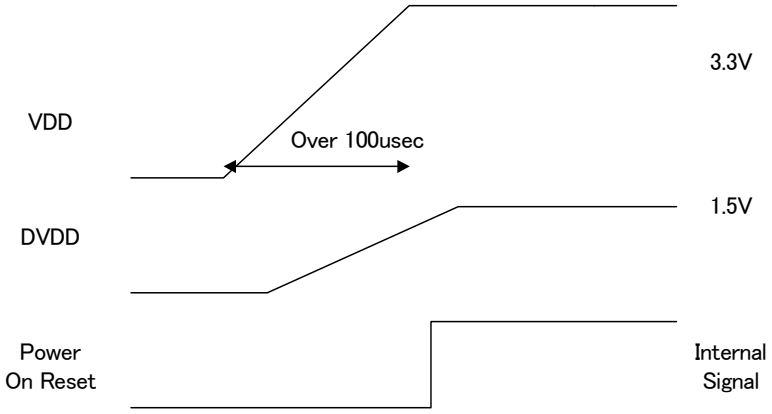


Figure 12. Power on sequence

When power-on-reset is released, MPU starts initial sequence. INT port informs the host that the initialization has been completed. After verifying if the initialization is completed, the host will need to send the command to the IC. In the case that WDTR is released as well, MPU starts initial sequence. If WDTR is released, all registers have been initialized so the host will need to resend the command to the IC.

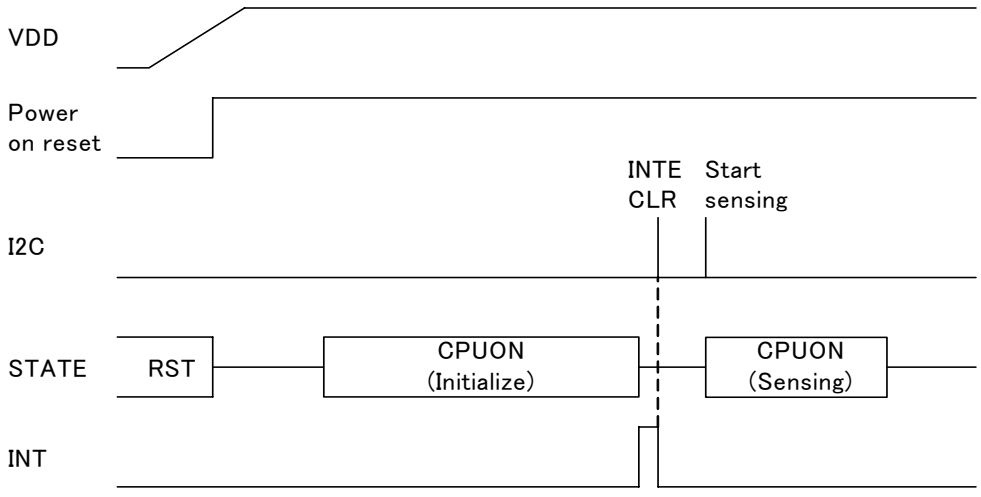


Figure 13. Timing chart of initialization

Operational mode

This IC has three operational modes, [Stop mode], [Intermittent mode], and [Normal mode].

【Stop mode】

It is the state where detection is disabled.
Detection is stopped by setting '0' to ACT of the sensor motion control register CNT (address 0xFF).
A detection process is stopped and consumption current decreases by performing the power down of AFE.

【Normal mode】

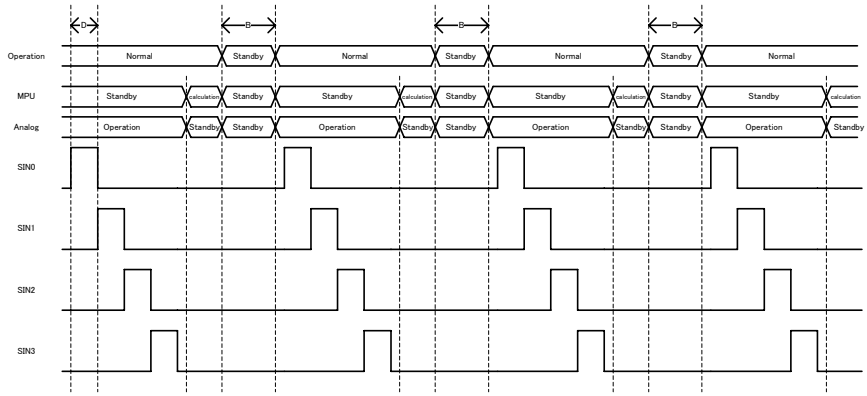
In normal mode, detection is continuous.
Sensing is started by setting '1' to ACT of the sensor motion control register CNT (address 0xFF).
Starting detection and soft calibration is operated simultaneously.
Sensing in normal mode is defined as normal sensing.

【Intermittent mode】

Detection is thinned out. If the touch detection beyond a definite period of time is not recognized, it will shift to intermittent operation. In this state, since the frequency of sensing is low, current consumption can be reduced.
Sensing in intermittent operation is defined as check sensing.

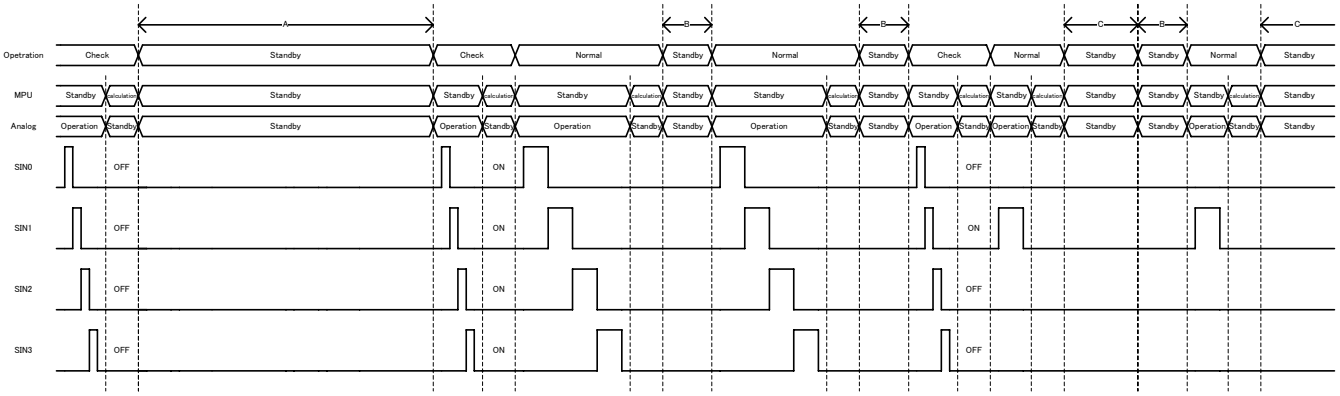
【 Normal operation 】

①An effective sensor is sensing by the SENS setting.



【 Intermittent operation 】

①All sensors are checked sensing by each CHK setting of the register.
②The sensor of ON judgment is done normal sensing by the check sensing result, and it uses it for the touch judgment that outputs only the result.
③It stands by until time equal with all channel sensing when sensors of ON judgment are less than 8 channels in the check sensing result.
④It stands by at time that even the next check timing was set when there is no sensor of ON judgment in the check sensing result.
⑤The frequency of the sensor while check sensing is operated is specified by the register. Minimum is 1 time. (A below figure is shown twice.)



A: Check waiting time. It is possible to set it at CHK_WAIT_TIME. (About 4 to 1024ms)
B: Sense waiting time. It is possible to set it at SENS_WAIT_TIME. (About 0 to 1020ms)
C: Sense adjustment time. It changes according to the number of sensors in which not sensing. (About 4ms unit)
D: Sensing time of each sensor

Figure14. Operation sequence of normal operation and intermittent operation

Initialized operation

This IC is initialized and all registers are cleared by Power-on reset, WDT time-out reset, and Software reset command. When initialization is complete, the register INI is '1' and I/O port INT is “H”.
After the IC is initialized, write the configuration values to registers. After setting configuration values, the next action is sensor calibration. Set ‘1’ to the registers ACT, CFG and CAL on Address 0xFF, and calibration sequence is performed.

The initialization process after the ROM hardware reset

- Power activation
- WDT timeout
- Software reset

Also in the case of hardware reset by any, all the register is cleared.
Since reset to MPU is also operated, MPU follows the firmware in Program ROM and initializes IC.

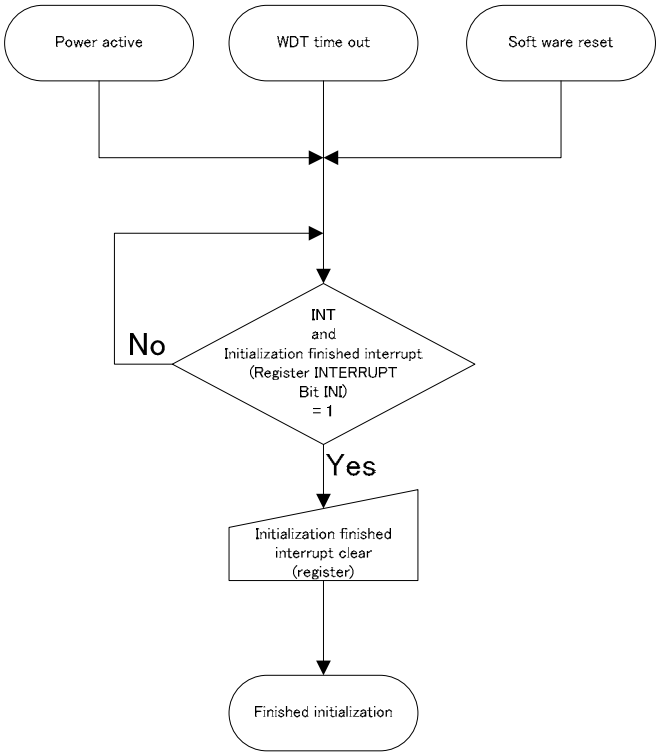


Figure15. The initialization process after hardware reset