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High-performance Clock Generator Series

DVD-video Reference Clock Generators for A/V Equipments

BU2280FV, BU2360FV, BU2362FV

No.12005EBT04

●Description

These clock generators are an IC generating three types of clocks - VIDEO, AUIDIO and SYSTEM clocks – necessary for DVD player systems, with a single chip through making use of the PLL technology. Particularly, the AUDIO clock is a DVD-Video reference and yet achieves high C/N characteristics to provide a low level of distortion factor.

●Features

1) Connecting a crystal oscillator generates multiple clock signals with a built-in PLL.
2) AUDIO clock of high C/N characteristics providing a low level of distortion factor
3) The AUDIO clock provides switching selection outputs.
4) Single power supply of 3.3 V

●Applications

DVD players

●Lineup

Part name			BU2280FV	BU2360FV	BU2362FV
Power source voltage [V]			3.0 ~ 3.6	2.7 ~ 3.6	2.7 ~ 3.6
Reference frequency [MHz]			27.0000	27.0000	27.0000
Output frequency [MHz]	DVD VIDEO	2	-	-	-
		1	27.0000	27.0000	27.0000
		1/2	-	-	-
	DVD AUDIO, CD (Switching outputs)	768fs	36.8640 /33.8688	-	-
		512fs	24.5760 /22.5792	24.5760 /22.5792	24.5760 /22.5792
		384fs	18.4320 /16.9344	-	-
		256fs	-	-	-
		other	-	-	36.8640 /16.9344
	SYSTEM	768 (48k type)	-	-	36.8640
		768 (44.1k type)	33.8688	33.8688	33.8688
		384 (44.1k type)	-	-	16.9344
Jitter 1σ [psec]			70	70	70
Long-term-Jitter p-p [nsec]			8.0	2.5	5.0
Package			SSOP-B24	SSOP-B16	SSOP-B16

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	BU2280FV	BU2360FV	BU2362FV	Unit
Supply voltage	VDD	-0.5 ~ +7.0	-0.5 ~ +7.0	-0.5 ~ +7.0	V
Input voltage	VIN	-0.5~VDD+0.5	-0.5~VDD+0.5	-0.5~VDD+0.5	V
Storage temperature range	T_{stg}	-30 ~ +125	-30 ~ +125	-30 ~ +125	℃
Power dissipation	PD	630 *1	450 *2	450 *2	mW

*1 In the case of exceeding Ta = 25℃, 6.3mW to be reduced per 1℃
*2 In the case of exceeding Ta = 25℃, 4.5mW to be reduced per 1℃
*Operating is not guaranteed.
*The radiation-resistance design is not carried out.
*Power dissipation is measured when the IC is mounted to the printed circuit board.

●Recommended Operating Range

Parameter	Symbol	BU2280FV	BU2360FV	BU2362FV	Unit
Parameter	VDD	3.0 ~ 3.6	2.7 ~ 3.6	2.7 ~ 3.6	V
Supply voltage	VIH	0.8VDD~VDD	0.8VDD~VDD	0.8VDD~VDD	V
Input “H” Voltage	VIL	0.0 ~ 0.2VDD	0.0 ~ 0.2VDD	0.0 ~ 0.2VDD	V
Input “L” Voltage	T_{opr}	-5 ~ +70	-25 ~ +85	-25 ~ +85	℃
Operating temperature	CL	15	15	15	pF
Output load	CL_27M1	-	40 (CLK27M1)	-	pF
27M output load 1	CL_27M2	-	25 (CLK27M2)	-	pF

●Electrical characteristics

◎BU2280FV(VDD=3.3V, Ta=25℃, Crystal frequency 27.0000MHz, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output L voltage	VOL	-	-	0.4	V	IOL=4.0mA
Output H voltage	VOH	2.4	-	-	V	IOH=-4.0mA
Consumption current	IDD	-	30	50	mA	At no load
CLK768FS	CLK768-44	-	33.8688	-	MHz	At FSEL=L, XTAL×3136 / 625 / 4
	CLK768-48	-	36.8640	-	MHz	At FSEL=H, XTAL×2048 / 375 / 4
CLK512FS	CLK512-44	-	22.5792	-	MHz	At FSEL=L, XTAL×3136 / 625 / 6
	CLK512-48	-	24.5760	-	MHz	At FSEL=H, XTAL×2048 / 375 / 6
CLK384FS	CLK384-44	-	16.9344	-	MHz	At FSEL=L, XTAL×3136 / 625 / 8
	CLK384-48	-	18.4320	-	MHz	At FSEL=H, XTAL×2048 / 375 / 8
CLK33M	CLK33M	-	33.8688	-	MHz	XTAL×147 / 40 / 4
CLK16M	CLK16M	-	16.9344	-	MHz	XTAL×147 / 40 / 8
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1σ	P-J 1σ	-	70	-	psec	*1
Period-Jitter MIN-MAX	P-J MIN-MAX	-	420	-	psec	*2
Rise Time	Tr	-	2.5	-	nsec	Period of transition time required for the output reach 80% from 20% of VDD.
Fall Time	Tf	-	2.5	-	nsec	Period of transition time required for the output reach 20% from 80% of VDD.
Output Lock-Time	Tlock	-	-	1	msec	*3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to XTALIN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

◎BU2360FV(VDD=3.3V, Ta=25℃, Crystal frequency 27.0000MHz, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output L voltage	VOL	-	-	0.4	V	IOL=4.0mA
Output H voltage	VOH	2.4	-	-	V	IOH=-4.0mA
FSEL input VthL	$V_{th}L$	0.2VDD	-	-	V	*4
FSEL input VthH	$V_{th}H$	-	-	0.8VDD	V	*4
Hysteresis range	V_{hys}	0.2	-	-	V	Vhys = VthH - VthL *4
Action circuit current	IDD	-	27.0	40.5	mA	At no load
CLK27M	CLK27M	-	27.0000	-	MHz	XTAL direct out
CLK33M	CLK33M	-	33.8688	-	MHz	XTAL×3136 / 625 / 4
CLK512FS	CLK512_48	-	24.5760	-	MHz	At FSEL=H, XTAL×2048 / 375 / 6
	CLK512_44	-	22.5792	-	MHz	At FSEL=L, XTAL×3136 / 625 / 6
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1σ	P-J 1σ	-	70	-	psec	*1
Period-Jitter MIN-MAX	P-J MIN-MAX	-	420	-	psec	*2
Rise Time	Tr	-	2.5	-	nsec	Period of transition time required for the output reach 80% from 20% of VDD.
Fall Time	Tf	-	2.5	-	nsec	Period of transition time required for the output reach 20% from 80% of VDD.
Output Lock-Time	Tlock	-	-	1	msec	*3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to XTALIN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

◎BU2362FV(VDD=3.3V, Ta=25℃, Crystal frequency 27.0000MHz, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Output L voltage	VOH	2.4	-	-	V	IOH=-4.0mA
Output H voltage	VOL	-	-	0.4	V	IOL=4.0mA
Action circuit current	IDD	-	35	45	mA	At no load
CLK512FS	CLK512-44	-	22.5792	-	MHz	At FSEL1=OPEN XTAL*3136/625/6
	CLK512-48	-	24.5760	-	MHz	At FSEL1=L XTAL*2048/375/6
CLKA	CLKA-A	-	16.9344	-	MHz	At FSEL1=OPEN XTAL*3136/625/8
	CLKA-B	-	36.8640	-	MHz	At FSEL1=L XTAL*2048/375/8
CLK36M	CLK36M	-	36.8640	-	MHz	XTAL*2048/375/4
CLK33M	CLK33M	-	33.8688	-	MHz	XTAL*3136/625/4
CLK16M	CLK16M	-	16.9344	-	MHz	XTAL*3136/625/8
CLK27M	CLK27M	-	27.0000	-	MHz	XTAL direct out
Duty	Duty	45	50	55	%	Measured at a voltage of 1/2 of VDD
Period-Jitter 1σ	P-J 1σ	-	70	-	psec	*1
Period-Jitter MIN-MAX	P-J MIN-MAX	-	420	-	psec	*2
Rise Time	Tr	-	2.5	-	nsec	Period of transition time required for the output reach 80% from 20% of VDD.
Fall Time	Tf	-	2.5	-	nsec	Period of transition time required for the output reach 20% from 80% of VDD.
Output Lock-Time	Tlock	-	-	1	msec	*3

Note) The output frequency is determined by the arithmetic (frequency division) expression of a frequency input to XTALIN.
If the input frequency is set to 27.0000MHz, the output frequency will be as listed above.

Common to BU2280FV, BU2360FV and BU2362FV:

*1 Period-Jitter 1σ

This parameter represents standard deviation (=1 σ) on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

*2 Period-Jitter MIN-MAX

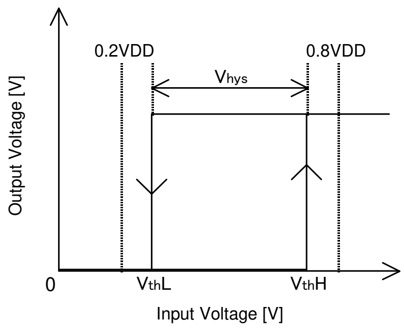
This parameter represents a maximum distribution width on cycle distribution data at the time when the output clock cycles are sampled 1000 times consecutively with the TDS7104 Digital Phosphor Oscilloscope of Tektronix Japan, Ltd.

*3 Output Lock-Time

The Lock-Time represents elapsed time after power supply turns ON to reach a 3.0V voltage, after the system is switched from Power-Down state to normal operation state, or after the output frequency is switched, until it is stabilized at a specified frequency, respectively.

BU2360FV

∗4 This parameter represents lower and upper limit voltages at the Schmitt trigger input PIN having hysteresis characteristics shown in figure below. The width requested by these differences is assumed to be a hysteresis width.



●Reference data (BU2280FV basic data)

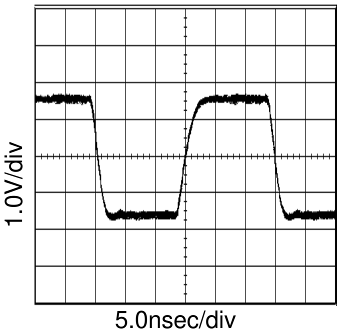


Fig.1 33.9MHz output waveform
VDD=3.3V, at CL=15pF

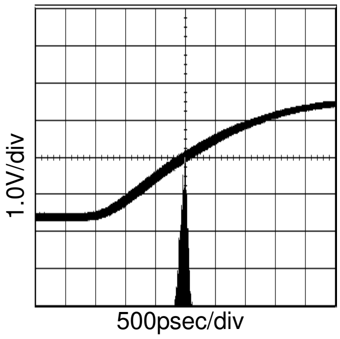


Fig.2 33.9MHz Period-Jitter
VDD=3.3V, at CL=15pF

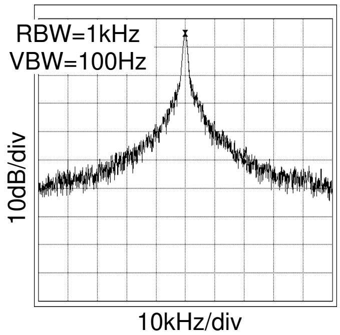


Fig.3 33.9MHz Spectrum
VDD=3.3V, at CL=15pF

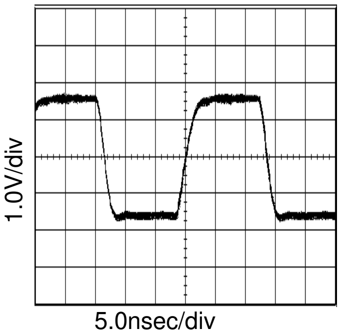


Fig.4 36.9MHz output waveform
VDD=3.3V, at CL=15pF

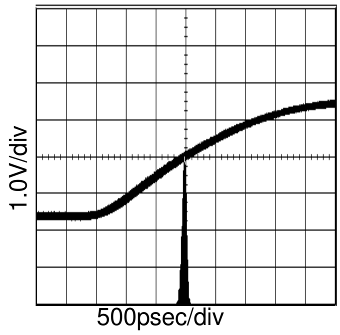


Fig.5 36.9MHz Period-Jitter
VDD=3.3V, at CL=15pF

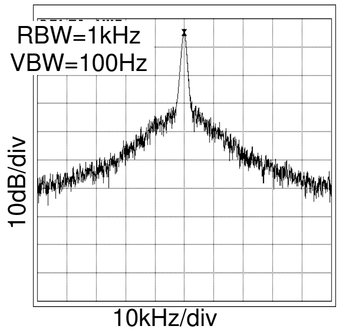


Fig.6 36.9MHz Spectrum
VDD=3.3V, at CL=15pF

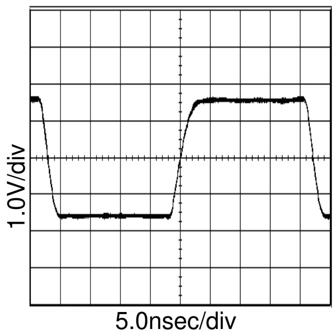


Fig.7 22.6MHz output waveform
VDD=3.3V, at CL=15pF

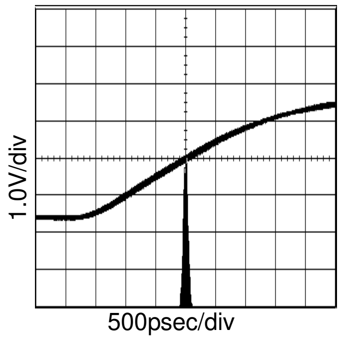


Fig.8 22.6MHz Period-Jitter
VDD=3.3V, at CL=15pF

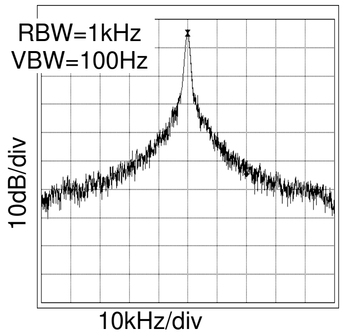


Fig.9 22.6MHz Spectrum
VDD=3.3V, at CL=15pF

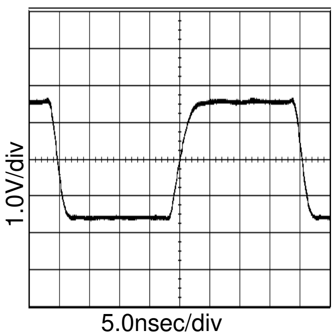


Fig.10 24.6MHz output waveform
VDD=3.3V, at CL=15pF

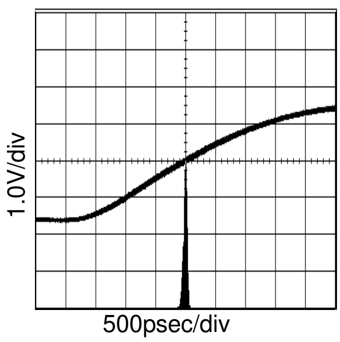


Fig.11 24.6MHz Period-Jitter
VDD=3.3V, at CL=15pF

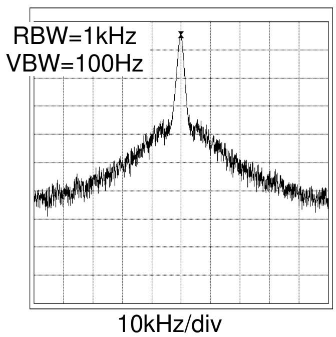


Fig.12 24.6MHz Spectrum
VDD=3.3V, at CL=15pF

●Reference data (BU2280FV basic data)

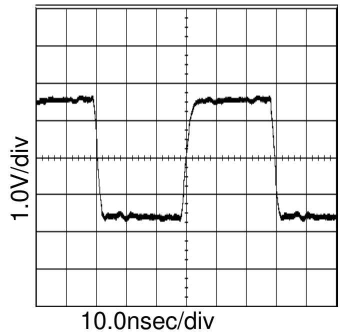


Fig.13 16.9MHz output waveform
VDD=3.3V, at CL=15pF

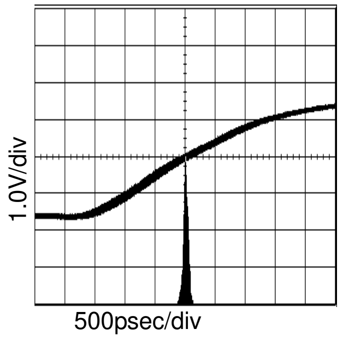


Fig.14 16.9MHz Period-Jitter
VDD=3.3V, at CL=15pF

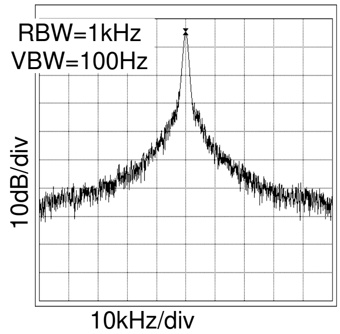


Fig.15 16.9MHz Spectrum
VDD=3.3V, at CL=15pF

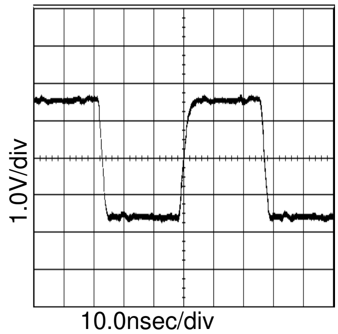


Fig.16 18.4MHz output waveform
VDD=3.3V, at CL=15pF

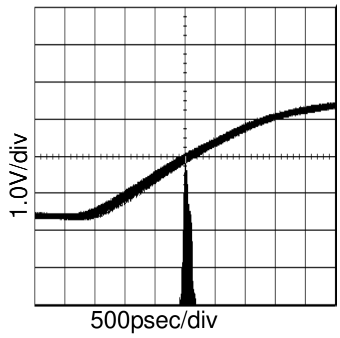


Fig.17 18.4MHz Period-Jitter
VDD=3.3V, at CL=15pF

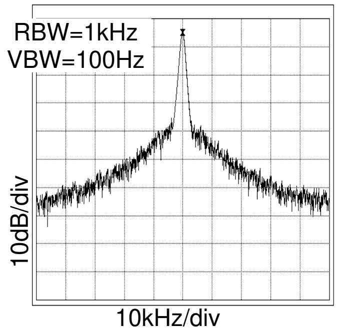


Fig.18 18.4MHz Spectrum
VDD=3.3V, at CL=15pF

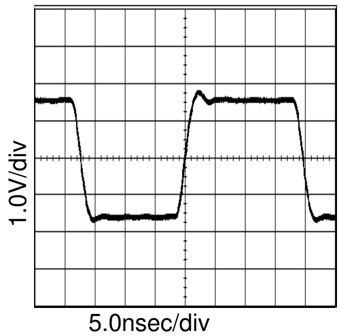


Fig.19 27MHz output waveform
VDD=3.3V, at CL=15pF

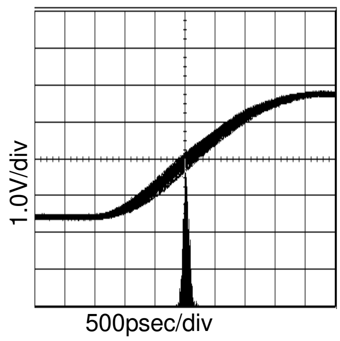


Fig.20 27MHz Period-Jitter
VDD=3.3V, at CL=15pF

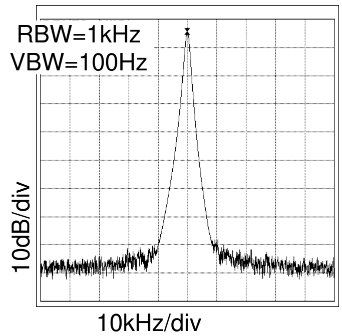


Fig.21 27MHz Spectrum
VDD=3.3V, at CL=15pF

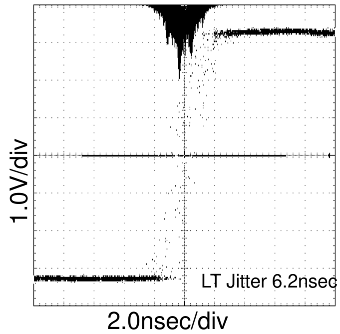


Fig.22 24.6MHz LT Jitter
VDD=3.3V, at CL=15pF

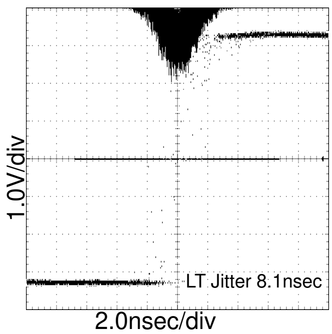


Fig.23 22.6MHz LT Jitter
VDD=3.3V, at CL=15pF

●Reference data (BU2280FV Temperature and Supply voltage variations data)

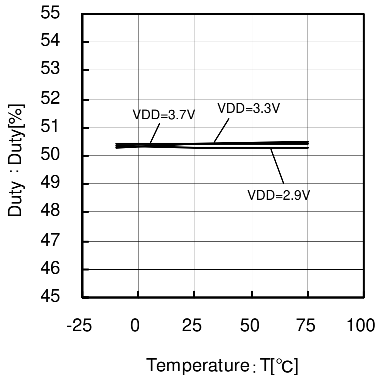


Fig.24 33.9MHz
Temperature-Duty

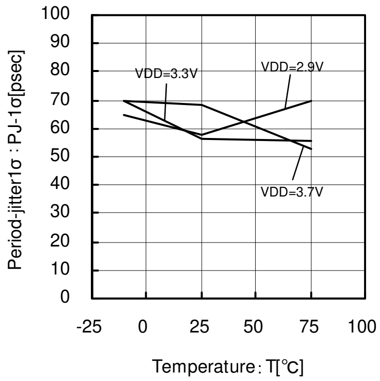


Fig.25 33.9MHz
Temperature-Period-Jitter 1σ

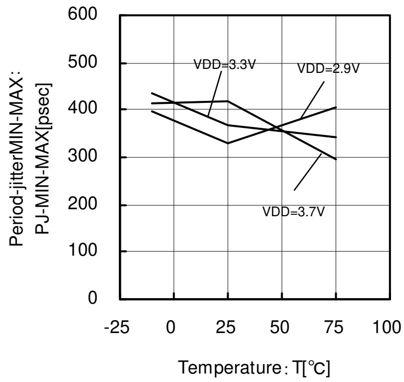


Fig.26 33.9MHz
Temperature-Period-Jitter MIN-MAX

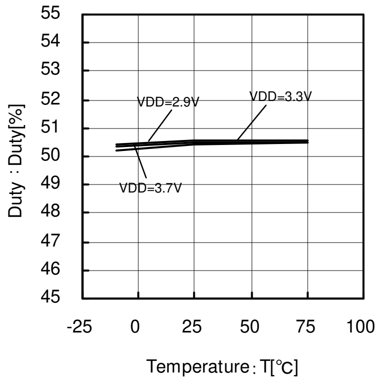


Fig.27 36.9MHz
Temperature-Duty

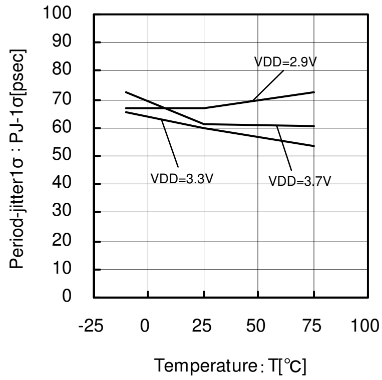


Fig.28 36.9MHz
Temperature-Period-Jitter 1σ

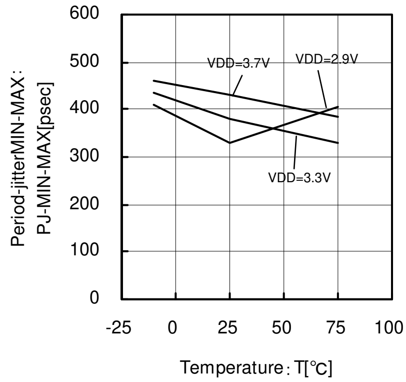


Fig.29 36.9MHz
Temperature r-Period-Jitter MIN-MAX

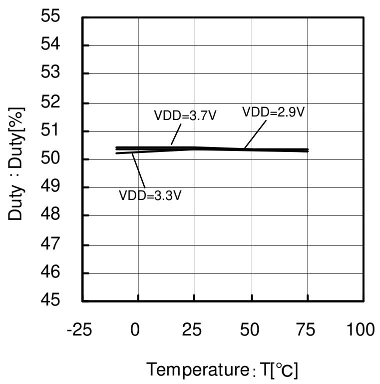


Fig.30 22.6MHz
Temperature-Duty

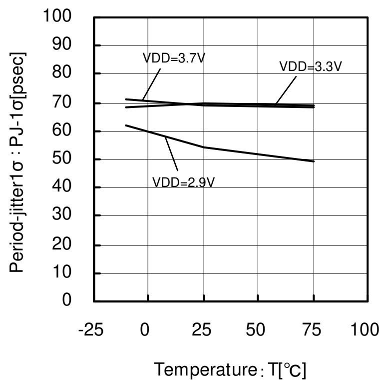


Fig.31 22.6MHz
Temperature-Period-Jitter 1σ

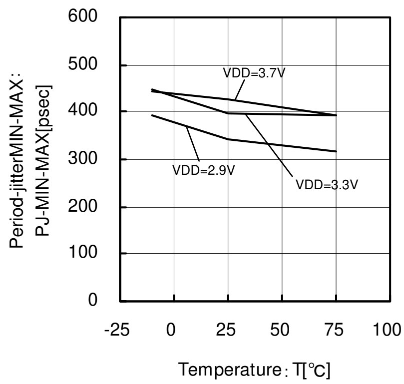


Fig.32 22.6MHz
Temperature-Period-Jitter MIN-MAX

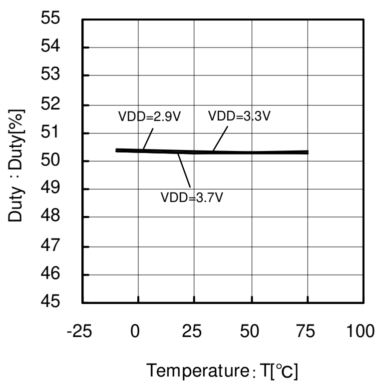


Fig.33 24.6MHz
Temperature-Duty

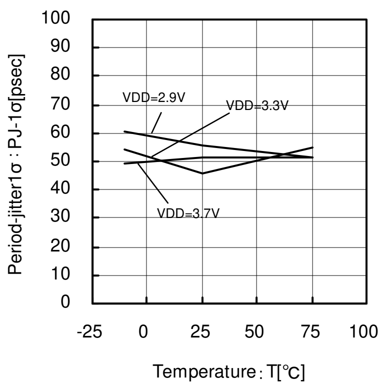


Fig.34 24.6MHz
Temperature-Period-Jitter 1σ

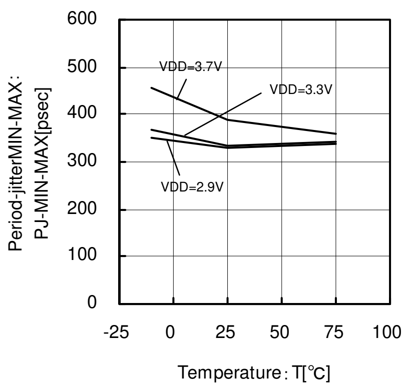


Fig.35 24.6MHz
Temperature-Period-Jitter MIN-MAX

●Reference data (BU2280FV Temperature and Supply voltage variations data)

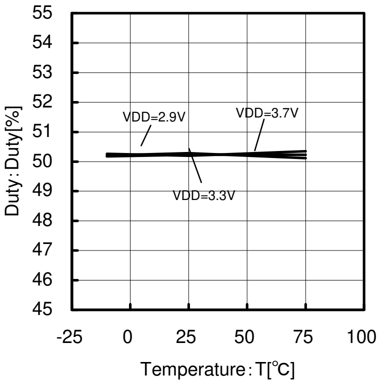


Fig.36 16.9MHz
Temperature-Duty

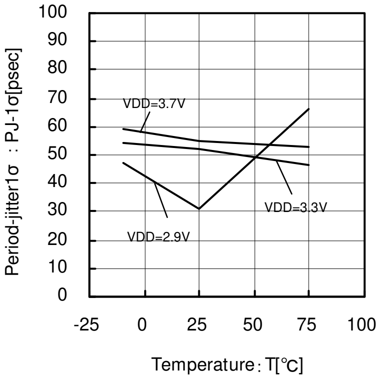


Fig.37 16.9MHz
Temperature-Period-Jitter 1σ

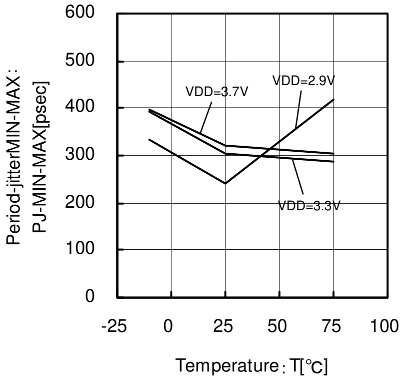


Fig.38 16.9MHz
Temperature-Period-Jitter MIN-MAX

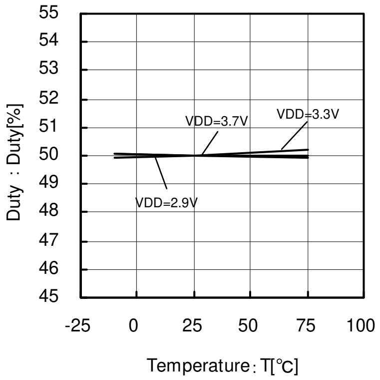


Fig.39 18.4MHz
Temperature-Duty

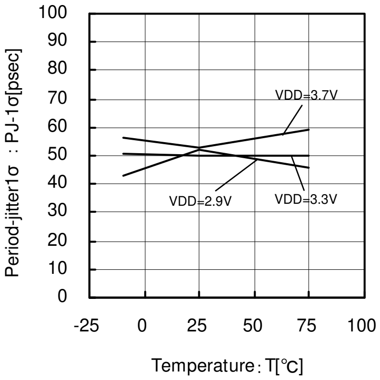


Fig.40 18.4MHz
Temperature-Period-Jitter 1σ

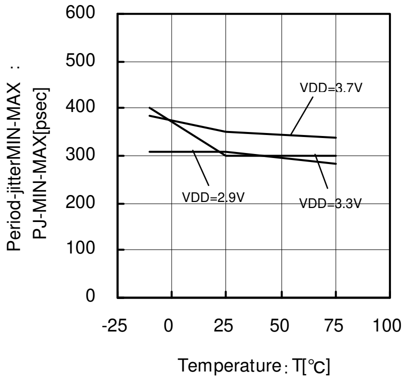


Fig.41 18.4MHz
Temperature-Period-Jitter MIN-MAX

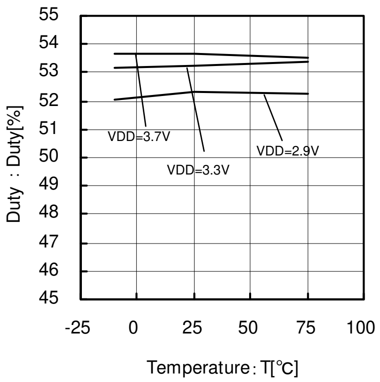


Fig.42 27MHz
Temperature-Duty

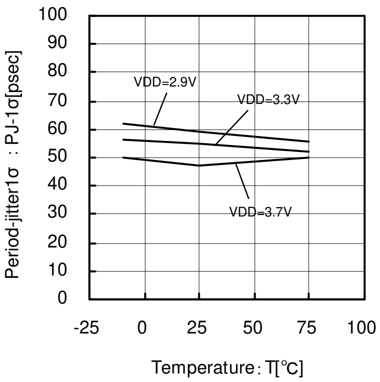


Fig.43 27MHz
Temperature-Period-Jitter 1σ

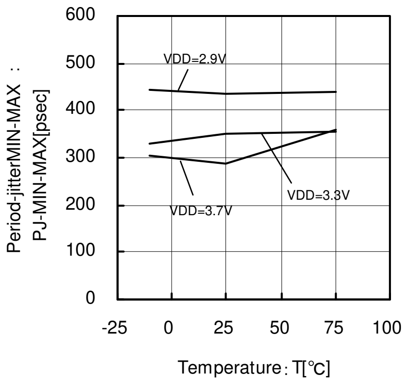


Fig.44 27MHz
Temperature-Period-Jitter MIN-MAX

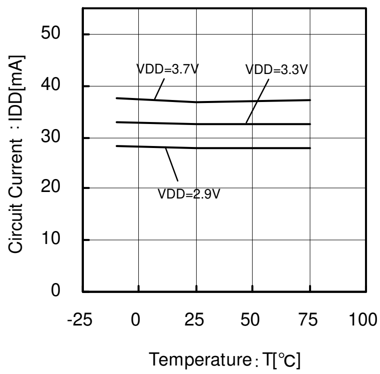


Fig.45 Action circuit current
(with maximum output load)
Temperature-Consumption current

●Reference data (BU2360FV basic data)

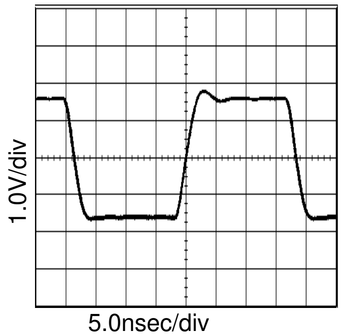


Fig.46 27MHz output waveform
VDD=3.3V, at CL=40pF

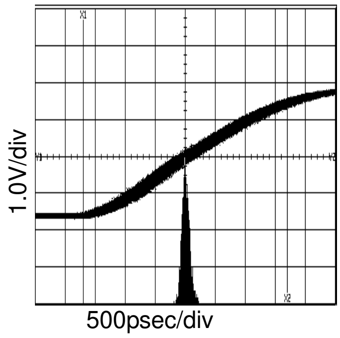


Fig.47 27MHz Period-Jitter
VDD=3.3V, at CL=40pF

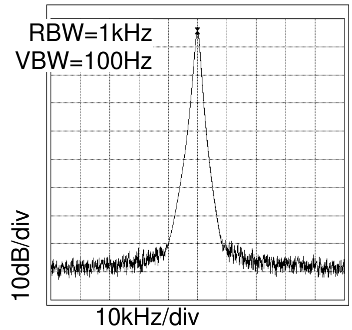


Fig.48 27MHz Spectrum
VDD=3.3V, at CL=40pF

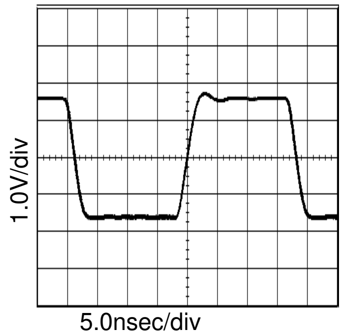


Fig.49 27MHz output waveform
VDD=3.3V, at CL=25pF

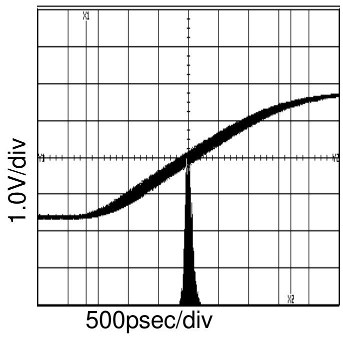


Fig.50 27MHz Period-Jitter
VDD=3.3V, at CL=25pF

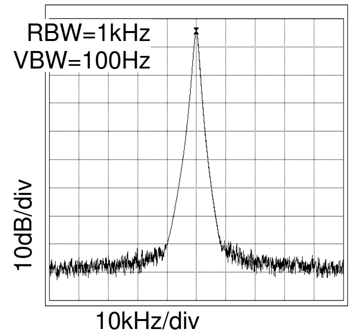


Fig.51 27MHz Spectrum
VDD=3.3V, at CL=25pF

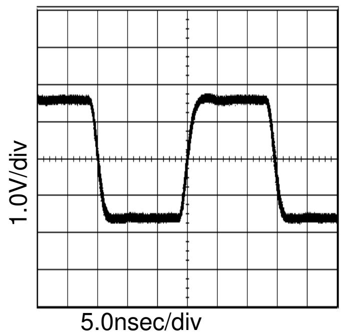


Fig.52 33.9MHz output waveform
VDD=3.3V, at CL=15pF

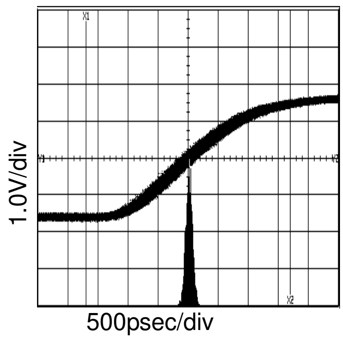


Fig.53 33.9MHz Period-Jitter
VDD=3.3V, at CL=15pF

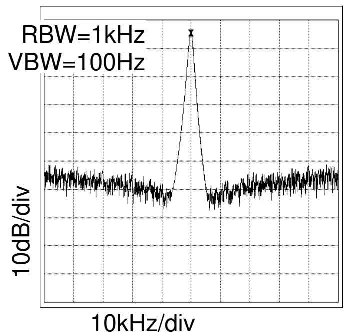


Fig.54 33.9MHz Spectrum
VDD=3.3V, at CL=15pF

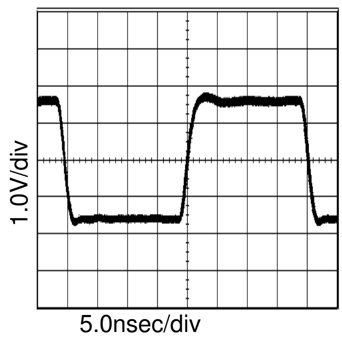


Fig.55 24.6MHz output waveform
VDD=3.3V, at CL=15pF

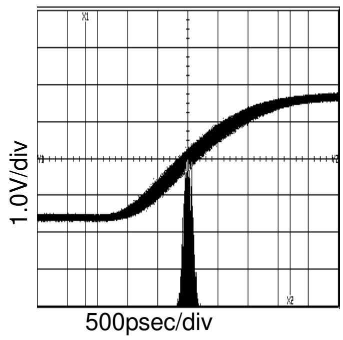


Fig.56 24.6MHz Period-Jitter
VDD=3.3V, at CL=15pF

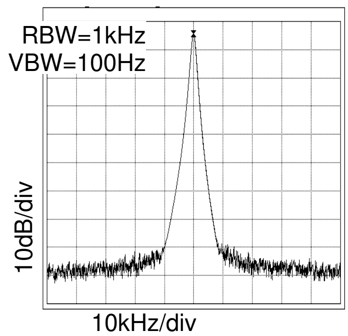


Fig.57 24.6MHz Spectrum
VDD=3.3V, at CL=15pF

● Reference data (BU2360FV basic data)

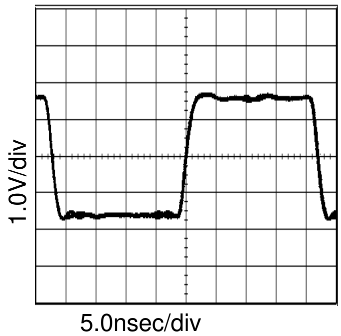


Fig.58 22.6MHz output waveform
VDD=3.3V, at CL=15pF

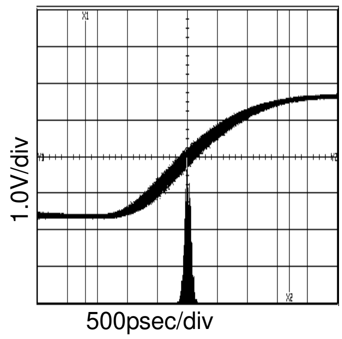


Fig.59 22.6MHz Period-Jitter
VDD=3.3V, at CL=15pF

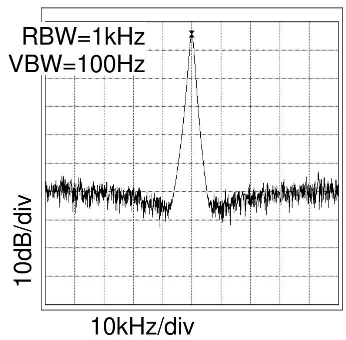


Fig.60 22.6MHz Spectrum
VDD=3.3V, at CL=15pF

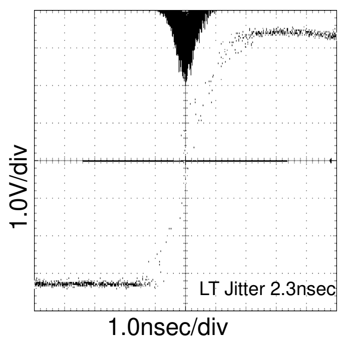


Fig61. 24.6MHz LT Jitter
VDD=3.3V, at CL=15pF

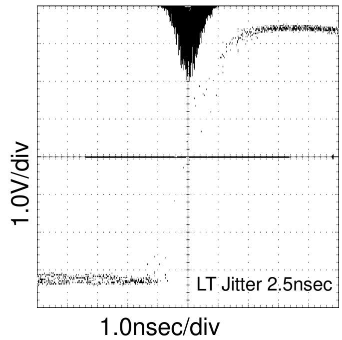


Fig62. 22.6MHz LT Jitter
VDD=3.3V, at CL=15pF

● Reference data (BU2360FV Temperature and Supply voltage variations data)

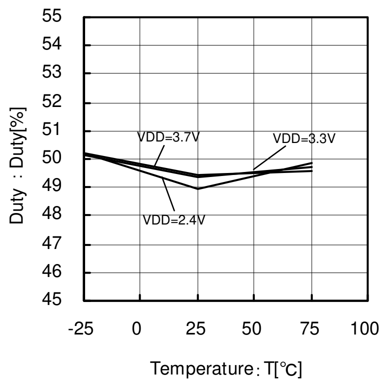


Fig.63 27MHz (40pF)
Temperature-Duty

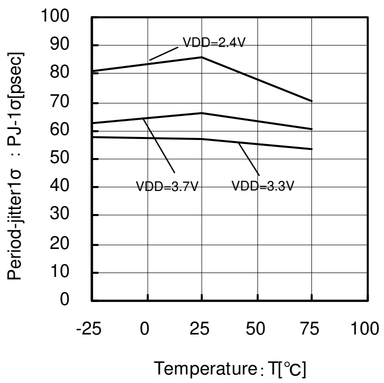


Fig.64 27MHz (40pF)
Temperature-Period-Jitter 1σ

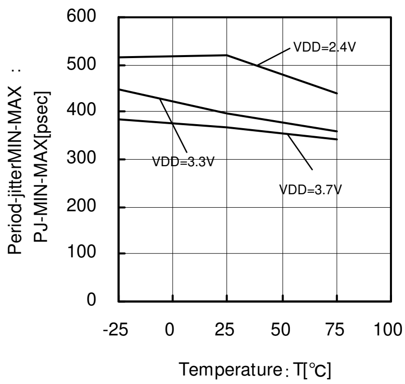


Fig.65 27MHz (40pF)
Temperature-Period-Jitter MIN-MAX

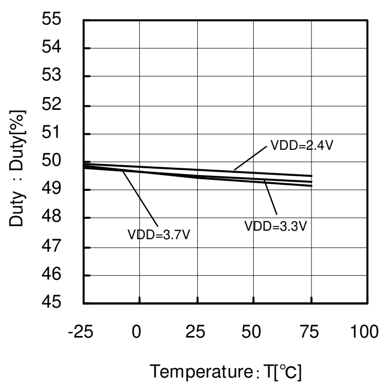


Fig.66 27MHz (25pF)
Temperature-Duty

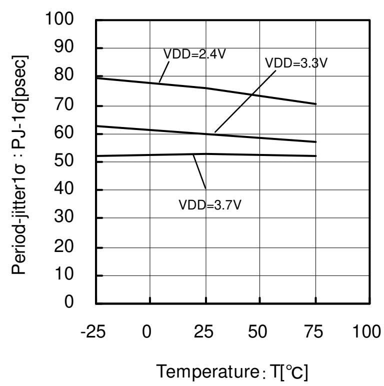


Fig.67 27MHz (25pF)
Temperature-Period-Jitter 1σ

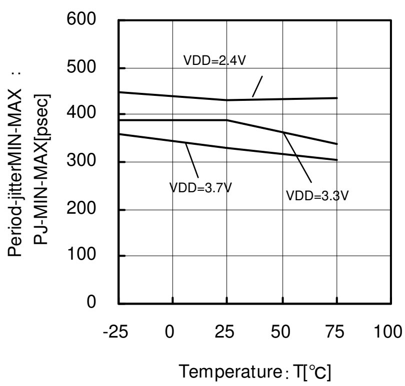


Fig.68 27MHz (25pF)
Temperature-Period-Jitter MIN-MAX

●Reference data (BU2360FV Temperature and Supply voltage variations data)

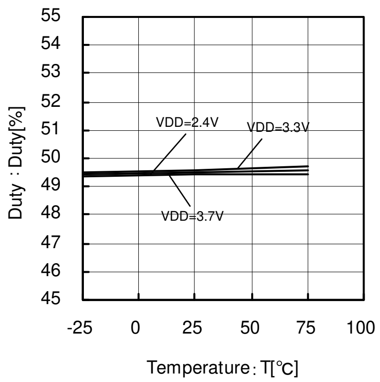


Fig.69 33.9MHz
Temperature-Duty

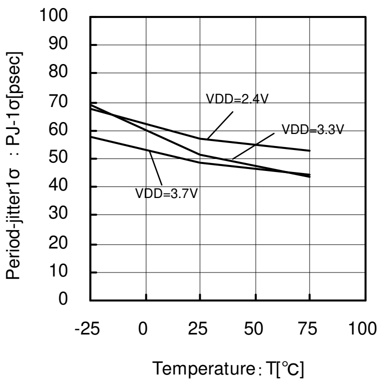


Fig.70 33.9MHz
Temperature-Period-Jitter 1σ

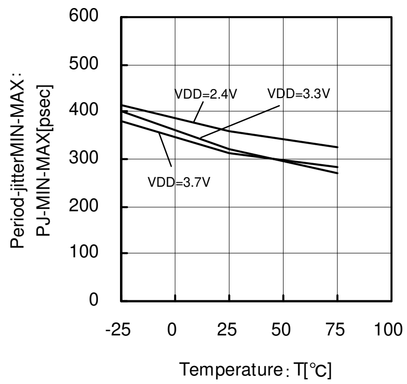


Fig.71 33.9MHz
Temperature-Period-Jitter MIN-MAX

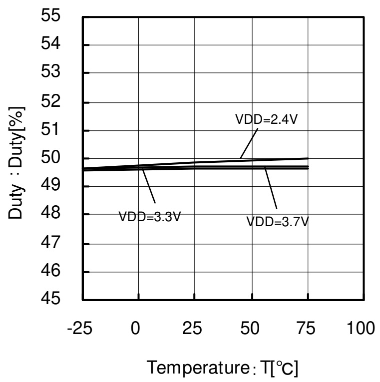


Fig.72 24.6MHz
Temperature-Duty

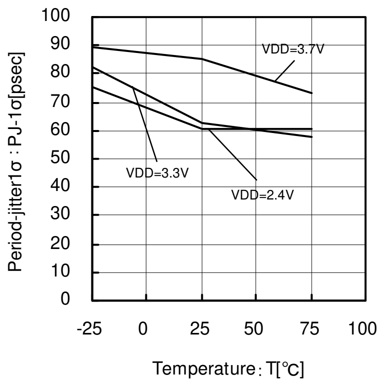


Fig.73 24.6MHz
Temperature-Period-Jitter 1σ

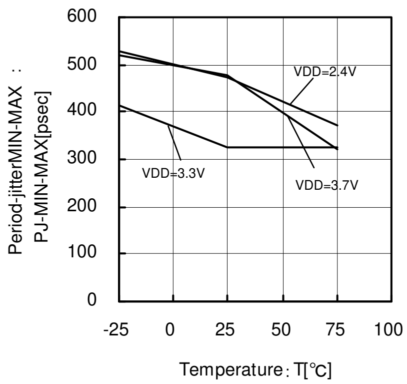


Fig.74 24.6MHz
Temperature-Period-Jitter MIN-MAX

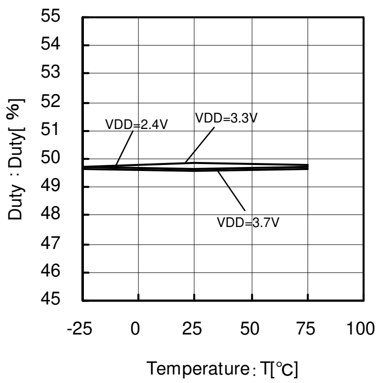


Fig.75 22.6MHz
Temperature-Duty

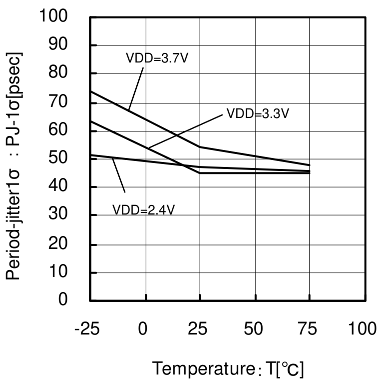


Fig.76 22.6MHz
Temperature-Period-Jitter 1σ

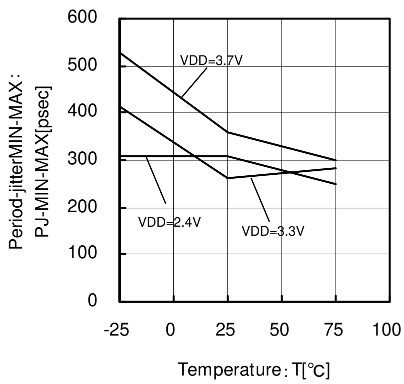


Fig.77 22.6MHz
Temperature-Period-Jitter MIN-MAX

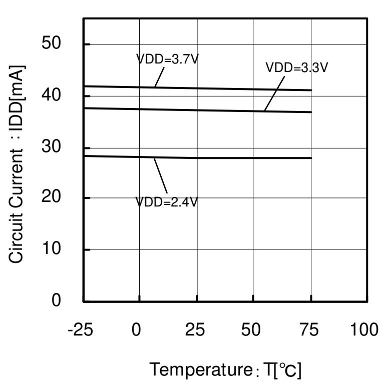


Fig.78 Action circuit current
(with maximum output load)
Temperature-Consumption current

●Reference data(BU2362FV basic data)

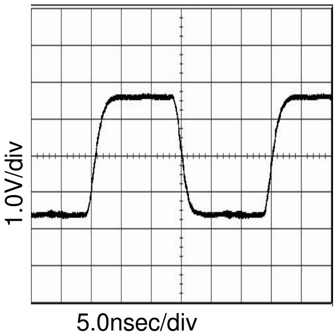


Fig.79 33.9MHz output waveform
VDD=3.3V, at CL=15pF

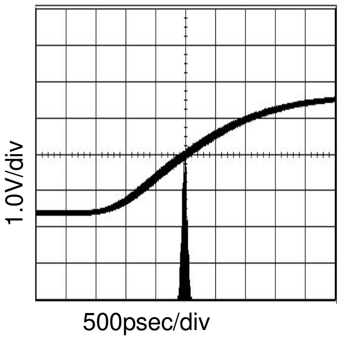


Fig.80 33.9MHz Period-Jitter
VDD=3.3V, at CL=15pF

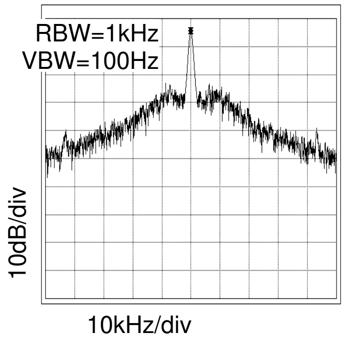


Fig.81 33.9MHz Spectrum
VDD=3.3V, at CL=15pF

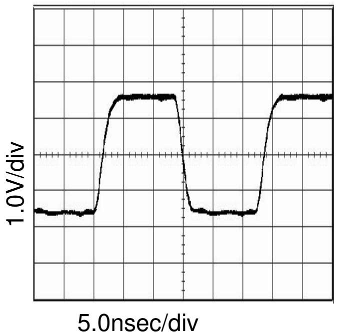


Fig.82 36.9MHz output waveform
VDD=3.3V, at CL=15pF

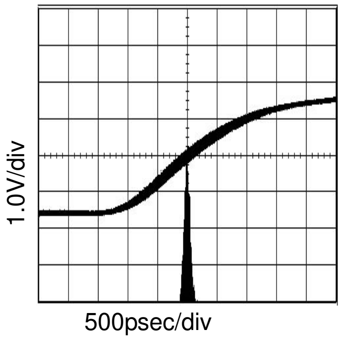


Fig.83 36.9MHz Period-Jitter
VDD=3.3V, at CL=15pF

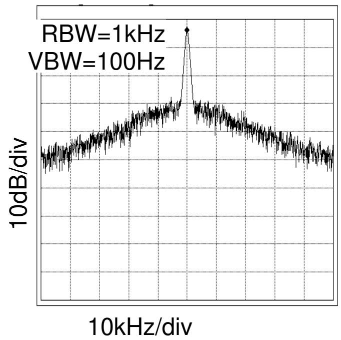


Fig.84 36.9MHz Spectrum
VDD=3.3V, at CL=15pF

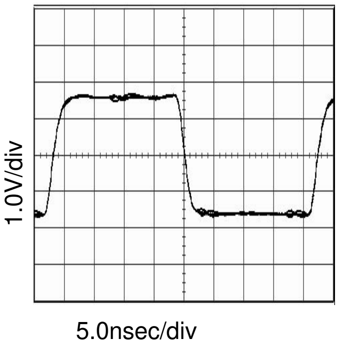


Fig.85. 22.6MHz output waveform
VDD=3.3V, at CL=15pF

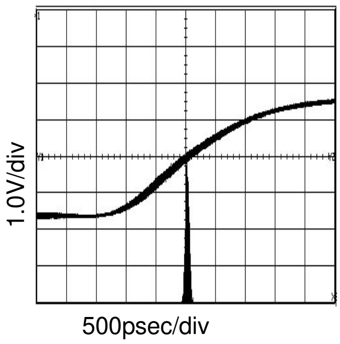


Fig.86 22.6MHz Period-Jitter
VDD=3.3V, at CL=15pF

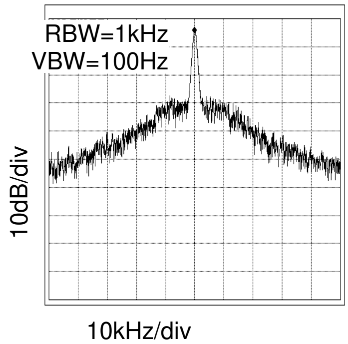


Fig.87 22.6MHz Spectrum
VDD=3.3V, at CL=15pF

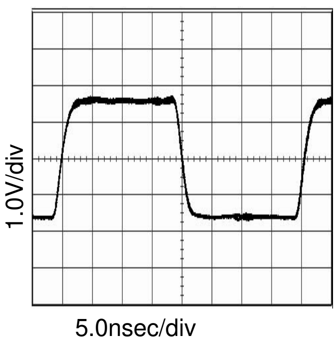


Fig.88 24.6MHz output waveform
VDD=3.3V, at CL=15pF

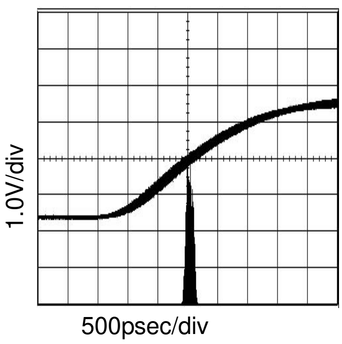


Fig.89 24.6MHz Period-Jitter
VDD=3.3V, at CL=15pF

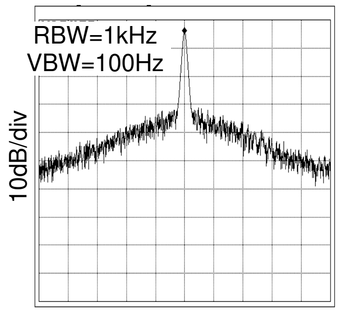


Fig.90 24.6MHz Spectrum
VDD=3.3V, at CL=15pF

●Reference data(BU2362FV basic data)

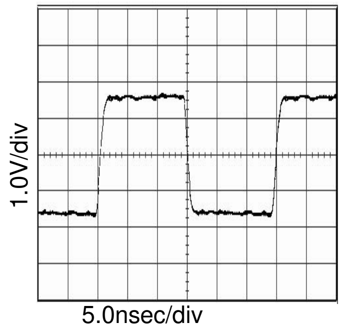


Fig.91 16.9MHz output waveform
VDD=3.3V, at CL=15pF

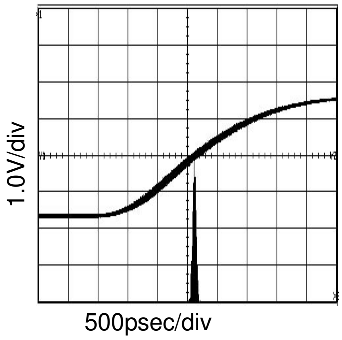


Fig.92 16.9MHz Period-Jitter
VDD=3.3V, at CL=15pF

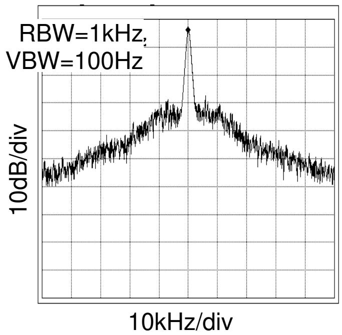


Fig.93 16.9MHz Spectrum
VDD=3.3V, at CL=15pF

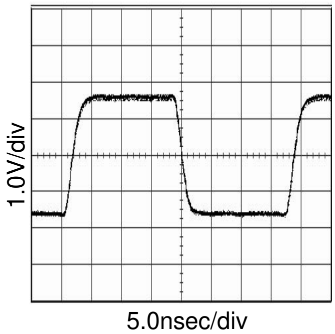


Fig.94 27MHz output waveform
VDD=3.3V, at CL=15pF

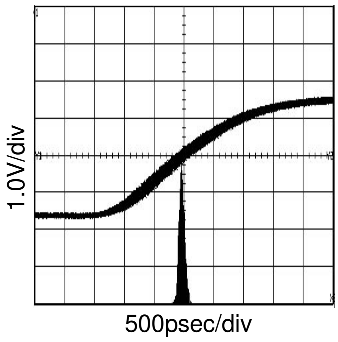


Fig.95 27MHz Period-Jitter
VDD=3.3V, at CL=15pF

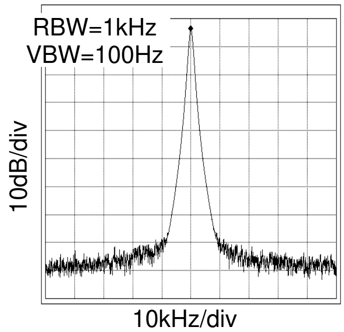


Fig.96 27MHz Spectrum
VDD=3.3V, at CL=15pF

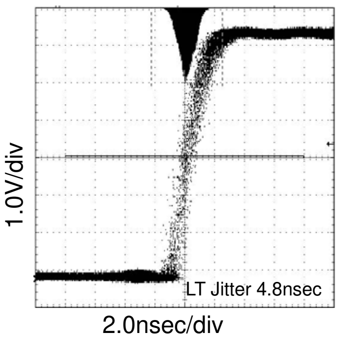


Fig.97 24.6MHz LT Jitter
VDD=3.3V, at CL=15pF

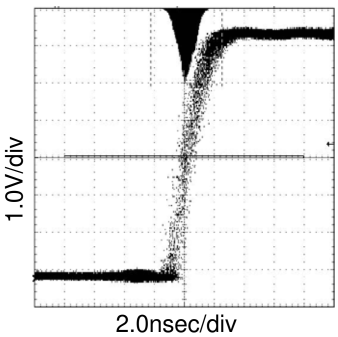


Fig.98 22.6MHz LT Jitter
VDD=3.3V, at CL=15pF

●Reference data (BU2362FV Temperature and Supply voltage variations data)

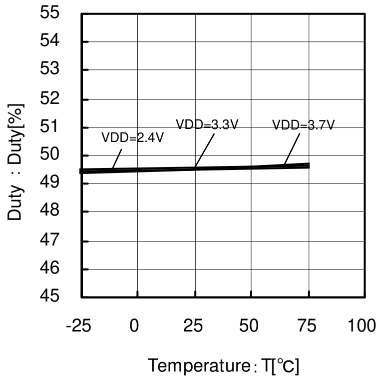


Fig.99 33.9MHz
Temperature-Duty

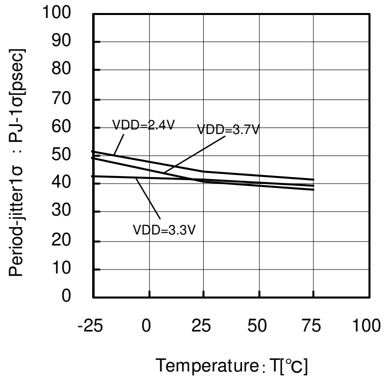


Fig.100 33.9MHz
Temperature-Period-Jitter 1σ

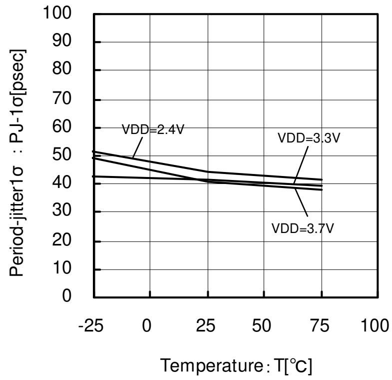


Fig.101 33.9MHz
Temperature-Period-Jitter MIN-MAX

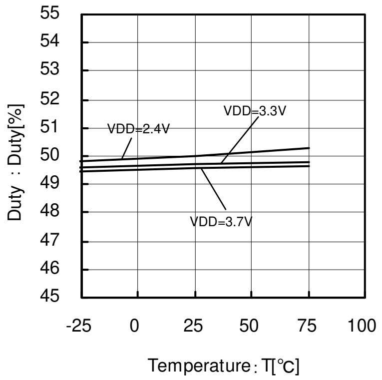


Fig.102 36.9MHz
Temperature-Duty

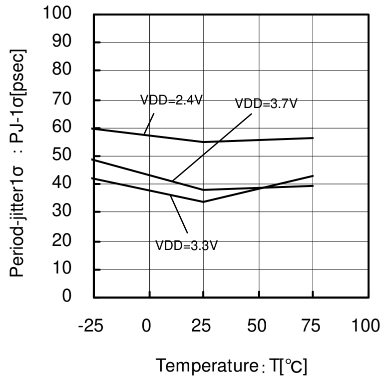


Fig.103 36.9MHz
Temperature-Period-Jitter 1σ

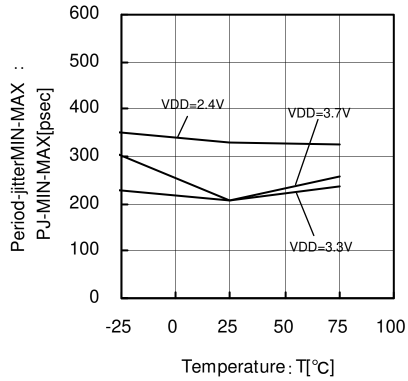


Fig.104 36.9MHz
Temperature-Period-Jitter MIN-MAX

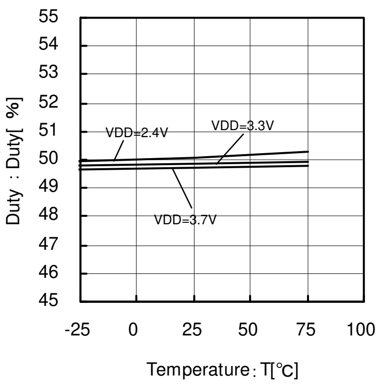


Fig.105 22.6MHz
Temperature-Duty

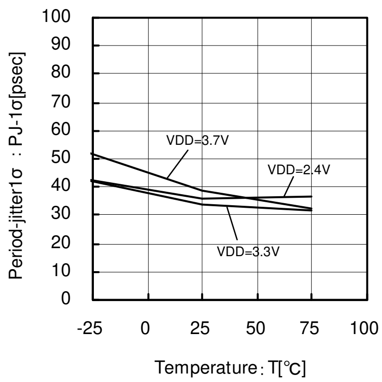


Fig.106 22.6MHz
Temperature-Period-Jitter 1σ

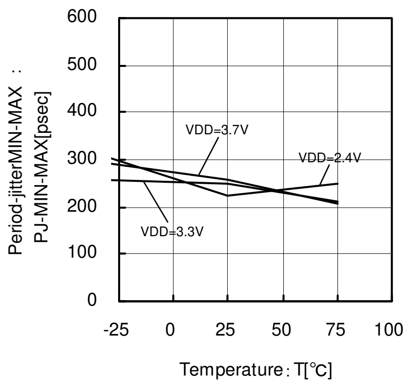


Fig.107 22.6MHz
Temperature-Period-Jitter MIN-MAX

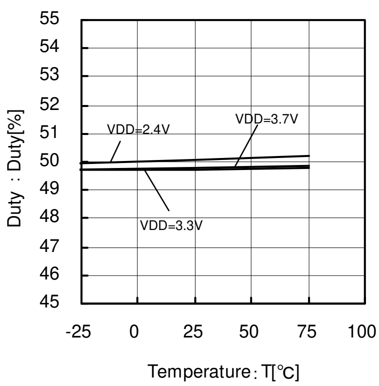


Fig.108 24.6MHz
Temperature-Duty

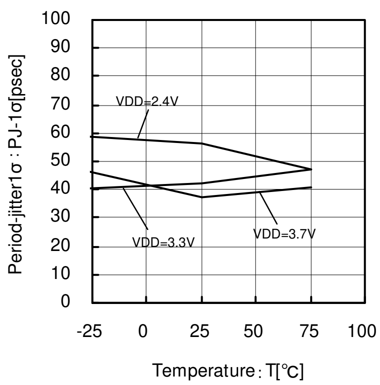


Fig.109 24.6MHz
Temperature-Period-Jitter 1σ

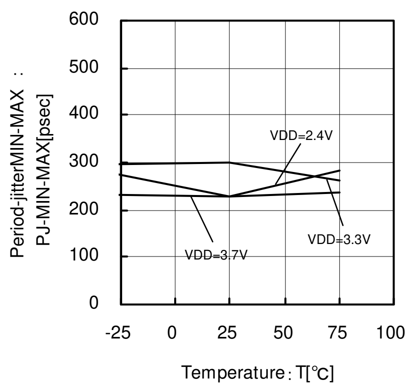


Fig.110 24.6MHz
Temperature-Period-Jitter MIN-MAX

●Reference data (BU2362FV Temperature and Supply voltage variations data)

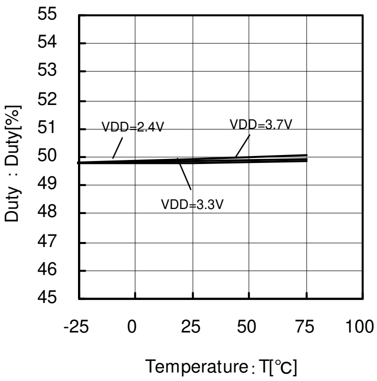


Fig.111 16.9MHz
Temperature-Duty

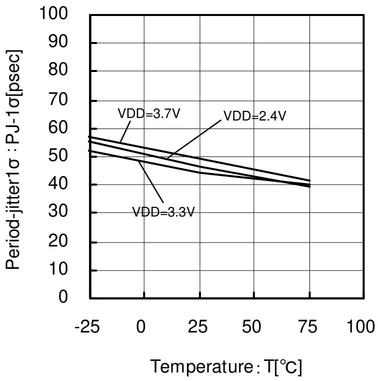


Fig.112 16.9MHz
Temperature-Period-Jitter 1σ

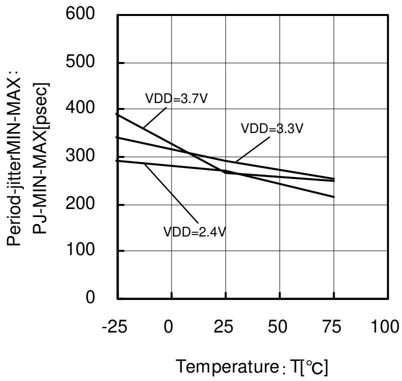


Fig.113 16.9MHz)
Temperature-Period-Jitter MIN-MAX

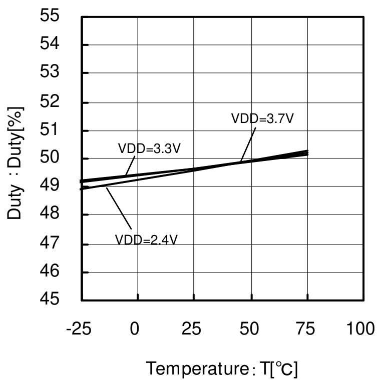


Fig.114 27MHz
Temperature-Duty

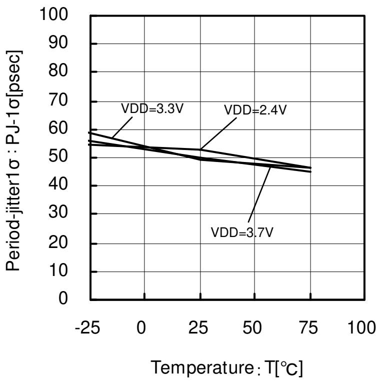


Fig.115 27MHz
Temperature-Period-Jitter 1σ

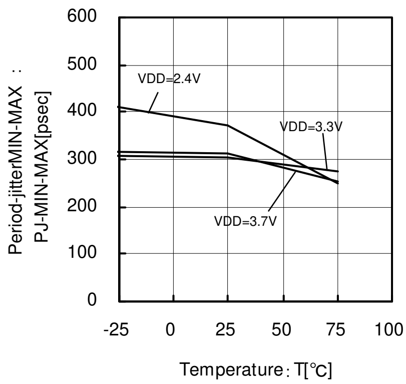


Fig.116 27MHz
Temperature-Period-Jitter MIN-MAX

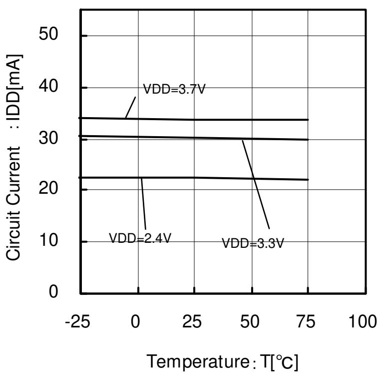


Fig.117 Action circuit current
(with maximum output load)
Temperature-Consumption current

●Block diagram, Pin assignment

◎BU2280FV

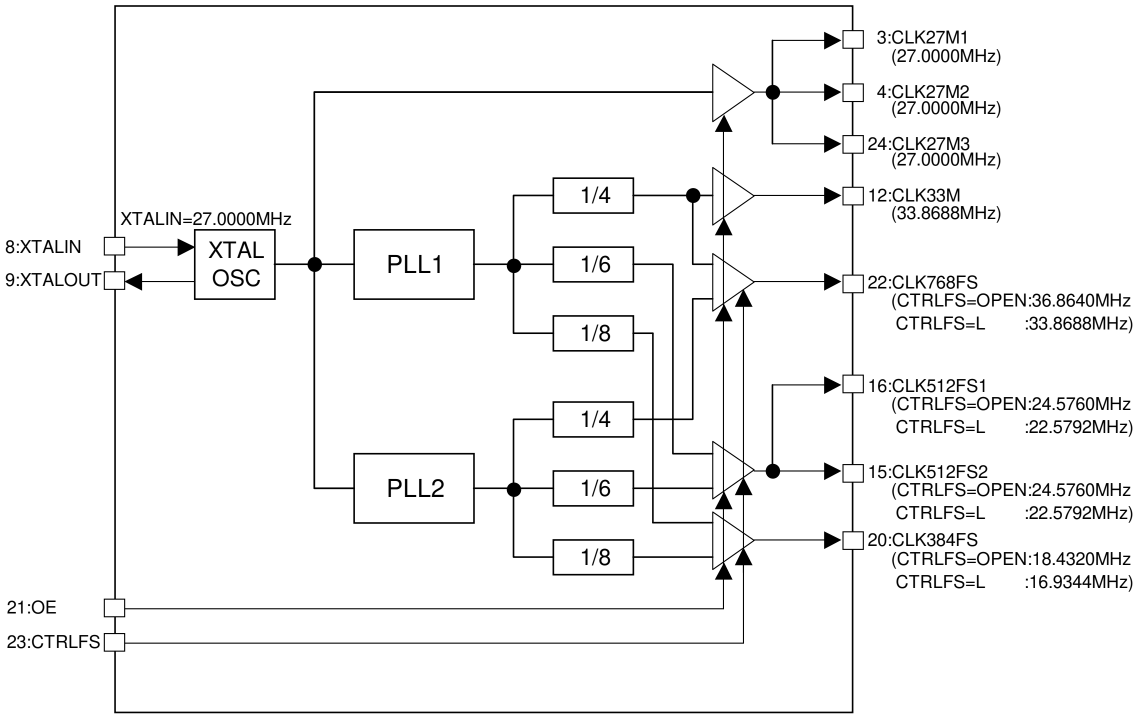


Fig.118

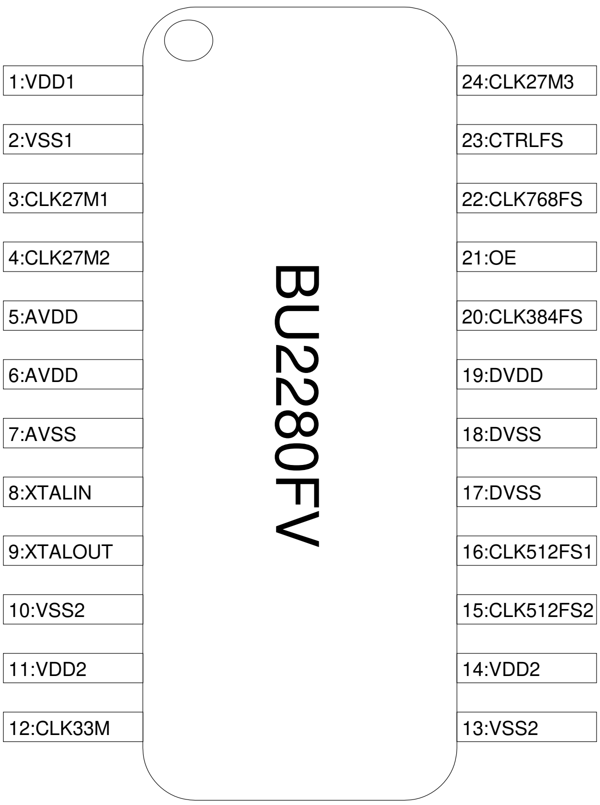


Fig.119

CTRLFS	CLK384FS	CLK512FS	CLK768FS
L	16.9344MHz	22.5792MHz	33.8688MHz
OPEN	18.4320MHz	24.5760MHz	36.8640MHz

●Block diagram, Pin assignment

◎BU2360FV

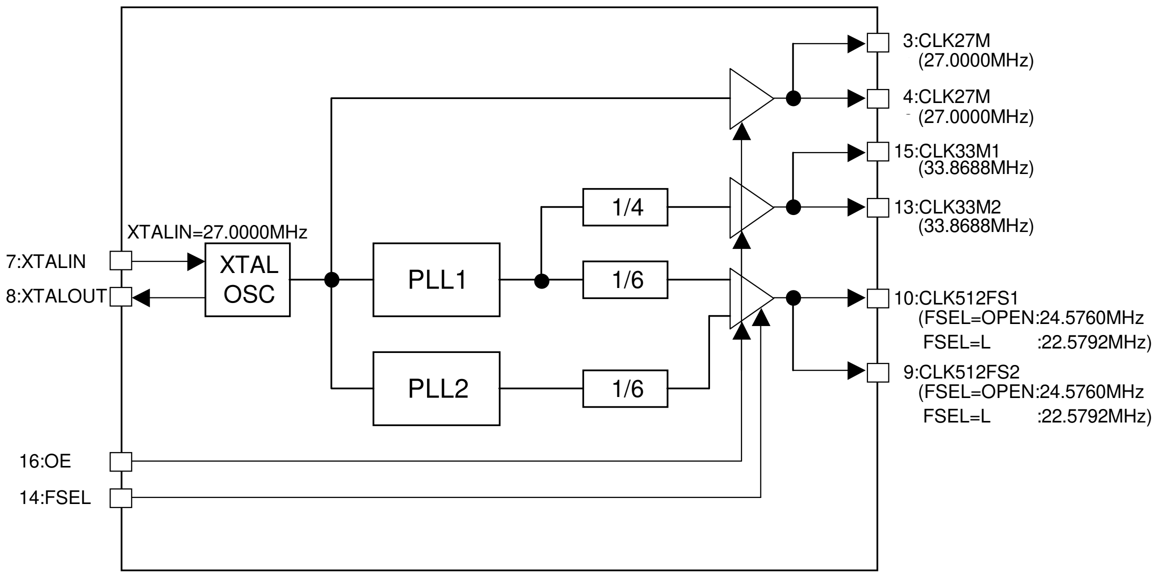


Fig.120

Fig.121

FSEL	CLK512FS1 / 2
L	22.5792MHz
OPEN	24.5760MHz

●Block diagram, Pin assignment

◎BU2362FV

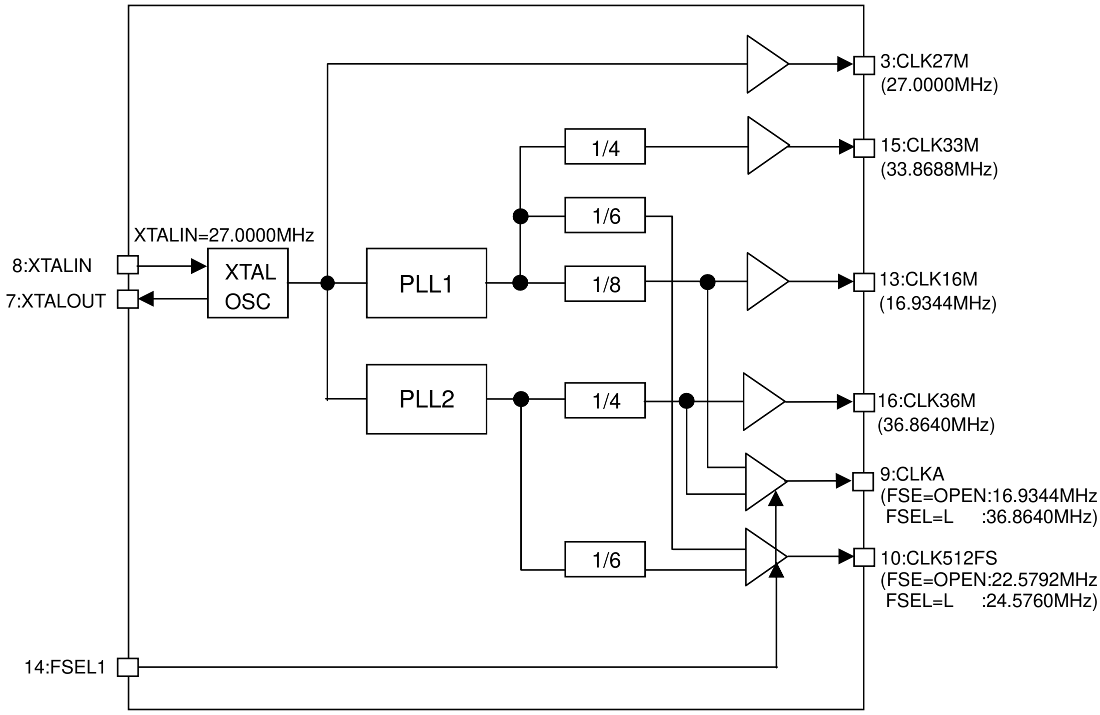


Fig.122

Fig.123

FSEL1	CLK512FS	CLKA
OPEN	22.5792MHz	16.9344MHz
L	24.5760MHz	36.8640MHz

●Example of application circuit

◎BU2280FV

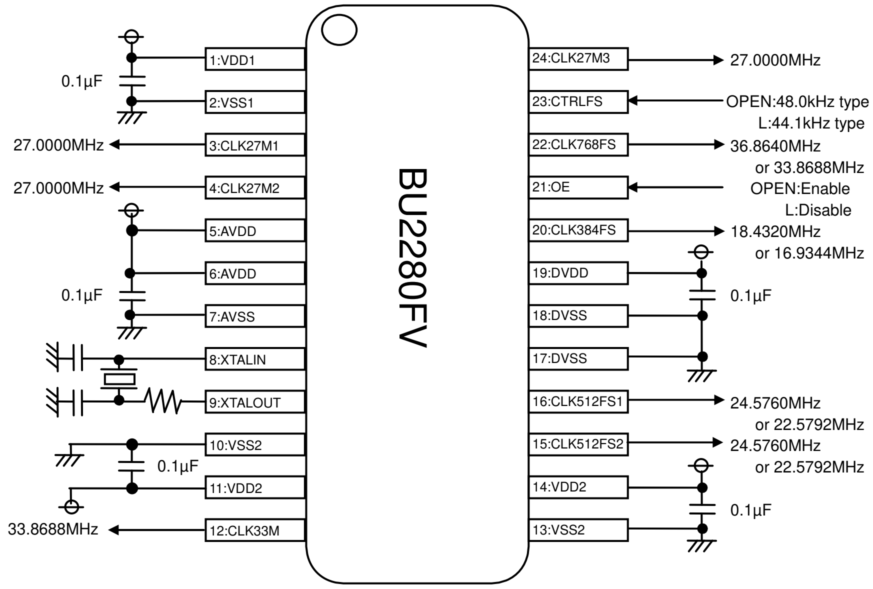


Fig.124

Description of terminal

PIN No.	PIN Name	PIN Function
1	VDD1	Power supply for 27MHz
2	VSS1	GND for 27MHz
3	CLK27M1	27.0000MHz Clock output terminal 1
4	CLK27M2	27.0000MHz Clock output terminal 2
5	AVDD	Power supply for Analog block
6	AVDD	Power supply for Analog block
7	AVSS	GND for Analog block
8	XTALIN	Crystal input terminal
9	XTALOUT	Crystal output terminal
10	VSS2	GND for 33MHz
11	VDD2	Power supply for 33MHz
12	CLK33M	33.8688MHz Clock output terminal
13	VSS2	GND for 33MHz
14	VDD2	Power supply for 33MHz
15	CLK512FS2	CTRLFS=OPEN:24.5760MHz, CTRLFS=L:22.5792MHz
16	CLK512FS1	CTRLFS=OPEN:24.5760MHz, CTRLFS=L:22.5792MHz
17	DVSS	GND for Digital block
18	DVSS	GND for Digital block
19	DVDD	Power supply for Digital block
20	CLK384FS	CTRLFS=OPEN:18.4320MHz, CTRLFS=L:16.9344MHz
21	OE	Output enable (with pull-up), OPEN:enable, L:disable
22	CLK768FS	CTRLFS=OPEN:36.8640MHz, CTRLFS=L:33.8688MHz
23	CTRLFS	15, 16, 20, 22PIN output selection (with pull-up) OPEN:24.5760MHz(15PIN, 16PIN), 18.4320MHz(20PIN), 36.8640MHz(22PIN) L:22.5792MHz(15PIN, 16PIN), 16.9344MHz(20PIN), 33.8688MHz(22PIN)
24	CLK27M3	27.0000MHz Clock output terminal 3

Note) Basically, mount ICs to the printed circuit board for use.
(If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)
Mount 0.1µF capacitors in the vicinity of the IC PINs between 1PIN (VDD1) and 2PIN (VSS1), 5PIN-6PIN (AVDD) and 7PIN (AVSS), 10PIN (VSS2) and 11PIN (VDD2), 13PIN(VSS2) and 14PIN (VDD2), 17PIN-18PIN (DVSS) and 19PIN(DVDD), respectively.
Depending on the conditions of the printed circuit board, mount an additional electrolytic capacitor between the power supply and GND terminal.
For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to BU2280FV from the printed circuit board or to insert a capacitor (of 1Ω or less), which bypasses high frequency desired, between the power supply and the GND terminal.

●Example of application circuit

◎BU2360FV

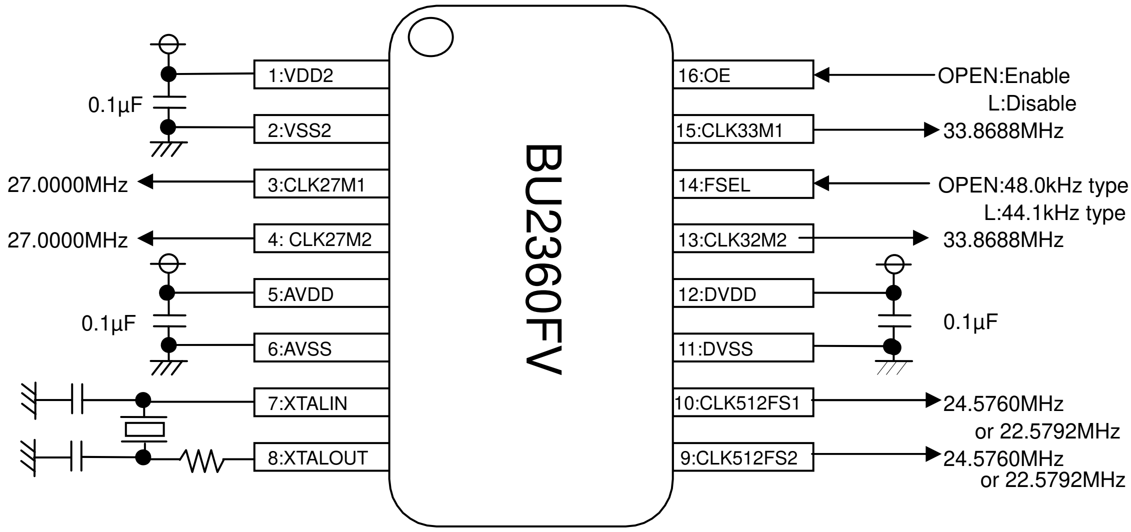


Fig.125

Description of terminal

PIN No.	PIN name	PIN function
1	VDD2	Power supply for 27MHz
2	VSS2	GND for 27MHz
3	CLK27M1	27.0000MHz Clock output terminal 1 (CL=40pF)
4	CLK27M2	27.0000MHz Clock output terminal 2 (CL=25pF)
5	AVDD	Power supply for Analog block
6	AVSS	GND for Analog block
7	XTALIN	Crystal input terminal
8	XTALOUT	Crystal output terminal
9	CLK512FS2	FSEL=OPEN:24.5760MHz, FSEL=L:22.5792MHz
10	CLK512FS1	FSEL=OPEN:24.5760MHz, FSEL=L:22.5792MHz
11	DVSS	GND for Digital block
12	DVDD	Power supply for Digital block
13	CLK33M2	33.8688MHz Clock output terminal 2
14	FSEL	9, 10PIN output selection (with pull-up) OPEN:24.5760MHz(9, 10PIN), L:22.5792MHz(9, 10PIN)
15	CLK33M1	33.8688MHz Clock output terminal 1
16	OE	Output enable (with pull-up), OPEN:enable, L:disable

Note) Basically, mount ICs to the printed circuit board for use.
(If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)
Mount 0.1µF capacitors in the vicinity of the IC PINs between 1PIN (VDD2) and 2PIN (VSS2), 5PIN (AVDD) and 6PIN (AVSS), 11PIN (DVSS) and 12PIN (DVDD), respectively.
Depending on the conditions of the printed circuit board, mount an additional electrolytic capacitor between the power supply and GND terminal.
For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to BU2360FV from the printed circuit board or to insert a capacitor (of 1Ω or less), which bypasses high frequency desired, between the power supply and the GND terminal.

● Example of application circuit

◎BU2362FV

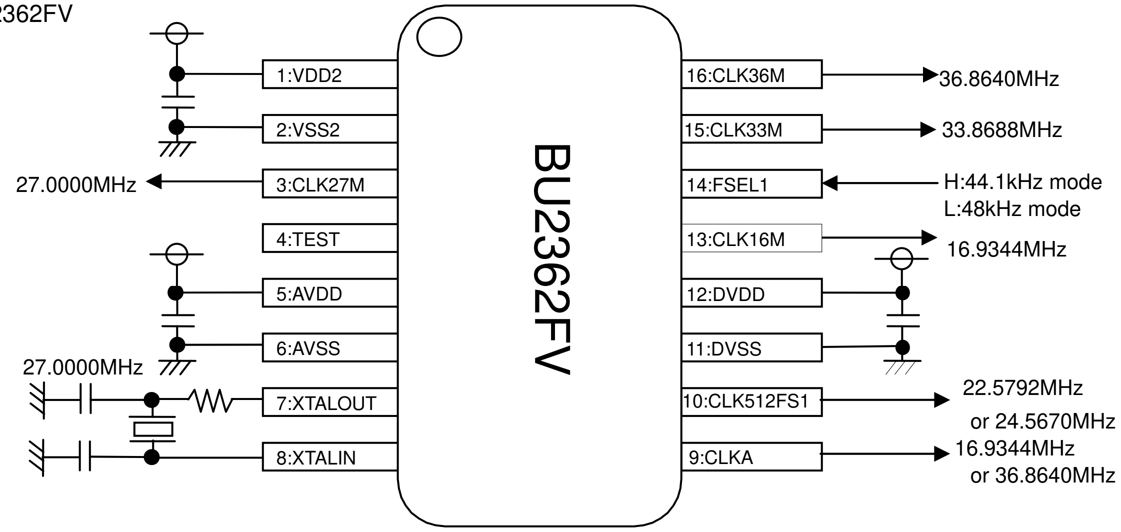


Fig.126

Description of terminal

Pin No.	PIN NAME	Function
1	VDD2	Power supply for CLK27, CLK36M
2	VSS2	GND for CLK27, CLK36M
3	CLK27M	27MHz Clock output terminal
4	TEST	Input pin for TEST : with pull-down (Please set "L" or OPEN, normally)
5	AVDD	Power supply for Analog block
6	AVSS	GND for Analog block
7	XTALOUT	Crystal output terminal
8	XTALIN	Crystal input terminal
9	CLKA	CLKA output terminal (16.9344MHz or 36.8640MHz)
10	CLK512FS	512fs Clock output terminal (22.5792MHz or 24.5760MHz)
11	DVSS	Power supply for Digital block
12	DVDD	GND for Digital block
13	CLK16M	16.9344MHz Clock output terminal
14	FSEL1	CLKA or CLK512FS pin output select : with pull-up
15	CLK33M	33.8688MHz Clock output terminal
16	CLK36M	36.8640MHz Clock output terminal

● Notes for use (BU2362FV)

Basically, mount ICs to the printed circuit board for use. (If the ICs are not mounted to the printed circuit board, the characteristics of ICs may not be fully demonstrated.)
Mount 0.1μF capacitors in the vicinity of the IC PINs between 1PIN (VDD2) and 2PIN (VSS2), 5PIN (AVDD) and 6PIN (AVSS), 11PIN (DVSS) and 12PIN (DVDD), respectively.
For the fine-tuning of frequencies, insert several numbers of pF in the 7PIN and 8PIN to GND.
Depending on the conditions of the printed circuit board, mount an additional electrolytic capacitor between the power supply and GND terminal.
For EMI protection, it is effective to put ferrite beads in the origin of power supply to be fed to BU2362FV from the printed circuit board or to insert a capacitor (of 1Ω or less), which bypasses high frequency desired, between the power supply and the GND terminal.

*Even though we believe that the example of recommended circuit is worth of a recommendation, please be sure to thoroughly recheck the characteristics before use.

●Notes for use

1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as applied voltage (VDD or VIN), operating temperature range (Topr), etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

2) Recommended operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

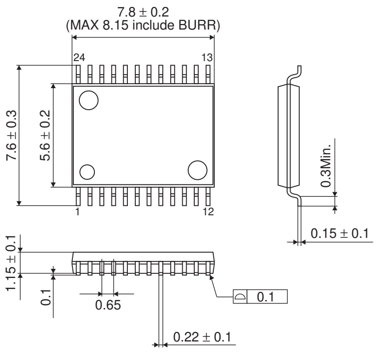
11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Ordering part number

B	U		2	2	8	0		F	V	-	E	2

- Part No.
- Part No. 2280, 2360,2362
- Package FV:SSOP-B24, FV:SSOP-B16
- Packaging and forming specification E2: Embossed tape and reel

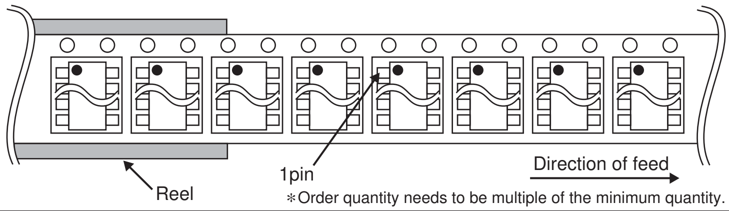
SSOP-B24



(Unit : mm)

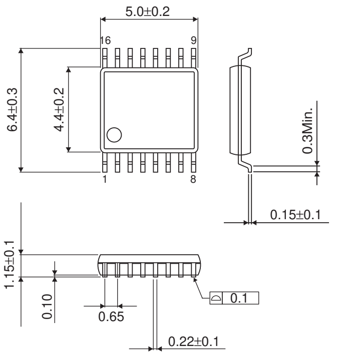
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

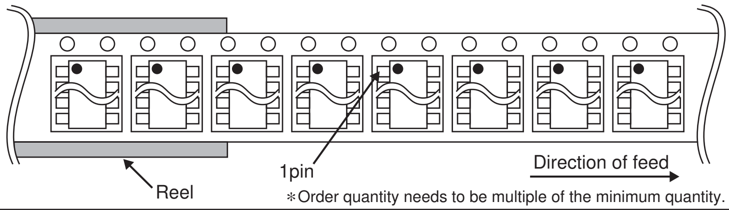
SSOP-B16



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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