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System Lens Drivers

# μ-step System Lens Driver for Digital Still Cameras

**BU24033GW**

●General Description

BU24033GW is a system Lens Driver that uses μ-step driving to make the configuration of the sophisticated, high precision and low noise lens driver system possible. This IC has a built-in driver for both DC motor and voice coil motor and a μ-step controller that decreases CPU power. Therefore, multifunctional lens can be applied.

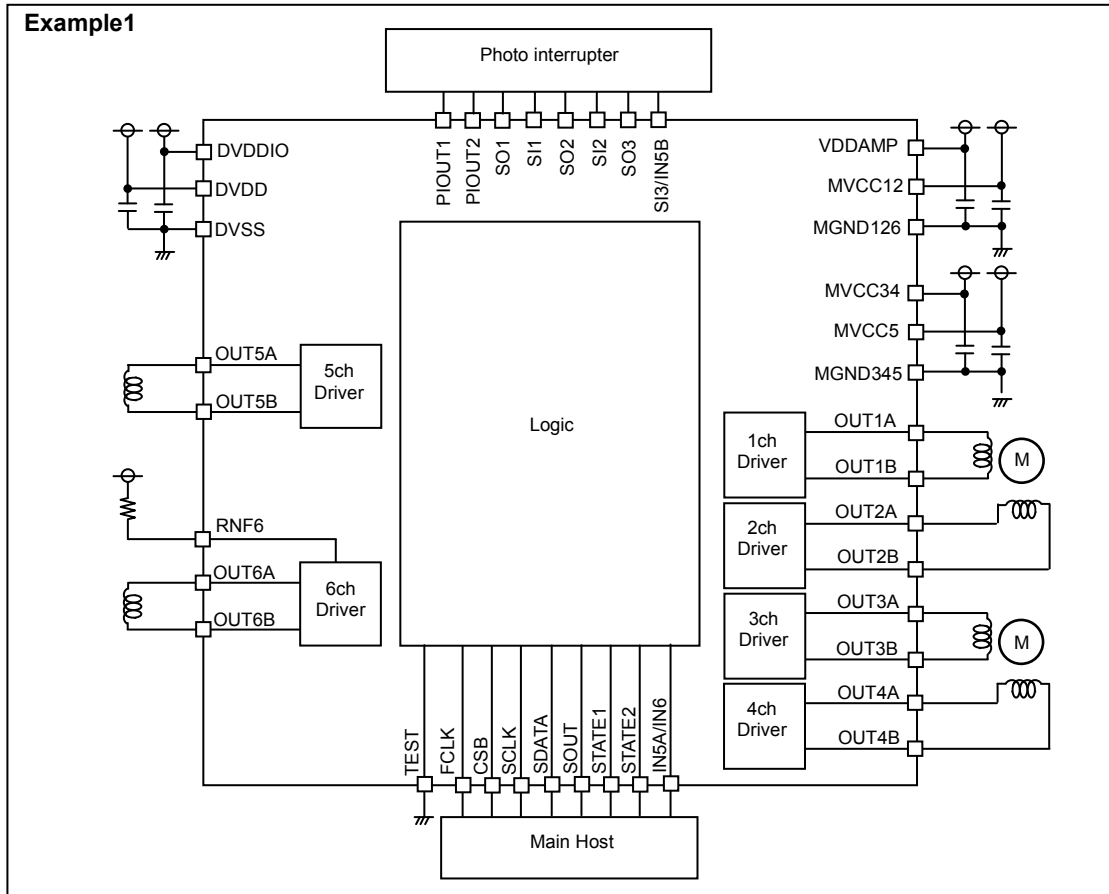
●Features

- Built-in 6 channels Driver block
  - 1ch-5ch: Voltage control type H-bridge (Adaptable to STM 2systems)
  - 6ch: Current control type H-bridge
- Built-in 2 channels PI driving circuit
- Built-in 3 channels Waveforming circuit
- Built-in FLL digital servo circuit
- Built-in PLL circuit

●Applications

- Digital still cameras

●Typical Application Circuit



●Key Specifications

- I/O Power Supply Voltage: 1.62V to 3.6V
- Digital Power Supply Voltage: 2.7V to 3.6V
- Driver Power Supply Voltage: 2.7V to 5.5V
- Output Current (1ch-4ch,6ch): ±500mA(Max)
- Output Current (5ch): ±600mA(Max)
- Input Clock Frequency: 1MHz to 28MHz
- FET ON Resistance (1ch-4ch): 1.5Ω(Typ)
- FET ON Resistance (5ch,6ch): 1.0Ω(Typ)
- Operating Temperature Range: -20°C to +85°C

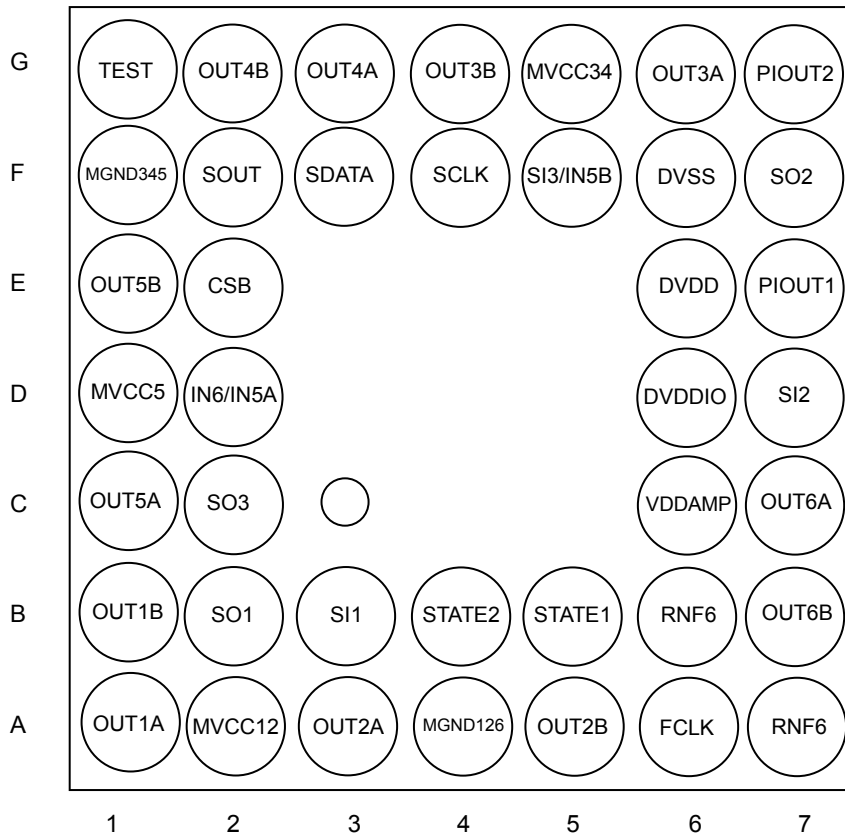
●Package

UCSP75M3

3.00mm x 3.00mm x 0.85mm

●Pin Configuration

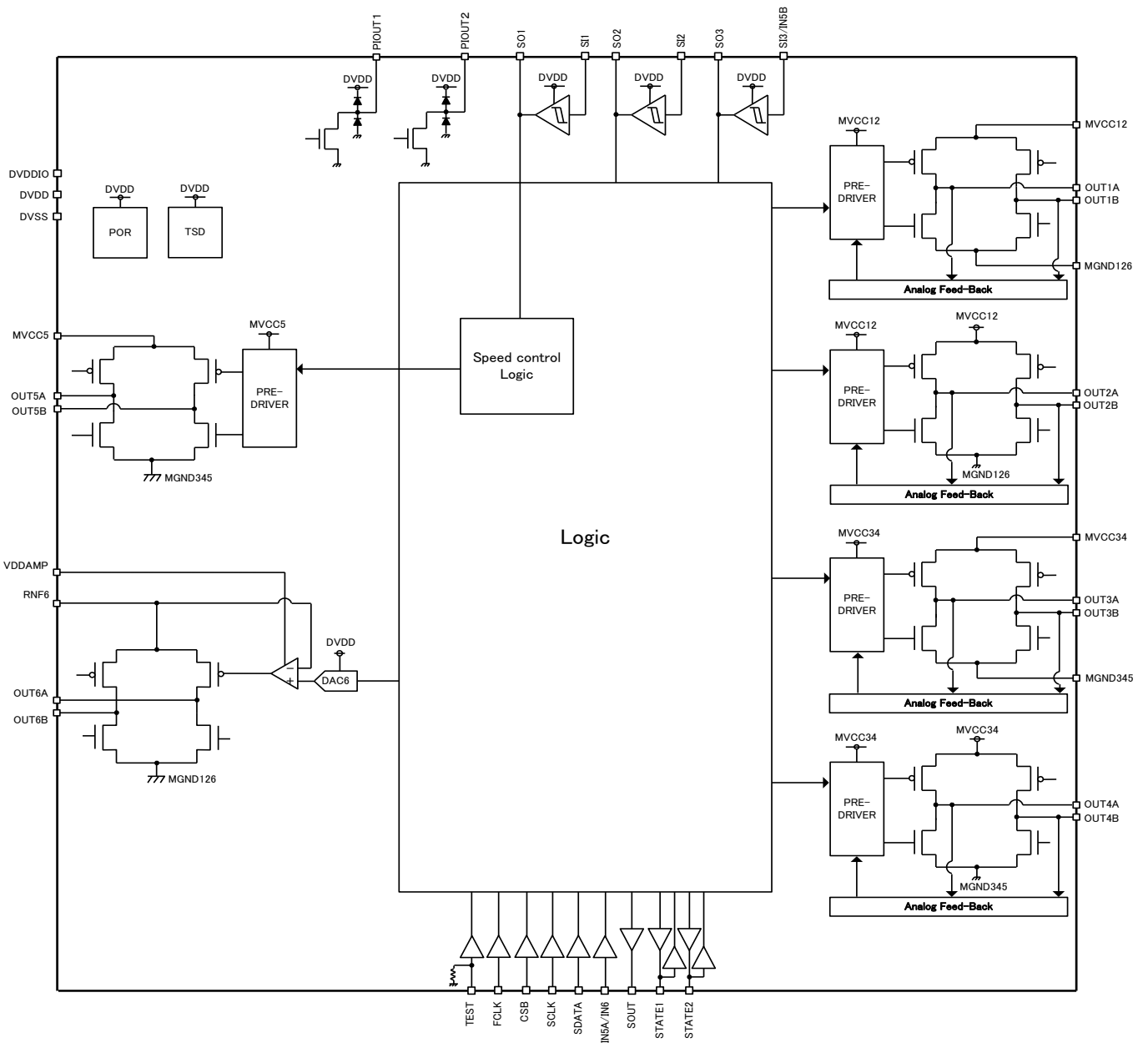
(Bottom view)



●Pin Description

Land Matrix No.	Pin Name	Power Supply	Function	Land Matrix No.	Pin Name	Power Supply	Function
E6	DVDD	-	Digital power supply	A2	MVCC12	-	1ch, 2ch Driver power supply
D6	DVDDIO	-	I/O power supply	A4	MGND126	-	1ch, 2ch, 6ch Driver ground
F6	DVSS	-	ground	A1	OUT1A	MVCC12	1ch Driver A output
A6	FCLK	DVDDIO	FCLK logic input	B1	OUT1B	MVCC12	1ch Driver B output
E2	CSB	DVDDIO	CSB logic input	A3	OUT2A	MVCC12	2ch Driver A output
F4	SCLK	DVDDIO	SCLK logic input	A5	OUT2B	MVCC12	2ch Driver B output
F3	SDATA	DVDDIO	SDATA logic input	G5	MVCC34	-	3ch, 4ch Driver power supply
F2	SOUT	DVDDIO	SOUT logic output	F1	MGND345	-	3ch, 4ch, 5ch Driver ground
D2	IN6/IN5A	DVDDIO	IN6/IN5A logic input	G6	OUT3A	MVCC34	3ch Driver A output
B5	STATE1	DVDDIO	STATE1 logic input/output	G4	OUT3B	MVCC34	3ch Driver B output
B4	STATE2	DVDDIO	STATE2 logic input/output	G3	OUT4A	MVCC34	4ch Driver A output
G1	TEST	DVDDIO	TEST logic output	G2	OUT4B	MVCC34	4ch Driver B output
E7	PIOUT1	DVDD	PI driving output 1	D1	MVCC5	-	5ch Driver power supply
G7	PIOUT2	DVDD	PI driving output 2	C1	OUT5A	MVCC5	5ch Driver A output
B3	SI1	DVDD	Waveforming input1	E1	OUT5B	MVCC5	5ch Driver B output
B2	SO1	DVDD	Waveforming output1	C6	VDDAMP	-	6ch Power supply of current driver control
D7	SI2	DVDD	Waveforming input2	A7,B6	RNF6	-	6ch Driver power supply
F7	SO2	DVDD	Waveforming output2	C7	OUT6A	RNF6	6ch Driver A output
F5	SI3/IN5B	DVDD	Waveforming input3/IN5B logic input	B7	OUT6B	RNF6	6ch Driver B output
C2	SO3	DVDD	Waveforming output3				

●Block Diagram



●Description of Blocks

Stepping Motor Driver ( 1ch-4ch Driver)

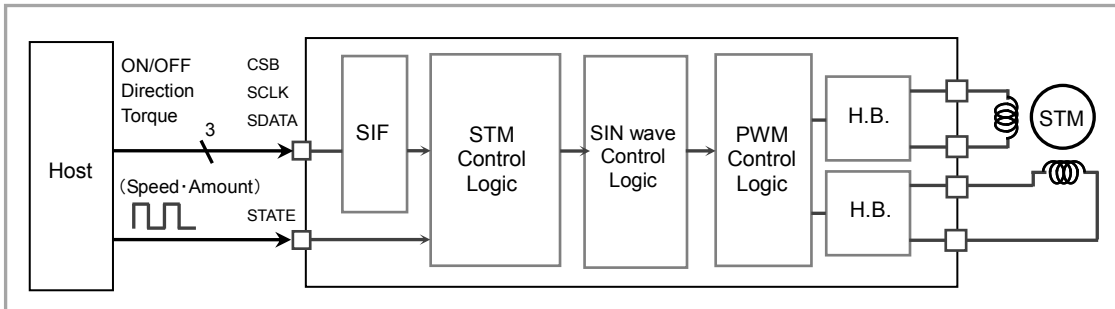
- Built-in stepping motor driver of PWM driving type.
- Maximum 2 stepping motors can be driven independently.
- Built-in voltage feedback circuit of D-class type.
- 3ch/4ch drivers can also drive independently for DC motor or voice coil motor.

(1) Control

It corresponds to both Clock IN and Autonomous control.

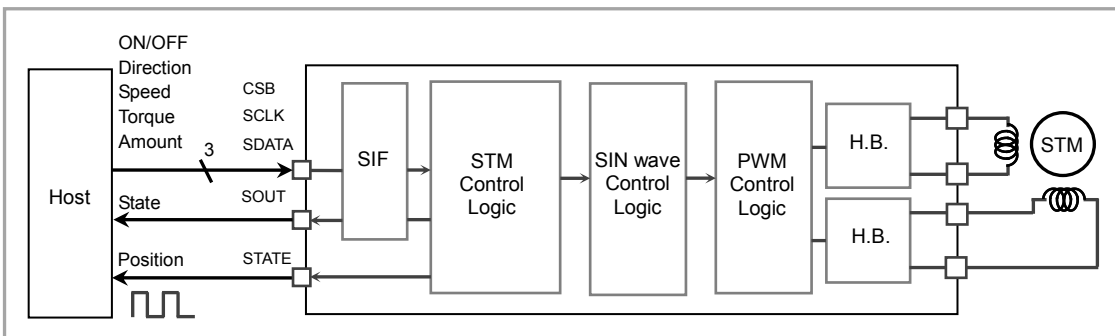
( i )Clock IN Control

Set the registers for the stepping motor control.  
 The stepping motor is rotated and synchronized with the input clock in the STATE pin.  
 It is possible to select the mode of stepping motor control from  $\mu$ -step, 1-2 phase excitation, 2 phase excitation and the number of edge for electrical angle cycle from 4, 8, 32, 64, 128, 256, 512 or 1024.



( ii )Autonomous Control

The stepping motor is rotated by setting the registers for the stepping motor control.  
 The state of rotation command (executing:1, finished:0), Cache register and motor position are the output from the serial output (SOUT pin). Also, the signal (MO output) which is synchronized with the motor rotation is the output from STATE pin.  
 It is possible to select the mode of stepping motor control from  $\mu$ -step (1024 portion), 1-2 phase excitation and 2 phase excitation.  
 Built-in Cache registers.  
 Cache registers enable the setting of subsequent process while the motor is in operation. Through these registers, operations are done continuously.



●Description of Blocks

Voltage Driver (5ch Driver)

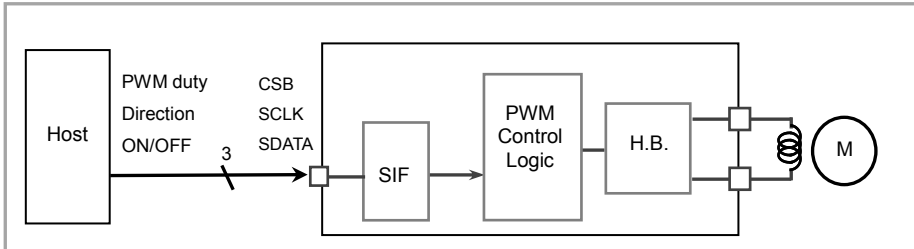
Built-in voltage driver of PWM driving type.  
Built-in digital FLL speed control logic.

(1) Control

( i )Register Control

■at speed control = OFF

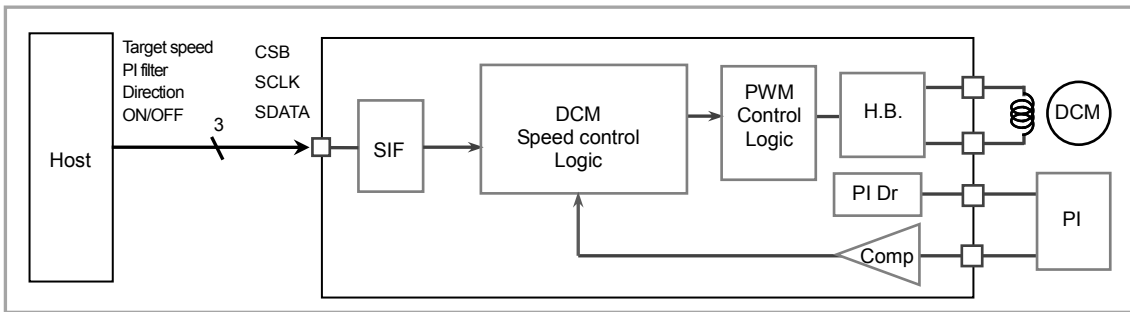
The PWM drive is executed by the PWM duty ratio, the PWM direction and the PWM ON/OFF which are controlled by the register settings.



■at speed control = ON

The speed control drive is executed by the target speed value, the direction, the coefficient value of PI filter and the turning ON/OFF which are controlled by the register settings.

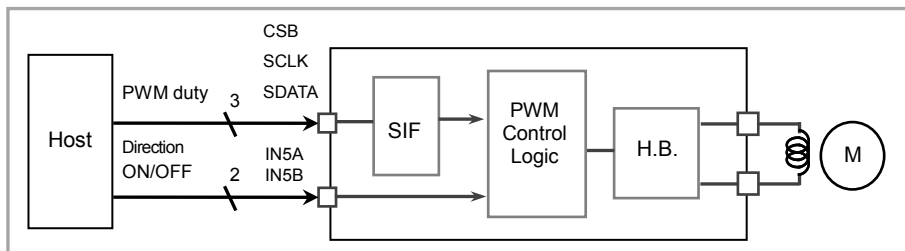
The motor speed is adjusted by comparing the target speed with the motor speed detected at the signal of photo-interrupter.



( ii )External Pin Control (only at speed control = OFF)

■at speed control = OFF

The PWM drive is executed by the PWM duty ratio which is controlled by the register setting. The PWM direction and the PWM ON/OFF are controlled by IN5A/IN5B pin.



●Description of Blocks

Current Driver (6ch Driver)

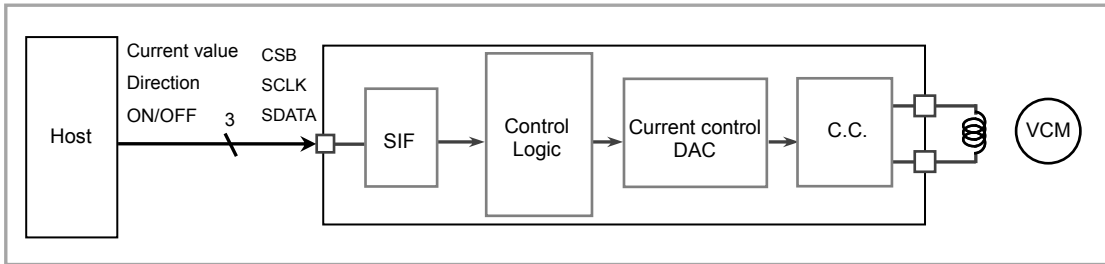
Built-in constant current driver.

The voltage of RNF pin and the external resistor (RRNF) determine the amount of output current. The internal high-precision amplifier (CMOS gate input) is used for constant current control. If any resistance component exists in the wirings of RNF pin and the external resistor (RRNF), the precision can be reduced. To avoid this, pay utmost attention to the wirings.

(1) Control

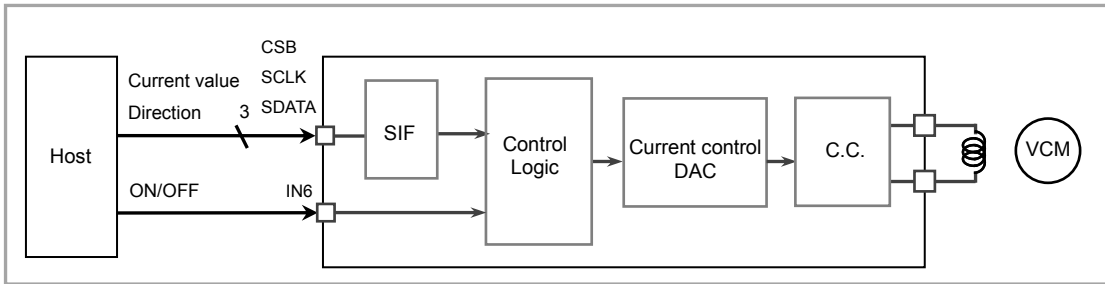
( i )Register Control

The constant current drive is executed by the output current value, the current direction and the current ON/OFF which are controlled by the register settings.



( ii )External Pin Control

The constant current drive is executed by the output current value and current direction which are controlled by the register setting. Constant current driving ON/OFF is controlled by IN6 pin.



**●Absolute Maximum Ratings (Ta=25°C)**

Parameter	Symbol	Limit	Unit	Remark
Power Supply Voltage	DVDDIO DVDD	-0.3 to +4.5	V	
	MVCC	-0.3 to +7.0	V	MVCC12, MVCC34, MVCC5, VDDAMP
Input Voltage	VIN	-0.3 to supply voltage+0.3	V	
Input / Output Current <sup>*1</sup>	IIN	+500	mA	MVCC12, MVCC34, RNF6
		+600	mA	MVCC5
		+50	mA	by PIOOUT pin
Storage Temperature Range	TSTG	-55 to +125	°C	
Operating Temperature Range	TOPE	-20 to +85	°C	
Permissible Dissipation <sup>*2</sup>	PD	1000	mW	

<sup>\*1</sup> Must not exceed PD.

<sup>\*2</sup> To use at a temperature higher than Ta=25 °C, derate 10mW per 1 °C  
(At mounting 50mm x 58mm x 1.75mm glass epoxy board.)

**●Recommended Operating Rating (Ta=25°C)**

Parameter	Symbol	Limit	Unit	Remark
I/O Power Supply Voltage	DVDDIO	1.62 to 3.6	V	
Digital Power Supply Voltage	DVDD	2.7 to 3.6	V	DVDD ≤ MVCC
Driver Power Supply Voltage	MVCC	2.7 to 5.5	V	MVCC12, MVCC34, MVCC5, VDDAMP
Clock Operating Frequency	FCLK	1 to 28	MHz	Reference clock



## ●Electrical Characteristic

(Unless otherwise specified, Ta=25°C, DVDDIO=DVDD=3.0V, MVCC=5.0V, DVSS=MGND=0.0V)

Parameter	Symbol	Limit			Unit	Conditions	
		MIN	TYP	MAX			
<Current Consumption>							
Quiescence (DVDDIO)	ISSDO	-	0	10	$\mu$ A	CMD_RS=0	
	(DVDD)	ISSD	-	50	95		$\mu$ A
	(MVCC)	ISSM	-	0	10		$\mu$ A
Operation (DVDDIO)	IDDDO	-	0.1	1	mA	CMD_RS=STB=CLK_EN=1 FCLK=24MHz CLK_DIV setting : 0h, No load	
	(DVDD)	IDDD	-	6	10		mA
<Logic Block>							
Low-level Input Voltage	VIL	DVSS	-	0.3DVDDIO	V		
High-level Input Voltage	VIH	0.7DVDDIO	-	DVDDIO	V		
Low-level Input Current	IIL	0	-	10	$\mu$ A	VIL=DVSS	
High-level Input Current	IIH	0	-	10	$\mu$ A	VIH=DVDDIO	
Low-level Output Voltage	VOL	DVSS	-	0.2DVDDIO	V	IOL=1.0mA	
High-level Output Voltage	VOH	0.8DVDDIO	-	DVDDIO	V	IOH=1.0mA	
<PI Driving Circuit>							
Output Voltage	PIVO	-	0.15	0.5	V	IIH=30mA	
<Waveforming Circuit>							
High-level Threshold Voltage	VthH	-	-	1.9	V	DVDD=3.25V	
Low-level Threshold Voltage	VthL	0.9	-	-	V	DVDD=3.25V	
Hysteresis Width	Vhys	0.2	-	0.6	V	DVDD=3.25V	
<Voltage Driver Block 1ch-4ch>							
ON-resistance	Ron	-	1.5	2.0	$\Omega$	IO=±100mA (the sum of high and low sides)	
OFF-leak Current	IOZ	-10	0	+10	$\mu$ A	Output Hiz setting	
Average Voltage Accuracy between different Output Pins	Vdiff	-5	-	+5	%	Vdiff setting : 2Bh	
<Voltage Driver Block 5ch>							
ON-resistance	Ron	-	1.0	1.5	$\Omega$	IO=±100mA (the sum of high and low sides)	
OFF-leak Current	IOZ	-10	0	+10	$\mu$ A	Output Hiz setting	
<Current Driver Block 6ch>							
ON-resistance	Ron	-	1.0	1.5	$\Omega$	IO=±100mA (the sum of high and low sides)	
OFF-leak Current	IOZ	-10	0	+10	$\mu$ A	Output Hiz setting	
Output Current	IO	193	200	207	mA	DAC setting : 80h RRNF=1 $\Omega$	

● Typical Performance Curves

(Unless otherwise specified, Ta=25°C, DVDDIO=DVDD=3.0V, MVCC=5.0V, DVSS=MGND=0.0V)

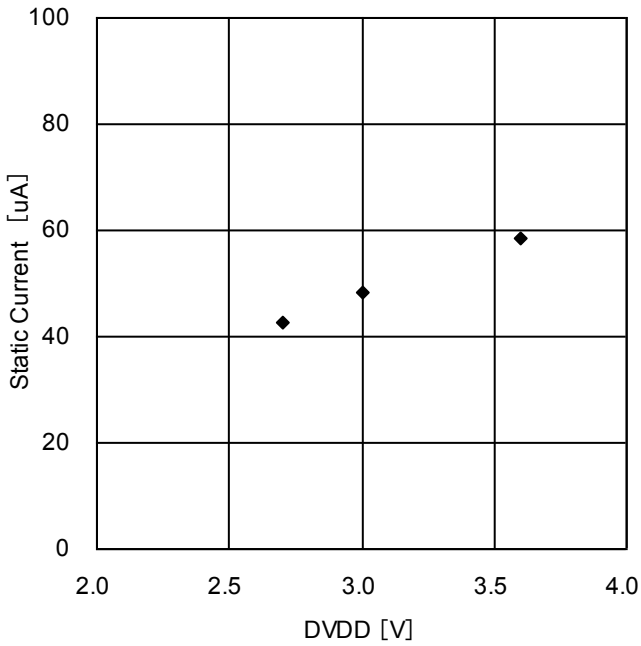


Figure 1. DVDD Static Current Voltage Dependency

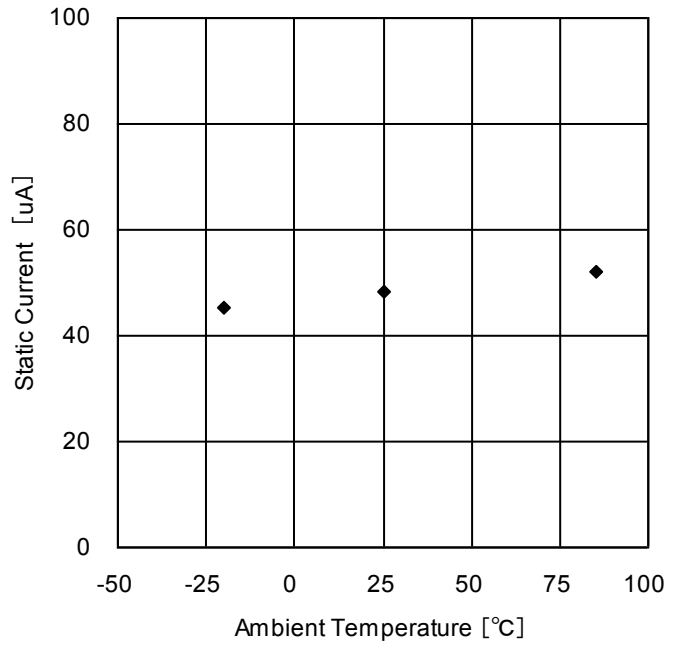


Figure 2. DVDD Static Current Temperature Dependency

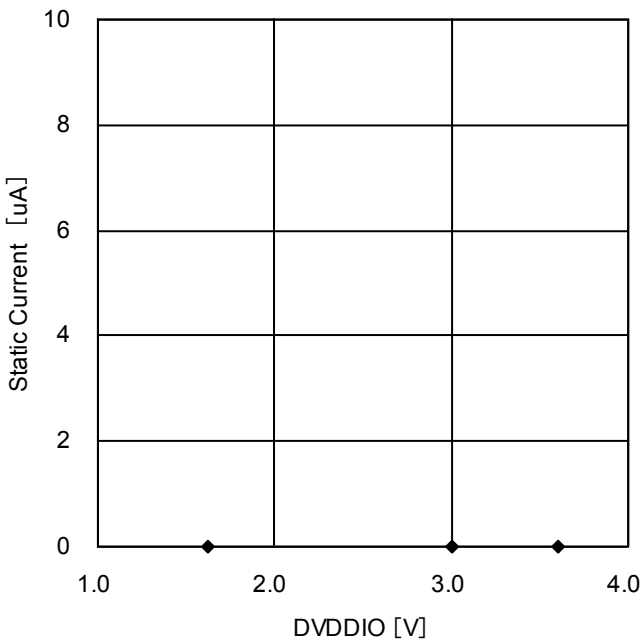


Figure 3. DVDDIO Static Current Voltage Dependency

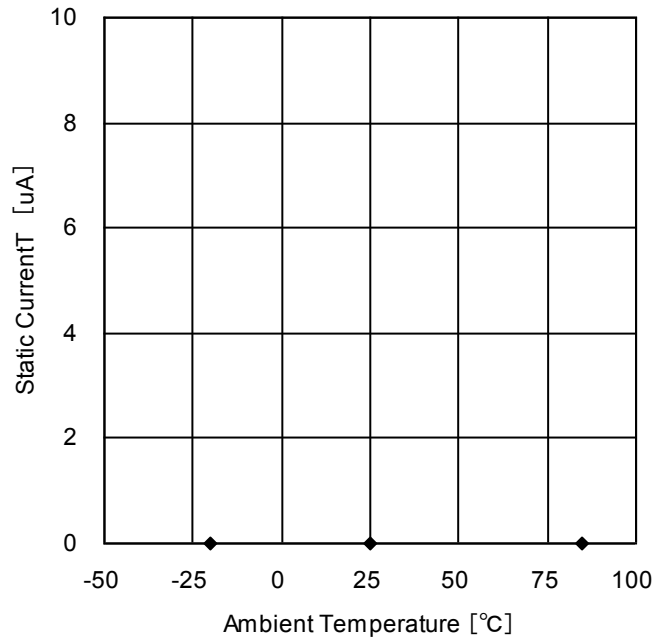


Figure 4. DVDDIO Static Current Temperature Dependency

● Typical Performance Curves

(Unless otherwise specified, Ta=25°C, DVDDIO=DVDD=3.0V, MVCC=5.0V, DVSS=MGND=0.0V)

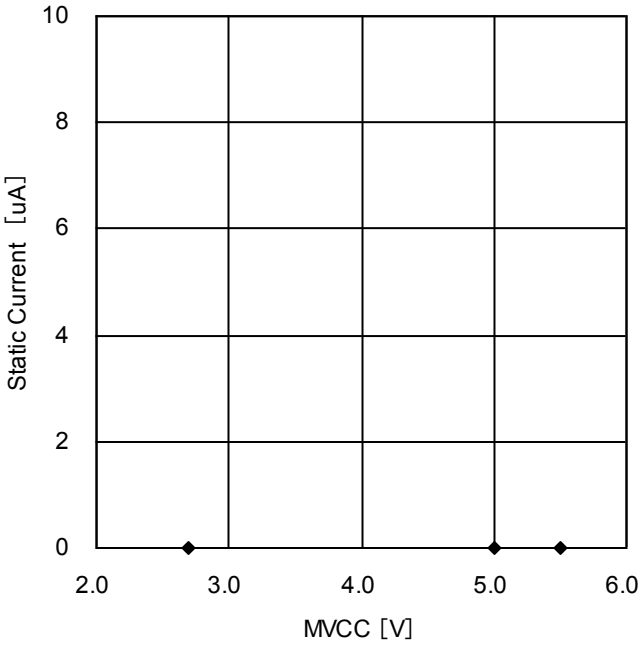


Figure 5. MVCC Static Current Voltage Dependency

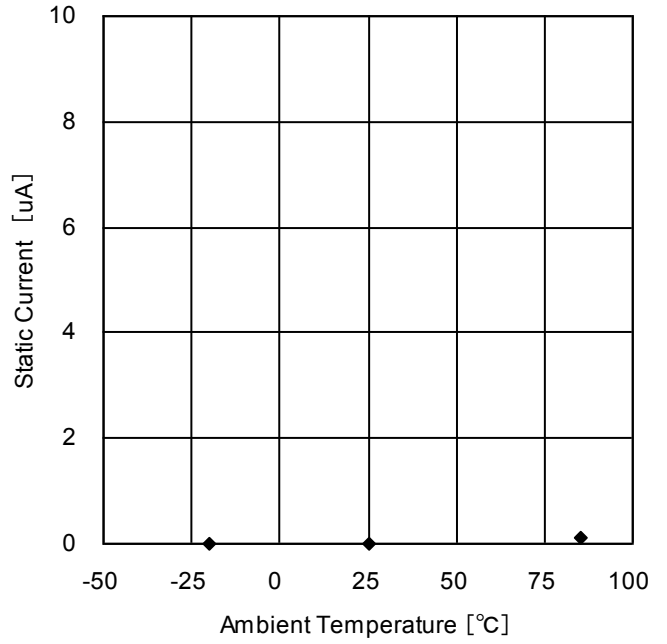


Figure 6. MVCC Static Current Temperature Dependency

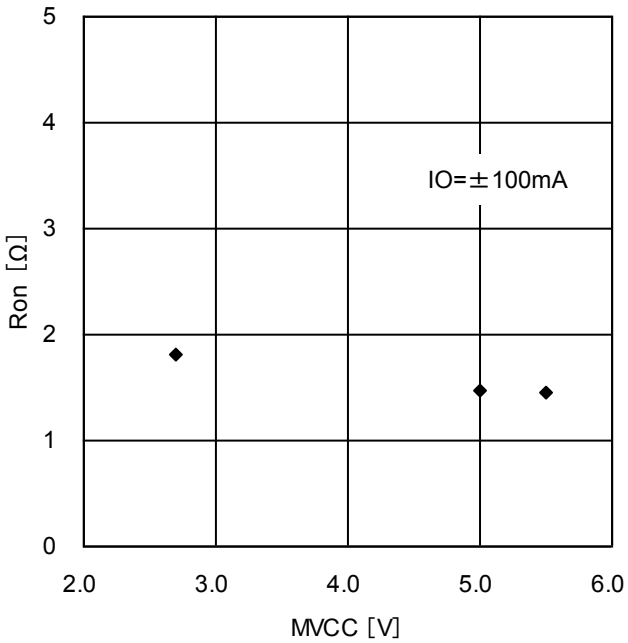


Figure 7. Output ON-Resistance MVCC Dependency (1ch-4ch driver block)

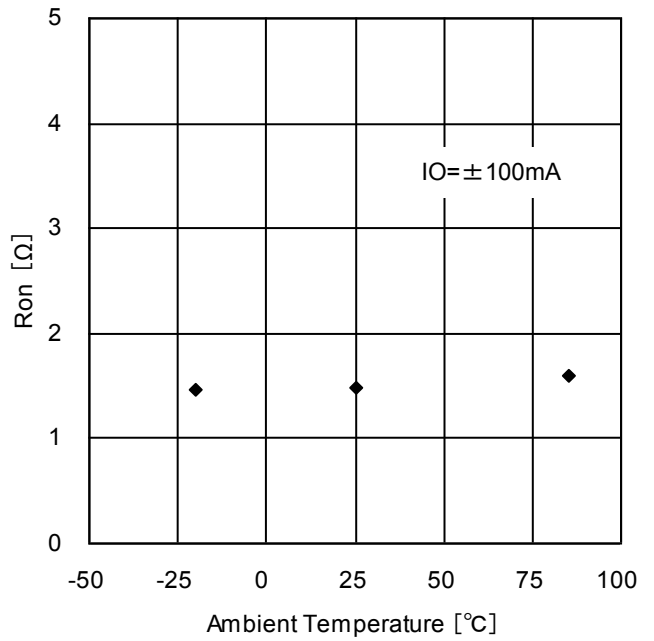


Figure 8. Output ON-Resistance Temperature Dependency (1ch-4ch driver block)

● Typical Performance Curves

(Unless otherwise specified,  $T_a=25^\circ\text{C}$ ,  $DVDDIO=DVDD=3.0\text{V}$ ,  $MVCC=5.0\text{V}$ ,  $DVSS=MGND=0.0\text{V}$ )

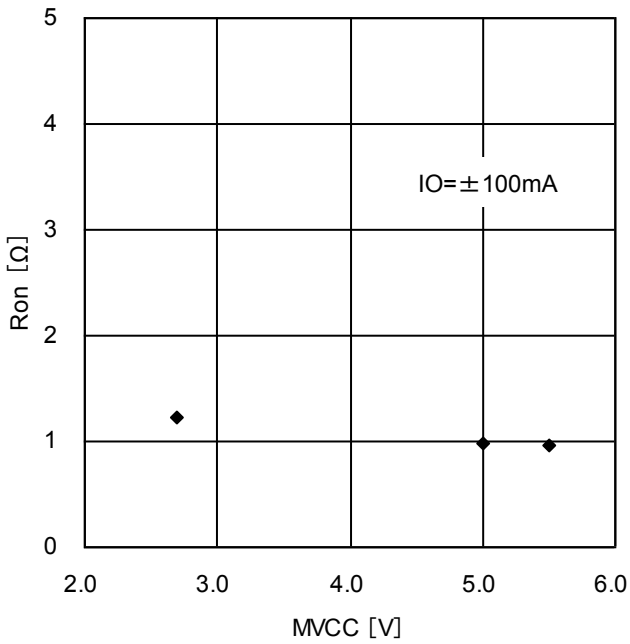


Figure 9. Output ON-Resistance  
MVCC Dependency  
(5ch,6ch driver block)

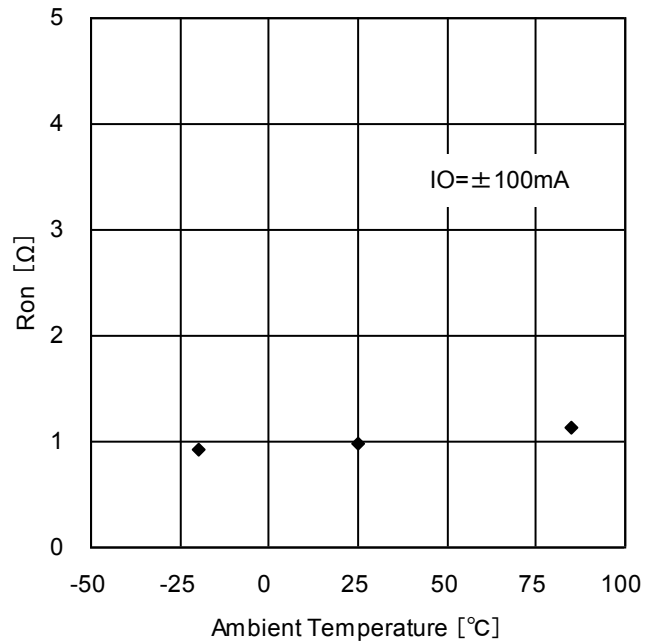


Figure 10. Output ON-Resistance  
Temperature Dependency  
(5ch,6ch driver block)

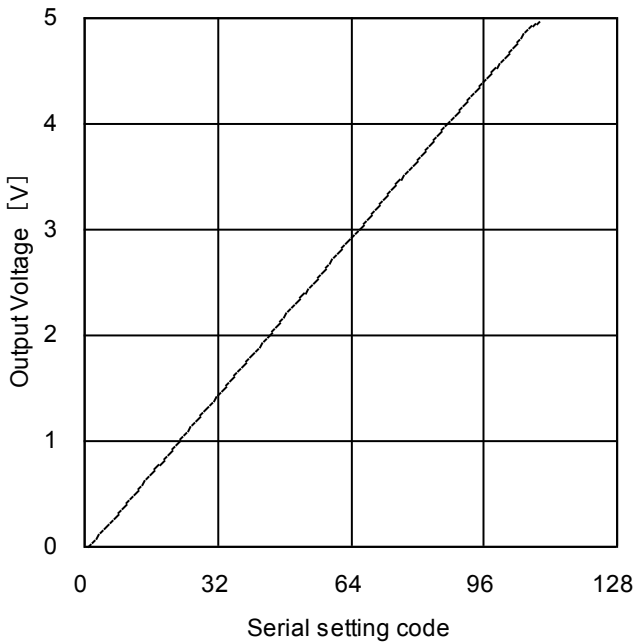


Figure 11. Average Voltage Accuracy  
between different output pins  
(Voltage driver block)

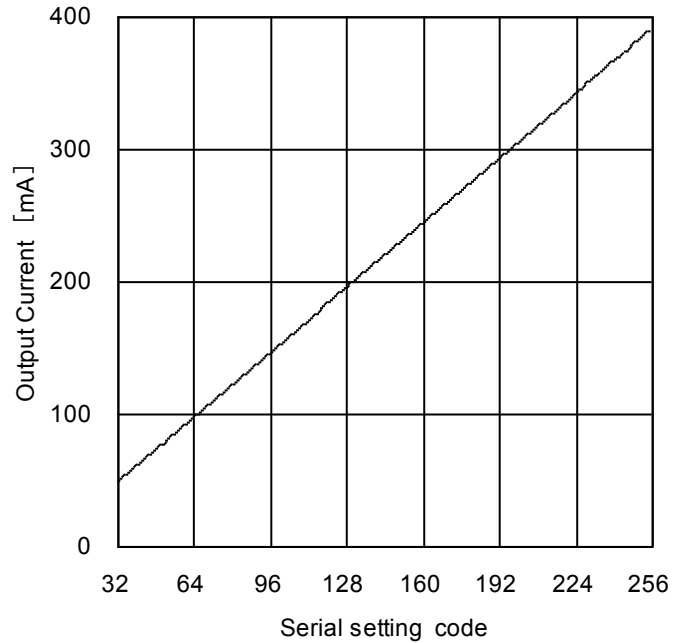


Figure 12. Output Current  
(Current driver block,  $RRNF = 1.0\ \Omega$ ,  $RL = 5.0\ \Omega$ )

● Typical Performance Curves

(Unless otherwise specified, Ta=25°C, DVDDIO=DVDD=3.0V, MVCC=5.0V, DVSS=MGND=0.0V)

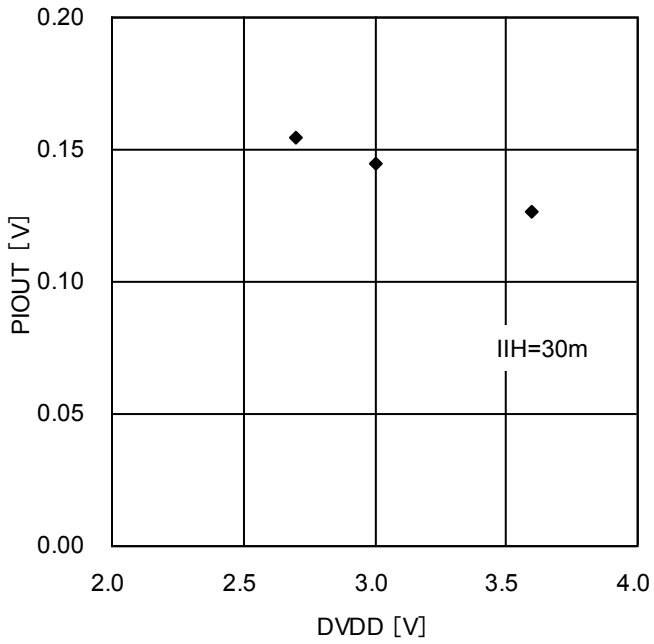


Figure 13. Output Voltage  
DVDD Dependency  
(PI driving circuit)

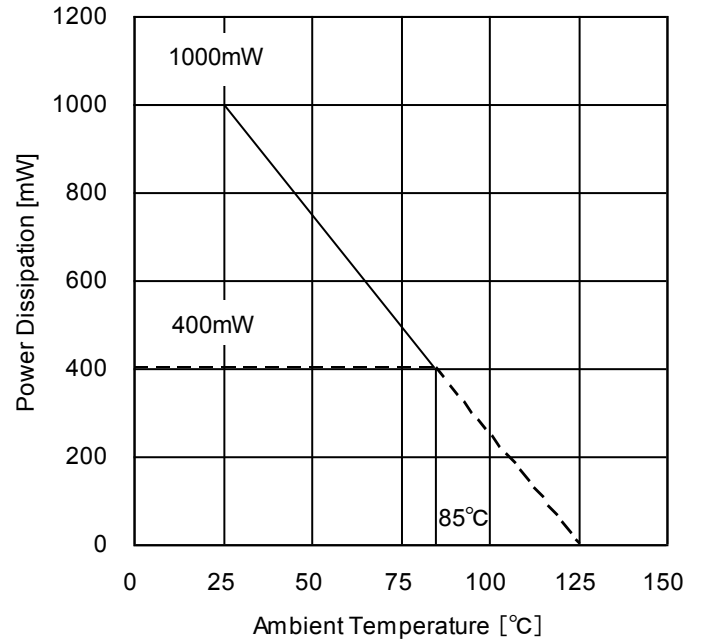
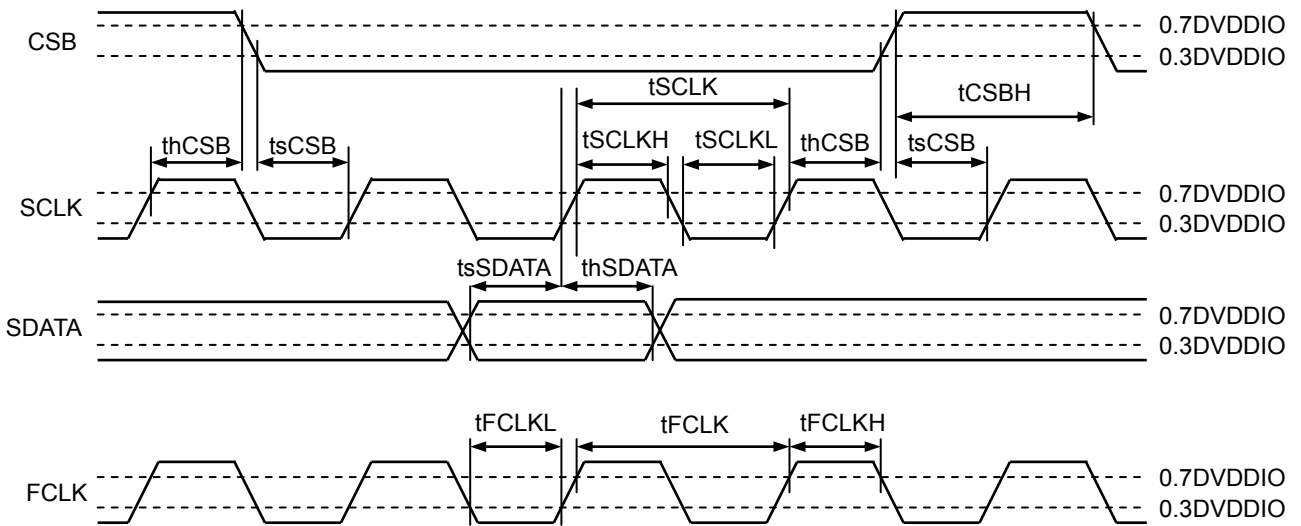


Figure 14. Power Dissipation Curve

●Timing Chart

(Unless otherwise specified, Ta=25°C, DVDDIO=DVDD=3.0V)

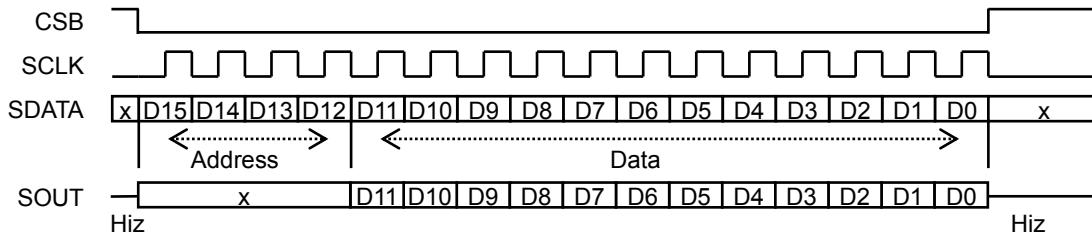
Parameter	Symbol	Specification
SCLK input cycle	tSCLK	More than 100 nsec
SCLK L-level input time	tSCLKL	More than 50 nsec
SCLK H-level input time	tSCLKH	More than 50 nsec
SDATA setup time	tsSDATA	More than 50 nsec
SDATA hold time	thSDATA	More than 50 nsec
CSB H-level input time	tCSBH	More than 380 nsec
CSB setup time	tsCSB	More than 50 nsec
CSB hold time	thCSB	More than 50 nsec
FCLK input cycle	tFCLK	More than 36 nsec
FCLK L-level input time	tFCLKL	More than 18 nsec
FCLK H-level input time	tFCLKH	More than 18 nsec



(note1) FCLK is asynchronous with SCLK.  
 (note2) Duty of FCLK, SCLK are free.

●Serial interface

Control commands are framed by a 16-bit serial input (MSB first) and are sent through CSB, SCLK, and SDATA pins. The 4 higher-order bits specify addresses, while the remaining 12 bits specify data. Data of every bit is sent through SDATA pin, which is retrieved during the rising edge of SCLK. Data becomes valid when CSB is Low and is registered during the rising edge of CSB. Furthermore, the interface will be synchronized with the falling edges of SCLK to output the SOUT data of the 12 bits.

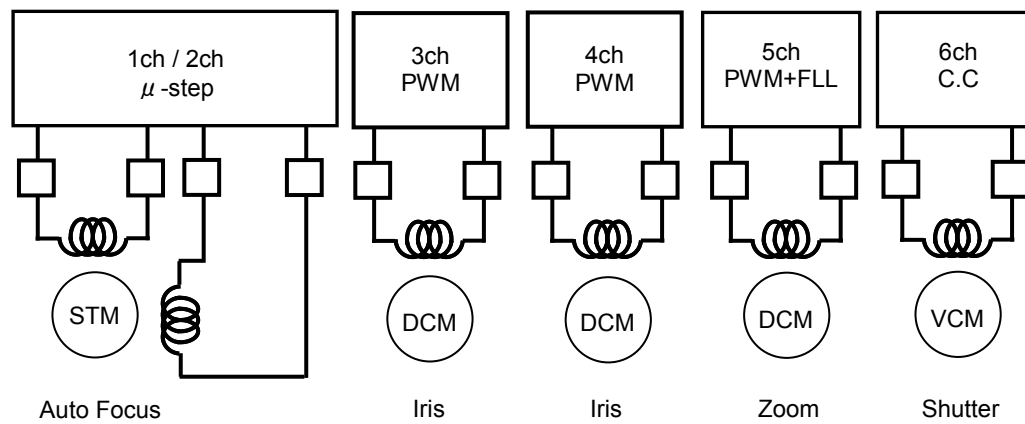
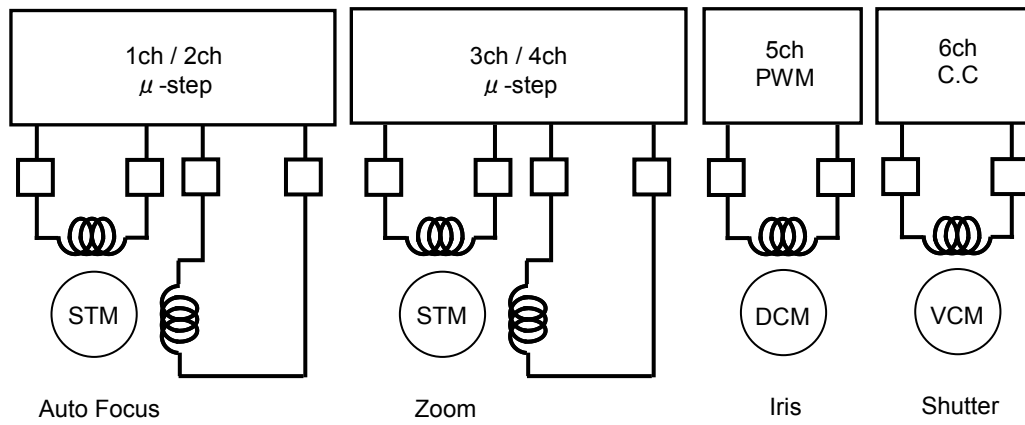
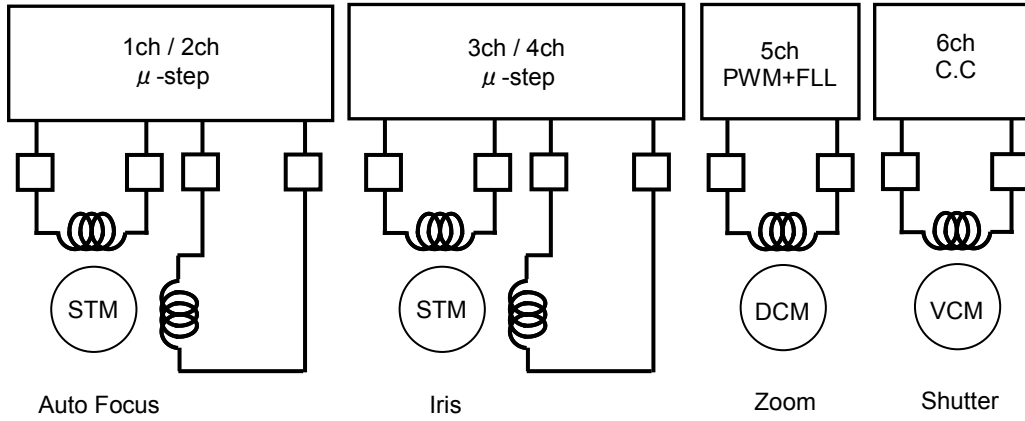


<Register map>

Address[3:0]				Data[11:0]												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	A_Mode[1:0]		A_SEL[2:0]		A_different_output_voltage[6:0]								
0	0	0	1	0	0	0	0	A_Cycle[5:0]						0	0	
				0	0	1	0	A_Cycle[13:6]								
				0	1	1	0	A_BEXC	0	0	A_BSL	A_AEXC	0	0	A_AS_L	
				1	1	1	0	0	0	A_POS[1:0]	0	0	A_PS	A_Stop		
0	0	1	0	A_EN	A_RT	A_Pulse[9:0]										
0	0	1	1	A_ACT	A_BUSY	B_ACT	B_BUSY	L	L	L	L	L	L	L	L	
0	1	0	0	B_Mode[1:0]		B_SEL[2:0]		B_different_output_voltage[6:0]								
0	1	0	1	0	0	0	0	B_Cycle[5:0]						0	0	
				0	0	1	0	B_Cycle[13:6]								
				0	1	1	0	B_BEXC	0	0	B_BSL	B_AEXC	0	0	B_AS_L	
				1	0	0	0	0	0	3_CHOP[1:0]	0	0	4_CHOP[1:0]			
				1	0	1	3_State_CTL[1:0]		3_PWM_Duty[6:0]							
				1	1	0	4_State_CTL[1:0]		4_PWM_Duty[6:0]							
0	1	1	0	B_EN	B_RT	B_Pulse[9:0]										
0	1	1	1	A_Position[9:6]				B_Position [9:6]				L	L	L	L	
1	0	1	1	0	0	0	0	0	0	Edge	0	0	0	B_CTL	A_CTL	
				0	0	1	0	0	0	0	0	0	EXT_CTL[2:0]			
1	1	0	1	0	0	Chopping[1:0]		CacheM	0	0	CLK_EN	CLK_DIV[3:0]				
				0	0	0	0	0	0	0	0	0	0	PI_CTL2	PI_CTL1	
				0	0	1	0	0	0	0	5_SPEN	0	0	5_CHOP[1:0]		
				0	1	0	5_State_CTL[1:0]		5_PWM_Duty[6:0]							
				0	1	1	0	5_TARSP[7:0]								
				0	1	1	1	0	5_PSP[2:0]			0	5_ISP[2:0]			
				1	0	0	0	0	0	0	0	0	0	SPC_Limit[1:0]		
				0	0	0	0	6_IOUT[7:0]								
1	1	1	0	0	1	0	0	0	0	0	0	0	6_State_CTL[1:0]			
				1	0	1	0	0	0	0	0	0	HYS3	HYS2	HYS1	
				1	1	0	0	0	0	0	0	STB	0	0	STM_RS	CMD_RS
Addresses other than those above				Setting prohibited												

(Note 1) The notations A B in the register map correspond to Ach and Bch respectively. Ach is defined as 1ch and 2ch driver, Bch as 3ch and 4ch driver.  
 (Note 2) After reset (Power ON reset), the initial condition is saved in all registers.  
 (Note 3) The addresses 4'b0011, and 4'b0111 have data (ACT, BUSY, Position [9:6]), which are internal register values and output from SOUT pin.  
 (Note 4) For Mode, different output voltage, Cycle, EN, and RT registers, data that are written before the access to the Pulse register becomes valid and determines the rising edge of CSB after the access to the Pulse register.  
 (The Mode, different output voltage, Cycle, EN, RT, and Pulse registers contain Cache registers. Any registers other than those do not contain Cache registers.)

●Application Example





● I/O Equivalence Circuit

Pin	Equivalent Circuit Diagram	Pin	Equivalent Circuit Diagram
FCLK CSB SCLK SDATA IN6/IN5A		TEST (note1)	
SOUT		STATE1 STATE2	
SI1 SI2 SI3/IN5B		SO1 SO2 SO3	
PIOUT1 PIOUT2		OUT1A OUT1B OUT2A OUT2B	
OUT3A OUT3B OUT4A OUT4B		OUT5A OUT5B	

(note1) Short TEST pin to DVSS.

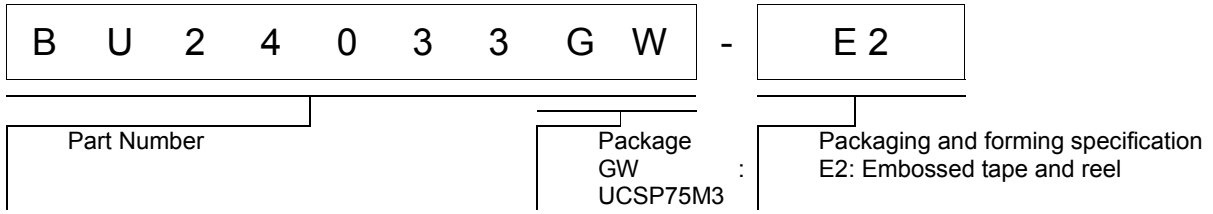
● I/O Equivalence Circuit

Pin	Equivalent Circuit Diagram
OUT6A OUT6B	<p>The diagram shows a full-bridge H-bridge circuit. At the top, there is a node labeled 'RNF6' which is connected to a ground symbol. The bridge consists of four MOSFETs: two on the left and two on the right. The gates of the top two MOSFETs are connected to a common input terminal. The gates of the bottom two MOSFETs are connected to another common input terminal. The two output nodes, labeled 'P', are connected to the midpoints of the left and right legs of the bridge. The bottom node of the bridge is connected to a ground symbol.</p>

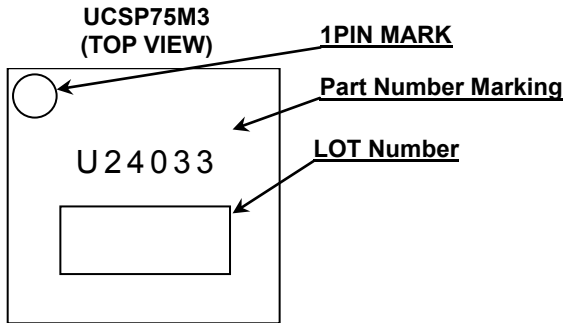
**●Operational Notes**

- 1) Absolute maximum ratings  
If applied voltage, operating temperature range, or other absolute maximum ratings are exceeded, the LSI may be damaged. Do not apply voltages or temperatures that exceed the absolute maximum ratings. If you expect that any voltage or temperature could be exceeding the absolute maximum ratings, take physical safety measures such as fuses to prevent any conditions exceeding the absolute maximum ratings from being applied to the LSI.
- 2) GND potential  
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.
- 3) Thermal design  
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (PD) in actual operating conditions.
- 4) Short circuit between pins and malfunctions  
Ensure that when mounting the IC on the PCB the direction and position are correct. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
- 5) Operation in strong magnetic field  
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- 6) Power ON sequence  
Set DVDD after the setting of DVDDIO or set it simultaneously.  
There is no restriction on the setting of MVCC.
- 7) Thermal shutdown  
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.
- 8) PI drive circuit  
The output voltage of PIOUT should not exceed the voltage of the power supply voltage DVDD.

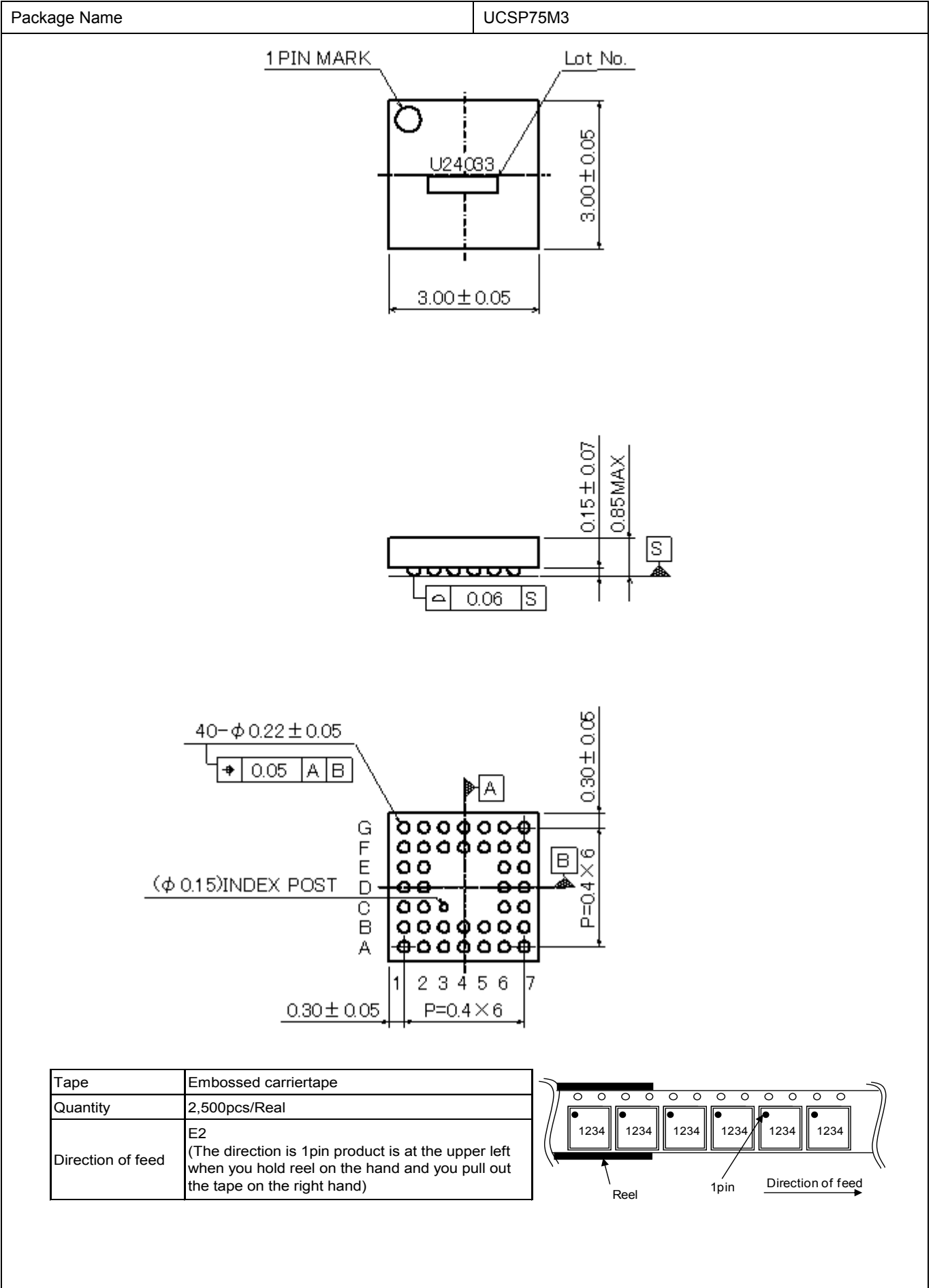
●Ordering Information



●Marking Diagram



●Physical Dimension Tape and Reel Information



## ●Revision History

Date	Revision	Changes
26.Sep.2012	001	New Release
18.Apr.2013	002	Update some English words, sentences, descriptions, grammar and formatting.
20.May.2016	003	Correct typical application circuit. Correct comments of Figure 7, Figure 8, Figure 9 and Figure 10.

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- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment <sup>(Note 1)</sup>, transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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### Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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