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24bit Audio CODEC series

3W+3W Class AB/D Speaker AMP Stereo Audio CODEC

BU26156RFS

General Description

BU26156RFS is Low Power Stereo Audio CODECs with built-in various acoustic effects. BU26156RFS has stereo line and monaural mic inputs that can input to 2Vrms, stereo speaker amplifier that can change Class AB / D and stereo Headphone Outputs.BU26156 also has built-in voltage regulator for the stability of CODEC characteristic that is sensitive to the outside noise.

Features

- 24bit Stereo ADC, DAC
- 2Vrms Input available, Stereo Line Input with ALC
- Monoraul MIC Input with ALC
- Switch Class AB/D 3W Stereo Speaker Amplifier
- AM Avoidance Function
- Stereo Headphone Output Amplifier
- Digital signal processing
- High Power Supply Rejection Ratio characteristic

Applications

- Radio cassette recorder
- PC Speaker

Important Characteristic

- Supply Voltage
  - SPLVDD,SPRVDD: 2.7V to 5.5V
  - HVDD1: 2.7V to 3.6V
  - HPVDD: 2.7V to 3.6V
  - IOVDD: 1.65V to 5.5V
- Mic-ADC SNR: 87[dB](Typ.)
- Line-ADC SNR: 93[dB](Typ.)
- DAC-SP SNR: 86[dB](Typ.)
- DAC-LOUT SNR: 95[dB](Typ.)
- Operating Temperature: -20℃ to +85℃

Package W(Typ.) x D(Typ.) x H(Max.)

HTSSOP-A44R 18.50mm x 9.50mm x 1.00mm

Figure 1. HTSSOP-A44R

Basic Block Diagram

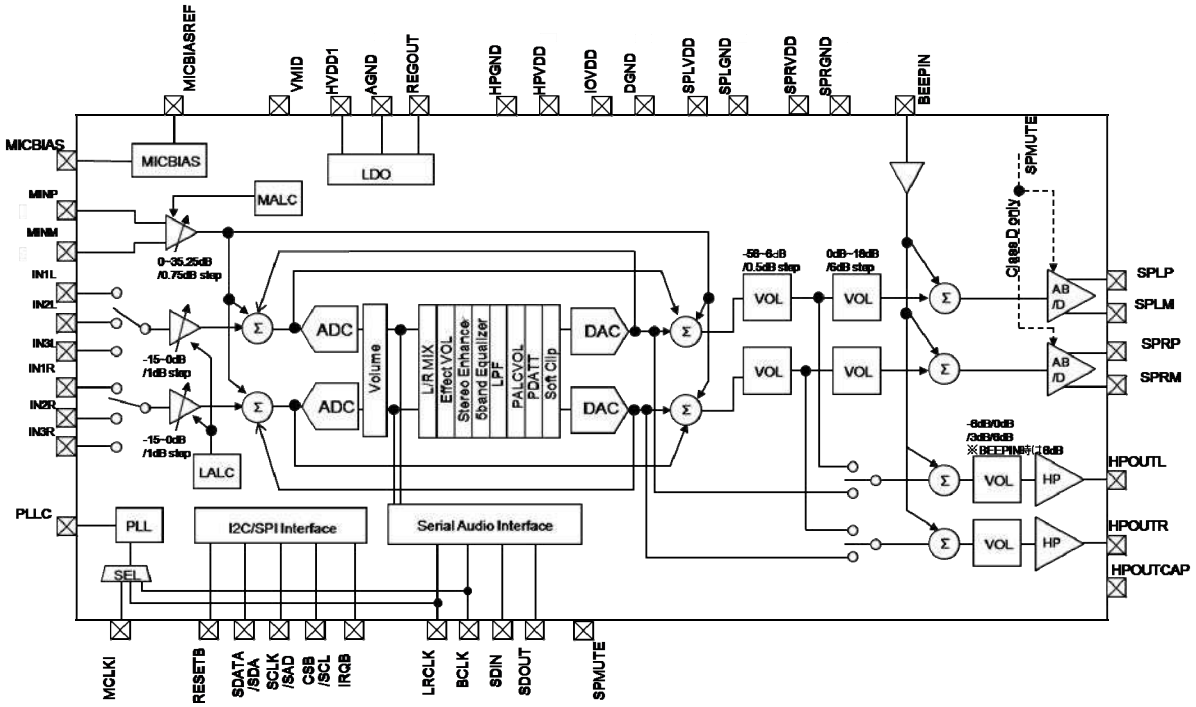


Figure 2.

Pin Layout HTSSOP-A44R

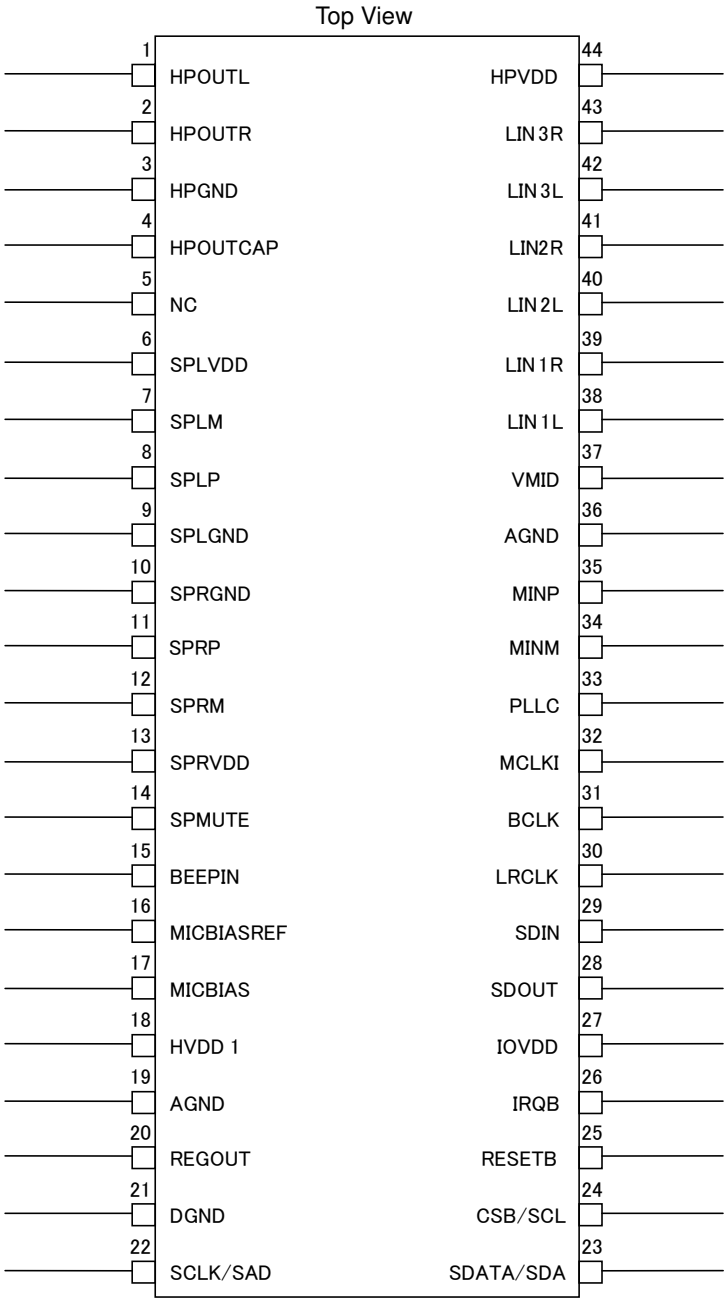


Figure 3.

Pin Description

No	Name	I/O	Power	Function	Reset	No use
25	RESETB	I	IOVDD	Reset pin “L” level : Reset enable. “H” level : Reset disable.	(input)	-
23	SDATA /SDA	IO	IOVDD	3 wire interface: data input output pin It is indicated as SDATA on the description of AC characteristics. 2 wire interface : data input output pin(Note1) It is indicated as SDA on the description of AC characteristics.	(input)	-
22	SCLK /SAD	I	IOVDD	3 wire interface : Serial clock input pin It is indicated as SCLK on the description of AC characteristics. 2 wire interface: Slave address pin Future explanation indicates SAD. Choose from the following two kinds. SAD Pin=HGND : ”0011010”	(input)	DGND

				SAD Pin=IOVDD : ”0011011”		
24	CSB /SCL	I	IOVDD	3 wire interface : chip select input pin It is indicated as CSB on the description of AC characteristics. 2 wire interface : Serial clock input pin (Note1) It is indicated as SCL on the description of AC characteristics.	(input)	-
30	LRCLK	IO	IOVDD	SAI LR clock input/output pin	(input)	DGND
31	BCLK	IO	IOVDD	SAI bit clock input/output pin	(input)	DGND
29	SDIN	I	IOVDD	SAI serial data input pin	(input)	DGND
28	SDOUT	O	IOVDD	SAI serial data output pin	DGND	Open
32	MCLKI	I	IOVDD	Master Clock pin	(input)	DGND
26	IRQB	O	IOVDD	Interrupt output Pin	IOVDD	Open
38	LIN1L	I	REGOUT	Line analog input Lch pin 1	(input)	Open, or coupling capacitor connected to AGND near by BU26156
39	LIN1R	I	REGOUT	Line analog input Rch pin 1	(input)	
40	LIN2L	I	REGOUT	Line analog input Lch pin 2	(input)	
41	LIN2R	I	REGOUT	Line analog input Rch pin 2	(input)	
42	LIN3L	I	REGOUT	Line analog input Lch pin 3	(input)	
43	LIN3R	I	REGOUT	Line analog input Rch pin 3	(input)	
35	MINP	I	REGOUT	Analog microphone + input	(input)	
34	MINM	I	REGOUT	Analog microphone - input	(input)	
15	BEEPIN	I	REGOUT	Line input pin. The input signal for this pin can output Headphone output pins or Speaker output pins.	(input)	
16	MICBIASREF	O	HVDD1	External filter pin for microphone bias. A capacitor is connected between MICBIASREF and AGND.	ANGD	Open
1	MICBIAS	O	HVDD1	Microphone bias voltage output pin A capacitor is connected between MICBIASCAP and AGND.	AGND	Open
37	VMID	O	REGOUT	Analog reference voltage pin A capacitor is connected between VMID and AGND.	AGND	-
20	REGOUT	O	HVDD1	Regulator output pin A capacitor is connected between REGOUT and HGND1. Please put in the chip close as much as possible.	AGND	-
8	SPLP	O	SPLVDD	speaker Lch output + pin	SPLGND	Open
7	SPLM	O	SPLVDD	speaker Lch output - pin	SPLGND	Open
11	SPRP	O	SPRVDD	speaker Rch output + pin	SPRGND	Open
12	SPRM	O	SPRVDD	speaker Rch output - pin	SPRGND	Open
14	SPMUTE	I	IOVDD	Test control pin “L” level : Release MUTE “H” level : MUTE	DGND	Open
1	HPOUTL	O	HPVDD	Headphone Lch output pin	HPGND	Open
2	HPOUTR	O	HPVDD	Headphone Rch output pin	HPGND	Open
32	LOUTCAP	O	HVDD1	Headphone Output capacitance pin	AGND	Open
33	PLLC	O	REGOUT	PLL filter pin The width of the clock frequency to input can be expanded.	AGND	Open
27	IOVDD	P	-	Interface Power Supply pin A capacitor is connected between IOVDD and HGND1.	-	-
6	SPLVDD	P	-	Speaker Lch Power Supply pin It is used on the same voltage as SPRVDD. A capacitor is connected between SPLVDD and SPLGND.	-	-
9	SPLGND	P	-	Speaker Lch ground pin	-	-
13	SPRVDD	P	-	Speaker Rch Power Supply pin It is used on the same voltage as SPLVDD. A capacitor is connected between SPRVDD and SPRGND.	-	-
10	SPRGND	P	-	Speaker Rch ground pin	-	-
18	HVDD1	P	-	High voltage power supply 1 pin A capacitor is connected between HVDD1 and HGND1.	-	-
19, 36	AGND	P	-	Analog ground pin	-	-
21	DGND	P		Digital ground pin		

44	HPVDD	P		Headphone Power Supply pin. A capacitor is connected between HPVDD and HPGND.		
3	HPGND	P		Headphone ground pin.		
5	NC	-		No Connection pin. Set open this pin.		Open

(Note1)In case of 2 wire serial, if this pin is used with external pull-up resistor, it possibly gets noise from power. Therefore tamper noise design is required in the noisy environment.

Application Examples

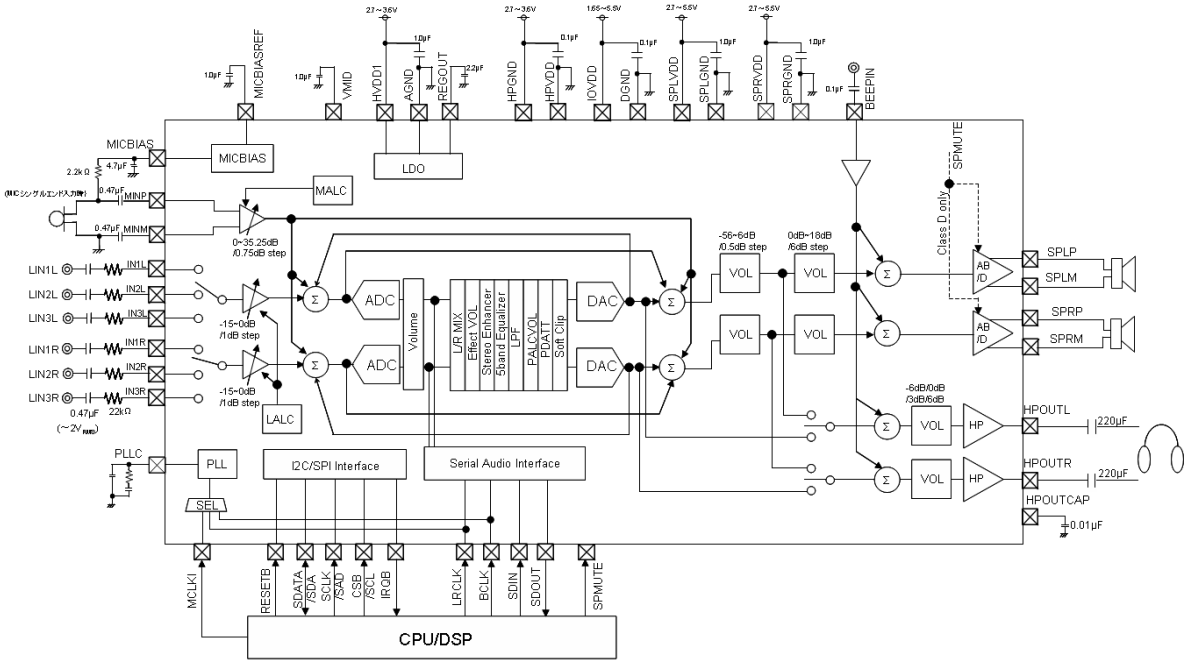


Figure 4. Application Examples1(Use internal speaker amplifier)

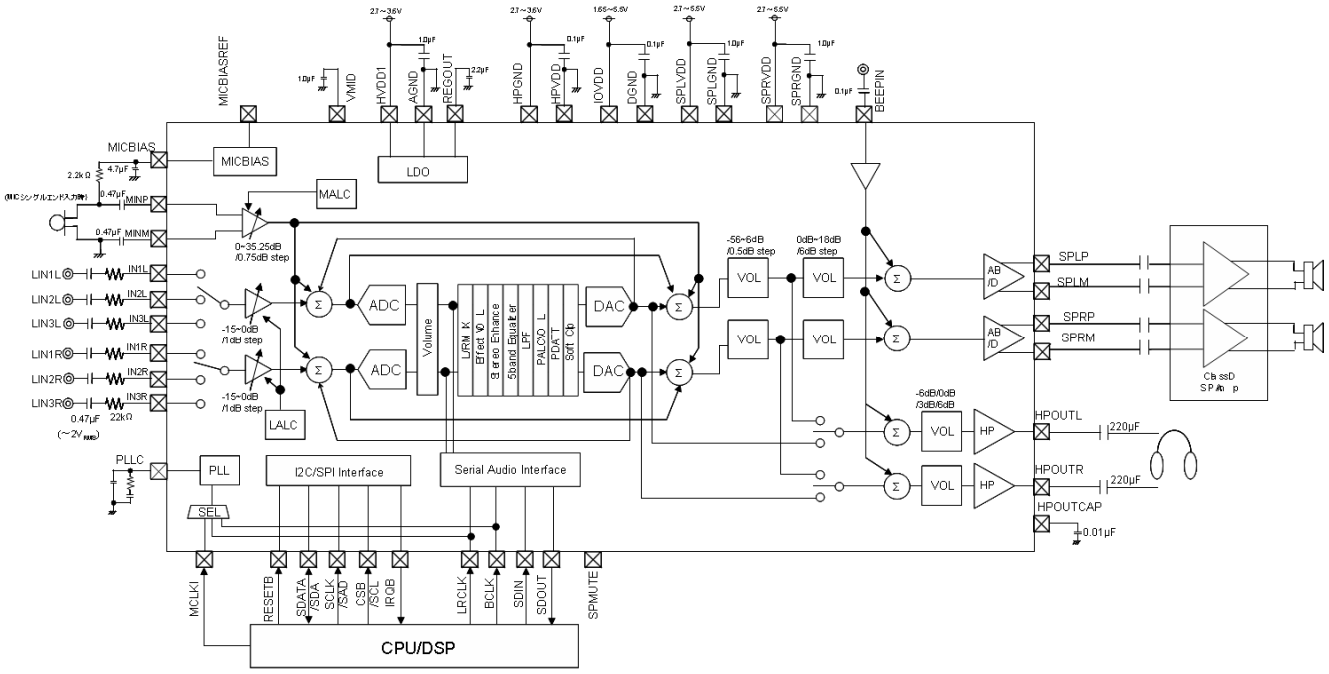


Figure 5. Application Examples2 (Use external speaker amplifier)

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
SPLVDD, SPRVDD Supply Voltage	SPLVDD SPRVDD	-	-0.3 to 7.0	V
HPVDD Supply Voltage	HPVDD	-	-0.3 to 4.5	V
HVDD1 Supply Voltage	HVDD1	-	-0.3 to 4.5	V
IOVDD Supply Voltage	IOVDD	-	-0.3 to 7.0	V
Input Voltage	V_{IN}	MCLKI, LRCLK, BCLK, SDIN, SDATA/SDA, SCLK/SAD, CSB/SCL, SPMUTE	-0.3 to IOVDD+0.3	V
		LIN1L, LIN1R, LIN2L, LIN2R, MINL, MINR, BEEPIN	-0.3 to REGOUT+0.3	V
Storage Temperature	Tstg	-	-55 to +150	°C
Package power dissipation	Θjc	HTSSOP-A44R	2 (Tjmax=+125℃)	℃/W
Output Current 1	IOSP	SPLM, SPLP, SPRM, SPRP	-1.0 to +1.0	A
Output Current 2	IOLO	HPOUTL, HPOUTR	-100 to +100	mA
Output Current 3	IOREGO	REGOUT	-30 to 0	mA
Output Current 4	IOO	All digital pins	-8 to +8	mA

Do not short the output pin to another output pin, power supply pin or GND pin.
(Output pin includes an IO pin which is in output mode)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Condition

Parameter	Symbol	Condition	Rating	Unit
SPLVDD, SPRVDD Supply Voltage	SPLVDD SPRVDD	SPLVDD=SPRVDD	2.7 to 5.5	V
HPVDD Supply Voltage	HPVDD	-	2.7 to 3.6	V
HVDD1 Supply Voltage	HVDD1	-	2.7 to 3.6	V
IOVDD Supply Voltage	IOVDD	-	1.65 to 5.5	V
Operating Temperature	Top	-	-20 to +85	°C

*The radiation-proof design is not carried out.

Electrical Characteristics

DC Characteristics

(ALL GND terminals=0V, HVDD1=3.3V, IOVDD=3.3V, SPLVDD=SPRVDD=HPVDD=3.3V, Ta=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pin
“H” Input Voltage 1	VIH1	DGND=0V	IOVDD×0.8	-	IOVDD+0.3	V	RESETB, SDATA/SDA, SCLK/SAD, CSB/SCL, SPMUTE and MCLKI pins.
“H” Input Voltage 2	VIH2	DGND=0V	IOVDD×0.7	-	IOVDD+0.3	V	LRCLK, BCLK and SDIN pins.
“L” Input Voltage	VIL	DGND=0V	-0.3	-	IOVDD×0.2	V	All Digital Input
“H” Output Voltage	VOH	IOH=-1mA	IOVDD×0.85	-	-	V	Except SDA
“L” Output Voltage 1	VOL1	IOL=1mA	-	-	IOVDD×0.15	V	Except SDA
“L” Output Voltage 2	VOL2	IOL=3mA, IOVDD ≧2V IOVDD <2V	- -	- -	0.4 IOVDD×0.2	V	SDA
“H” Input Leakage Current 1	IIH1	VIH= IOVDD	-	-	10	µA	Except SPMUTE
“L” Input Leakage Current	IIL	VIL=DGND	-10	-	-	µA	All Digital Input
“Z” Output Leakage Current	IOZH	VOH=IOVDD	-	-	10	µA	SDA
“Z” Output Leakage Current	IOZL	VOL=DGND	-10	-	-	µA	SDA
Stanby Current							
HVDD1	IDDSH1	RESETB=”L”	-	0.1	10	µA	
SPLVDD+SPRVDD	IDDSSP		-	0.1	10	µA	
HPVDD	IDDSHP		-	0.1	10	µA	
IOVDD	IDDSIO		-	0.1	10	µA	
Operating Current 1, DAC→mixvol→Headphone Output (fs48kHz, No Load, No signal input, Sound effect off)							
HVDD1	IDDO1H1	Headphone Output, No Load, No signal input, Sound effect off	-	6.2	9.5	mA	
SPLVDD+SPRVDD	IDDO1SP		-	0.02	0.1	mA	
HPVDD	IDDO1HP		-	1.0	1.3	mA	
IOVDD	IDDO1IO		-	0.03	0.1	mA	
Operating Current 2, DAC→mixvol→D-class Speaker Output (fs48kHz, No Load, No signal input, Sound effect off)							
HVDD1	IDDO2H1	D-class Speaker Output, No Load, No signal input, Sound effect off	-	6.2	8.2	mA	
SPLVDD+SPRVDD	IDDO2SP		-	3.3	7.4	mA	SPVDD=3.3V
SPLVDD+SPRVDD	IDDO2SP_5		-	5.0	-	mA	SPVDD=5V
HPVDD	IDDO2HP		-	0.03	0.1	mA	
IOVDD	IDDO2IO		-	0.03	0.1	mA	
Operating Current 3, DAC→mixvol→AB-class Speaker Output (fs48kHz, No Load, No signal input, Sound effect off)							
HVDD1	IDDO3H1	AB-class Speaker Output, No Load, No signal input, Sound effect off	-	6.2	8.2	mA	
SPLVDD+SPRVDD	IDDO3SP		-	5.0	9.6	mA	SPVDD=3.3V
SPLVDD+SPRVDD	IDDO3SP_5		-	6.0	-	mA	SPVDD=5V

HPVDD	IDDO3HP		-	0.03	0.1	mA	
IOVDD	IDDO3IO		-	0.03	0.1	mA	
Operating Current 4, MicIN→linemix→ADC (fs48kHz, Sin1kHz-Full Scale input, Micbias Enable, Mic ALC off, Sound Effect off)							
HVDD1	IDDO4H1	fs48kHz, No signal input,, Micbias Enable, Mic ALC off, Sound Effect off	-	12.3	16.9	mA	
SPLVDD+SPRVDD	IDDO4SP		-	0.02	0.1	mA	
HPVDD	IDDO4HP		-	0.03	0.1	mA	
IOVDD	IDDO4IO		-	0.03	0.1	mA	
Operating Current 5, LineIn→llinemix→ADC (fs48kHz, Sin1kHz-Full Scale input, LineALC off, Sound Effect off)							
HVDD1	IDDO5H1	fs48kHz, No signal input, Line ALC off, Sound Effect off	-	11.2	13.8	mA	
SPLVDD+SPRVDD	IDDO5SP		-	0.02	0.1	mA	
HPVDD	IDDO5HP		-	0.03	0.1	mA	
IOVDD	IDDO5IO		-	0.03	0.1	mA	

Operating Power

(ALL GND terminals=0V, IOVDD=3.3V, HVDD1=3.3V, SPLVDD=SPRVDD=5.0V, HPVDD=3.3V, Ta=25°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Regulator Output						
REGOUT Output Level	VREGOUT	-	1.7	1.8	1.9	V
BEEP Input						
Full Scale Input Signal Level	VBINFS	-	-	-	1	Vpp
Line Input (R_{LIN}=22 kΩ / Line Gain=-9dB / Digital Volume=0.0dB / Line ALC=OFF)						
Full Scale Input Signal Level	VLINFS	LIN1L, LIN2L, LIN3L, LIN1R, LIN2R, LIN3R	-	-	2.0	Vrms
Mic Input (MIC Gain=20.25dB / Digital Volume=0.0dB / Mic ALC=OFF)						
Full Scale Input Signal Level	VMINFS1	MINP,MINM	-	-	0.124	Vp-p
Input Resistance	RMIN1	MINP,MINM	20	30	40	kΩ
Mic Input (MIC Gain=9.0dB / Digital Volume=0.0dB / Mic ALC=OFF)						
Full Scale Input Signal Level	VMINFS2	MINP,MINM	-	-	0.454	Vp-p
Input Resistance	RMIN2	MINP,MINM	20	30	40	kΩ
Analog Reference Level(VMID-pin)						
Analog Reference Voltage	VREF	-	0.9x REGOUT/2	1.0x REGOUT/2	1.1x REGOUT/2	V
Microphone Bias(MICBIAS-pin)						
Output Voltage (VMIC<HVDD1*0.85)	VMIC	IMIC = -2mA, MICBCON=0	1.51x REGOUT/2	1.67x REGOUT/2	1.83x REGOUT/2	V
		IMIC = -2mA, MICBCON=1	2.00x REGOUT/2	2.22x REGOUT/2	2.44x REGOUT/2	V
		IMIC = -2mA, MICBCON=2	2.51x REGOUT/2	2.78x REGOUT/2	3.05x REGOUT/2	V
		IMIC = -2mA, MICBCON=3	3.00x REGOUT/2	3.33x REGOUT/2	3.66x REGOUT/2	V
Output Current	IMIC	-	-	-	2	mA

(HGND1=0V, IOVDD=3.3V, HVDD1=3.3V, SPLVDD=SPRVDD=5.0V, HPVDD=3.3V, Ta=25°C, 1kHz signal, fs=48kHz)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Analog Line Input to ADC out (R_{LIN}=22kΩ/ Line Gain=0dB / LineMix Gain = 0dB / Digital Volume=0.0dB / Line ALC=OFF)						
S/(N+D)	SND1	-1dBFS/ A-weighted	-	81	-	dB
S/N	SNR1	A-weighted	-	93	-	dB

Power Supply Rejection Ratio	PSRR1	HVDD1 on 100mVp-p, 1kHz ripple, no signal input	-	90	-	dB
Analog Mic Inputs to ADC out (MIC Gain=20.25dB / Line Mix Gain = 0dB / Digital Volume=0.0dB / Mic ALC=OFF)						
S/(N+D)	SND2	-1dBFS/ A-weighted	-	79	-	dB
S/N	SNR2	A-weighted	-	81	-	dB
Power Supply Rejection Ratio	PSRR2	HVDD1 on 100mVp-p, 1kHz ripple, no signal input	-	89	-	dB
Analog Mic Inputs to ADC out (MIC Gain=9.0dB / Digital Volume=0.0dB / Mic ALC=OFF)						
S/(N+D)	SND3	-1dBFS/ A-weighted	-	80	-	dB
S/N	SNR3	A-weighted	-	87	-	dB
Power Supply Rejection Ratio	PSRR3	HVDD1 on 100mVp-p, 1kHz ripple, no signal input	-	90	-	dB
DAC to Headphone OUT (HPOUTL/HPOUTR, with 220µFcuppling 16Ω load)						
Output Power	Po4	THD+N=1%, RL=16Ω	-	60	-	mW
Total Harmonic Distortion	THD4	-6dBFS input / A-weighted	-	79	-	dB
Signal to Noise Ratio	SNR4	A-weighted	-	90	-	dB
Power Supply Rejection Ratio	PSRR4	HPVDD on 100mVp-p,1kHz ripple, no signal input	-	60	-	dB
		HVDD1 on 100mVp-p,1kHz ripple	-	80	-	dB
DAC to Class-AB Speaker OUT (SPLP/SPLM, SPRP/SPRM, with 8Ω / 50pF load)						
Output Power	Po5-1	SPMIXG=12dB, RL=8Ω,THD=1%	-	1.4	-	W
	Po5-2	SPMIXG=12dB, RL=8Ω,THD=10%	-	1.7	-	W
	Po5-3	SPMIXG=12dB, RL=4Ω,THD=1%	1.5	2.5	-	W
	Po5-4	SPMIXG=12dB, RL=4Ω,THD=10%	2	3	-	W
Total Harmonic Distortion	THD5	Po=1W, RL=8Ω / A-weighted	-	62	-	dB
Signal to Noise Ratio	SNR5	A-weighted	-	91	-	dB
Power Supply Rejection Ratio	PSRR5	SPLVDD/SPRVDD on 100mVp-p,1kHz ripple	-	60	-	dB
		HVDD1 on 100mVp-p,1kHz ripple	-	80	-	dB
DAC to Class-D Speaker OUT (SPLVDD=SPRVDD=5V,SPLP/SPLM, SPRP/SPRM, with 8Ω / 50pF load)						
Output Power	Po6-1	SPMIXG=12dB, RL=8Ω,THD=1%	-	1.4	-	W
	Po6-2	SPMIXG=12dB, RL=8Ω,THD=10%	-	1.7	-	W
	Po6-3	SPMIXG=12dB, RL=4Ω,THD=1%	1.5	2.5	-	W
	Po6-4	SPMIXG=12dB, RL=4Ω,THD=10%	2	3	-	W
Total Harmonic Distortion	THD6	Po=1W, RL=8Ω / A-weighted	-	62	-	dB
Signal to Noise Ratio	SNR6	A-weighted	-	89	-	dB
Power Supply Rejection Ratio	PSRR6	SPLVDD/SPRVDD on 100mVp-p,1kHz ripple	-	72	-	dB
		HVDD1 on 100mVp-p,1kHz ripple	-	80	-	dB
Class D oscillator frequency (AM Avoidance)						
Oscillator frequency	AM0	AMA[1:0]=0b00	360	400	440	kHz
	AM1	AMA[1:0]=0b01	450	500	550	kHz
	AM2	AMA[1:0]=0b10	540	600	660	kHz

	AM3	AMA[1:0]=0b11	630	700	770	kHz
Microphone Bias (MICBIAS-pin)						
Output Noise Voltage	VMICN7	22Hz to 22kHz, VMIC =1.67 x REGOUT/2	-	5	-	µV
Power Supply Rejection Ratio	PSRR7	HVDD1 on 100mVp-p,1kHz ripple Load=1mA	-	80	-	dB

AC Characteristics

Clock
PLL not use

(DGND=0V, IOVDD=3.3V, HVDD1=3.3V,Ta=25°C)

Parameter	Symbol	Min	Max.	Unit
MCLKI Frequency	fC	2.048M	49.152M	Hz
MCLKI Period	tC	1/fC	1/fC	s
MCLKI Length	tCH	tC*0.4	-	s
MCLKI Length	tCL	tC*0.4	-	s

PLL use (External Loop back filter not used)

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C)

Parameter	Symbol	Min	Max.	Unit
MCLKI Frequency	fC	2M	54M	Hz
MCLKI Period	tC	1/fC	1/fC	s
MCLKI Length	tCH	tC*0.4	-	s
MCLKI Length	tCL	tC*0.4	-	s

PLL use (External Loop back filter used)

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C)

Parameter	Symbol	Min	Max.	Unit
MCLKI Frequency	fC	32k	2M	Hz
MCLKI Period	tC	1/fC	1/fC	s
MCLKI Length	tCH	tC*0.4	-	s
MCLKI Length	tCL	tC*0.4	-	s

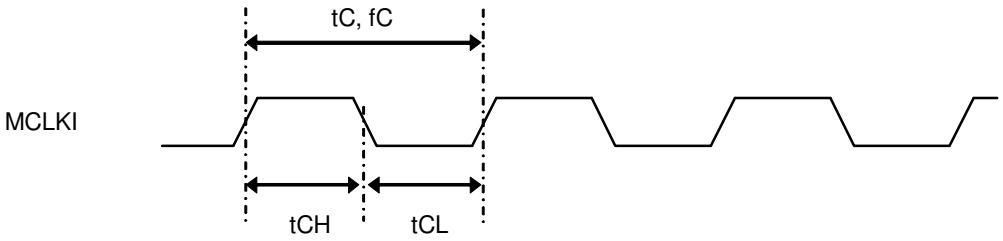


Figure 6.

Reset

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C)

Parameter	Symbol	Min	Max.	Unit
RESETB pulse width	tW_RST	5	-	µs

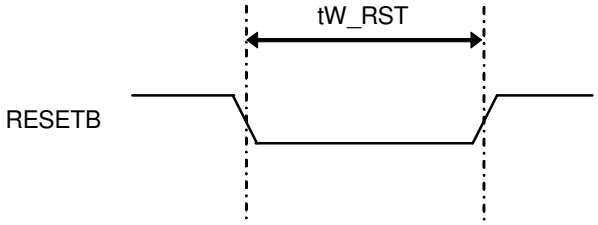


Figure 7.

When Reset pin is made Low level, internal LDO is power down mode.
It is necessary for 1ms until REGOUT pin becomes Low level. The recommendation of tW_RST is 1ms over.

2 wire serial interface

(DGND =0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C, CL=30pF)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max.	Min	Max.	
SCL Frequency	f_{SCL}	-	100	-	400	kHz
SCL “L” Length	t_{LOW}	4.7	-	1.3	-	µs
SCL “H” Length	t_{HIGH}	4.0	-	0.6	-	µs
Hold time under Repeat [Start] Condition	$t_{HD:STA}$	4.0	-	0.6	-	µs
Setup Time under Repeat[Start] Condition	$t_{SU:STA}$	4.0	-	0.6	-	µs
Data Hold Time	$t_{HD:DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU:DAT}$	250	-	100	-	ns
Setup Time under [Stop] Condition	$t_{SU:STO}$	4.0	-	0.6	-	µs

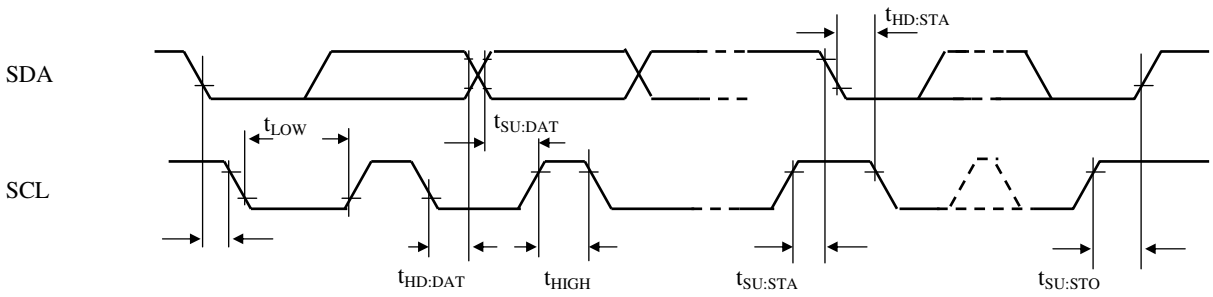


Figure 8.

3 wire serial interface

(DGND=0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C, CL=30pF)

Parameter	Symbol	Min	Max.	Unit
SCLK Low to Chip Select enable	tSLCL	100	-	ns
Chip Select enable to SCLK Low	tCLSL	100	-	ns
Chip Select enable to SCLK High	tCLSH	100	-	ns
SCLK High to Chip Select enable	tSHCL	100	-	ns
SCLK High Pulse Width	tSH	50	-	ns
SCLK Low Pulse Width	tSL	50	-	ns
Input Data Setup time	tIDS	30	-	ns
Input Data Hold time	tIDH	30	-	ns
SCLK last edge to Chip Select disable	tCHS2	100	-	ns
Chip Select High Pulse Width	tCH	100	-	ns
Output Data Valid	tODV	-	40	ns
Chip Select High to Data Transition	tCHDTS	-	40	ns

Two kinds of timing is supported depends on the SCLK pin level at data transfer start. Read or Write is selected by LSB level of INDEX.

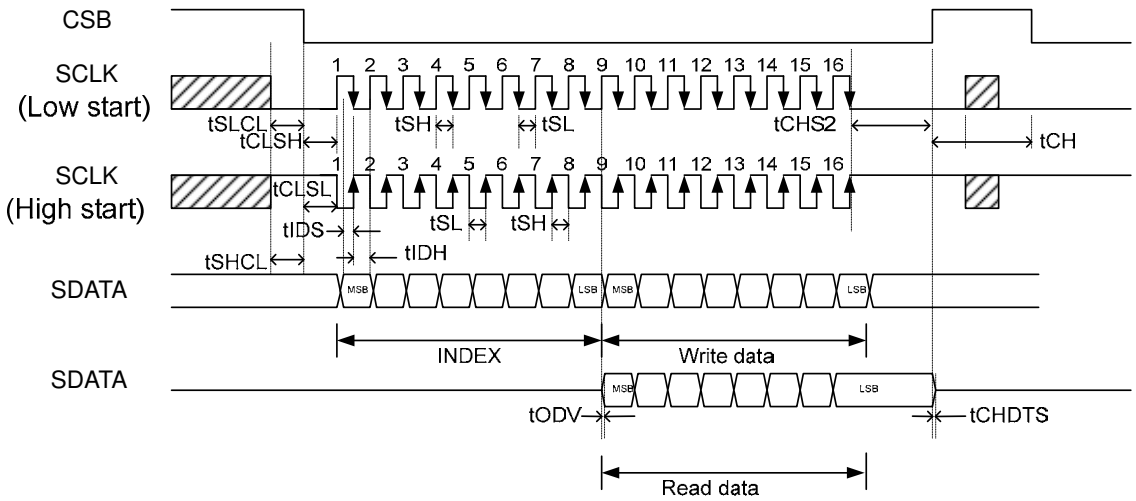


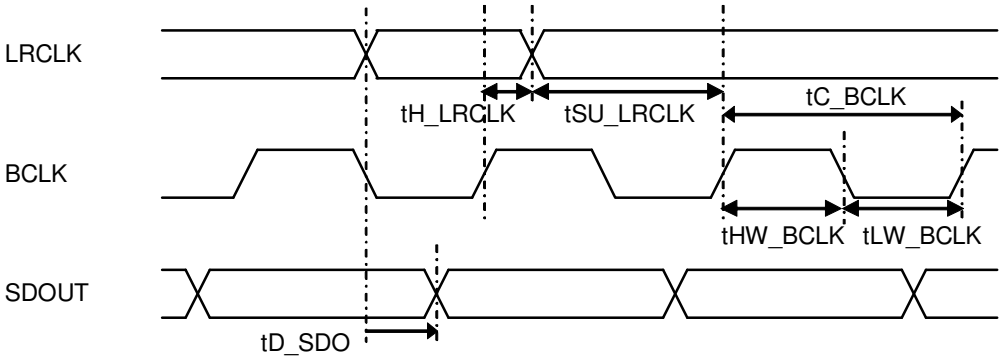
Figure 9.

Serial Audio Interface (Slave)

(DGND=0V, IOVDD=3.3V, HVDD1=3.3V, Ta=25°C, CL=30pF)

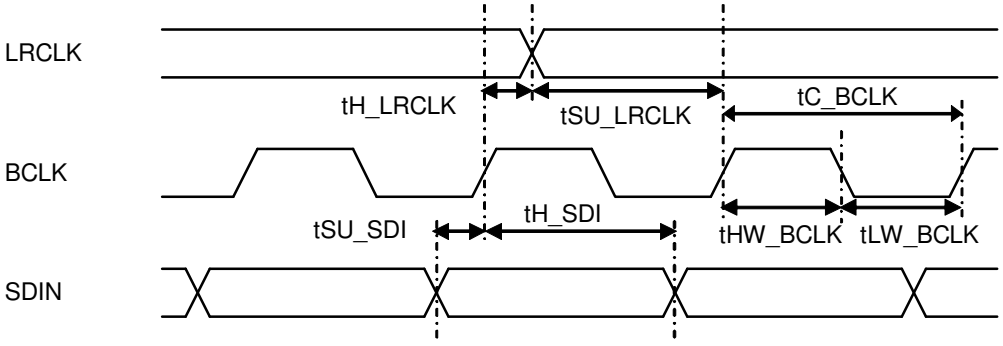
Parameter	Symbol	Min	Max.	Unit
SAI_BCLK Period	tC_BCLK	32fs	128fs	Hz
SAI_BCLK “H” Length	tHW_BCLK	73	-	ns
SAI_BCLK “L” Length	tLW_BCLK	73	-	ns
SAI_LRCLK Hold Time	tH_LRCLK	20	-	ns
SAI_LRCLK Setup Time	tSU_LRCLK	20	-	ns
SAI_SDOUT Delay Time	tD_SDO (Note1)	-	80	ns
SAI_SDIN Setup Time	tSU_SDI	20	-	ns
SAI_SDIN Hold Time	tH_SDI	20	-	ns

(Note1) tD_SDO is the delay time from later one of SAI_BCLK transition and SAI_LRCLK transition.



SAI Transmit

Figure 10.



SAI Receive

Figure 11.

Power Supply Sequence

Please power on/off the LSI with all kind of power at the same time.
Each power supply should power up/down in 50ms.Also keep all power supply in the ON state or the OFF state.
Please avoid partial ON or partial OFF states.Don't have to keep the sequence of power on/off

Please keep RESETB pin "L" level until all power supply become ON state. The CPU I/F available when all power supply are powered on, exceed tW_PURST, RESET are disabled and exceed $tW_{\_REGU}$. It is regardless that turn of power on and off of IOVDD and HVDD.

Parameter	Symbol	Min	Typ	Max	Unit
Power On Delay Time	t_{VDD_ON}	0	-	50	ms
Power Down Delay Time	t_{VDD_OFF}	0	-	50	ms
Reset Time after Power ON	t_{w_PURST}	1	-	-	μs
Wait time for Regulator starting after reset release	t_{w_REGU}	1	-	-	ms

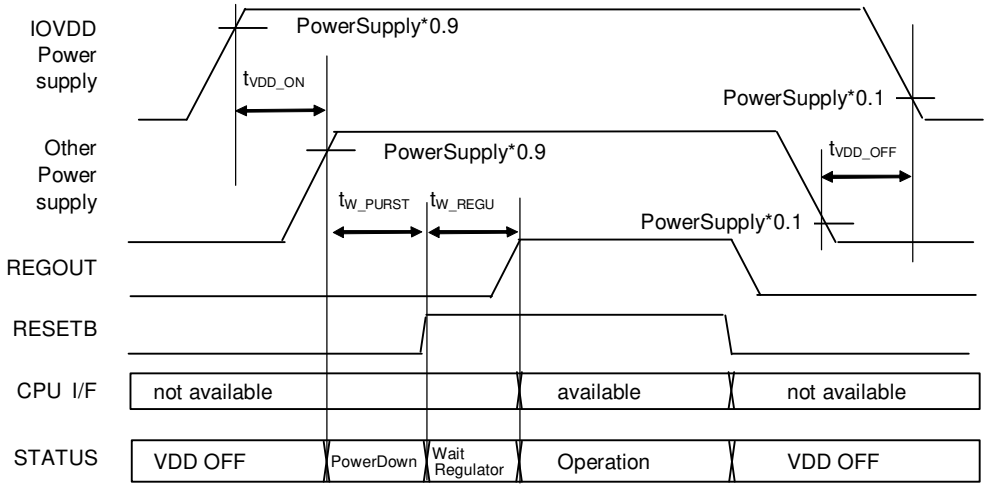


Figure 12.

Function Description

Clock control

Main modules that make up sound path of the LSI inside operate with 256fs Audio Clock.
Audio Clock can be selected whether divided clock of 256fs/512fs/1024fs from MCLKI or generated clock from Audio PLL.
In case of used external loop filter of PLL, input clock must be 2MHz to 54MHz frequency. In case of not used external filter of PLL, input clock must be 32 kHz to 2MHz frequency. It is possible to select internal clock either MCLKI port or LRCLK port or BCLK port.
Internal Clock is selected Clock Input/Output Control Register. These frequency mean 512fs and master clock is divided by 2 from PLL output when sampling frequency is 16 kHz to 24 kHz, and these frequency mean 1024fs and master clock is divided by 4 from PLL output when sampling frequency is 8 kHz to 12 kHz.

・・PLL condition setting (changing) sequence
1. Stop PLL output by setting PLLOE bit to “0”
2. Disable PLL by setting PLLEN bit to “0”
3. Set FPLLM, FPPNL, FPLLNH, FPLLD, FPLLFL, FPLLFH, FPLLFDL, FPLLFDH
4. Set PLLEN bit to “1”
5. Wait for the PLL stabilizing time as the table “PLL Stabilizing Time”
6. Set PLLOE bit to “1”
7. Start recording or playback.

PLL Stabilizing Time

PLL Stabilizing Time
10msec

- Related Register
Sampling Rate Setting Register
FPLLM, FPPNL, FPLLNH, FPLLD, FPLLFL, FPLLFH, FPLLFDL, FPLLFDH Register
Clock Enable Register
Clock Input/Output Control Register

When pll is used.
The LSI support audio PLL function that can generate precise audio clock from wide range of clock frequency. Then, it can be realize audio function without external clock generator for audio. The LSI supports following cases.

■ case 1: PLLISEL=0 or 2, MST=0, MCLKOE=0
Audio PLL generate system clock as 256fs from LRCLK

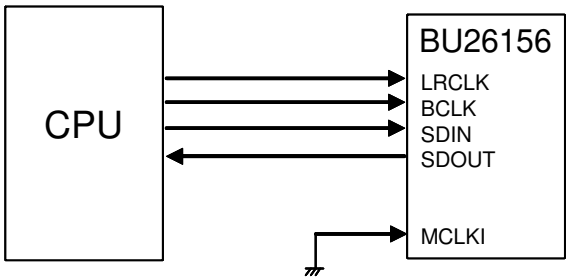


Figure 13.

When PLL is not used.
Please generate Audio clock on the CPU and supply to the LSI when PLL is not used. Then CPU and the LSI are synchronized.

■case 2: MST="0", MCLKOE="0"
Audio Clock is generated by the CPU and supplied to MCLKI pin of the LSI. LRCLK and BCLK are also provided from the CPU.

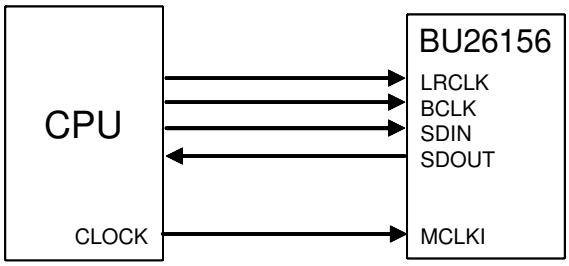


Figure 14.

Serial Audio Interface

The LSI supports SAI formats.

WSLI="0", DLYI="0", FMTI="0"

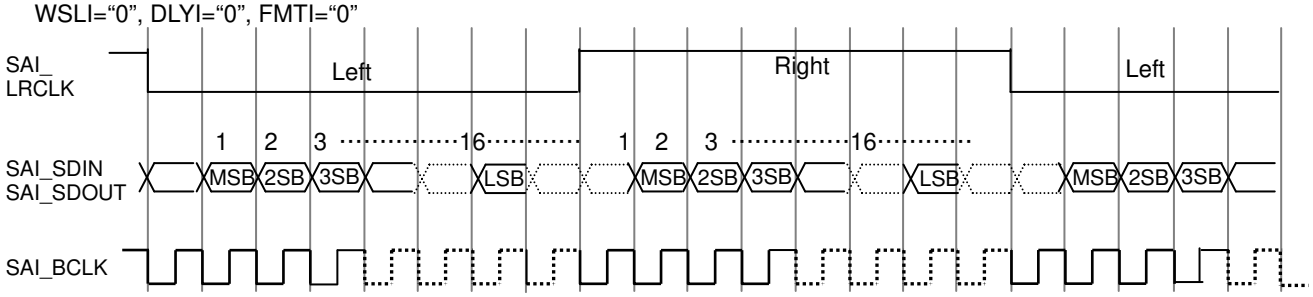


Figure 15.

WSLI="1", DLYI="0", FMTI="0"

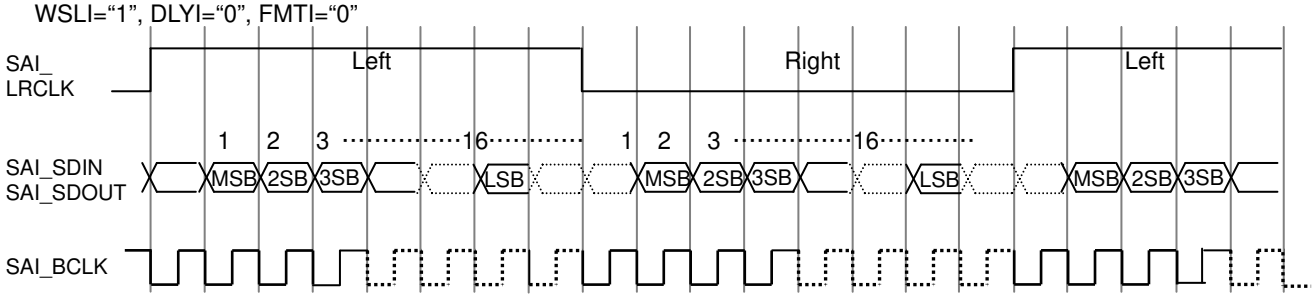


Figure 16.

WSLI="0", DLYI="1", FMTI="0"

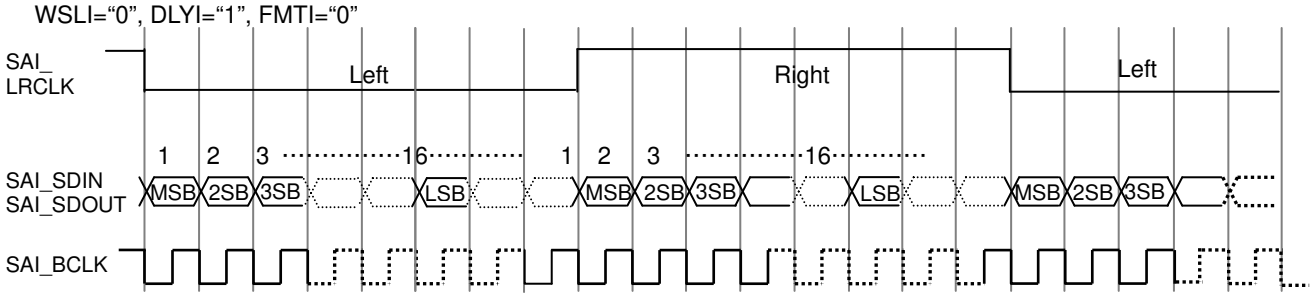


Figure 17.

WSLI="1", DLYI="1", FMTI="0"

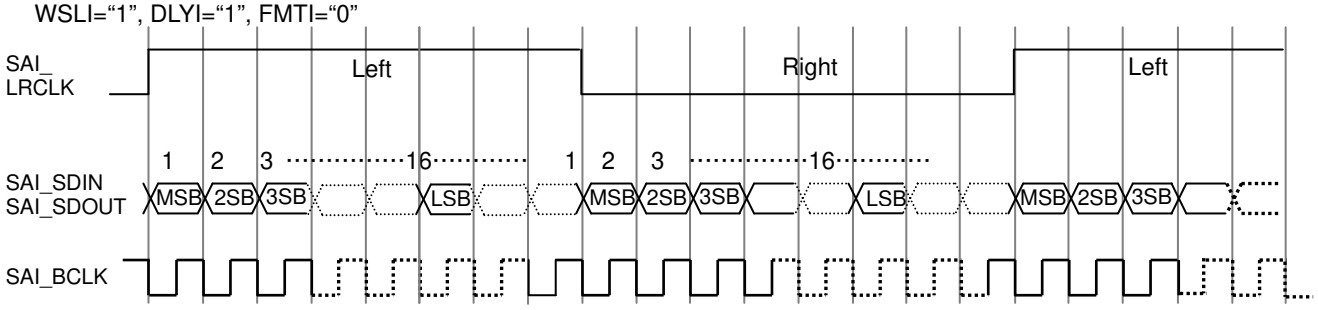


Figure 18.

DLYI="0", FMTI="1"
Flame synchronous transfer mode: R channel data is transferred right after L channel data.

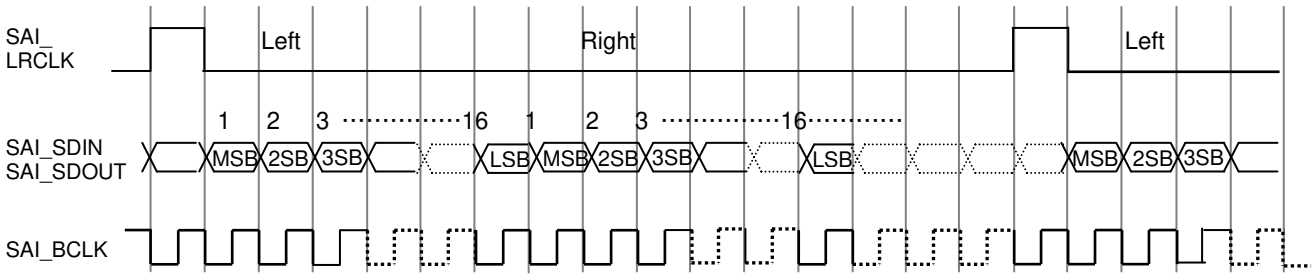


Figure 19.

DLYI="1", FMTI="1"
Flame synchronous transfer mode: R channel data is transferred right after L channel data.

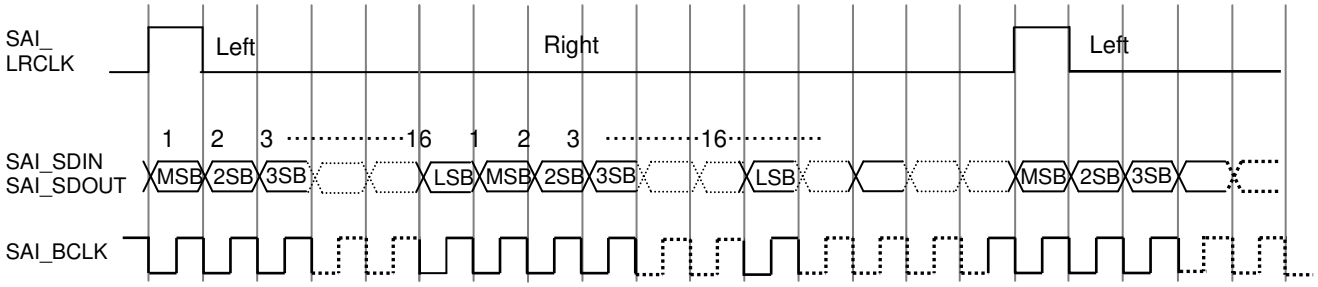


Figure 20.

- Related Register
SAI Transmitter Control Register
SAI Receiver Control Register

2 wire serial interface

This LSI has 2 wire serial interfaces. The LSI operates as a slave device. The address is fixed at “0011010”.

- Format

The followings are the protocol of the LSI.
Write (MSB first)
Start Condition (Set SDA level from “H” to “L” during SCL=“H”)
Slave Address (0011010) +W (0) (8bit)
Write Address (8bit)
Write Data (8bit)
…
Stop Condition (Set SDA level from “L” to “H” during SCL=“H”)

Read (MSB first)
Start Condition
Slave Address (0011010) +W (0) (8bit)
Read Address (8bit)
(Stop Condition) Start Condition
Slave Address (0011010) +R (1) (8bit)
Read Data (8bit)

The following shows the wave form of the LSI.
The yellow gridding shows that slave device drives the bus.
The symbol in the wave form means as following table.

Unit	Description
W/R	0: Write 1: Read
A	0: ACK(Acknowledge) 1: NAK(Not Acknowledge)
A[7-0]	Address (8bit)
D[7-0]	Data(8bit)

Write

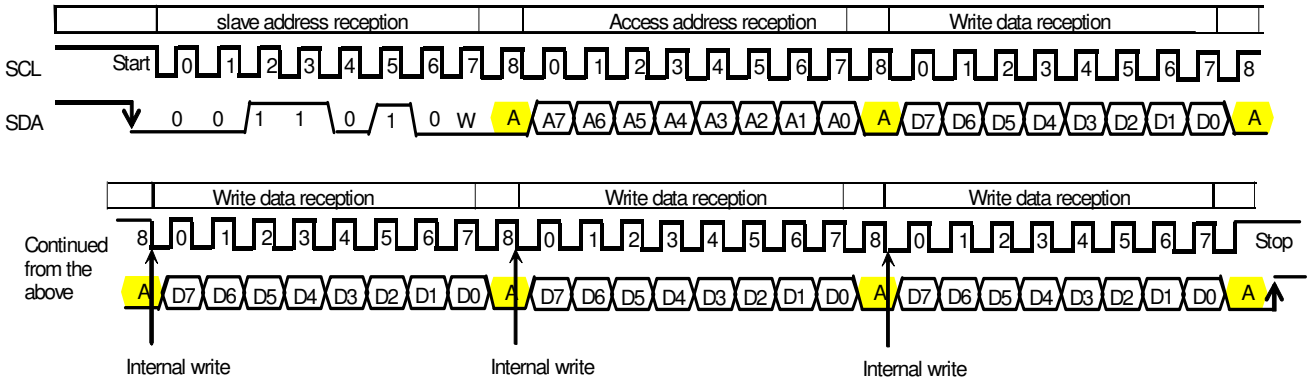


Figure 21.

In case there is no Stop or Start condition after internal register is written (Above figure: Internal Write), the slave device becomes continuous write mode and the next received 8 bits of data will be written into the internal register addressed by incremented by two to the current address.

Read

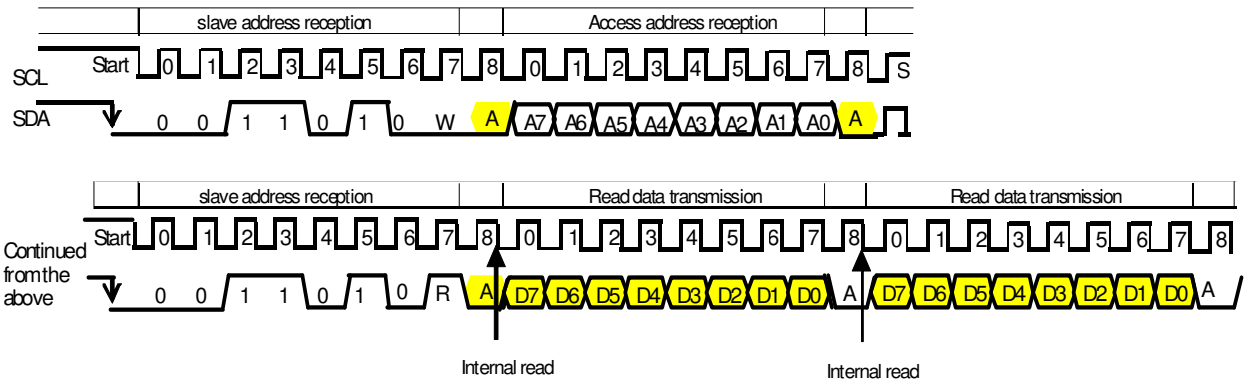


Figure 22.

If the Master device returns ACK (acknowledge) after the 8 bit data transferred from the LSI becomes continuous read mode. The next received 8 bits of data will be read from the internal register addressed by incremented by two to the current address.

Analog Block Gain Diagram

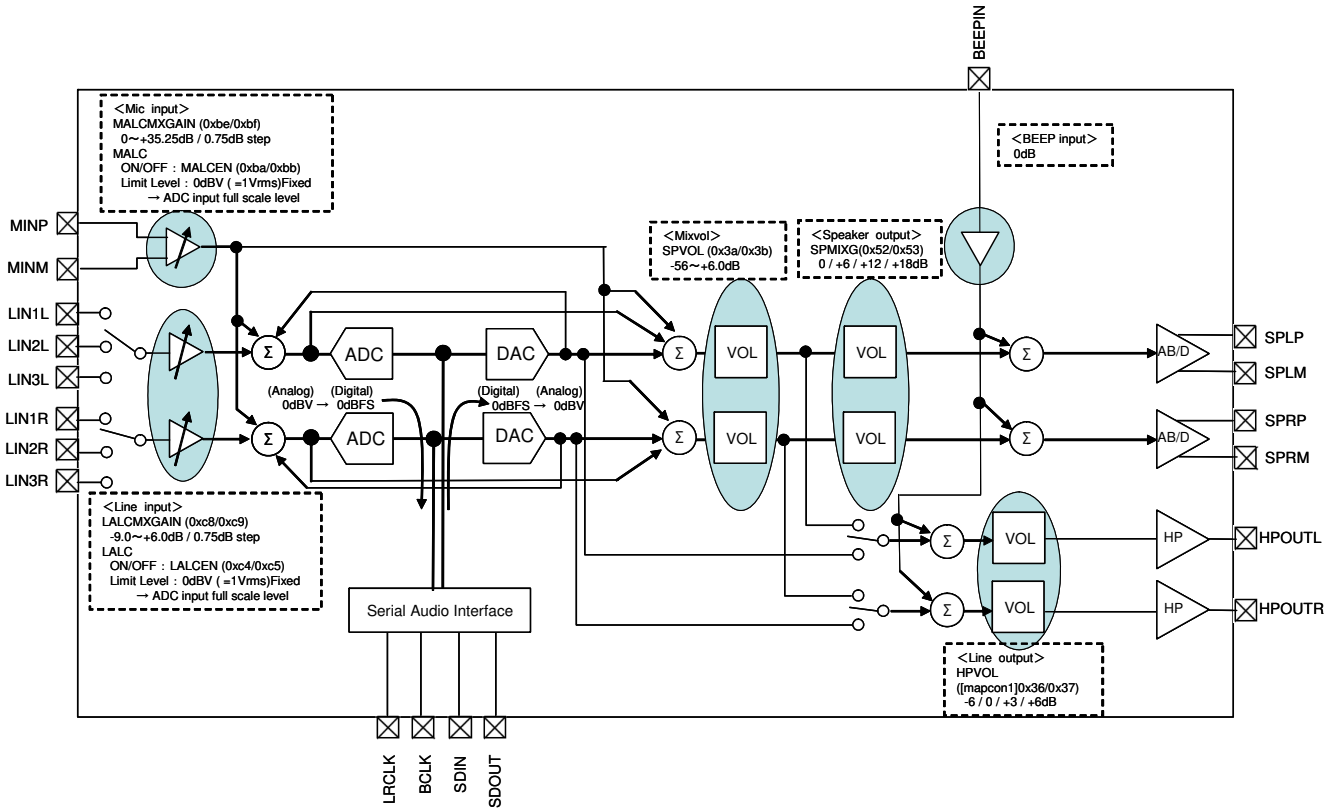


Figure 23.

State transition regarding SAI input and output control.

The following shows state transition about sound control. A change state is carried out by RECPLAY bit setup.

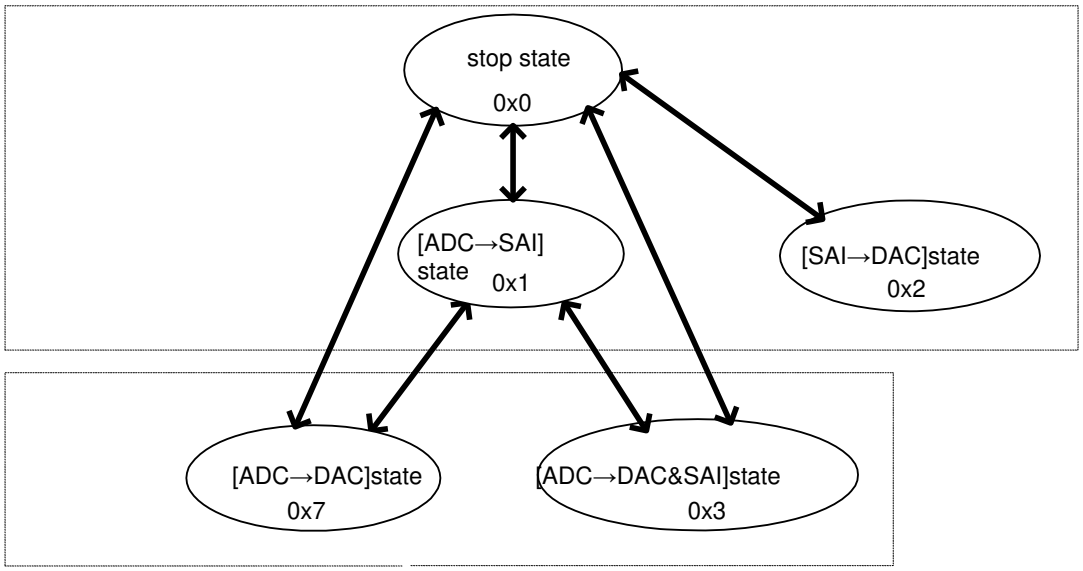


Figure 24.

(1) Stop STATE (RECPLAY=0x0)
Sound activity is stopped.
(2) [ADC→SAI] STATE (RECPLAY =0x1)
Analog input signal (MIC input/LINE input) is converted to digital data and outputted from SAI terminals.
(3) [SAI→DAC] STATE (RECPLAY =0x2)
Digital signal from SAI is converted to analog data and it is outputted from speaker or line amplifier.
(4) [ADC→DAC] STATE (RECPLAY =0x7)
Analog input signal (MIC input/LINE input) is converted to digital data and outputed speaker or line amplifier through DAC.
(5) [ADC→DAC & SAI] STATE (RECPLAY =0x3)
Analog input signal (MIC input/LINE input) is converted to digital data and outputed from SAI terminals.
At one time, digital signal inputted from SAI is converted to analog data and it is outputted from speaker or line amplifier.
Set this state for using SDIN to SDOUT path when LINDACEN bit enable.

*Please don't use "DAC output to LIMIX path" with path (4) and path (5).

Signal Flow

ADC used signal flow

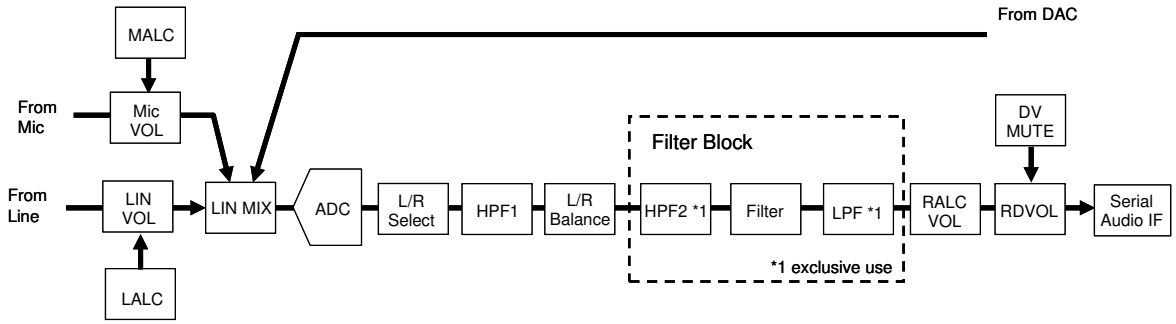


Figure 25.

Name	Function	Related Register	Setting
Mic ALC MICVOL	Analog Microphone volume and ALC	MIC ALC Control MIC ALC Max Gain Analog Input Power Management	0dB to +35.25dB, 0.75dB step
LineIN ALC LINVOL	Analog line input volume and ALC	Line ALC Control Line ALC Max Gain Analog Input Power Management	-15 to +0dB, 1dB step
LIN MIX	Mixing the LINE input, MIC input and outputted signal from DAC	Line In Control Analog Path Control	Analog input control.from Mic, Line and DAC. Mixing control
ADC	24bit AD Converter	Analog Input Power Management	ADC Enable/Disable
L/R Select	ADC(Lch/Rch) to Audio Bass	[I2SL / I2SR / MONOREC] Record L/R Balance Volume Control	-6.0dB to 6.0dB(0.1step)
HPF1	High path filter for DC cut	DSP Filter Function Enable	HPF Enable/Disable
L/R Balance	L/R balance volume control	[RBVOLL / RBVOLR] Record L/R Balance Volume Control	-6.0dB to 6.0dB(0.1step)
HPF2	High pass filter for ADC	DSP Filter Function Enable High Pass Filter2 Cut-off Control	HPF Enable/DIsable setting order setting Cut-off frequency setting
Filter	Sound filters setting	Sound Effect Mode DSP Filter Function Enable EQ Band N Gain Setting Programmable EQ Band N Coeffeicient-a0/1	Sound effect mode setting. Each filters Enable/Disable. Each filter gain settings. Each sound effects characteristics setting
LPF	Programmable LPF setting for ADC	Rec Programmable LPF Setting Rec Programmable LPF Cutoff Coef	LPF Enable/DIsable setting Order setting. Cut-off frequency setting
RALCVOL	Digital Boost Volume for ADC	Recording Digital Boost Volume Register	-12.000d to 35.625dB(0.375Step)
RDVOL	Digital attenuator and fader for ADC	Record Digital Attenuator Control Digital Volume Control Function Enable Mixer & Volume Control	Volume setting -71.5dB to 0dB (0.5dBstep) Fader enable/disenable setting (working together DVMUTE)

*Filter Block can be used for either ADC path or DAC path.
For example, if Filter Block is connected to DAC, ADC is not effected by filter.
Regarding the detail of register setting, please refer to selection of [SEMODE] register.

DAC used singal frow

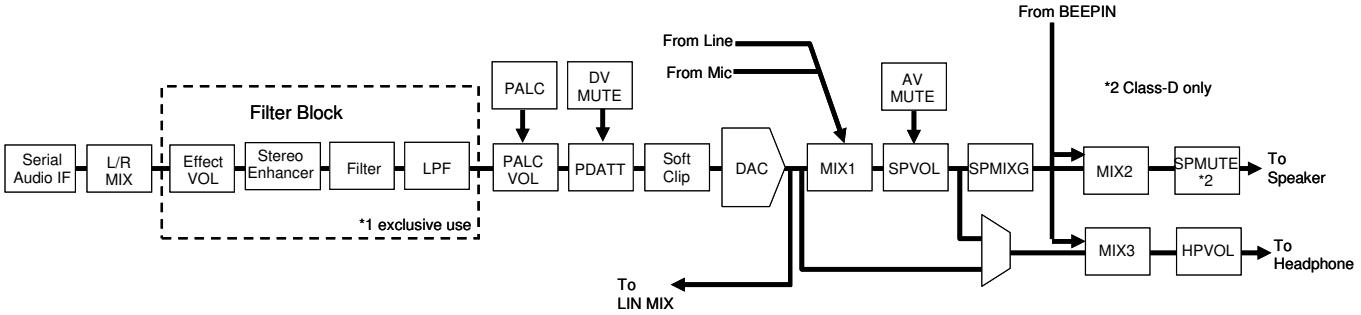


Figure 26.

Name	Function	Related Register	Setting
L/R MIX	Lch/Rch mixer for SAI input signal	Mixer & Volume Control	Mixer setting
Effect Vol	Digital volume in front of sound effect blocks.	Playback Effect Volume	-71.5dB to 0dB (0.5dBstep)
Stereo Enhancer	Stereo enhancer.	Stereo Gain	3D effect
Filter	Each sound filters are enabled.	Sound Effect Mode DSP Filter Function Enable EQ Band N Gain Setting Programmable EQ Band N Coeffeicient-a0/1	Sound effect mode setting. Each filters Enable/Disable Each filters gain setting Each sound effects characteristics setting
LPF	Programmable LPF for DAC path.	Play Programmable LPF Setting Play Programmable LPF Cutoff Coef	HPF Enable/Disable setting Order setting Cut-off frequency setting
PALC PALCVOL	Digital Playback ALC and Volume	Playback ALC Attack Time Control Playback ALC Decay Time Control Playback Target Level Control Playback ALC Min Gain Control Playback ALC Volume Control Playback ALC Zerocross Timeout Playback Limiter Fast Release Setting	ALC operation settings
PDATT	Digital Attenuator for DAC path. Fader for noise reduction at changing the digital volume	Playback Digital Attenuator Control Digital Volume Control Function Enable Mixer & Volume Control	Volume setting -71.5dB to 0.5dB (0.5dBstep) Fader ON/OFFsetting Fade time setting
Soft Clip	Softclip limiter for output suppression	Soft Clip Enable Soft Clip Threshold Soft Clip Gain	Softclip Enable/Disable Threshold level, Gain setting
DAC	24bit DA Converter	DAC Power Management	DAC Enable/Disable
MIX1	Mixing DAC output and analog input.	Speaker Amplifier Output Control 2	Gain setting Mixing paths setting
SPVOL	Analog Volume for DAC to analog output path.	Speaker Amplifier Volume Control Amplifier Volume Fader Control Amplifier Volume Control Function Enable	Volume setting -54 to +6dB Fader ON/OFF setting Fade time setting
SPMIXG	Analog Volume for Speaker output path	Speaker Amplifier Output Control 1	Gain setting
MIX2	Mixing Speaker output signal and BEEPIN input signal.	SPAMP input Control BEEPIN Amp Control	Mixing paths setting
MIX3	Mixing Headphone output signal and BEEPIN input singlal.	SPAMP input Control BEEPIN Amp Control	Mixing paths setting
HPVOL	Analog Volume for Headphone output path	Headphone output Gain Setting	Gain setting

*Filter Block can be used for either ADC path or DAC path.
For example, if Filter Block is connectd to DAC, ADC is not effcetd by filter.
Regadrding the detail of register setting, please refer to selection of [SEMDE] register.