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## **Standard ICs**

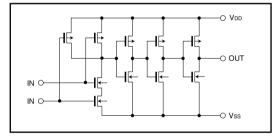
# Quad 2-input AND gate BU4081B / BU4081BF / BU4081BFV

The BU4081B, BU4081BF, and BU4081BFV are dual-input positive-logic AND gates with four circuits mounted on a single chip. An inverter-type buffer is added to the gate output, improving input / output transmission speed, and an increased load capacitance suppresses fluctuation in transmission time to a minimum.

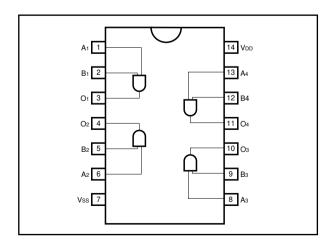
- Features
- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.

- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

#### Logic circuit diagram



#### Block diagram





•Absolute maximum ratings (Ta = 25°C,Vss = 0V)

Parameter	Symbol	Limits	Unit
Power supply voltage	VDD	- 0.3 ~ + 18	V
Power dissipation	Pd	1000 (DIP), 450 (SOP), 350 (SSOP)	mW
Operating temperature	Topr	- 40 ~ + 85	°C
Storage temperature	Tstg	- 55 ~ + 150	°C
Input voltage	Vin	$-0.3 \sim V_{DD} + 0.3$	V
I / O pin current	lı/o	± 10	mA

•Electrical characteristics (unless otherwise noted, Vss = 0V, Ta = 25°C)

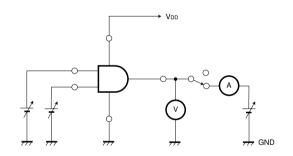
Parameter	Symbol	Min.	Тур.	Max.	Unit	V <sub>DD</sub> (V)		Measurement circuit
		3.5				<b>V</b> DD <b>(V)</b>		
Input high level voltage	Vін	7.0		_	v	10		Fig.1
		-				-		
		11.0				15		
Input low level voltage	VIL			1.5	V	5		Fig.1
				3.0		10		
				4.0		15		
Input high level current	Ін	_		0.3	μA	15	VIH = 15V	Fig.1
Input low level current	lı∟	—	—	- 0.3	μA	15	VIL = 0V	Fig.1
Output high level voltage	Vон	4.95	_	_	V	5	lo = 0mA	Fig.1
		9.95		_		10		
		14.95		_		15		
Output low level voltage	Vol	_		0.05	V	5	lo = 0mA	Fig.1
		—	—	0.05		10		
		—	—	0.05		15		
Output high level current	Іон	- 0.16	—	_	mA	5	Vон = 4.6V	Fig.1
		- 0.4	—	—		10	Vон = 9.5V	
		- 1.2	—	-		15	Vон = 13.5V	
Output low level current	lo∟	0.44	—	-	mA	5	Vol = 0.4V	Fig.1
		1.1	_	_		10	Vol = 0.5V	
		3.0	_	—		15	Vol = 1.5V	
Static current dissipation	ldd	_	_	1	μΑ	5	VI = VDD or GND	_
		_	_	2		10		
		_	_	4		15		

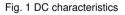


### Switching characteristics (unless otherwise noted, $V_{SS} = 0V$ , $Ta = 25^{\circ}C$ , $C_{L} = 50pF$ )

Parameter	Symbol	Min.	Тур.	Max.	Unit	Vdd (V)	Conditions	Measurement circuit
Output rise time	tтıн	_	180	_	ns	5		Fig.2
		—	90	—		10		
		—	65	—		15		
Output fall time	t⊤н∟	_	100	_	ns	5		Fig.2
		—	50	_		10		
			40	_		15		
"L" to "H" Propagation delay time	tрін	_	160		ns	5		Fig.2
			65			10		
			50			15		
"H" to "L" Propagation delay time	tphl	_	160		ns	5		Fig.2
		_	65	_		10		
		_	50	_		15		
Input capacitance	Cin	_	5	_	pF			_

Measurement circuits





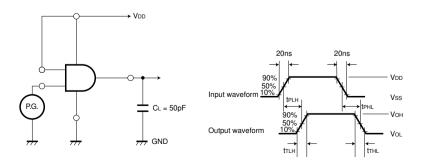


Fig. 2 Switching characteristics

• Electrical characteristic curve

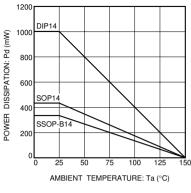
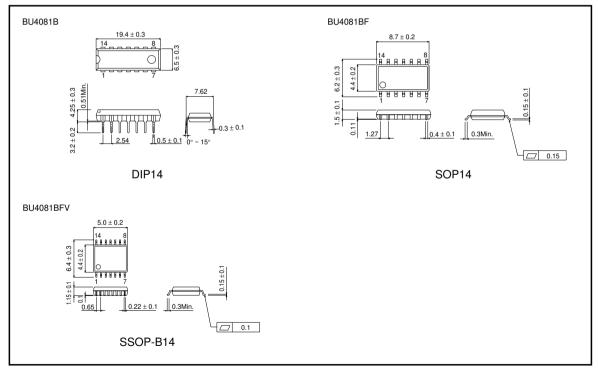


Fig. 3 Power dissipation vs. Ta





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