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LVDS Interface LSI

67bit LVDS Receiver

BU90R102

General Description

The BU90R102 receiver operates from 8MHz to 160MHz wide clock range.
The BU90R102 converts the 10 Lane (2Channel) LVDS serial data streams back into 67bit of LVCMOS parallel data.
Data is transmitted seven times (7X) stream and reduce the cable number by 3(1/3) or less.
I/O Voltage range is 2.3 to 3.6V, so it is available for many products.
Flexible Input /Output mode is suitable for a variety of application Interface.

Key Specifications

■Supply Voltage Range	2.30 to 3.60 V
■Operating Frequency	8 to 160 MHz
■Operating Temperature Range	-40 to +85 ℃

Package

HQFP144VM

W(Typ) x D(Typ) x H(Max)
20.0mm × 20.0mm × 1.6mm

Applications

■Security camera, Digital camera
■Tablet
■Flat panel display

Features

■The maximum data rate is 1120Mbps/Lane
■It enables to receive the 60bit of RGB data, 7bit of Timing and Control data
■Support clock frequency from 8MHz up to 160MHz
■Flexible Input /Output mode
1. Single-in / Single-out
2. Single-in / Dual-out
3. Dual-in / Single-out
4. Dual-in / Dual-out

■Power down mode
■Clock edge selectable
■Support spread spectrum clock generator input

Block Diagram

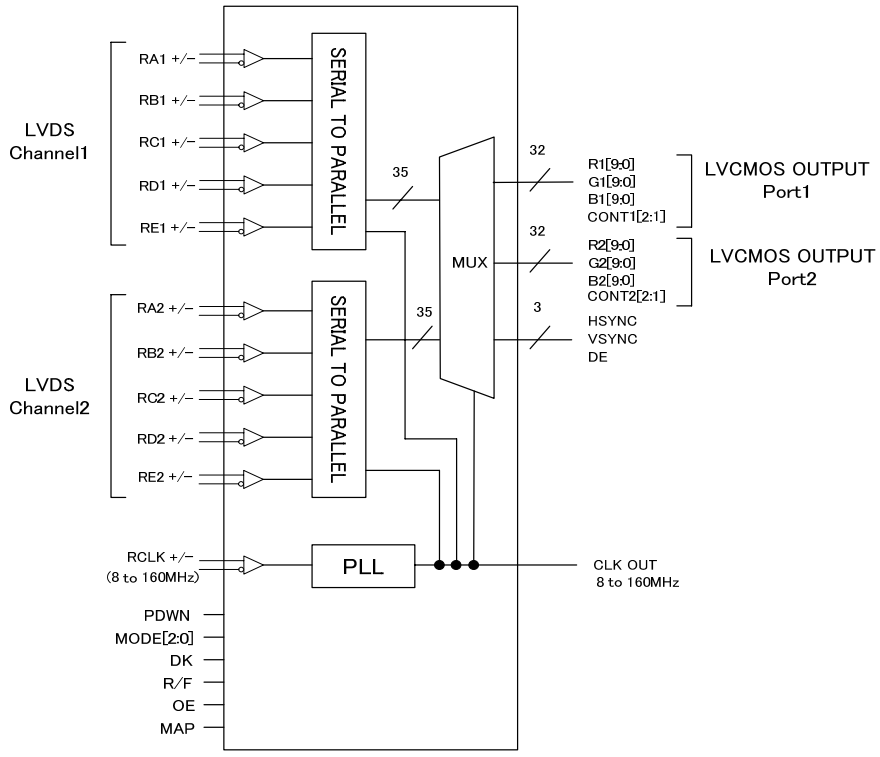


Figure 1. Block Diagram

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Contents

Pin Configuration

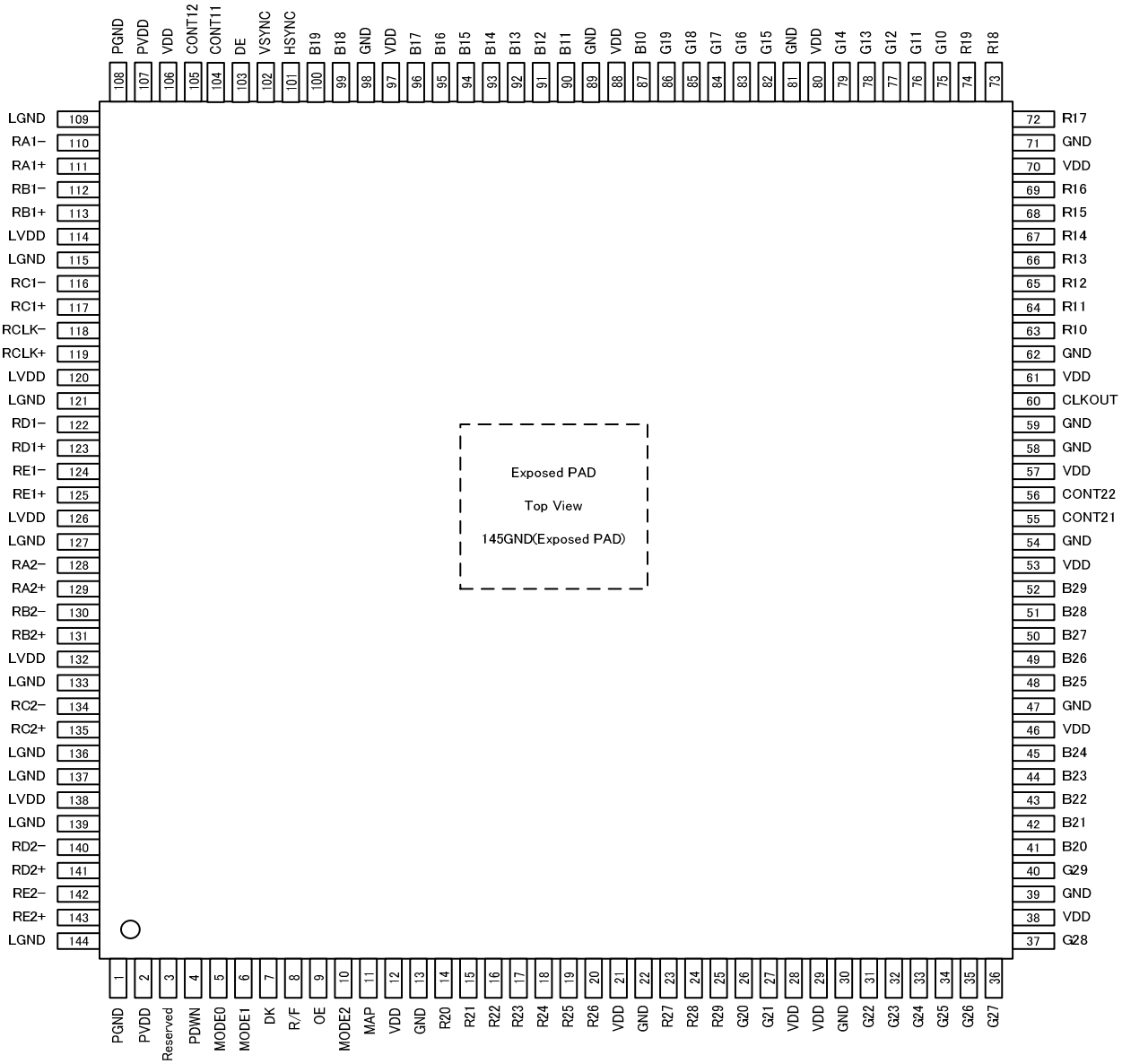


Figure 2. Pin Configuration (Top View)

Pin Descriptions

<table>
<tr><th>Pin name</th><th>Pin No.</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>RA1+, RA1-</td><td>111,110</td><td>LVDS Input</td><td rowspan="5">LVDS Data input (Channel1)
+: positive input of differential pair
-: negative input of differential pair</td></tr>
<tr><td>RB1+, RB1-</td><td>113,112</td><td>LVDS Input</td></tr>
<tr><td>RC1+, RC1-</td><td>117,116</td><td>LVDS Input</td></tr>
<tr><td>RD1+, RD1-</td><td>123,122</td><td>LVDS Input</td></tr>
<tr><td>RE1+, RE1-</td><td>125,124</td><td>LVDS Input</td></tr>
<tr><td>RCLK+, RCLK-</td><td>119,118</td><td>LVDS Input</td><td>LVDS CLK input</td></tr>
<tr><td>RA2+,RA2-</td><td>129,128</td><td>LVDS Input</td><td rowspan="5">LVDS Data input (Channel2)
+: positive input of differential pair
-: negative input of differential pair
（These pins are disabled when Single Link mode）</td></tr>
<tr><td>RB2+,RB2-</td><td>131,130</td><td>LVDS Input</td></tr>
<tr><td>RC2+,RC2-</td><td>135,134</td><td>LVDS Input</td></tr>
<tr><td>RD2+,RD2-</td><td>141,140</td><td>LVDS Input</td></tr>
<tr><td>RE2+,RE2-</td><td>143,142</td><td>LVDS Input</td></tr>
<tr><td>R19～R10</td><td>74-72,69-63</td><td>Output</td><td rowspan="3">LVCMOS Data Output</td></tr>
<tr><td>G19～G10</td><td>86-82,79-75</td><td>Output</td></tr>
<tr><td>B19～B10</td><td>100,99,96-90,87</td><td>Output</td></tr>
<tr><td>R29～R20</td><td>25-23,20-14</td><td>Output</td><td rowspan="3">LVCMOS Data Output</td></tr>
<tr><td>G29～G20</td><td>40,37-31,
27,26</td><td>Output</td></tr>
<tr><td>B29～B20</td><td>52-48,45-41</td><td>Output</td></tr>
<tr><td>CONT11,CONT12</td><td>104,105</td><td>Output</td><td rowspan="2">LVCMOS Data Output</td></tr>
<tr><td>CONT21,CONT22</td><td>55,56</td><td>Output</td></tr>
<tr><td>DE</td><td>103</td><td>Output</td><td>Data Enable Output</td></tr>
<tr><td>VSYNC</td><td>102</td><td>Output</td><td>VSYNC Output</td></tr>
<tr><td>HSYNC</td><td>101</td><td>Output</td><td>HSYNC Output</td></tr>
<tr><td>CLKOUT</td><td>60</td><td>Output</td><td>LVCMOS CLK Output</td></tr>
<tr><td>PDWN</td><td>4</td><td>Input</td><td>Power Down
H: Normal operation
L: Power down</td></tr>
<tr><td>MODE1,MODE0</td><td>6,5</td><td>Input</td><td>
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr>
<tr><td>H</td><td>H</td><td>Single Link(Single-in/Single-out)</td></tr>
<tr><td>H</td><td>L</td><td>Single Link(Single-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Dual Link(Dual-in/Single-out)</td></tr>
<tr><td>L</td><td>L</td><td>Dual Link(Dual-in/Dual-out)</td></tr>
</table>
</td></tr>
</table>

Pin Descriptions (Continued)

<table>
<tr><th>Pin name</th><th>Pin No.</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>DK</td><td>7</td><td>Input</td><td>Output Clock Delay Timing Select.
t_{DOUT}=Output Data Rate
<table><tr><th>MODE〔1:0〕</th><th>DK</th><th>OFFSET〔nsec〕</th></tr><tr><td rowspan="3">LL
HH
HL</td><td>L</td><td>0</td></tr><tr><td>M</td><td>-(6/28)t_{DOUT}</td></tr><tr><td>H</td><td>+(6/28)t_{DOUT}</td></tr><tr><td rowspan="3">LH</td><td>L</td><td>0</td></tr><tr><td>M</td><td>-(7/28)t_{DOUT}</td></tr><tr><td>H</td><td>+(7/28)t_{DOUT}</td></tr></table></td></tr>
<tr><td>R/F</td><td>8</td><td>Input</td><td>Output Clock Triggering Edge Select.
H:Rising edge
L:Falling edge</td></tr>
<tr><td>OE</td><td>9</td><td>Input</td><td>Output Enable.
H: Output Enable.
L: Output Disable.</td></tr>
<tr><td>MODE2</td><td>10</td><td>Input</td><td>DDR function enable
This function depends on the setting of MODE<1,0>.
MODE<1,0>=LH (Dual-in/Single-out MODE)
H:DDR (Double Edge Output)function ON
L:DDR (Double Edge Output) function OFF

MODE<1,0>=other
Must be tied to GND.</td></tr>
<tr><td>MAP</td><td>11</td><td>Input</td><td>LVDS mapping table select (Refer the Table 9～12)
H:Mapping Mode1
L:Mapping Mode2</td></tr>
<tr><td>Reserved</td><td>3</td><td>Input</td><td>Must be tied to VDD.</td></tr>
<tr><td>VDD</td><td>12,21,28,29,38,
46,53,57,61,70,80,
88,97,106</td><td>Power</td><td>Power Supply for Internal digital core and Output Driver.</td></tr>
<tr><td>GND</td><td>13,22,30,39,47,
54,58,59,62,71,81,
89,98,145</td><td>Ground</td><td>Ground for Internal digital core and Output Driver.</td></tr>
<tr><td>LVDD</td><td>114,120,126,
132,138</td><td>Power</td><td>Power Supply for LVDS core.</td></tr>
<tr><td>LGND</td><td>109,115,121,127,
133,136,137,139,
144</td><td>Ground</td><td>Ground for LVDS core.</td></tr>
<tr><td>PVDD</td><td>2,107</td><td>Power</td><td>Power Supply for PLL core.</td></tr>
<tr><td>PGND</td><td>1,108</td><td>Ground</td><td>Ground for PLL core.</td></tr>
</table>

Table 1. Output Settings

PDWN	OE	Data Outputs	CLKOUT
L	L	Hi-Z	Hi-Z
L	H	All Low	Fixed Low
H	L	Hi-Z	Hi-Z
H	H	Data Out	CLK Out

Absolute Maximum Ratings

Parameter	Symbol	Rating		Units
		Min	Max	
Supply Voltage	V_{DD}	-0.3	+4.0	V
Input Voltage	V_{IN}	-0.3	V_{DD}+0.3	V
Output Voltage	V_{OUT}	-0.3	V_{DD}+0.3	V
Storage Temperature Range	T_{stg}	-55	+125	℃
Junction Temperature	T_j	+125		℃
Power Dissipation	P_d	4.16(Note1)		W

(Note1) Package Power when IC mounting on the PCB board.
The size of PCB board : 114.3 × 76.2 × 1.6 (mm^3)
The material of PCB board : The FR4 glass epoxy board (3% or less copper foil area)

Recommended Operating Conditions

Parameter			Symbol	Rating			Units	Conditions
				Min	Typ	Max		
Supply Voltage			V_{DD}	2.3	3.3	3.6	V	VDD,LVDD, PVDD
Operating Temperature Range			T_a	-40	+25	+85	℃	-
CLK frequency	MODE<1:0>=LL Dual-in/Dual-out		LVDS Input	8	-	160	MHz	-
			Output	8	-	160	MHz	-
	MODE<1:0>=LH Dual-in/Single-out	Single Edge Output (MODE2=L)	LVDS Input	20	-	80	MHz	-
			Output	40	-	160	MHz	-
		Double Edge Output (MODE2=H)	LVDS Input	20	-	80	MHz	-
			Output	20	-	80	MHz	-
	MODE<1:0>=HL Single-in/Dual-out		LVDS Input	8	-	160	MHz	-
			Output	4	-	80	MHz	-
	MODE<1:0>=HH Single-in/Single-out		LVDS Input	8	-	160	MHz	-
			Output	8	-	160	MHz	-
Differential input CLK High Time (t_{RCIH}) (Figure 3)				$2\frac{t_{RCIP}}{7}$	-	$5\frac{t_{RCIP}}{7}$	ns	-
Differential input CLK Low Time (t_{RCIL}) (Figure 3)				$2\frac{t_{RCIP}}{7}$	-	$5\frac{t_{RCIP}}{7}$	ns	-

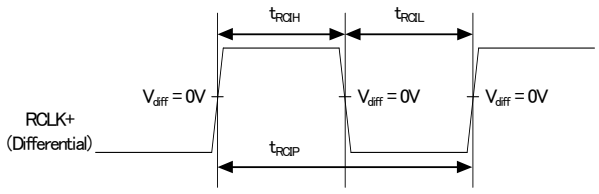


Figure 3. Differential input CLK

DC Characteristics

Table 2. LVCMOS DC Specifications (VDD=2.3~3.6V, Ta=-40~+85℃)

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
VIH	High Level Input Voltage	V_{DD}x0.7	-	V_{DD}	V	PDWN, MODE[2:0] R/F, OE, MAP PIN
VIL	Low Level Input Voltage	GND	-	V_{DD}x0.3	V	
VIH3	High Level Input Voltage 3	V_{DD}x0.8	-	V_{DD}	V	3-Level Inputs (DK Pin)
VIM3	Middle Level Input Voltage 3	V_{DD}x0.4	-	V_{DD}x0.6	V	
VIL3	Low Level Input Voltage 3	GND		V_{DD}x0.2	V	
VOH	High Level Output Voltage	V_{DD} -0.5	-	V_{DD}	V	IO = -8mA
VOL	Low Level Output Voltage	GND	-	0.4	V	IO = 8mA
IIL	Input Leakage Current	-10	-	+10	uA	0 ≤VIN ≤VDD

Table 3. LVDS Receiver DC Specifications (VDD=2.3~3.6V, Ta=-40~+85℃)

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
V_{TH}	Differential Input High Threshold	-	-	+100	mV	V_{OC} (Note2) =1.2V
V_{TL}	Differential Input Low Threshold	-100	-	-	mV	V_{OC} (Note2) =1.2V
I_{INL}	Differential Input Leakage Current	-30	-	+30	μA	V_{IN}=2.4V / 0V V_{DD}=3.6V
V_{OC}	Common mode Voltage	0.8	1.2	1.6	V	V_{ID} =200mV
$\|V_{ID}\|$	Differential Input Voltage	100	-	600	mV	-

(Note2) Common mode Voltage

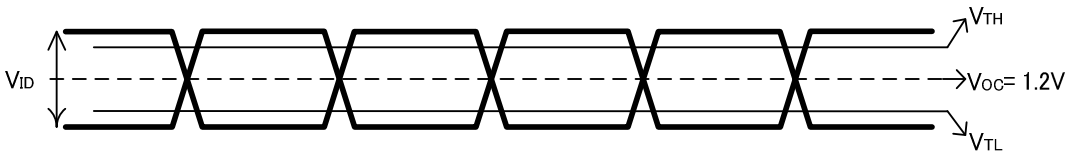


Figure 4. LVDS Receiver DC Specifications

AC characteristics

Table 4. Switching Characteristics (VDD=2.3~3.6V, Ta=-40~+85℃)

Symbol	Parameter		Limits			Units
			Min	Typ	Max	
t_{RCP}	CLKOUT Period (Figure 7)		6.25	-	250	ns
t_{RCH}	CLKOUT High Time (Figure 7)		-	$0.5t_{RCP}$	-	ns
t_{RCL}	CLKOUT Low Time (Figure 7)		-	$0.5t_{RCP}$	-	ns
t_{DOUT}	LVCMOS Data Out Period (Figure 8,9)		6.25	-	250	ns
t_{RS}	LVCMOS Data Setup to CLKOUT (Figure 8,9)		$0.45t_{RCP}$-0.45	-	-	ns
t_{RH}	LVCMOS Data Hold to CLKOUT (Figure 8,9)		$0.45t_{RCP}$-0.45	-	-	ns
t_{TLH}	LVCMOS Low to High Transition Time (Figure 6)		-	0.7	1.0	ns
t_{THL}	LVCMOS High to Low Transition Time (Figure 6)		-	0.7	1.0	ns
t_{sk}	Receiver Skew Margin (Figure 10)	t_{RCIP}=65MHz	0	-	650	ps
		t_{RCIP}=85MHz	0	-	450	ps
		t_{RCIP}=108MHz	0	-	250	ps
		t_{RCIP}=135MHz	0	-	170	ps
		t_{RCIP}=160MHz	0	-	150	ps
t_{RIP1}	Input Data Position 0 (Figure 10)		$-t_{sk}$	0.0	$+t_{sk}$	ns
t_{RIP0}	Input Data Position 1 (Figure 10)		$\frac{t_{RCIP}}{7} - t_{sk}$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{sk}$	ns
t_{RIP6}	Input Data Position 2 (Figure 10)		$2\frac{t_{RCIP}}{7} - t_{sk}$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{sk}$	ns
t_{RIP5}	Input Data Position 3 (Figure 10)		$3\frac{t_{RCIP}}{7} - t_{sk}$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{sk}$	ns
t_{RIP4}	Input Data Position 4 (Figure 10)		$4\frac{t_{RCIP}}{7} - t_{sk}$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{sk}$	ns
t_{RIP3}	Input Data Position 5 (Figure 10)		$5\frac{t_{RCIP}}{7} - t_{sk}$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{sk}$	ns
t_{RIP2}	Input Data Position 6 (Figure 10)		$6\frac{t_{RCIP}}{7} - t_{sk}$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{sk}$	ns
t_{RPLL}	Phase Locked Loop Set Time (Figure 11)		-	-	10.0	ms
t_{RCD}	RCLK+/- to CLKOUT Delay (Figure 12) MODE<1:0>=LL DK=L, 75MHz		82	-	180	ns
t_{RCIP}	Input CLK Period (Figure 10)		6.25	-	125.0	ns
t_{DEINT}	MODE<1:0>=HL (Single-in/Dual-out Mode)	DE input period (Figure 13)	$4t_{RCIP}$	t_{RCIP}*(2n) n=integer	-	ns
t_{DEH}		DE input High time (Figure 13)	$2t_{RCIP}$	-	-	ns
t_{DEL}		DE input Low time (Figure 13)	$2t_{RCIP}$	-	-	ns

Supply Current

Symbol	Parameter	Conditions			Limits		Units
					Typ	Max	
I_{RCCW}	Receiver Supply Current (Worst Case Pattern) Figure 5	CLKOUT=65MHz	CL=8pF	MODE<1:0>=HH Single-in/Single-out MODE2=L	-	134	mA
		CLKOUT=85MHz			-	165	mA
		CLKOUT=135MHz			-	244	mA
		CLKOUT=160MHz			-	284	mA
		CLKOUT=32.5MHz		MODE<1:0>=HL Single-in/Dual-out MODE2=L	-	110	mA
		CLKOUT=42.5MHz			-	134	mA
		CLKOUT=67.5MHz			-	190	mA
		CLKOUT=80MHz			-	230	mA
		CLKOUT=65MHz		MODE<1:0>=LH Dual-in/ Single out MODE2=L DDR Output Off	-	113	mA
		CLKOUT=85MHz			-	137	mA
		CLKOUT=135MHz			-	190	mA
		CLKOUT=150MHz			-	221	mA
		CLKOUT=160MHz			-	230	mA
		CLKOUT=32.5MHz		MODE<1:0>=LH Dual-in/ Single out MODE2=H DDR Output On	-	110	mA
		CLKOUT=42.5MHz			-	134	mA
		CLKOUT=67.5MHz			-	187	mA
		CLKOUT=75MHz			-	217	mA
		CLKOUT=80MHz			-	228	mA
		CLKOUT=65MHz		MODE<1:0>=LL Dual-in/ Dual-out MODE2=L	-	218	mA
		CLKOUT=85MHz			-	272	mA
		CLKOUT=135MHz			-	408	mA
		CLKOUT=160MHz			-	460	mA

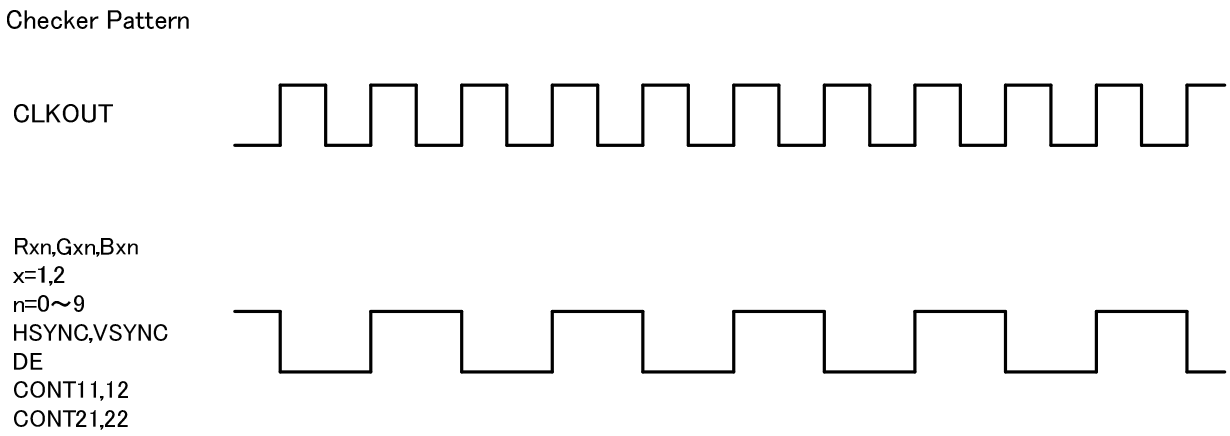


Figure 5. Test Pattern

AC Timing Diagrams

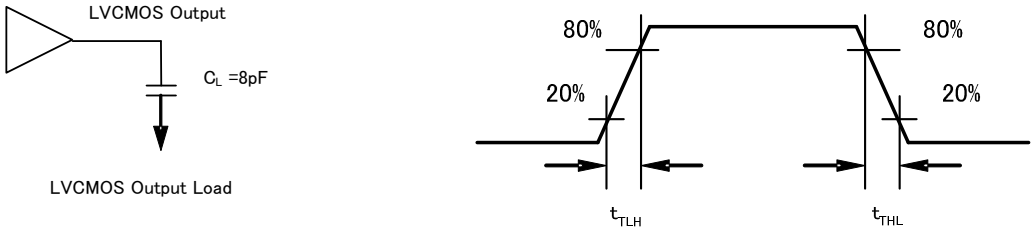


Figure 6. LVCMOS Output Load and Transition Time

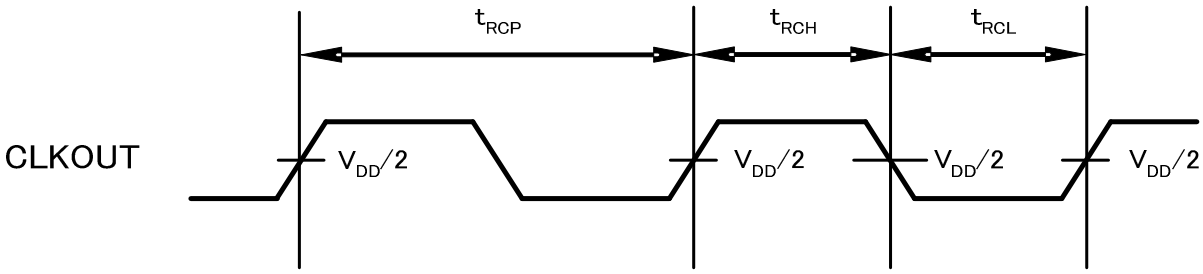


Figure 7. CLKOUT Period and High/Low Time

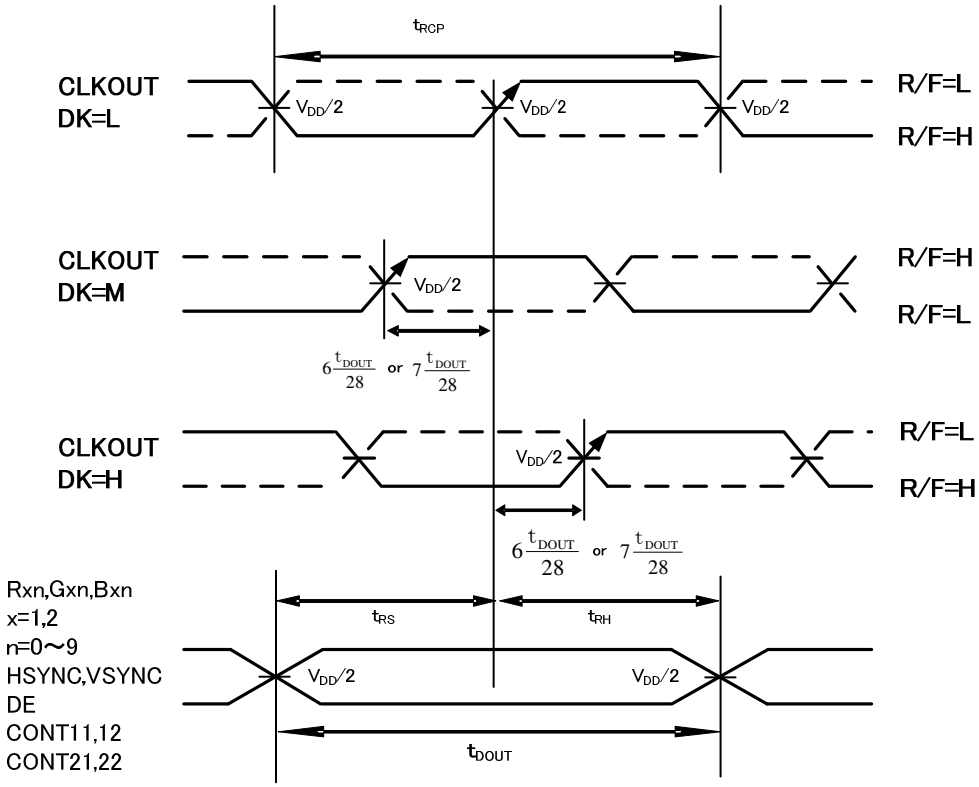


Figure 8. CLKOUT Position and Setup/Hold Timing

AC Timing Diagrams (Continued)

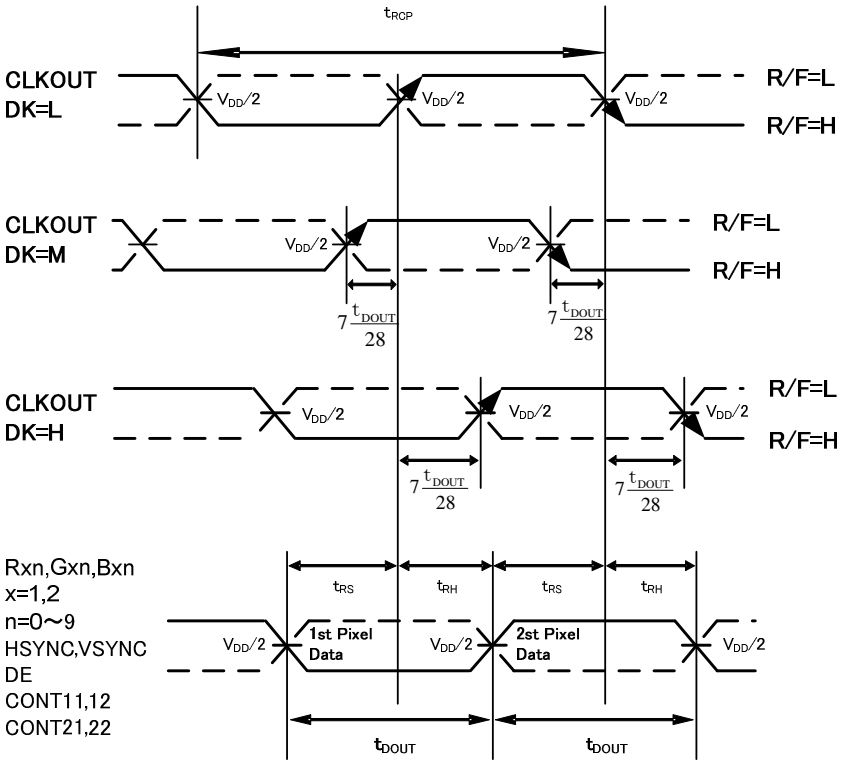


Figure 9. CLKOUT Position and Setup/Hold Timing for Double Edge Output Mode

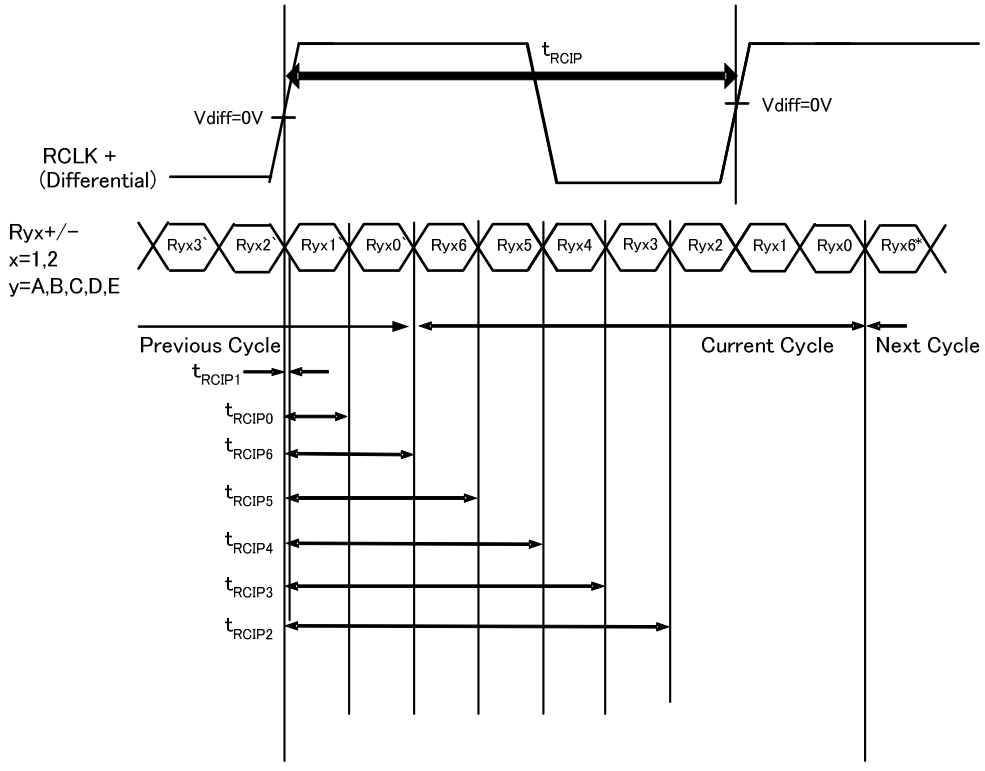


Figure 10. LVDS Input Data Position

AC Timing Diagrams (Continued)

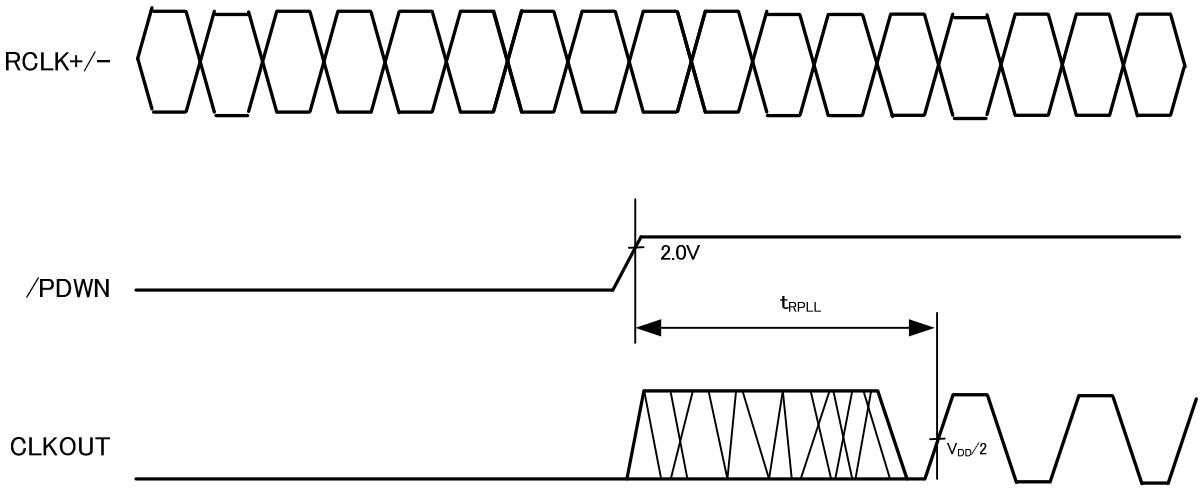


Figure 11. Phase Locked Loop Set Time

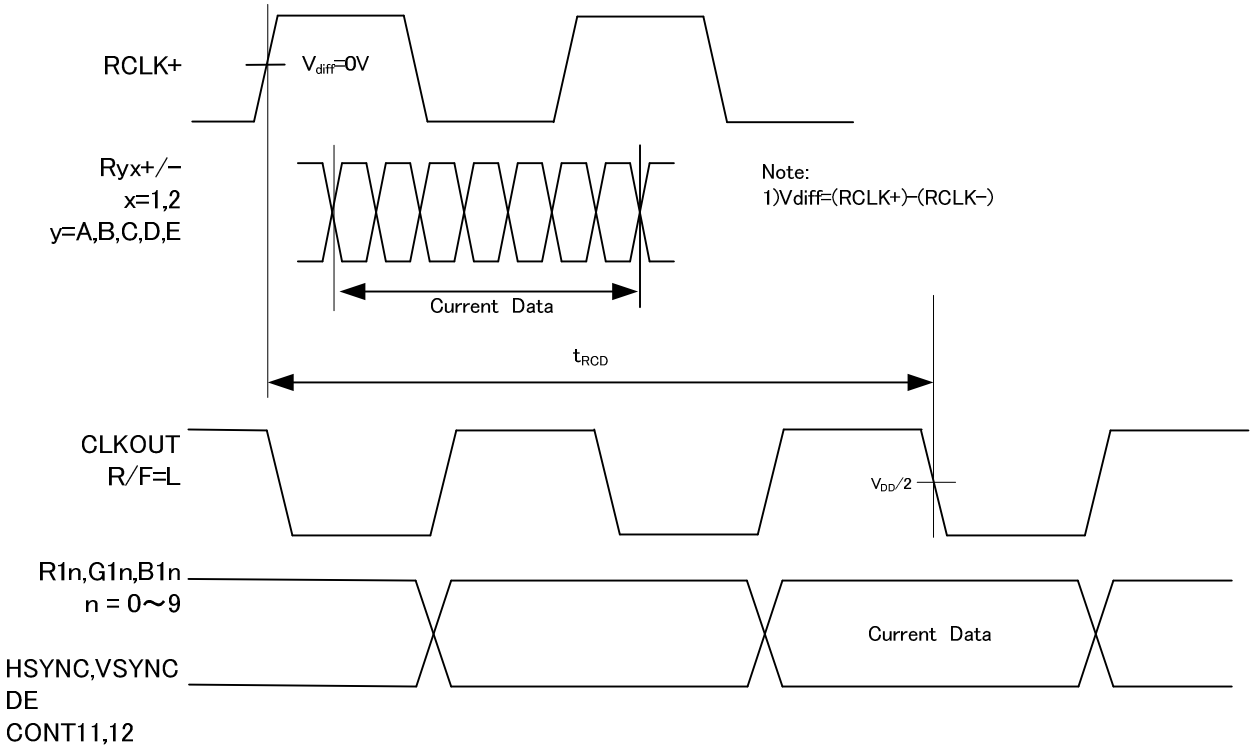


Figure 12. RCLK+/- to CLKOUT Delay

Table 5. Input DE signal of all Input/Output modes

In	Out	MODE1	MODE0	Input DE Signal
Single	Single	H	H	Optional
Single	Dual	H	L	Require (Figure 13)
Dual	Single	L	H	Optional
Dual	Dual	L	L	Optional

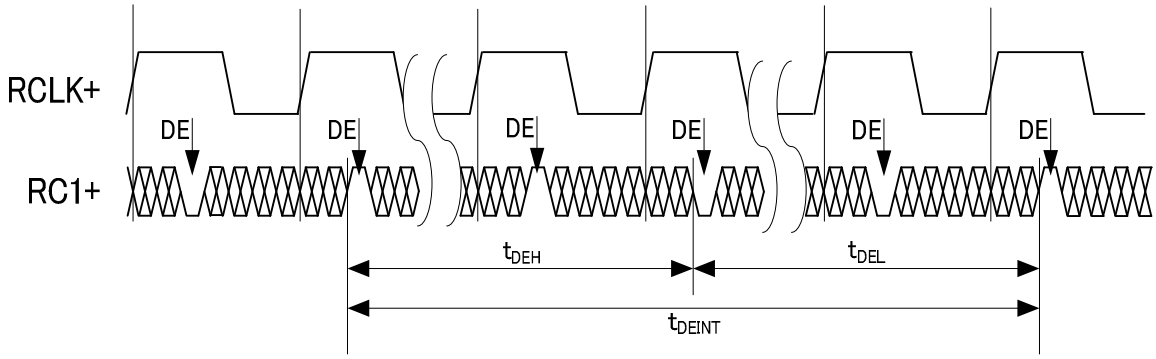


Figure 13. RC1 (DE) Input Timing (Single-in / Dual-out mode)

Output Data Mapping

Table 6. Output Color Data naming rule

X	Y	Z	Description	
X=R	-	-	Red Color Data	
X=G	-	-	Green Color Data	
X=B	-	-	Blue Color Data	
-	Y=None	-	Single Pixel	
-	Y=O	-	Dual Pixel	1st Pixel Data
-	Y=E	-		2nd Pixel Data
-	-	Z=0-9	Bit number	0: LSB(Least Significant Bit) 9: MSB(Most Significant Bit)

Table 7. LVCMOS Output Data Mapping (Single-out mode, MODE0=H)

Data Signals			Receiver Output Pin Names		
30-bit	24-bit	18-bit	30-bit	24-bit	18-bit
R0	-	-	R10	-	-
R1	-	-	R11	-	-
R2	R0	-	R12	R12	-
R3	R1	-	R13	R13	-
R4	R2	R0	R14	R14	R14
R5	R3	R1	R15	R15	R15
R6	R4	R2	R16	R16	R16
R7	R5	R3	R17	R17	R17
R8	R6	R4	R18	R18	R18
R9	R7	R5	R19	R19	R19
G0	-	-	G10	-	-
G1	-	-	G11	-	-
G2	G0	-	G12	G12	-
G3	G1	-	G13	G13	-
G4	G2	G0	G14	G14	G14
G5	G3	G1	G15	G15	G15
G6	G4	G2	G16	G16	G16
G7	G5	G3	G17	G17	G17
G8	G6	G4	G18	G18	G18
G9	G7	G5	G19	G19	G19
B0	-	-	B10	-	-
B1	-	-	B11	-	-
B2	B0	-	B12	B12	-
B3	B1	-	B13	B13	-
B4	B2	B0	B14	B14	B14
B5	B3	B1	B15	B15	B15
B6	B4	B2	B16	B16	B16
B7	B5	B3	B17	B17	B17
B8	B6	B4	B18	B18	B18
B9	B7	B5	B19	B19	B19

Output Data Mapping (Continued)

Table 8. LVCMOS Output Data Mapping (Dual-Out mode, MODE0=L)

1st Pixel Data						2nd Pixel Data					
Data Signals			Receiver output Pin Names			Data Signals			Receiver output Pin Names		
30-bit	24bit	18-bit	30-bit	24bit	18-bit	30-bit	24bit	18-bit	30-bit	24bit	18-bit
RE0	-	-	R10	-	-	RO0	-	-	R20	-	-
RE1	-	-	R11	-	-	RO1	-	-	R21	-	-
RE2	RE0	-	R12	R12	-	RO2	RO0	-	R22	R22	-
RE3	RE1	-	R13	R13	-	RO3	RO1	-	R23	R23	-
RE4	RE2	RE0	R14	R14	R14	RO4	RO2	RO0	R24	R24	R24
RE5	RE3	RE1	R15	R15	R15	RO5	RO3	RO1	R25	R25	R25
RE6	RE4	RE2	R16	R16	R16	RO6	RO4	RO2	R26	R26	R26
RE7	RE5	RE3	R17	R17	R17	RO7	RO5	RO3	R27	R27	R27
RE8	RE6	RE4	R18	R18	R18	RO8	RO6	RO4	R28	R28	R28
RE9	RE7	RE5	R19	R19	R19	RO9	RO7	RO5	R29	R29	R29
GE0	-	-	G10	-	-	GO0	-	-	G20	-	-
GE1	-	-	G11	-	-	GO1	-	-	G21	-	-
GE2	GE0	-	G12	G12	-	GO2	GO0	-	G22	G22	-
GE3	GE1	-	G13	G13	-	GO3	GO1	-	G23	G23	-
GE4	GE2	GE0	G14	G14	G14	GO4	GO2	GO0	G24	G24	G24
GE5	GE3	GE1	G15	G15	G15	GO5	GO3	GO1	G25	G25	G25
GE6	GE4	GE2	G16	G16	G16	GO6	GO4	GO2	G26	G26	G26
GE7	GE5	GE3	G17	G17	G17	GO7	GO5	GO3	G27	G27	G27
GE8	GE6	GE4	G18	G18	G18	GO8	GO6	GO4	G28	G28	G28
GE9	GE7	GE5	G19	G19	G19	GO9	GO7	GO5	G29	G29	G29
BE0	-	-	B10	-	-	BO0	-	-	B20	-	-
BE1	-	-	B11	-	-	BO1	-	-	B21	-	-
BE2	BE0	-	B12	B12	-	BO2	BO0	-	B22	B22	-
BE3	BE1	-	B13	B13	-	BO3	BO1	-	B23	B23	-
BE4	BE2	BE0	B14	B14	B14	BO4	BO2	BO0	B24	B24	B24
BE5	BE3	BE1	B15	B15	B15	BO5	BO3	BO1	B25	B25	B25
BE6	BE4	BE2	B16	B16	B16	BO6	BO4	BO2	B26	B26	B26
BE7	BE5	BE3	B17	B17	B17	BO7	BO5	BO3	B27	B27	B27
BE8	BE6	BE4	B18	B18	B18	BO8	BO6	BO4	B28	B28	B28
BE9	BE7	BE5	B19	B19	B19	BO9	BO7	BO5	B29	B29	B29

LVDS Input Data Mapping

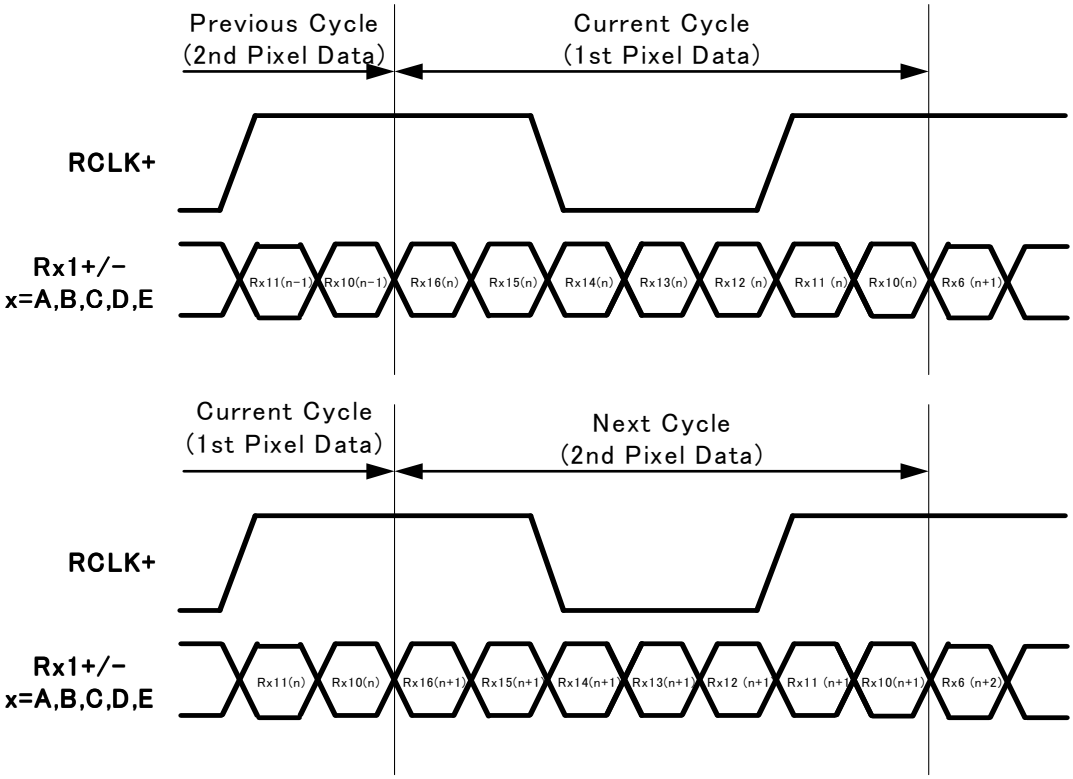


Figure 14. LVDS Input Data Mapping
MODE1=H (Single-in Mode)

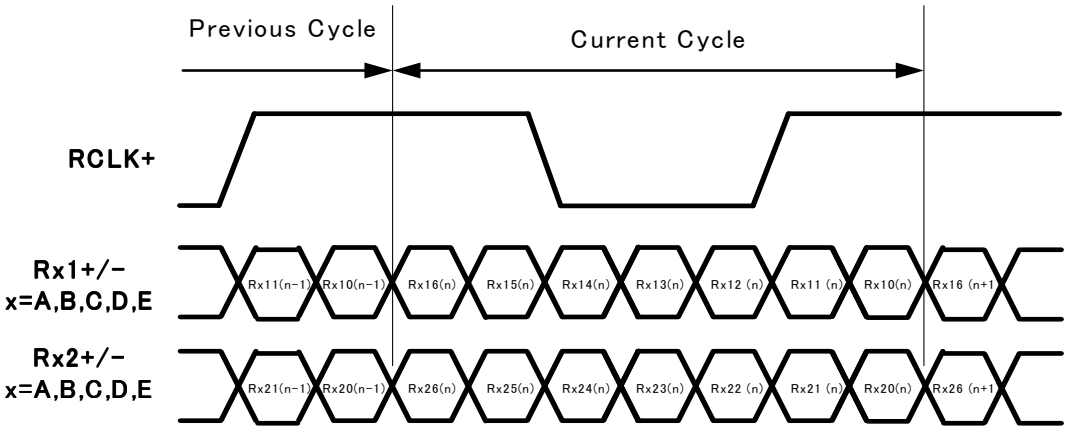


Figure 15. LVDS Input Data Mapping
MODE1=L (Dual-in Mode)

LVDS Input Data Mapping (Continued)

Table 9. LVDS Input Data Mapping (Single-in/Single-out mode, MODE<1:0>=HH)

LVDS Input Data	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14	R12
RA11	R15	R13
RA12	R16	R14
RA13	R17	R15
RA14	R18	R16
RA15	R19	R17
RA16	G14	G12
RB10	G15	G13
RB11	G16	G14
RB12	G17	G15
RB13	G18	G16
RB14	G19	G17
RB15	B14	B12
RB16	B15	B13
RC10	B16	B14
RC11	B17	B15
RC12	B18	B16
RC13	B19	B17
RC14	HSYNC	HSYNC
RC15	VSYNC	VSYNC
RC16	DE	DE
RD10	R12	R18
RD11	R13	R19
RD12	G12	G18
RD13	G13	G19
RD14	B12	B18
RD15	B13	B19
RD16	CONT11	CONT11
RE10	R10	R10
RE11	R11	R11
RE12	G10	G10
RE13	G11	G11
RE14	B10	B10
RE15	B11	B11
RE16	CONT12	CONT12

LVDS Input Data Mapping (Continued)

Table 10. LVDS Input Data Mapping (Single-in/Dual-out mode, MODE<1:0>=HL)

1st Pixel Data			2nd Pixel Data		
LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Input Pin Name)	LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Input Pin Name)
RA10(n)	R14	R12	RA10(n+1)	R24	R22
RA11(n)	R15	R13	RA11(n+1)	R25	R23
RA12(n)	R16	R14	RA12(n+1)	R26	R24
RA13(n)	R17	R15	RA13(n+1)	R27	R25
RA14(n)	R18	R16	RA14(n+1)	R28	R26
RA15(n)	R19	R17	RA15(n+1)	R29	R27
RA16(n)	G14	G12	RA16(n+1)	G24	G22
RB10(n)	G15	G13	RB10(n+1)	G25	G23
RB11(n)	G16	G14	RB11(n+1)	G26	G24
RB12(n)	G17	G15	RB12(n+1)	G27	G25
RB13(n)	G18	G16	RB13(n+1)	G28	G26
RB14(n)	G19	G17	RB14(n+1)	G29	G27
RB15(n)	B14	B12	RB15(n+1)	B24	B22
RB16(n)	B15	B13	RB16(n+1)	B25	B23
RC10(n)	B16	B14	RC10(n+1)	B26	B24
RC11(n)	B17	B15	RC11(n+1)	B27	B25
RC12(n)	B18	B16	RC12(n+1)	B28	B26
RC13(n)	B19	B17	RC13(n+1)	B29	B27
RC14(n)	HSYNC	HSYNC	RC14(n+1)	HSYNC	HSYNC
RC15(n)	VSYNC	VSYNC	RC15(n+1)	VSYNC	VSYNC
RC16(n)	DE	DE	RC16(n+1)	DE	DE
RD10(n)	R12	R18	RD10(n+1)	R22	R28
RD11(n)	R13	R19	RD11(n+1)	R23	R29
RD12(n)	G12	G18	RD12(n+1)	G22	G28
RD13(n)	G13	G19	RD13(n+1)	G23	G29
RD14(n)	B12	B18	RD14(n+1)	B22	B28
RD15(n)	B13	B19	RD15(n+1)	B23	B29
RD16(n)	CONT11	CONT11	RD16(n+1)	CONT21	CONT21
RE10(n)	R10	R10	RE10(n+1)	R20	R20
RE11(n)	R11	R11	RE11(n+1)	R21	R21
RE12(n)	G10	G10	RE12(n+1)	G20	G20
RE13(n)	G11	G11	RE13(n+1)	G21	G21
RE14(n)	B10	B10	RE14(n+1)	B20	B20
RE15(n)	B11	B11	RE15(n+1)	B21	B21
RE16(n)	CONT12	CONT12	RE16(n+1)	CONT22	CONT22

LVDS Input Data Mapping (Continued)

Table 11. LVDS Input Data Mapping (Dual-in/Single-out mode DDR On or Off, MODE<1:0> = LH, MODE2 = H or L)

1st Pixel Data			2nd Pixel Data		
LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14(n)	R12(n)	RA20	R14(n+1)	R12(n+1)
RA11	R15(n)	R13(n)	RA21	R15(n+1)	R13(n+1)
RA12	R16(n)	R14(n)	RA22	R16(n+1)	R14(n+1)
RA13	R17(n)	R15(n)	RA23	R17(n+1)	R15(n+1)
RA14	R18(n)	R16(n)	RA24	R18(n+1)	R16(n+1)
RA15	R19(n)	R17(n)	RA25	R19(n+1)	R17(n+1)
RA16	G14(n)	G12(n)	RA26	G14(n+1)	G12(n+1)
RB10	G15(n)	G13(n)	RB20	G15(n+1)	G13(n+1)
RB11	G16(n)	G14(n)	RB21	G16(n+1)	G14(n+1)
RB12	G17(n)	G15(n)	RB22	G17(n+1)	G15(n+1)
RB13	G18(n)	G16(n)	RB23	G18(n+1)	G16(n+1)
RB14	G19(n)	G17(n)	RB24	G19(n+1)	G17(n+1)
RB15	B14(n)	B12(n)	RB25	B14(n+1)	B12(n+1)
RB16	B15(n)	B13(n)	RB26	B15(n+1)	B13(n+1)
RC10	B16(n)	B14(n)	RC20	B16(n+1)	B14(n+1)
RC11	B17(n)	B15(n)	RC21	B17(n+1)	B15(n+1)
RC12	B18(n)	B16(n)	RC22	B18(n+1)	B16(n+1)
RC13	B19(n)	B17(n)	RC23	B19(n+1)	B17(n+1)
RC14	HSYNC(n)	HSYNC(n)	RC24	HSYNC(n+1)	HSYNC(n+1)
RC15	VSYNC(n)	VSYNC(n)	RC25	VSYNC(n+1)	VSYNC(n+1)
RC16	DE(n)	DE(n)	RC26	DE(n+1)	DE(n+1)
RD10	R12(n)	R18(n)	RD20	R12(n+1)	R18(n+1)
RD11	R13(n)	R19(n)	RD21	R13(n+1)	R19(n+1)
RD12	G12(n)	G18(n)	RD22	G12(n+1)	G18(n+1)
RD13	G13(n)	G19(n)	RD23	G13(n+1)	G19(n+1)
RD14	B12(n)	B18(n)	RD24	B12(n+1)	B18(n+1)
RD15	B13(n)	B19(n)	RD25	B13(n+1)	B19(n+1)
RD16	CONT11(n)	CONT11(n)	RD26	CONT11(n+1)	CONT11(n+1)
RE10	R10(n)	R10(n)	RE20	R10(n+1)	R10(n+1)
RE11	R11(n)	R11(n)	RE21	R11(n+1)	R11(n+1)
RE12	G10(n)	G10(n)	RE22	G10(n+1)	G10(n+1)
RE13	G11(n)	G11(n)	RE23	G11(n+1)	G11(n+1)
RE14	B10(n)	B10(n)	RE24	B10(n+1)	B10(n+1)
RE15	B11(n)	B11(n)	RE25	B11(n+1)	B11(n+1)
RE16	CONT12(n)	CONT12(n)	RE26	CONT12(n+1)	CONT12(n+1)

LVDS Input Data Mapping (Continued)

Table 12. LVDS Input Data Mapping (Dual-in/Dual-out mode, MODE<1:0> = LL)

1st Pixel Data			2nd Pixel Data		
LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)	LVDS Input Data (1st Pixel Data)	Mapping Mode1 (Output Pin Name)	Mapping Mode2 (Output Pin Name)
RA10	R14	R12	RA20	R24	R22
RA11	R15	R13	RA21	R25	R23
RA12	R16	R14	RA22	R26	R24
RA13	R17	R15	RA23	R27	R25
RA14	R18	R16	RA24	R28	R26
RA15	R19	R17	RA25	R29	R27
RA16	G14	G12	RA26	G24	G22
RB10	G15	G13	RB20	G25	G23
RB11	G16	G14	RB21	G26	G24
RB12	G17	G15	RB22	G27	G25
RB13	G18	G16	RB23	G28	G26
RB14	G19	G17	RB24	G29	G27
RB15	B14	B12	RB25	B24	B22
RB16	B15	B13	RB26	B25	B23
RC10	B16	B14	RC20	B26	B24
RC11	B17	B15	RC21	B27	B25
RC12	B18	B16	RC22	B28	B26
RC13	B19	B17	RC23	B29	B27
RC14	HSYNC	HSYNC	RC24	N/A	
RC15	VSYNC	VSYNC	RC25		
RC16	DE	DE	RC26		
RD10	R12	R18	RD20	R22	R28
RD11	R13	R19	RD21	R23	R29
RD12	G12	G18	RD22	G22	G28
RD13	G13	G19	RD23	G23	G29
RD14	B12	B18	RD24	B22	B28
RD15	B13	B19	RD25	B23	B29
RD16	CONT11	CONT11	RD26	CONT21	CONT21
RE10	R10	R10	RE20	R20	R20
RE11	R11	R11	RE21	R21	R21
RE12	G10	G10	RE22	G20	G20
RE13	G11	G11	RE23	G21	G21
RE14	B10	B10	RE24	B20	B20
RE15	B11	B11	RE25	B21	B21
RE16	CONT12	CONT12	RE26	CONT22	CONT22

Typical Application Circuit (24bit・Dual-in/Dual-out mode)

[Example]
BU90T82: LVCMOS Data Input (24bit) / rising edge
LVDS 350mV swing output / VESA mapping / Dual-out
BU90R102: LVDS 350mV swing input / VESA mapping / Dual-in
LVCMOS Data Input (48bit) / Dual-out / falling edge

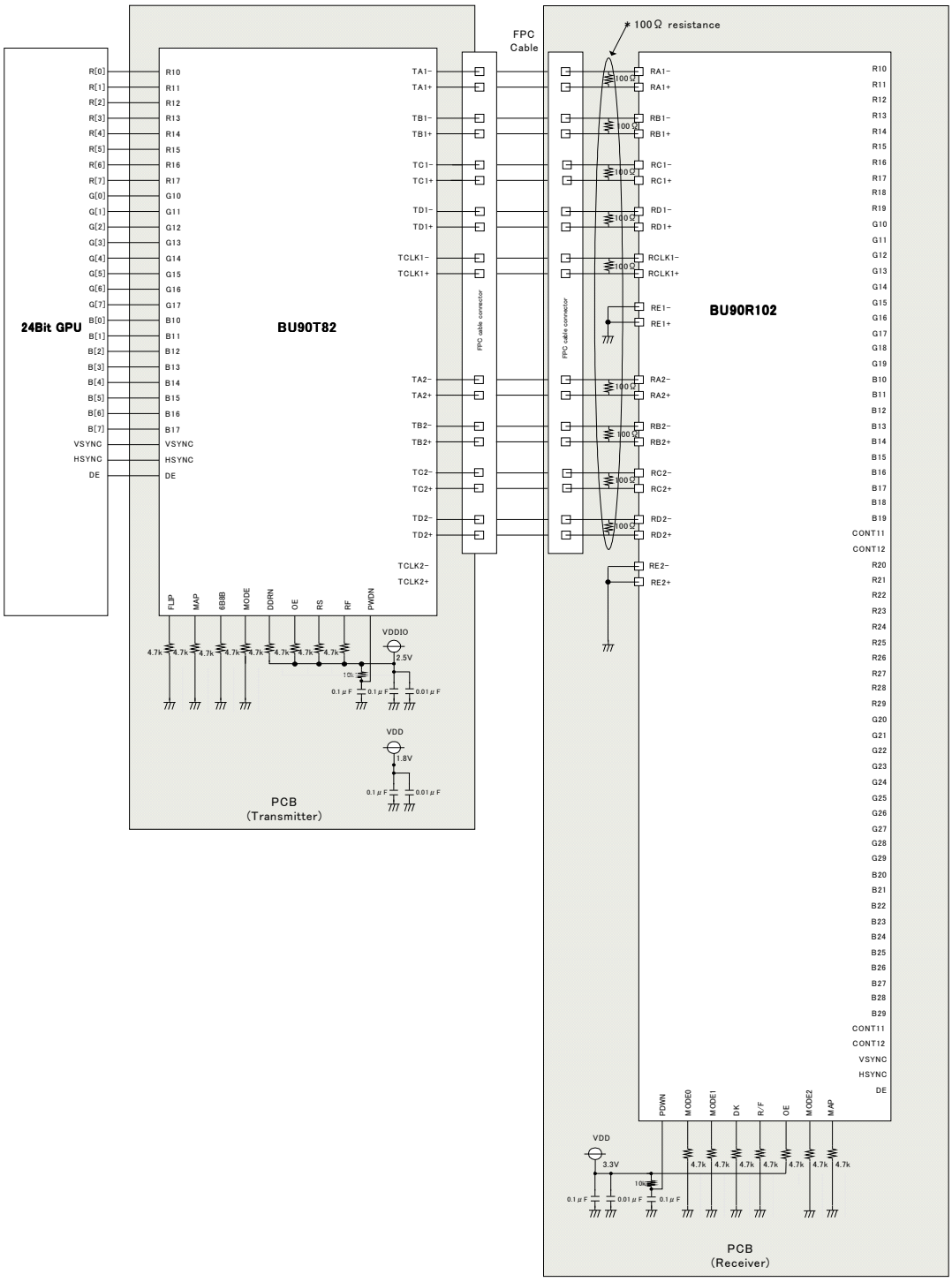


Figure 16. Typical Application Circuit (24bit Dual-in/Dual-out mode)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Unused Input Pins

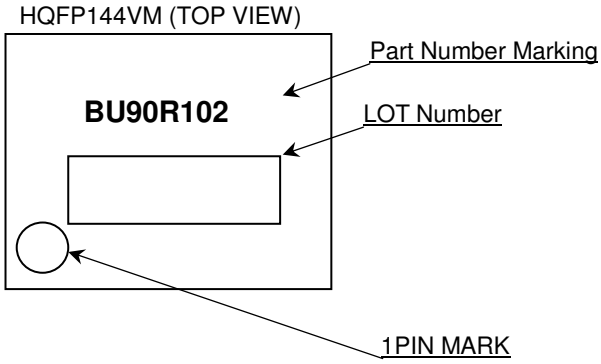
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Ordering Information

B U 9 0 R 1 0 2 - [ ]

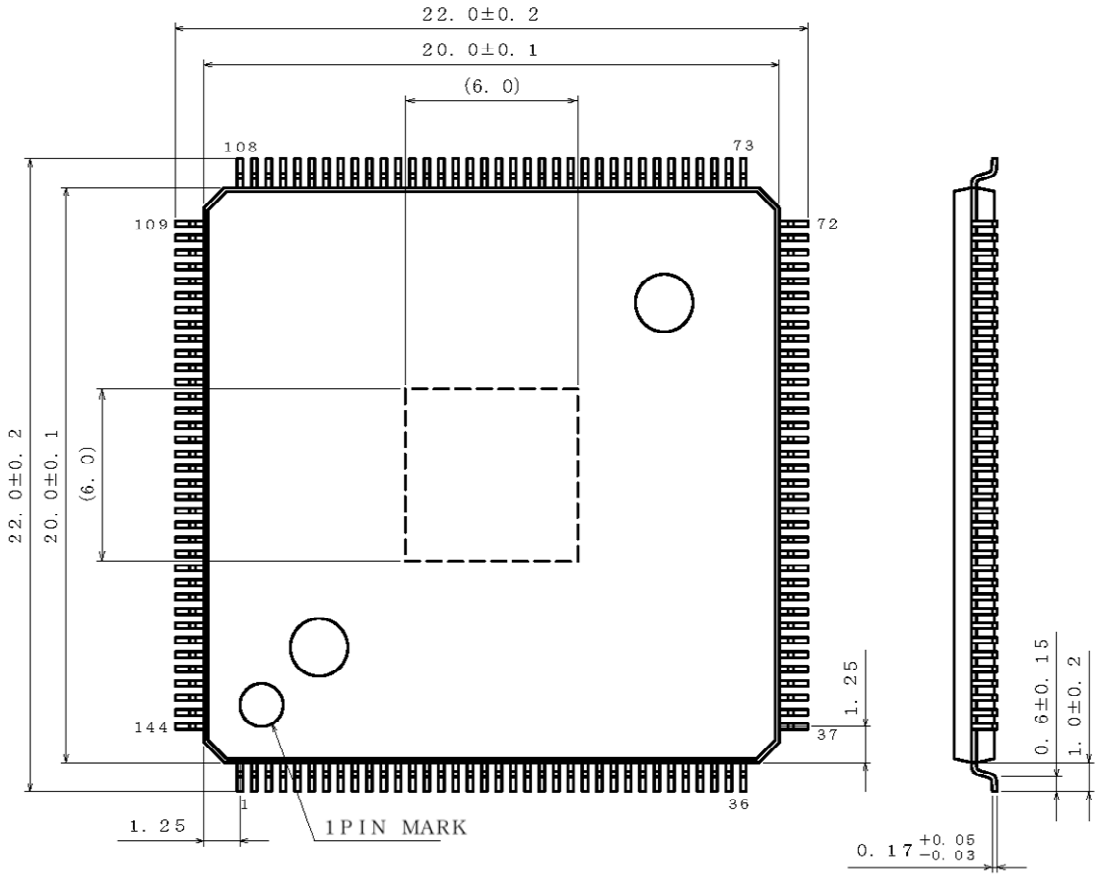
Part No.

Marking Diagrams



Physical Dimension, Tray Information

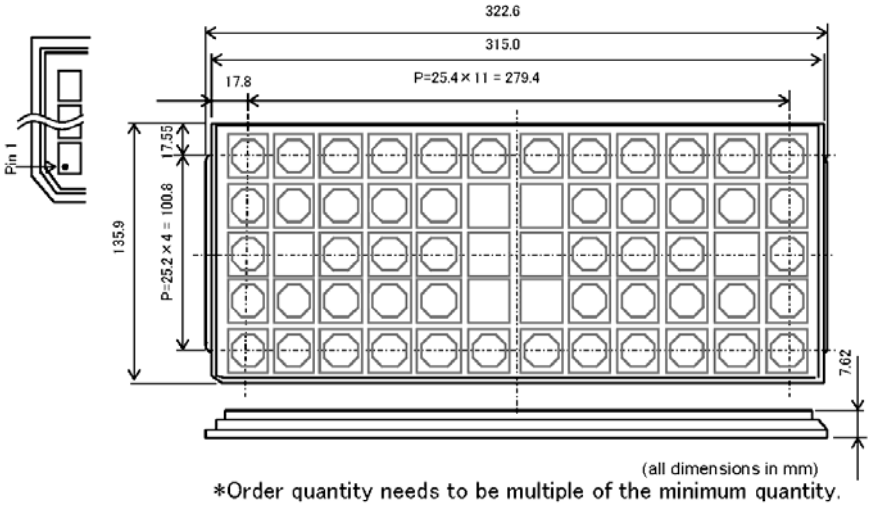
Package Name	HQFP144VM



(UNIT : mm)
PKG : HQFP144VM
Drawing No. EX001-0001

< Tray Information >

Tray	Tray(with dry pack)
Quantity	60pcs
Direction of feed	Direction of products is fixed in a tray



(all dimensions in mm)
*Order quantity needs to be multiple of the minimum quantity.