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LCD Segment Drivers

Multi-function LCD Segment Drivers

BU91510KV-M **MAX 216 Segment(54SEG x 4COM)**

General Description

The BU91510KV-M is 1/4 or 1/3 Duty General-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The BU91510KV-M can drive up to 216 LCD Segments directly. The BU91510KV-M can also control up to 6 General-purpose output pins / 6 PWM output pins.

Features

- AEC-Q100 Qualified (*Note 1*)
- Either 1/4 or 1/3 Duty can be selected with the Serial Control Data.
  - 1/4 Duty Drive: up to 216 Segments
  - 1/3 Duty Drive: up to 162 Segments
- Serial Data Control of Frame Frequency for Common and Segment Output Waveforms
- Serial Data Control of Switching between the Segment Output Pin, PWM Output Pin and General-purpose Output Pin Functions(Max 6 Pin)
- Built-in OSC Circuit
- The INHb Pin can Force the Display to the off State.
- Integrated Voltage Detected type Power on Reset (VDET) circuit
- No External Component
- Low Power Consumption Design

(*Note 1*) Grade 2

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments: 216 Segments
- Display Duty: 1/3, 1/4 Selectable
- Bias: 1/2, 1/3 Selectable
- Interface: 3wire Serial Interface

Package

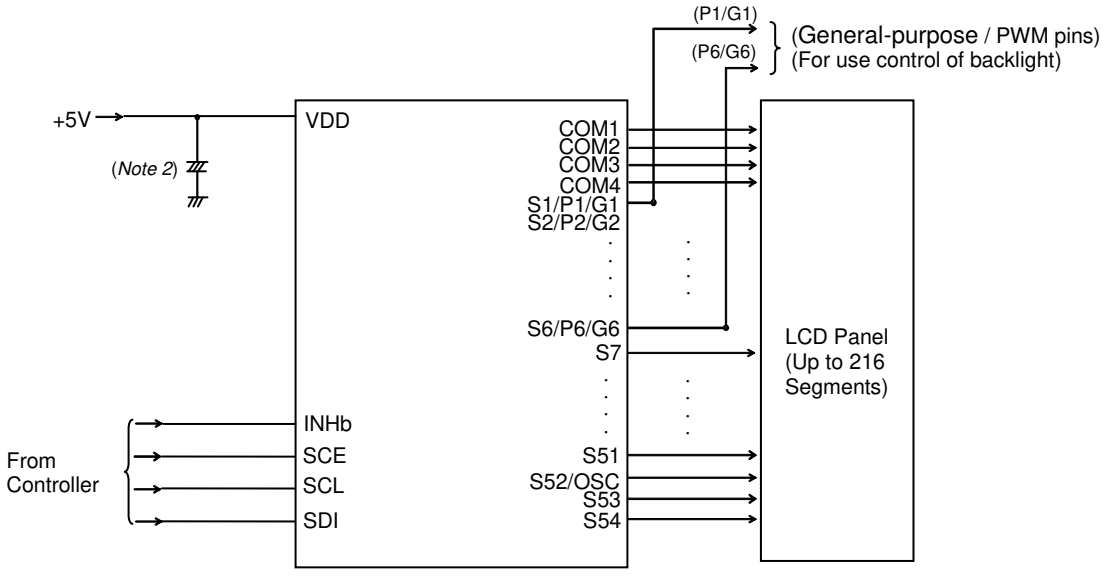
W(Typ) x D(Typ) x H(Max)

VQFP64
12.00mm x 12.00mm x 1.60mm

Applications

- Car Audio, Home Electrical Appliance, Meter Equipment etc.

Typical Application Circuit



(*Note 2*) Insert capacitors between VDD and VSS C ≥ 0.1µF

Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Block Diagram

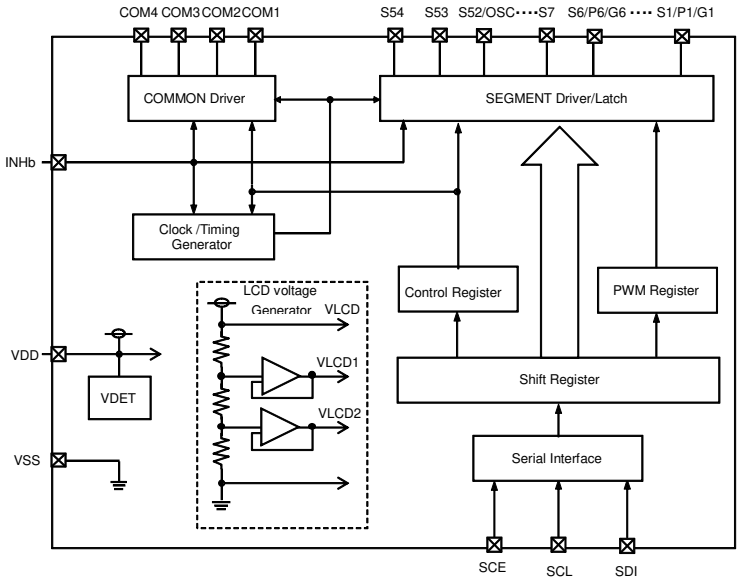


Figure 2. Block Diagram

Pin Arrangement

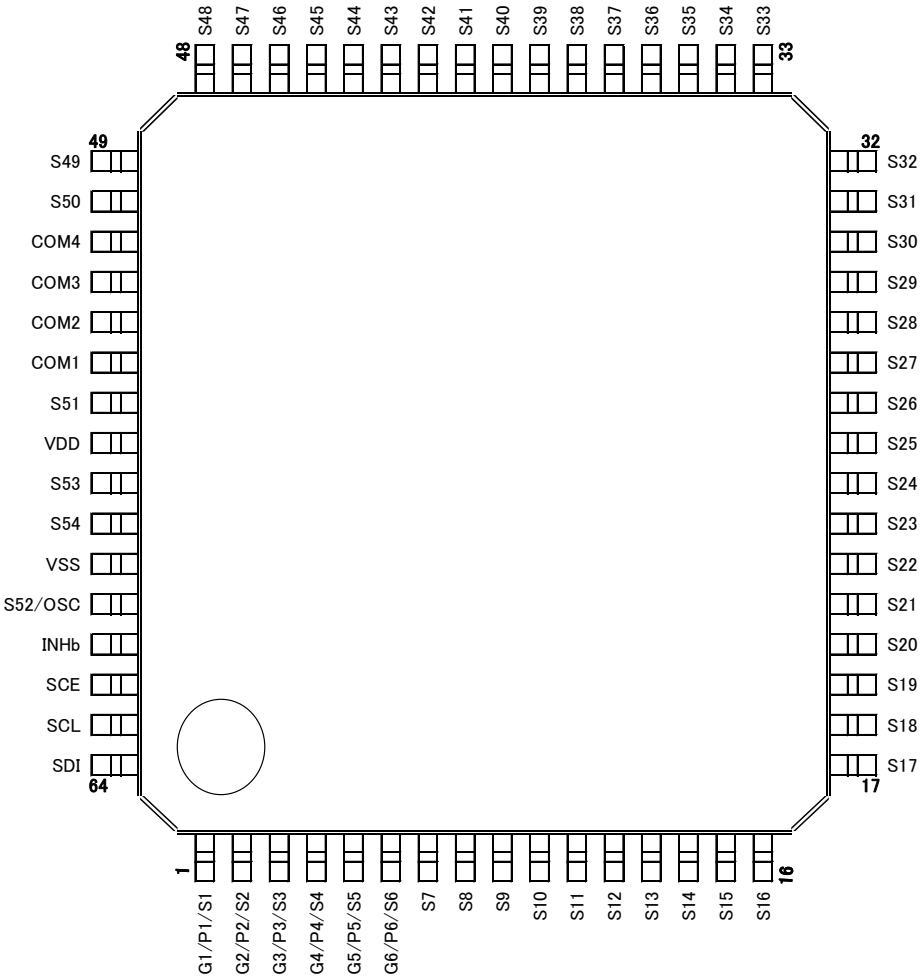


Figure 3. Pin Configuration (TOP VIEW)

Absolute Maximum Ratings (VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	VDD	VDD	-0.3 to +7.0	V
Input Voltage	V_{IN1}	SCE, SCL, SDI, INHb, OSC	-0.3 to +7.0	V
Allowable Loss	Pd	-	1.00(*Note*)	W
Operating Temperature	Topr	-	-40 to +105	°C
Storage Temperature	Tstg	-	-55 to +125	°C

(*Note*) When use more than Ta=25°C, subtract 10mW per degree. (Using ROHM standard board)
(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

Caution1: Operating the IC over absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Recommended Operating Conditions (Ta = -40°C to +105°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Supply Voltage	VDD	VDD	2.7	-	6.0	V

Electrical Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	V_H	SCE, SCL, SDI, INHb, OSC	-	-	0.03VDD	-	V
Power On Detection Voltage	V_{DET}	VDD	-	1.4	1.8	2.2	V
"H" Level Input Voltage	V_{IH1}	SCE, SCL, SDI, INHb, OSC	VDD=4.0V to 6.0V	0.4VDD	-	VDD	V
	V_{IH2}	SCE, SCL, SDI, INHb, OSC	VDD=2.7V to 4.0V	0.8VDD	-	VDD	V
"L" Level Input Voltage	V_{IL1}	SCE, SCL, SDI, INHb, OSC	-	0	-	0.2VDD	V
"H" Level Input Current	I_{IH1}	SCE, SCL, SDI, INHb, OSC	V_I = 6.0V	-	-	5.0	µA
"L" Level Input Current	I_{IL1}	SCE, SCL, SDI, INHb, OSC	V_I = 0V	-5.0	-	-	µA
"H" Level Output Voltage	V_{OH1}	S1 to S54	I_O = -20µA	VDD-0.9	-	-	V
	V_{OH2}	COM1 to COM4	I_O = -100µA	VDD-0.9	-	-	
	V_{OH3}	P1/G1 to P6/G6	I_O = -1mA	VDD-0.9	-	-	
"L" Level Output Voltage	V_{OL1}	S1 to S54	I_O = 20µA	-	-	0.9	V
	V_{OL2}	COM1 to COM4	I_O = 100µA	-	-	0.9	
	V_{OL3}	P1/G1 to P6/G6	I_O = 1mA	-	-	0.9	
Middle Level Output Voltage	V_{MID1}	S1 to S54	1/2 Bias I_O = ±20µA	1/2VDD -0.9	-	1/2VDD +0.9	V
	V_{MID2}	COM1 to COM4	1/2 Bias I_O = ±100µA	1/2VDD -0.9	-	1/2VDD +0.9	
	V_{MID3}	S1 to S54	1/3 Bias I_O = ±20µA	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID4}	S1 to S54	1/3 Bias I_O = ±20µA	1/3VDD -0.9	-	1/3VDD +0.9	
	V_{MID5}	COM1 to COM4	1/3 Bias I_O = ±100µA	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID6}	COM1 to COM4	1/3 Bias I_O = ±100µA	1/3VDD -0.9	-	1/3VDD +0.9	
Current Drain	I_{DD1}	VDD	Power-saving mode	-	-	15	µA
	I_{DD2}	VDD	VDD = 5.0V Output open 1/2 Bias Frame Frequency = 80Hz	-	70	150	
	I_{DD3}	VDD	VDD = 5.0V Output open 1/3 Bias Frame Frequency = 80Hz	-	95	200	

Oscillation Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency1	f_{OSC1}	-	VDD = 2.7V to 6.0V	150	-	360	kHz
Oscillator Frequency2	f_{OSC2}		VDD = 5.0V	255	300	345	kHz
External Clock Frequency(*Note 3*)	f_{OSC3}	OSC	External clock mode (OC=1)	30	-	600	kHz
External Clock Rise Time	tr			-	160	-	ns
External Clock Fall Time	tf			-	160	-	ns
External Clock Duty	t_{DTY}			30	50	70	%

(*Note 3*) Frame frequency is decided external clock and dividing ratio of FC0 to FC2 setting.

[Reference Data]

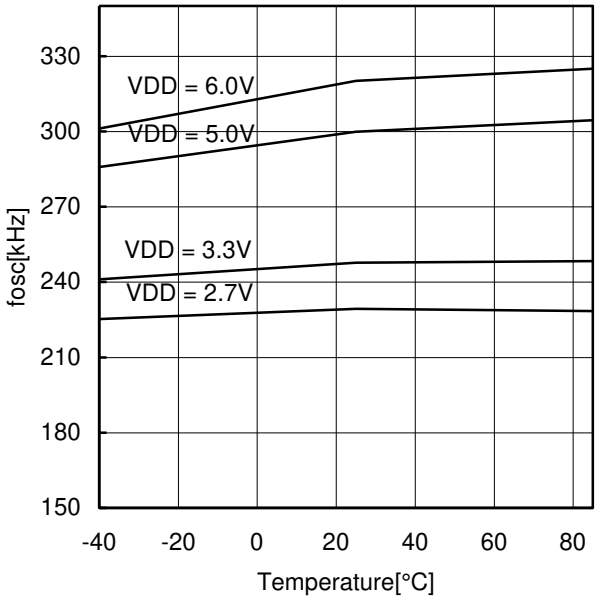
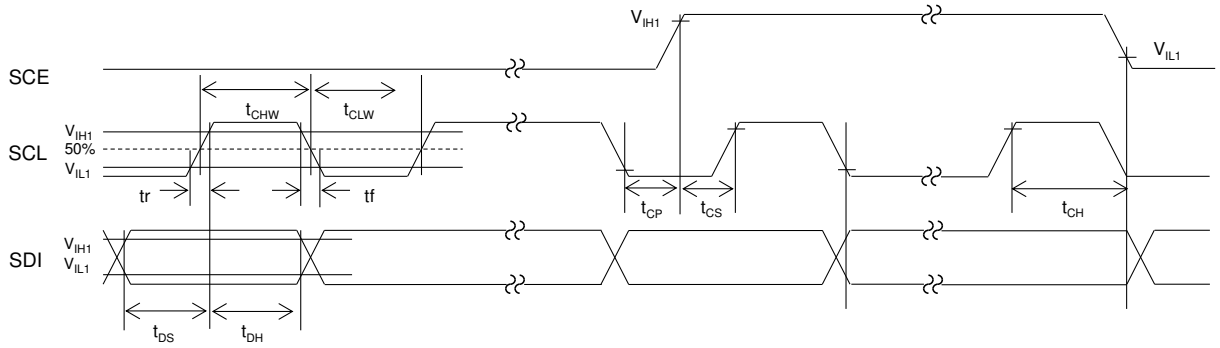


Figure 4. Oscillator Frequency Typical Temperature Characteristics

MPU Interface Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	t_{DS}	SCL, SDI	-	160	-	-	ns
Data Hold Time	t_{DH}	SCL, SDI	-	160	-	-	ns
SCE Wait Time	t_{CP}	SCE, SCL	-	160	-	-	ns
SCE Setup Time	t_{CS}	SCE, SCL	-	160	-	-	ns
SCE Hold Time	t_{CH}	SCE, SCL	-	160	-	-	ns
High-Level Clock Pulse Width	t_{CHW}	SCL	-	160	-	-	ns
Low-Level Clock Pulse Width	t_{CLW}	SCL	-	160	-	-	ns
Rise Time	tr	SCE, SCL, SDI	-	-	160	-	ns
Fall Time	tf	SCE, SCL, SDI	-	-	160	-	ns
INH Switching Time	t_C	INHb, SCE	-	10	-	-	µs

1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

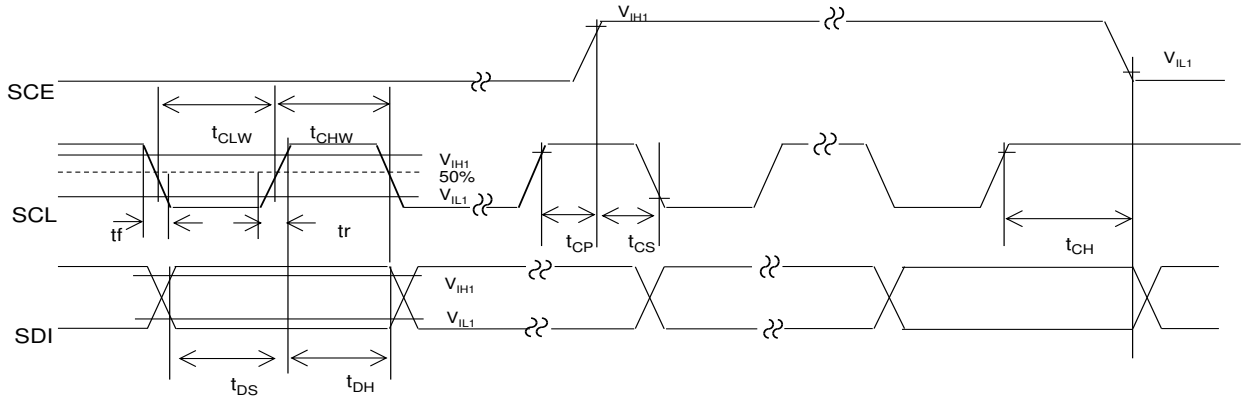


Figure 5. Serial Interface Timing

Pin Description

Pin Name	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S6/P6/G6	1 to 6	Segment output for displaying the Display Data transferred by serial data input. The S1/P1/G1 to S6/P6/G6 pins can also be used as General-purpose or PWM output when so set up by the control data.	-	O	OPEN
S7 to S51, S53, S54	7 to 50 55,57,58	Segment output for displaying the Display Data transferred by serial data input.		O	OPEN
COM1 to COM4	51 to 54	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
S52/OSC	60	Segment output for displaying the Display Data transferred by serial data input. The S52/OSC pin can be used external clock input pin when set up by the control data.	-	I O	VSS OPEN
SCE SCL SDI	62 63 64	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Synchronization clock SDI: Transfer data	H ↑ -	I I I	VSS VSS VSS
INHb	61	Display Off control input INHb = low (VSS) ...Display forced off S1/P1/G1 to S6/P6/G6 = low (VSS) S7 to S54 = low (VSS) COM1 to COM4 = low (VSS) Shuts off current to the LCD drive bias voltage generation divider resistors. Stop the internal oscillation circuit. INHb = high (VDD)...Display On However, serial data transfer is possible when the display is forced off.	L	I	VDD
VDD	56	Power supply pin for the logic circuit block. A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	59	Power supply pin. Must be connected to ground.	-	-	-

IO Equivalence Circuit

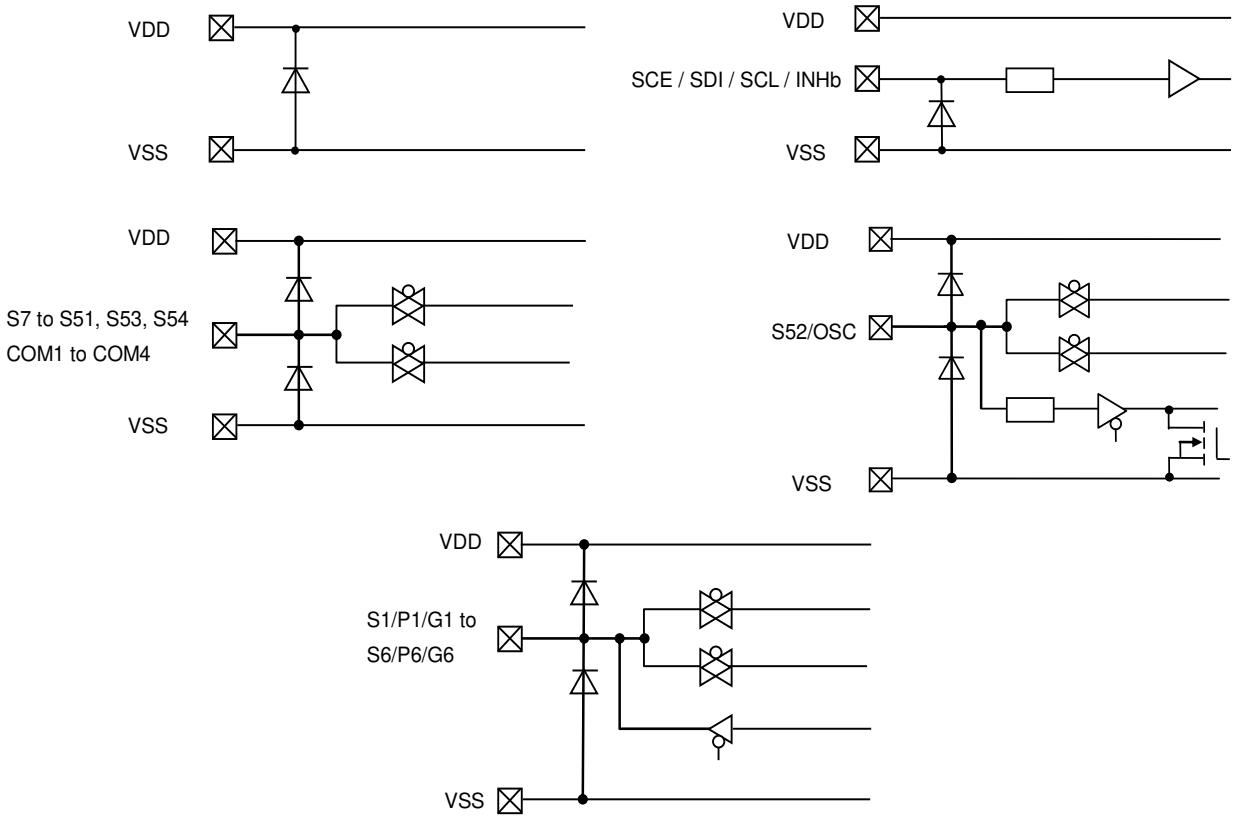


Figure 6. I/O Equivalence Circuit

Serial Data Transfer Formats

1. 1/4 Duty

(1)When SCL is stopped at the low level

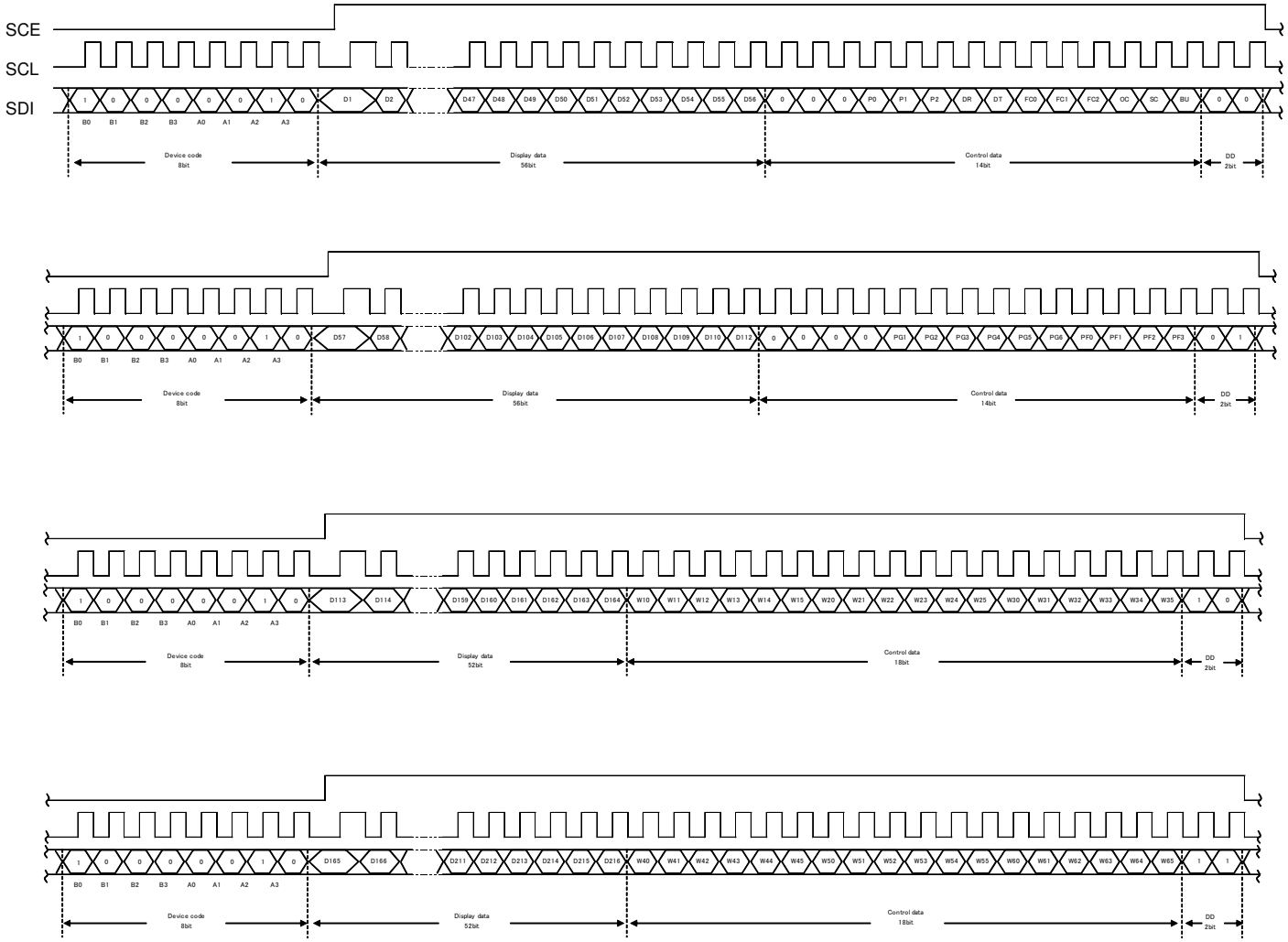


Figure 7. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

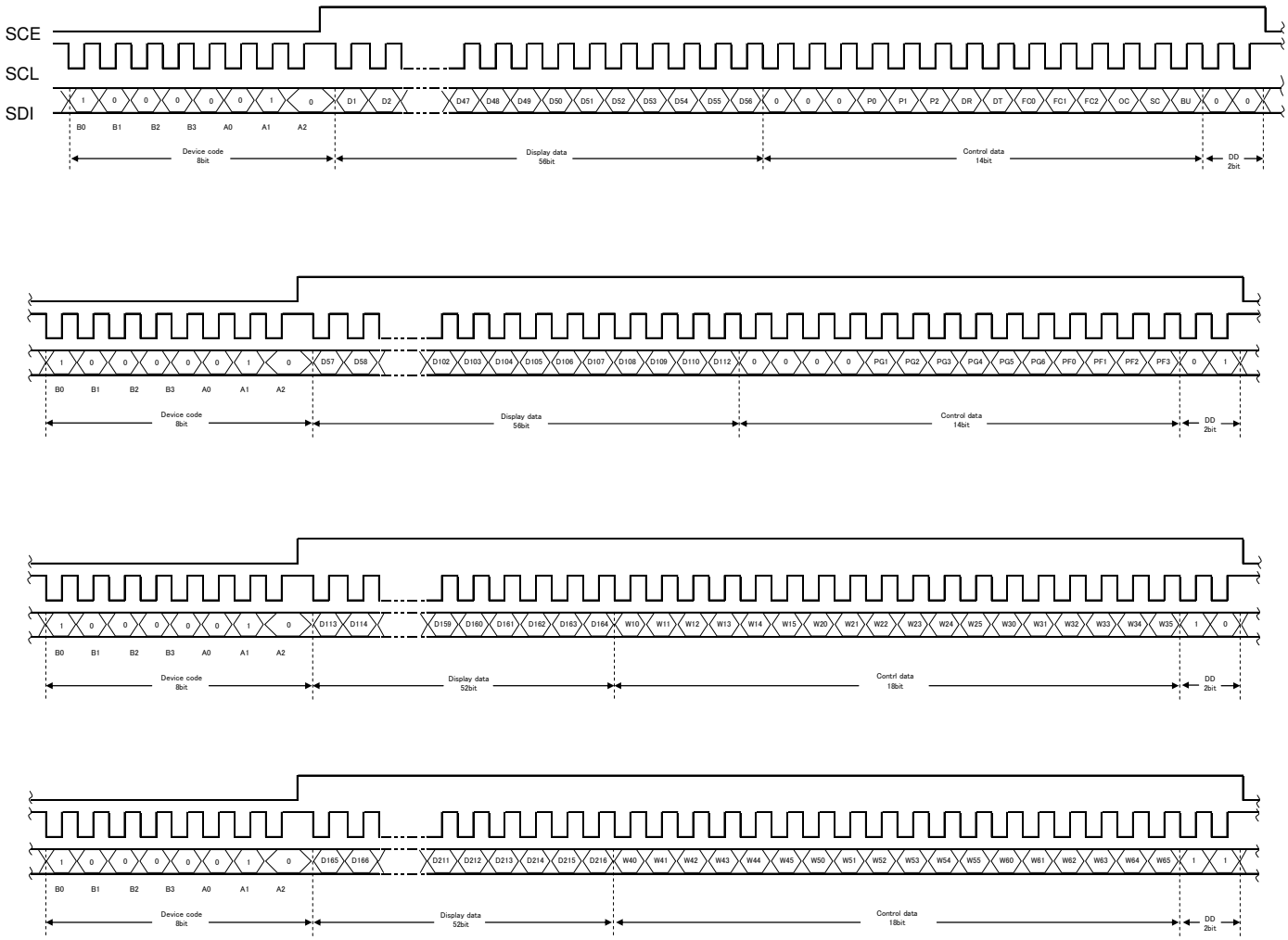


Figure 8. 3-SPI Data Transfer Format

Device code ·····“41H”
D1 to D216·····Display Data
P0 to P2 ·····Segment / PWM / General-purpose output pin switching control data
DR ·····1/3 Bias drive or 1/2 Bias drive switching control data
DT·····1/4 Duty drive or 1/3 Duty drive switching control data
FC0 to FC2 ·····Common / Segment output waveform frame frequency switching control data
OC ·····Internal oscillator operating mode / External clock operating mode switching control data
SC·····Segment on / off switching control data
BU·····Normal mode / power-saving mode switching control data
PG1 to PG6·····PWM / General-purpose output switching control data
PF0 to PF3·····PWM output frame frequency switching control data
W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55, W60 to W65 ·····PWM output duty switching control data
DD ·····Direction Data

Serial Data Transfer Formats – continued

2. 1/3 Duty

(1) When SCL is stopped at the low level

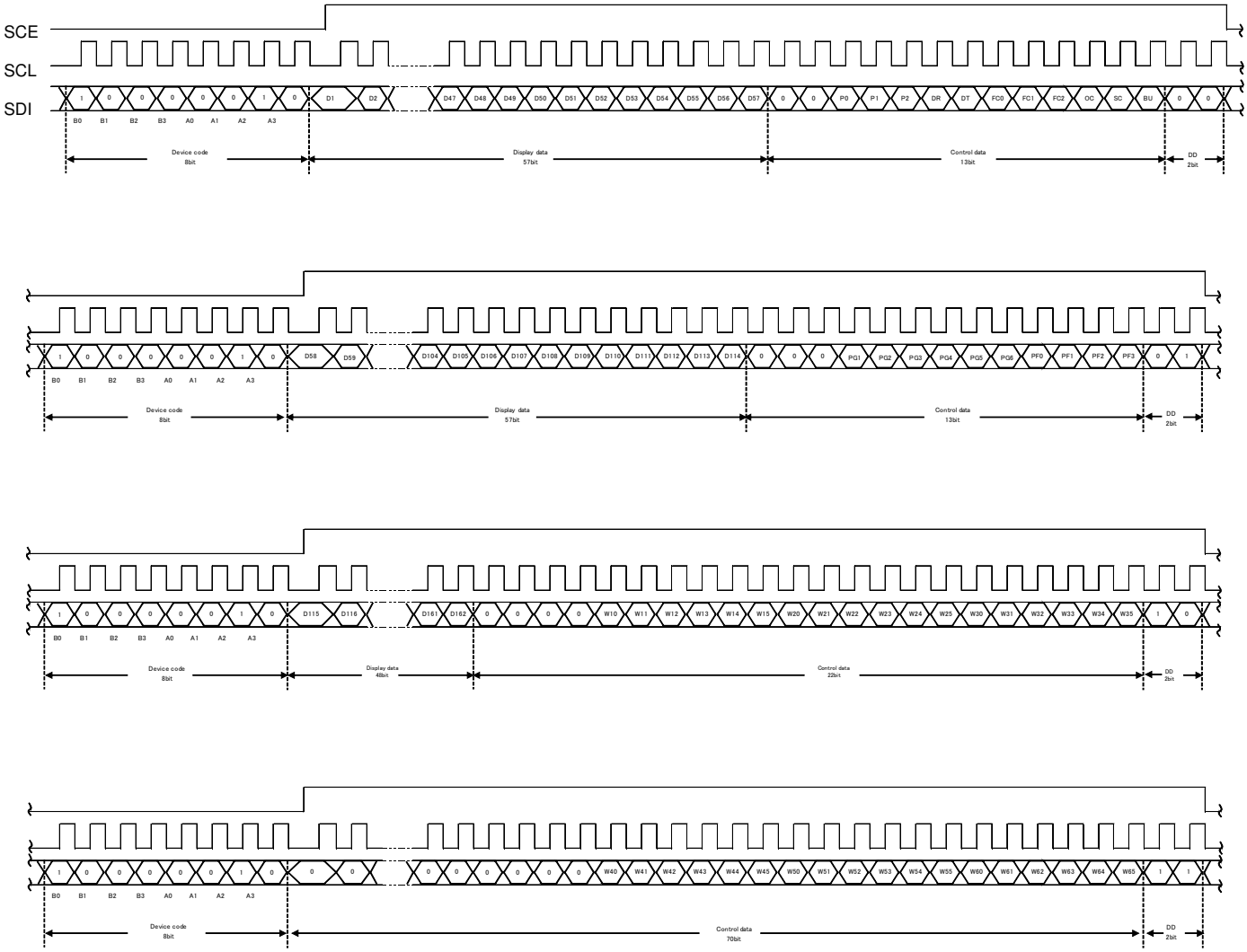


Figure 9. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level

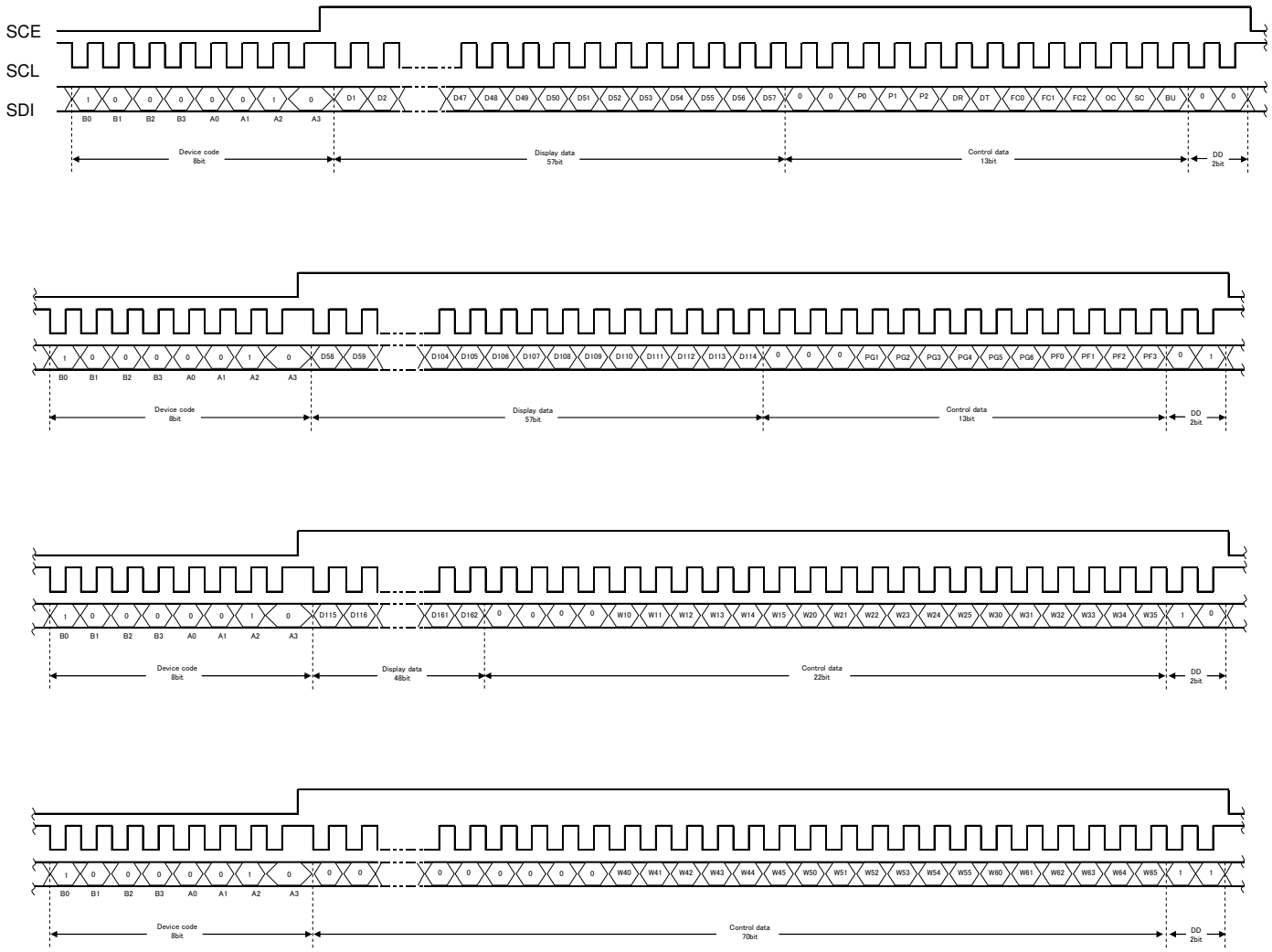


Figure 10. 3-SPI Data Transfer Format

Device code ……“41H”
D1 to D162……Display Data
P0 to P2 ……Segment / PWM / General-purpose output pin switching control data
DR ……1/3 Bias drive or 1/2 Bias drive switching control data
DT……1/4 Duty drive or 1/3 Duty drive switching control data
FC0 to FC2 ……Common / Segment output waveform frame frequency switching control data
OC ……Internal oscillator operating mode / External clock operating mode switching control data
SC……Segment on / off switching control data
BU……Normal mode/power-saving mode switching control data
PG1 to PG6……PWM / General-purpose output switching control data
PF0 to PF3……PWM output frame frequency switching control data
W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55, W60 to W65
……PWM output duty switching control data
DD ……Direction Data

Control Data Functions

1. P0, P1 and P2: Segment / PWM / General-purpose output pin switching control data

These control bits are used to select the function of the S1/P1/G1 to S6/P6/G6 output pins (Segment Output Pins or PWM Output Pins or General-purpose Output Pins).
Please refer to the table below.

P0	P1	P2	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	Reset Condition
0	0	0	S1	S2	S3	S4	S5	S6	○
0	0	1	P1/G1	S2	S3	S4	S5	S6	-
0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	-
0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	-
1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	-
1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	-
1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	-
1	1	1	S1	S2	S3	S4	S5	S6	-

PWM output or General-purpose Output Pin is selected by PGx(x=1 to 6) control data bit.

When the General-purpose Output Pin Function is selected, the correspondence between the output pins and the respective Display Data is given in the table below.

Output Pins	Corresponding Display Data	
	1/4 Duty Mode	1/3 Duty Mode
S1/P1/G1	D1	D1
S2/P2/G2	D5	D4
S3/P3/G3	D9	D7
S4/P4/G4	D13	D10
S5/P5/G5	D17	D13
S6/P6/G6	D21	D16

When the General-purpose Output Pin Function is selected, the respective output pin outputs a “HIGH” level when its corresponding display data is set to “1”. Likewise, it will output a “LOW” level, if its corresponding display data is set to “0”. For example, S4/P4/G4 is used as a General-purpose Output Pin in case of 1/4 Duty, if its corresponding Display Data – D13 is set to “1”, then S4/P4/G4 will output “HIGH” level. Likewise, if D13 is set to “0”, then S4/P4/G4 will output “LOW” level.

2. DR: 1/3 Bias drive or 1/2 Bias drive switching control data

This control data bit selects either 1/3 Bias drive or 1/2 Bias drive.

DR	Bias Drive Scheme	Reset Condition
0	1/3 Bias drive	○
1	1/2 Bias drive	-

3. DT: 1/4 Duty drive or 1/3 Duty drive switching control data

This control data bit selects either 1/4 Duty drive or 1/3 Duty drive.

DT	Duty Drive Scheme	Reset Condition
0	1/4 Duty drive	○
1	1/3 Duty drive	-

4. FC0, FC1 and FC2: Frame frequency switching control data

These control data bits set the frame frequency for common and segment output waveforms.

FC0	FC1	FC2	Frame Frequency fo(Hz)	Reset Condition
0	0	0	f_{OSC}/6144	○
0	0	1	f_{OSC}/5376	-
0	1	0	f_{OSC}/4608	-
0	1	1	f_{OSC}/3840	-
1	0	0	f_{OSC}/3072	-
1	0	1	f_{OSC}/2304	-
1	1	0	f_{OSC}/1920	-
1	1	1	f_{OSC}/1536	-

(*Note*) f_{OSC}: Internal oscillation frequency (300kHz Typ)

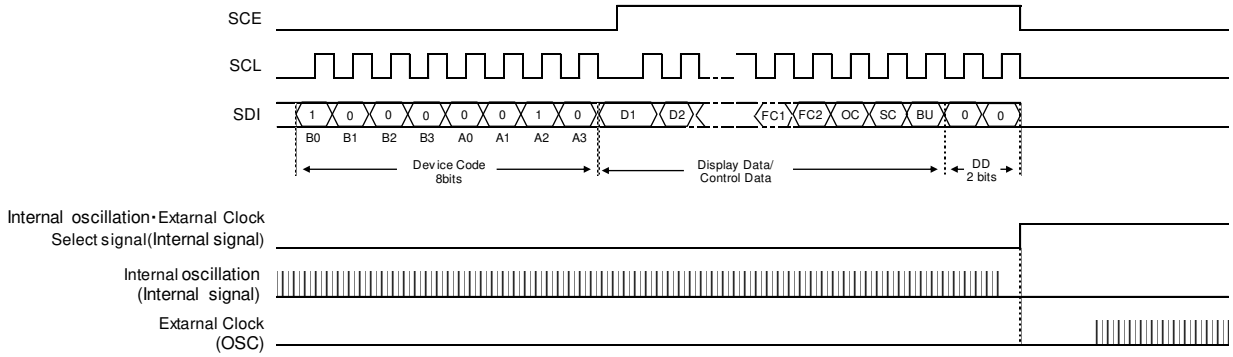
Control Data Functions – continued

5. OC: Internal oscillator operating mode / External clock operating mode switching control data

OC	Operating Mode	In/Out Pin(S52/OSC) Status	Reset Condition
0	Internal oscillator	S52 (segment output)	○
1	External Clock	OSC (clock input)	-

<External Clock input timing function>

Internal oscillation / external clock select signal behavior is below.
Input external clock after serial data sending.



6. SC: Segment on/off switching control data

This control data bit controls the on/off state of the segments.

SC	Display State	Reset Condition
0	On	-
1	Off	○

Note that when the segments are turned off by setting SC to “1”, the segments are turned off by outputting segment off waveforms from the segment output pins.

7. BU: Normal mode / Power-saving mode switching control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode	Reset Condition
0	Normal Mode	-
1	Power-saving Mode	○

Power-saving mode status: S1/P1/G1 to S6/P6/G6 = active only General-purpose output
S7 to S54 = low(VSS)
COM1 to COM4 = low(VSS)
Shut off current to the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible when Power-saving mode.

Control Data Functions – continued

8. PG1, PG2, PG3, PG4, PG5 and PG6: PWM / General-purpose output switching control data

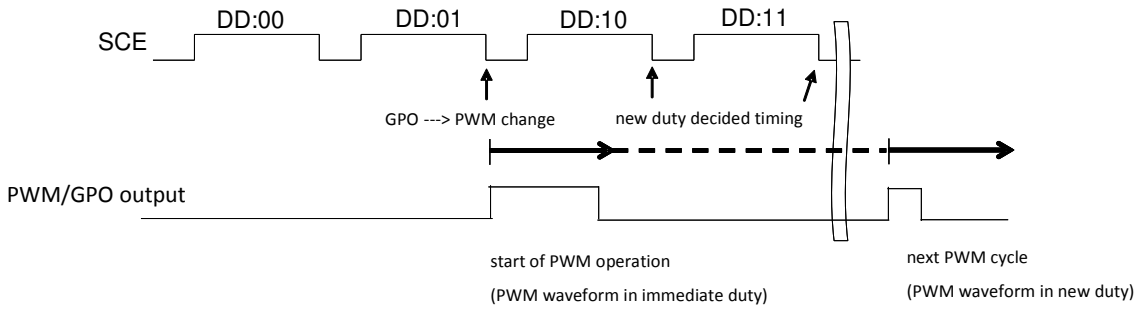
This control data bit select either PWM output or General-purpose output of Sx/Px/Gx pins.(x=1 to 6)

PGx(x=1 to 6)	Mode	Reset Condition
0	PWM output	○
1	General-purpose output	-

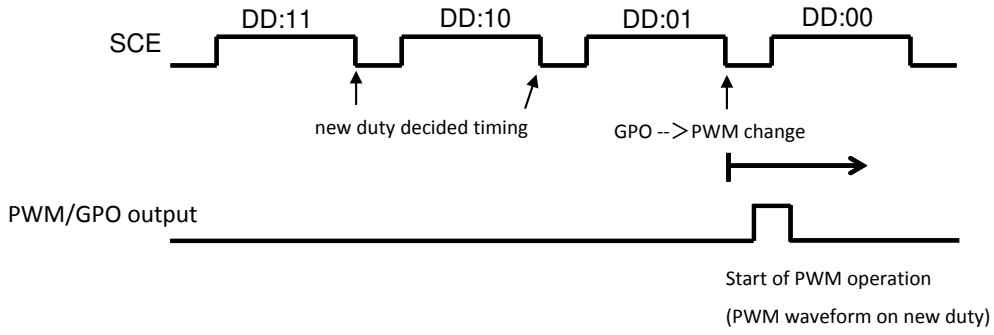
[PWM<->GPO Changing function]

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD:01 during GPO ---> PWM change.
- Please take care of reflect timing of new duty setting of DD:10, DD:11 is from the next PWM.



In order to avoid this operation, please input commands reversely as below.



Control Data Functions – continued

9. PF0, PF1, PF2 and PF3: PWM output frame frequency switching control data

These control data bits set the frame frequency for PWM output.

PF0	PF1	PF2	PF3	PWM Output Frame Frequency fp(Hz)	Reset Condition
0	0	0	0	fosc/2048	○
0	0	0	1	fosc/1920	-
0	0	1	0	fosc/1792	-
0	0	1	1	fosc/1664	-
0	1	0	0	fosc/1536	-
0	1	0	1	fosc/1408	-
0	1	1	0	fosc/1280	-
0	1	1	1	fosc/1152	-
1	0	0	0	fosc/1024	-
1	0	0	1	fosc/896	-
1	0	1	0	fosc/768	-
1	0	1	1	fosc/640	-
1	1	0	0	fosc/512	-
1	1	0	1	fosc/384	-
1	1	1	0	fosc/256	-
1	1	1	1	fosc/128	-

10. W10 to W15, W20 to W25, W30 to W35, W40 to W45, W50 to W55 and W60 to W65*(Note)*: PWM output duty switching control data

These control data bits set the high level pulse width for PWM output.

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	PWM Duty	Reset Condition
0	0	0	0	0	0	(1/64) x Tp	○
1	0	0	0	0	0	(2/64) x Tp	-
0	1	0	0	0	0	(3/64) x Tp	-
1	1	0	0	0	0	(4/64) x Tp	-
0	0	1	0	0	0	(5/64) x Tp	-
1	0	1	0	0	0	(6/64) x Tp	-
0	1	1	0	0	0	(7/64) x Tp	-
1	1	1	0	0	0	(8/64) x Tp	-
0	0	0	1	0	0	(9/64) x Tp	-
1	0	0	1	0	0	(10/64) x Tp	-
0	1	0	1	0	0	(11/64) x Tp	-
1	1	0	1	0	0	(12/64) x Tp	-
0	0	1	1	0	0	(13/64) x Tp	-
1	0	1	1	0	0	(14/64) x Tp	-
0	1	1	1	0	0	(15/64) x Tp	-
・・・	・・・	・・・	・・・	・・・	・・・	・・・	-
1	0	0	0	1	1	(50/64) x Tp	-
0	1	0	0	1	1	(51/64) x Tp	-
1	1	0	0	1	1	(52/64) x Tp	-
0	0	1	0	1	1	(53/64) x Tp	-
1	0	1	0	1	1	(54/64) x Tp	-
0	1	1	0	1	1	(55/64) x Tp	-
1	1	1	0	1	1	(56/64) x Tp	-
0	0	0	1	1	1	(57/64) x Tp	-
1	0	0	1	1	1	(58/64) x Tp	-
0	1	0	1	1	1	(59/64) x Tp	-
1	1	0	1	1	1	(60/64) x Tp	-
0	0	1	1	1	1	(61/64) x Tp	-
1	0	1	1	1	1	(62/64) x Tp	-
0	1	1	1	1	1	(63/64) x Tp	-
1	1	1	1	1	1	(64/64) x Tp	-

(Note) W10 to W15:S1/P1/G1 PWM duty data
W20 to W25:S2/P2/G2 PWM duty data
W30 to W35:S3/P3/G3 PWM duty data
W40 to W45:S4/P4/G4 PWM duty data
W50 to W55:S5/P5/G5 PWM duty data
W60 to W65:S6/P6/G6 PWM duty data

n = 1 to 6
Tp = 1/fp

Display Data and Output Pin Correspondence

1. 1/4 Duty

Output Pin*(Note)*	COM1	COM2	COM3	COM4
S1/P1/G1	D1	D2	D3	D4
S2/P2/G2	D5	D6	D7	D8
S3/P3/G3	D9	D10	D11	D12
S4/P4/G4	D13	D14	D15	D16
S5/P5/G5	D17	D18	D19	D20
S6/P6/G6	D21	D22	D23	D24
S7	D25	D26	D27	D28
S8	D29	D30	D31	D32
S9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

Display Data and Output Pin Correspondence – continued

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data				State of S21 Output Pin
D81	D82	D83	D84	
0	0	0	0	LCD Segments corresponding to COM1 to COM4 are OFF.
0	0	0	1	LCD Segment corresponding to COM4 is ON.
0	0	1	0	LCD Segment corresponding to COM3 is ON.
0	0	1	1	LCD Segments corresponding to COM3 and COM4 are ON.
0	1	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	1	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	1	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	1	LCD Segments corresponding to COM2, COM3 and COM4 are ON.
1	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	1	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	1	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	1	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	1	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	1	LCD Segments corresponding to COM1, COM2, and COM4 are ON.
1	1	1	0	LCD Segments corresponding to COM1, COM2, and COM3 are ON.
1	1	1	1	LCD Segments corresponding to COM1 to COM 4 are ON.

Display Data and Output Pin Correspondence – continued

2. 1/3 Duty

Output Pin(Note)	COM1	COM2	COM3
S1/P1/G1	D1	D2	D3
S2/P2/G2	D4	D5	D6
S3/P3/G3	D7	D8	D9
S4/P4/G4	D10	D11	D12
S5/P5/G5	D13	D14	D15
S6/P6/G6	D16	D17	D18
S7	D19	D20	D21
S8	D22	D23	D24
S9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D86	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162

(*Note*) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

Display Data and Output Pin Correspondence – continued

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data			State of S21 Output Pin
D61	D62	D63	
0	0	0	LCD Segments corresponding to COM1 to COM3 are OFF.
0	0	1	LCD Segment corresponding to COM3 is ON.
0	1	0	LCD Segment corresponding to COM2 is ON.
0	1	1	LCD Segments corresponding to COM2 and COM3 are ON.
1	0	0	LCD Segment corresponding to COM1 is ON.
1	0	1	LCD Segments corresponding to COM1 and COM3 are ON.
1	1	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	1	LCD Segments corresponding to COM1 to COM3 are ON.

LCD Driving Waveforms
(1/4 Duty 1/3 Bias Drive Scheme)

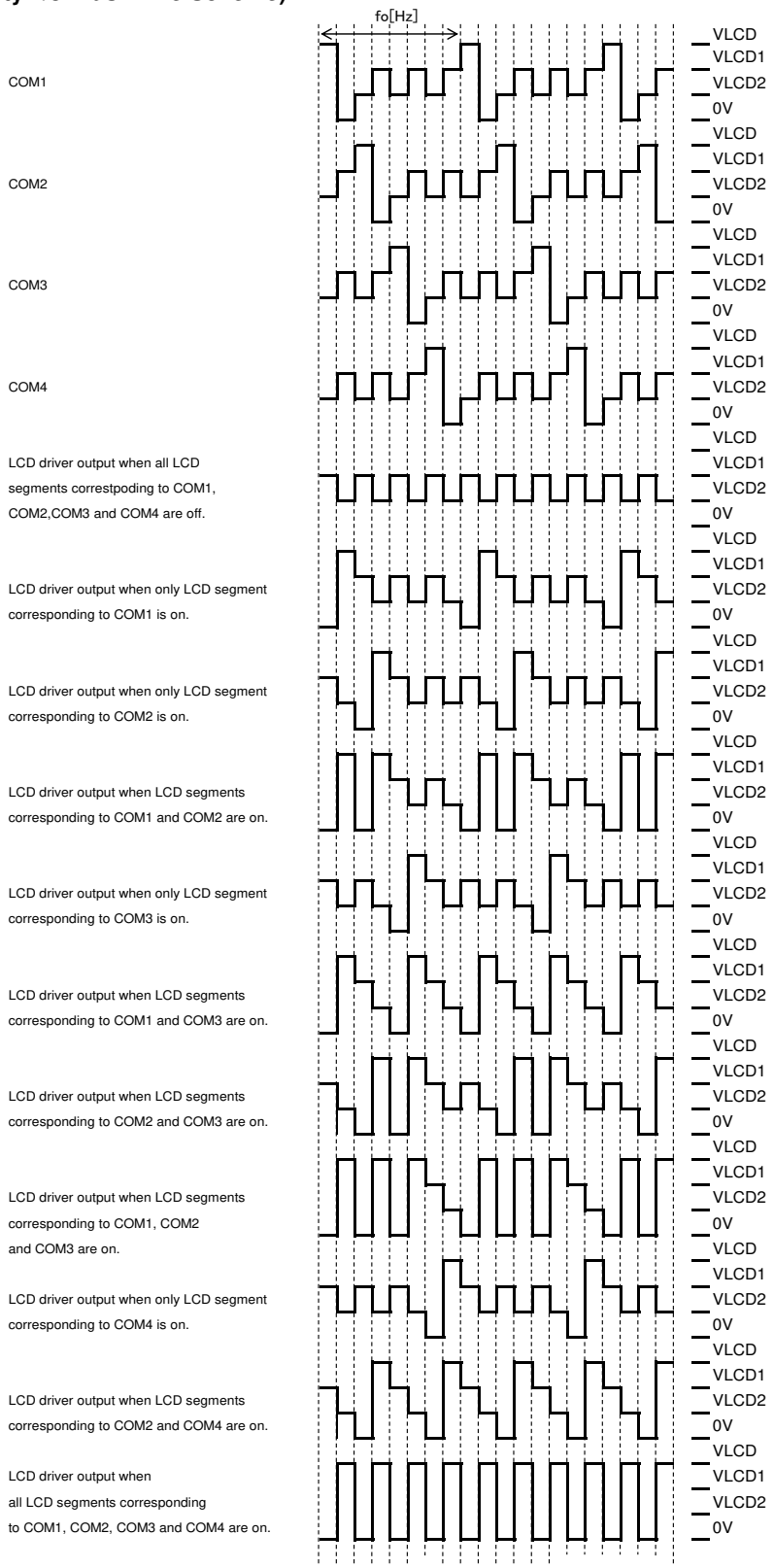


Figure 11. LCD Waveform (1/4 Duty, 1/3 Bias)

LCD Driving Waveforms– continued
(1/4 Duty 1/2 Bias Drive Scheme)

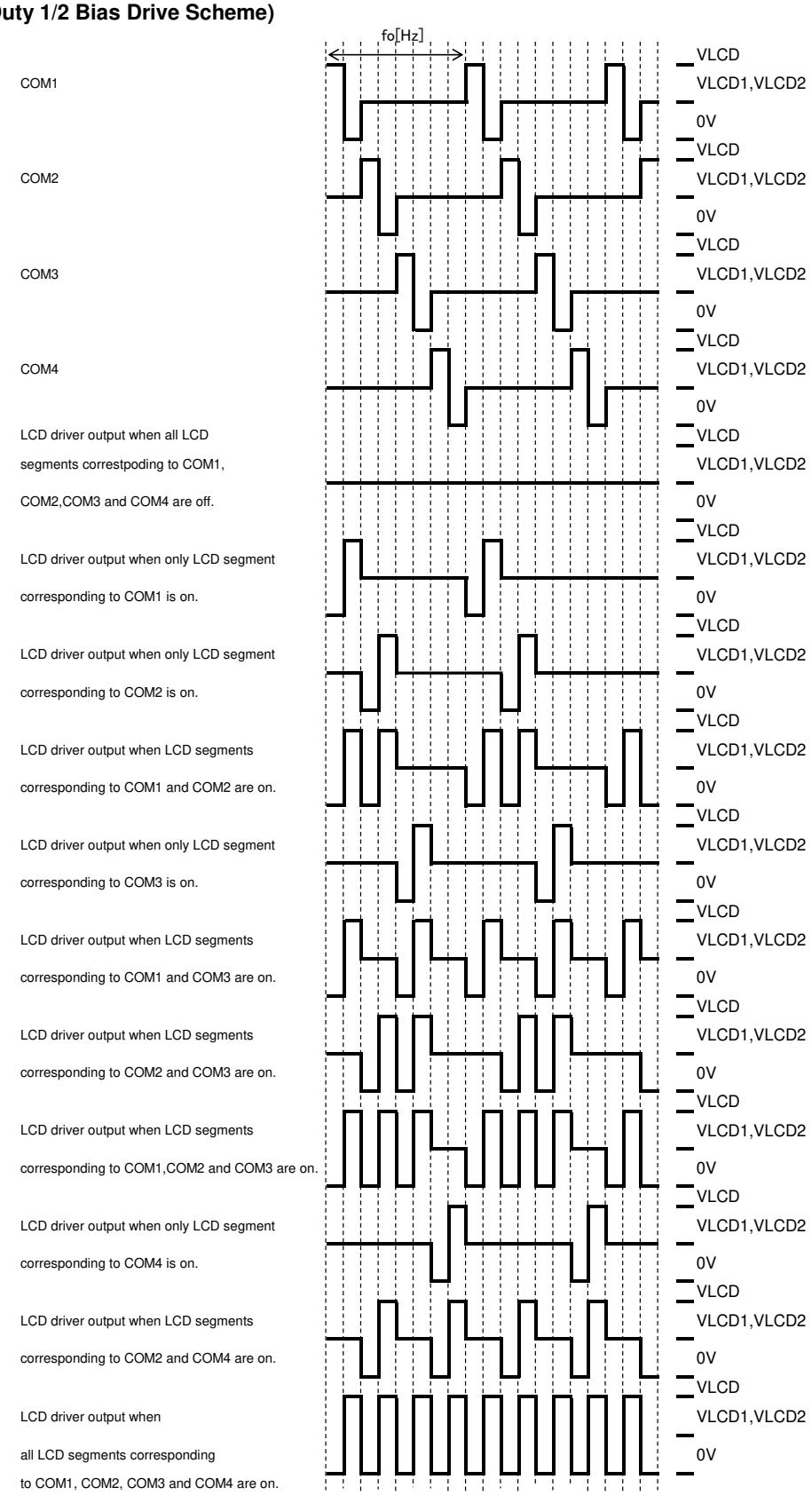


Figure 12. LCD Waveform (1/4 Duty, 1/2 Bias)

LCD Driving Waveforms– continued
(1/3 Duty 1/3 Bias Drive Scheme)

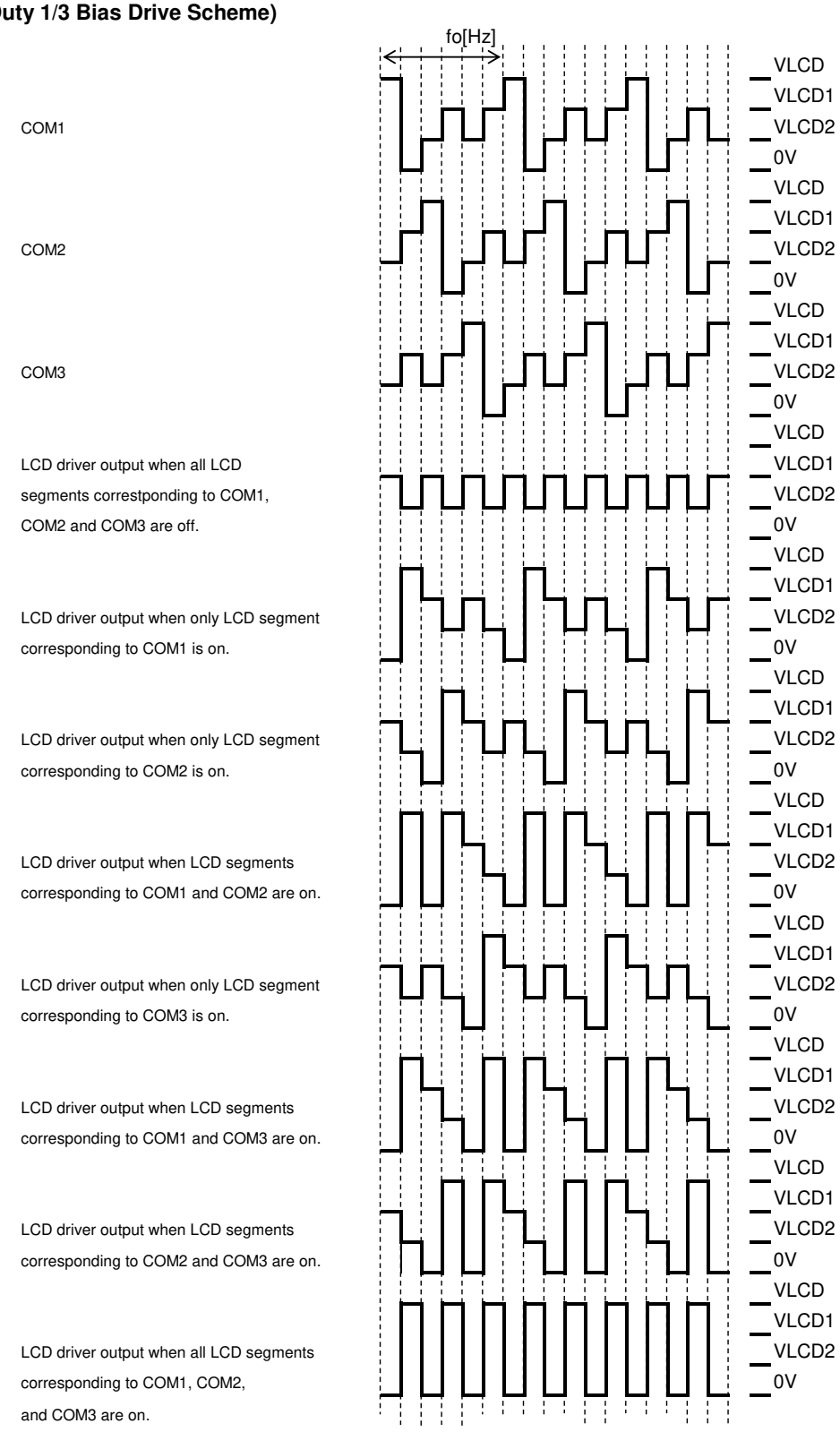


Figure 13. LCD Waveform (1/3 Duty, 1/3 Bias) (*Note*)

(*Note*) COM4 function is same as COM1 at 1/3 Duty.

LCD Driving Waveforms– continued
(1/3 Duty 1/2 Bias Drive Scheme)

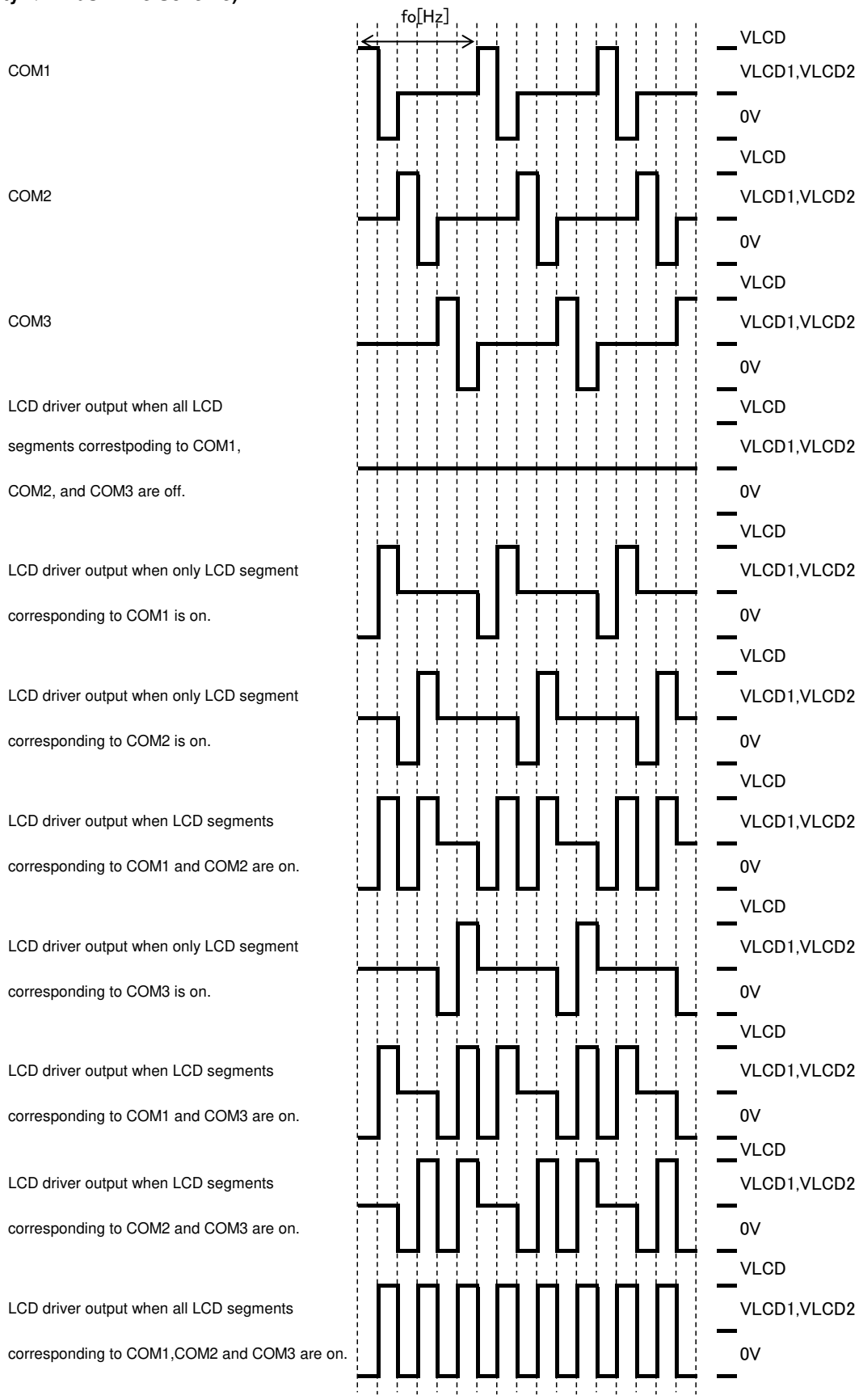


Figure 14. LCD Waveform (1/3 Duty, 1/2 Bias) (*Note*)

(*Note*) COM4 function is same as COM1 at 1/3 Duty.

The INHb Pin and Display Control

Since the IC internal data (the Display Data D1 to D216 and the control data) is undefined when power is first applied, applications should set the INHb pin low at the same
time as power is applied to turn off the display (This sets the S1/P1/G1 to S6/P6/G6, S7 to S54, COM1 to COM4 to the VSS level.) and during this period send serial data from the controller. The controller should then set the INHb pin high after the data transfer has completed. This procedure prevents meaningless displays at Power On.

1. 1/4 Duty

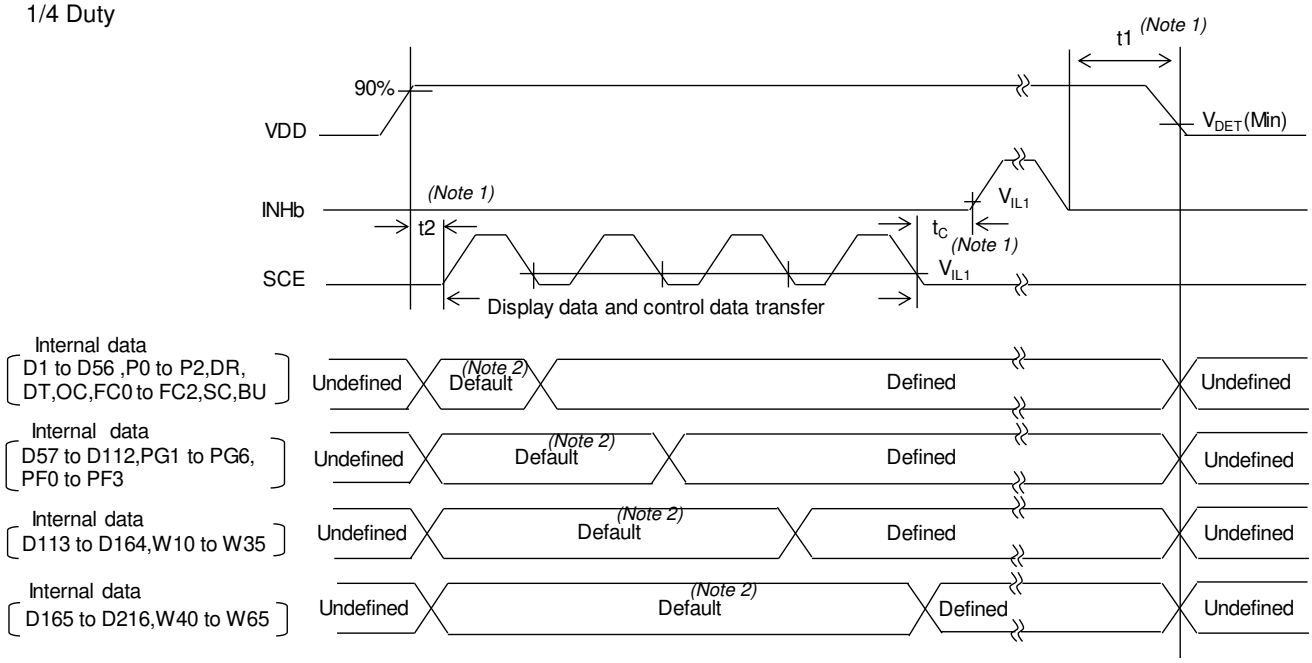


Figure 15. Power On/Off and INHb Control Sequence (1/4 Duty)

(Note 1) t1≥0, t2≥0, t_C: (Min) 10µs
When VDD level is over 90%, there may be cases where command is not received correctly in unstable VDD.
(Note 2) Display Data are undefined. Regarding default value, refer to "Reset Condition"

2. 1/3 Duty

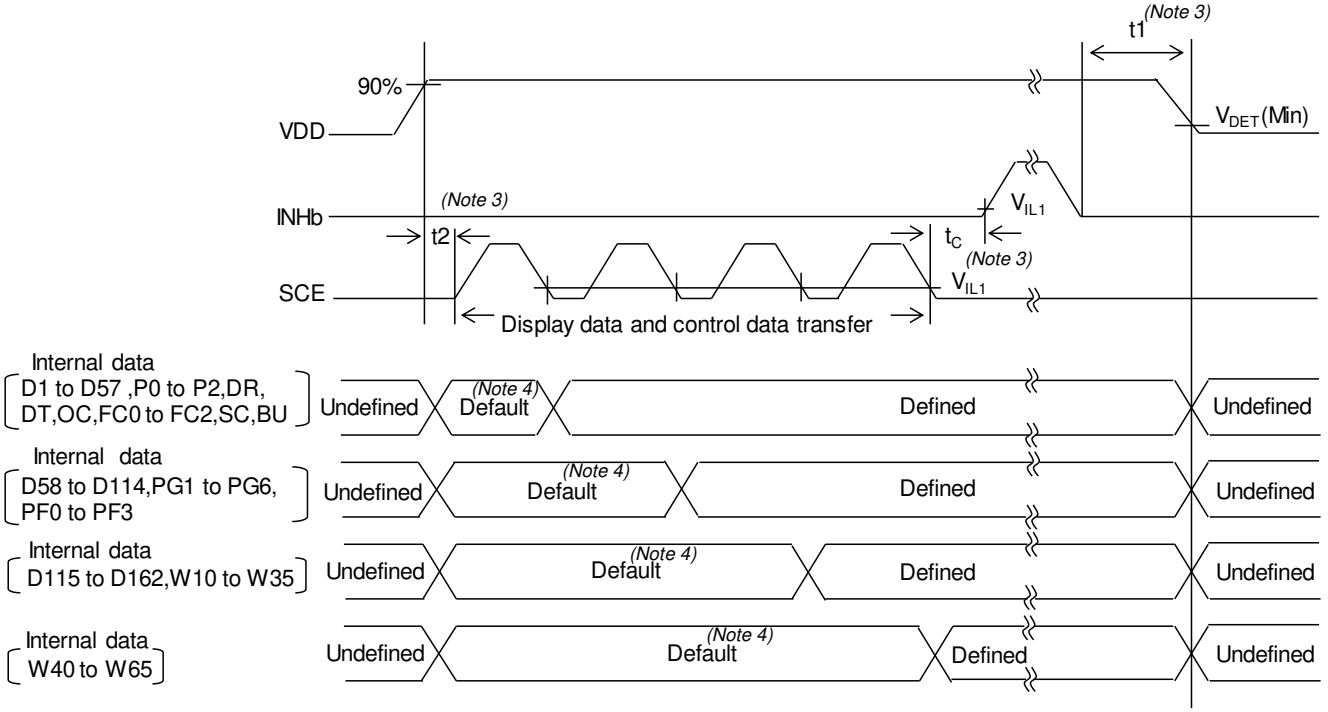


Figure 16. Power On/Off and INHb Control Sequence (1/3 Duty)

(Note 3) t1≥0, t2≥0, t_C: (Min) 10µs
When VDD level is over 90%, there may be cases where command is not received correctly in unstable VDD.
(Note 4) Display Data are undefined. Regarding default value, refer to "Reset Condition".

Oscillation Stabilization Time of the Internal Oscillation Circuit

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100μs (oscillation stabilization time) after oscillation has started.

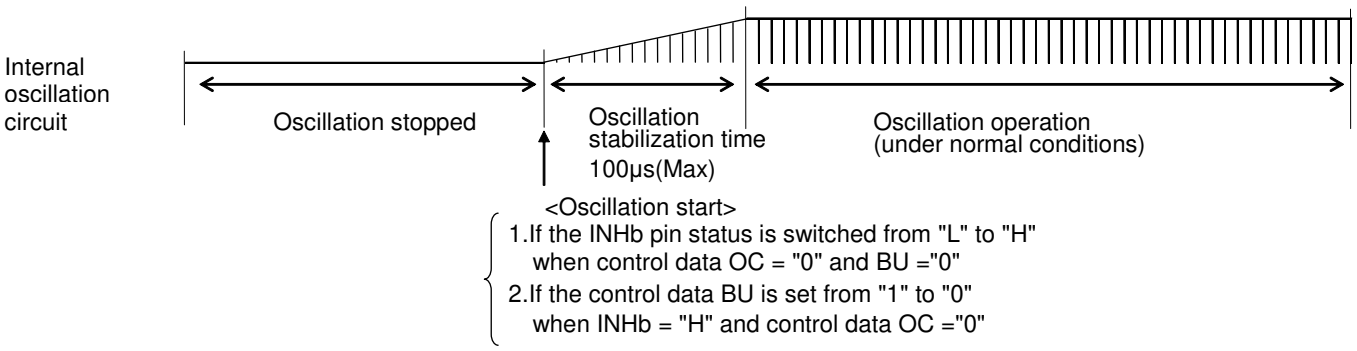


Figure 17. Oscillation Stabilization Time

Power-saving mode operation in external clock mode

After receiving [BU]=[1], BU91510KV-M enter to Power-saving mode synchronized with frame then Segment and Common pins output VSS level.
Therefore, in external clock mode, it is necessary to input the external clock based on each frame frequency setting after sending [BU]=[1].
For the required number of clock, refer to Control Data Functions "4. FC0, FC1 and FC2: Frame frequency switching control data".

For example, please input the external clock as below.
[FC0,FC1,FC2]=[0,0,0]: In case of f_{OSC}/6144 setting, it needs over 6144clk,
[FC0,FC1,FC2]=[0,1,0]: In case of f_{OSC}/4608 setting, it needs over 4608clk,
[FC0,FC1,FC2]=[1,1,1]: In case of f_{OSC}/1536 setting, it needs over 1536clk

Please refer to the timing chart below.

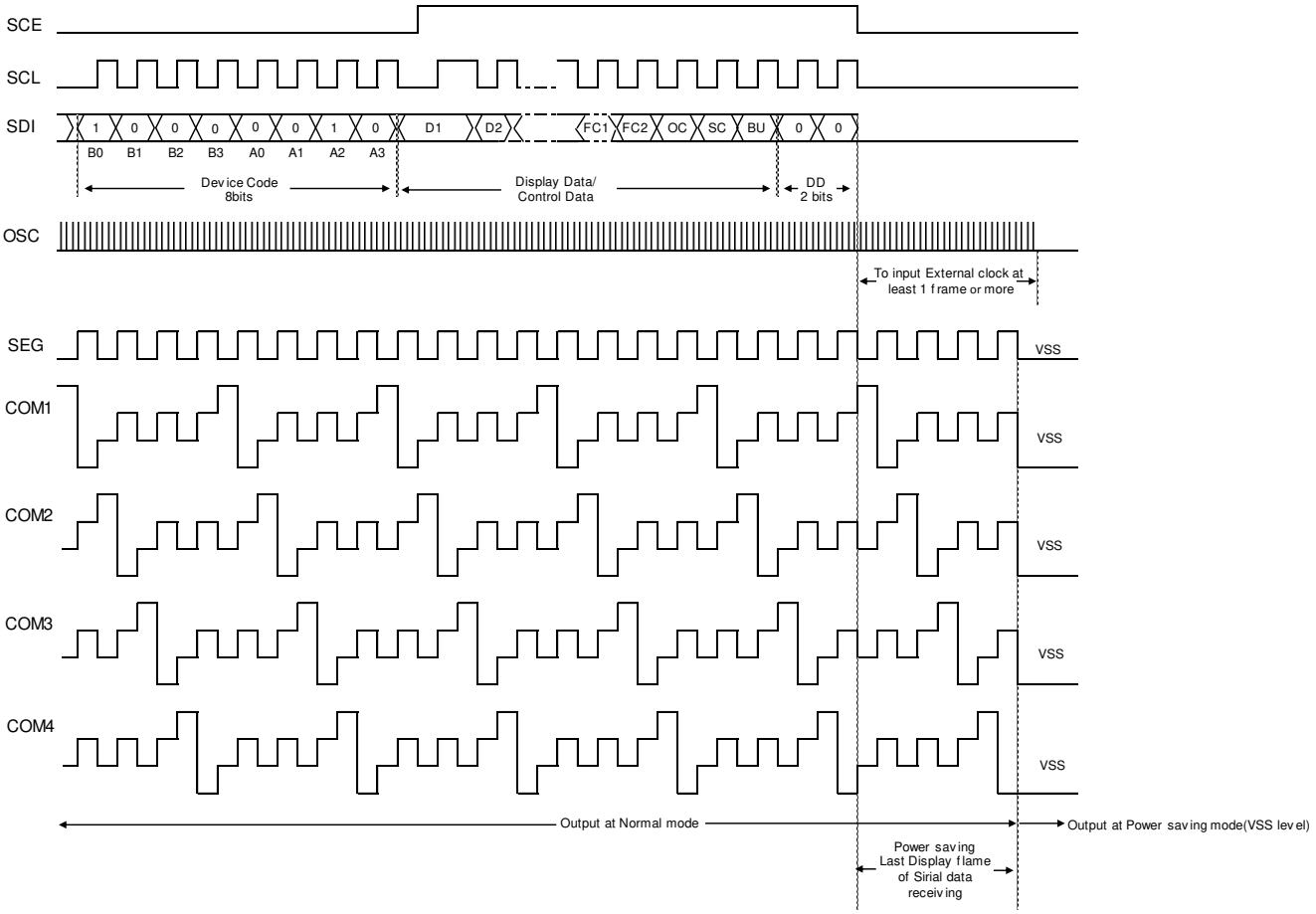


Figure 18. External Stop Timing(1/4 Duty)

Voltage Detection Type Reset Circuit (VDET)

The Voltage Detection Type Reset Circuit generates an output signal and resets the system when power is applied for the first time and when voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage (V_{DET} = 1.8V Typ)). To ensure that this reset function works properly, it is recommended that a capacitor must be connected to the power supply line so that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.

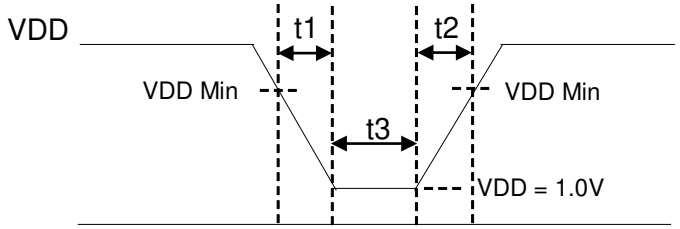


Figure 19. VDET Detection Timing

Power supply voltage VDD fall time: t1 > 1ms
Power supply voltage VDD rise time: t2 > 1ms
Internal reset power supply retain time: t3 > 1ms

If the above conditions cannot be satisfied, the IC may not initialize, so unintended display lighting may occur.
In order to reduce this effect, initialize the IC as soon as possible after turning on the power supply.
Refer to the IC initialization flow below.
But since commands are not received when the power is OFF, the IC initialization flow is not the same function as POR.

Set the BU command to power save mode ([BU] = [1]) and SC command to off (SC = 1) immediately after turning on the power.
In BU91510KV-M, command reception is possible (VDD:90%) 0ns after turning on the power.
Refer to the timing chart for "The INHb Pin and Display Control".

Reset Condition

When BU91510KV-M is initialized, the internal status after power supply has been reset as the following table.

Table 1. control data reset condition

Instruction	At Reset Condition
S1/P1/G1 to S6/P6/G6 Pin	[P0,P1,P2]=[0,0,0]:all segment output
LCD Bias	DR=0: 1/3 Bias
LCD Duty	DT=0: 1/4 Duty
Display Frequency	[FC0,FC1,FC2]=[0,0,0]:f_{OSC}/6144
Display Clock Mode	OC=0:Internal oscillator
LCD Display	SC=1:OFF
Power Mode	BU=1:Power saving mode
PWM / GPO Output	PGx=0:PWM output(x=1 to 6)
PWM Frequency	[PF0,PF1,PF2,PF3]=[0,0,0,0]:f_{OSC}/2048
PWM Duty	[Wn0 to Wn5]=[0,0,0,0,0,0] :(1/64)xTp(n=1 to 6,Tp=1/fp)