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LCD Segment Drivers

Multi-function LCD Segment Drivers

BU91530KVT-M **MAX 445 Segment(89SEGx5COM)**

General Description

The BU91530KVT-M is 1/5, 1/4, 1/3 duty or Static General-purpose LCD driver. The BU91530KVT-M can drive up to 445 LCD Segments directly. The BU91530KVT-M can also control up to 9 General-purpose output pins / 9 PWM output pins. These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wring.

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments: 445 Segments
- Display Duty Static, 1/3, 1/4, 1/5 Selectable
- Bias: 1/2, 1/3 Selectable
- Interface: 3wire Serial Interface

Features

- AEC-Q100 Qualified (*Note 1*)
- Key Input Function for Up to 30 Keys (A key scan is performed only when a key is pressed.)
- Either 1/5, 1/4, 1/3 Duty or Static
  Can be Selected with the Serial Control Data.
  1/5 Duty Drive: Up to 445 segments can be Driven
  1/4 Duty Drive: Up to 360 segments can be Driven
  1/3 Duty Drive: Up to 270 segments can be Driven
  Static Drive: Up to 90 Segments can be Driven
- Selectable Display Frame Frequency for Common and Segment Output Waveforms.
- Configurable Output Pin to Segment Output / PWM Output / General-purpose Output.(Max 9 Pins)
- Built-in OSC Circuit
- Integrated Voltage Detection Type Reset Circuit (VDET)
- No External Component
- Low Power Consumption Design
- Supports Line and Frame Inversion

(*Note 1*) Grade 2

Package

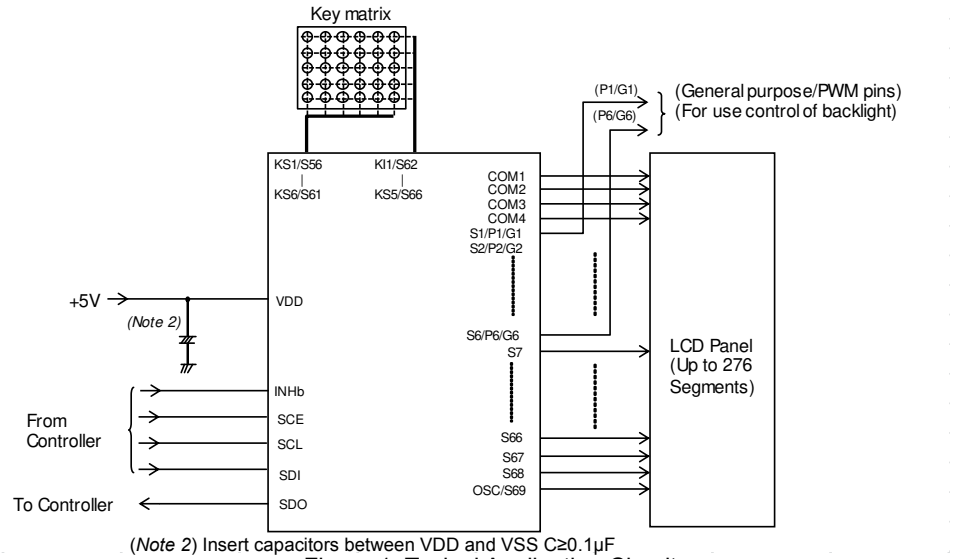
W(Typ) x D(Typ) x H(Max)

TQFP100V
16.00mm x 16.00mm x 1.20mm

Applications

- Car Audio, Home Electrical Appliance, Meter Equipment etc.

Typical Application Circuit



(*Note 2*) Insert capacitors between VDD and VSS C≥0.1μF

Figure 1. Typical Application Circuit

○Product structure：Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Block Diagram

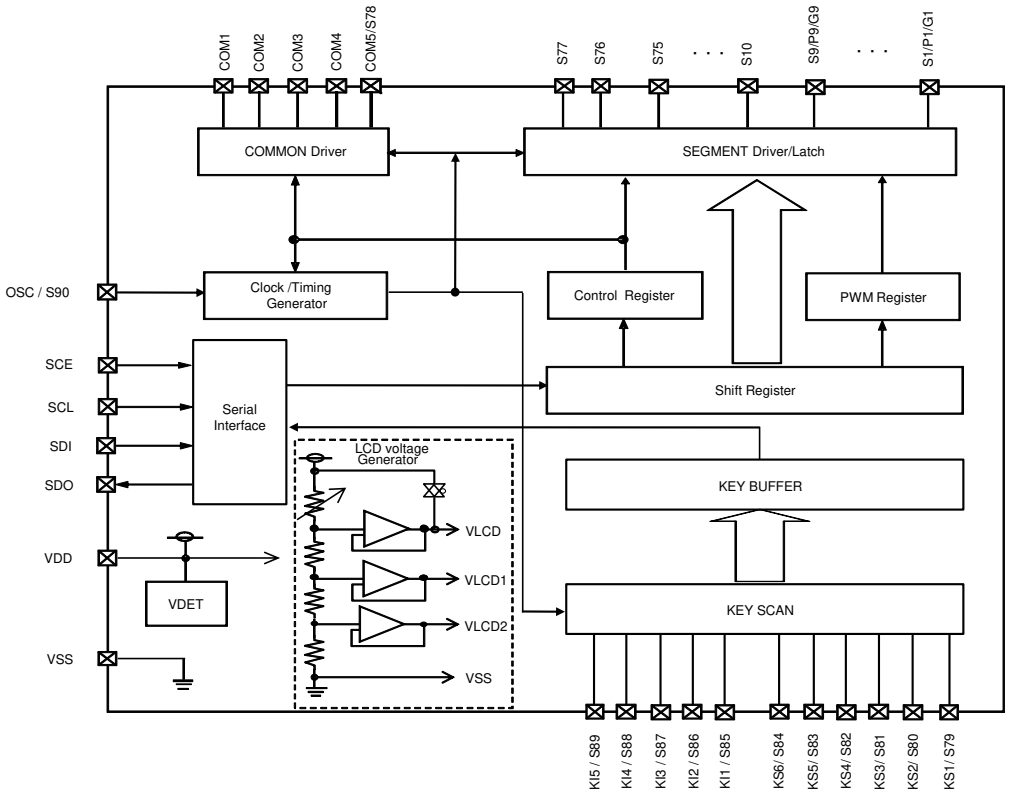


Figure 2. Block Diagram

Pin Arrangement

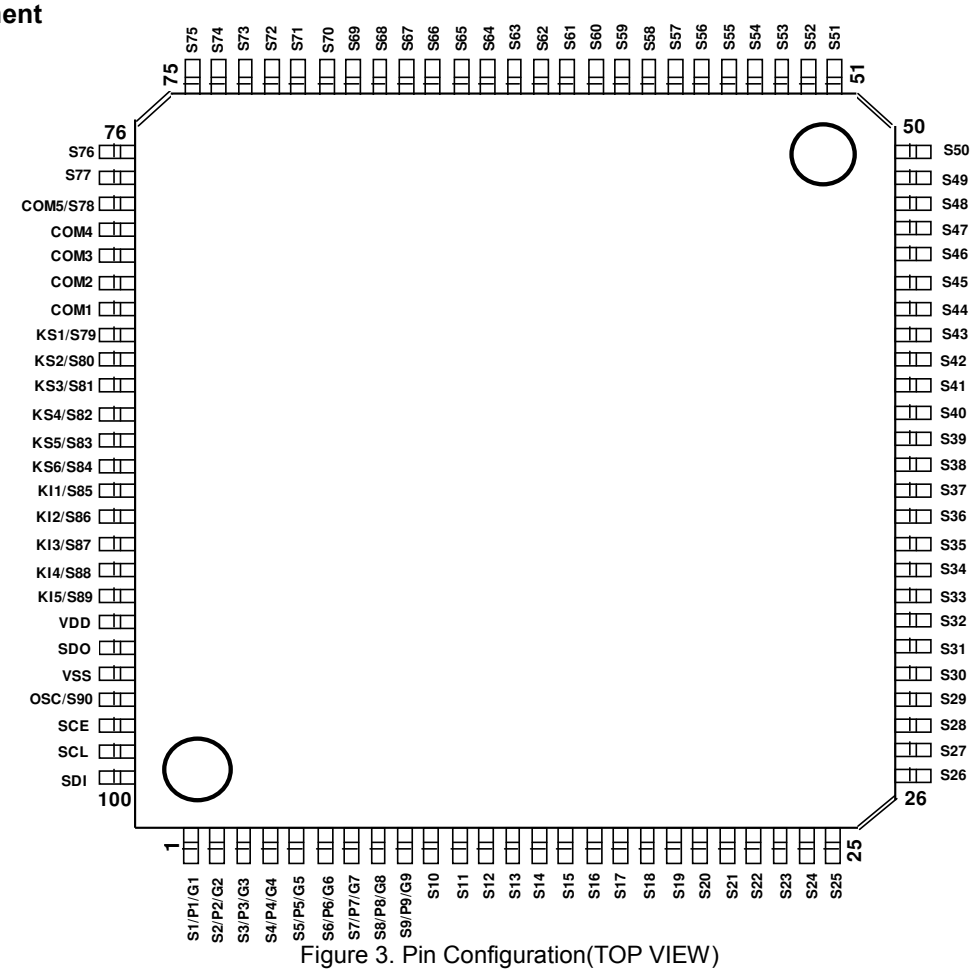


Figure 3. Pin Configuration(TOP VIEW)

Absolute Maximum Ratings (VSS = 0.0V)

Parameter	Symbol	Pin / Conditions	Ratings	Unit
Maximum Supply Voltage	VDD	VDD	-0.3 to +7.0	V
Input Voltage	V_{IN1}	SCE, SCL, SDI, OSC	-0.3 to +7.0	V
	V_{IN2}	KI1 to KI5	-0.3 to +7.0	V
Allowable Loss	Pd	-	1.49*(Note)*	W
Operating Temperature	Topr	-	-40 to +105	°C
Storage Temperature	Tstg	-	-55 to +125	°C

(*Note*) Derate by 1.49mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).
(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Recommended Operating Conditions (Ta = -40 to +105°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Supply Voltage	VDD	-	2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	V_{H1}	SCE, SCL, SDI, OSC	-	-	0.03VDD	-	V
	V_{H2}	KI1 to KI5	-	-	0.1VDD	-	
Power-on Detection Voltage	V_{DET}	VDD	-	1.4	1.8	2.2	V
"H" Level Input Voltage	V_{IH1}	SCE, SCL, SDI, OSC	4.0V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	V_{IH2}	SCE, SCL, SDI, OSC	2.7V ≤ VDD < 4.0V	0.8VDD	-	VDD	
	V_{IH3}	KI1 to KI5	-	0.7VDD	-	VDD	
"L" Level Input Voltage	V_{IL1}	SCE, SCL, SDI, OSC KI1 to KI5	-	0	-	0.2VDD	V
Input Floating Voltage	V_{IF}	KI1 to KI5	-	-	-	0.05VDD	V
Pull-down Resistance	R_{PD}	KI1 to KI5	VDD=5.0V	50	100	250	kΩ
Output Off Leakage Current	I_{OFFH}	SDO	V_O=6.0V	-	-	6.0	μA
"H" Level Input Current	I_{IH1}	SCE, SCL, SDI, OSC	V_I=5.5V	-	-	5.0	μA
"L" Level Input Current	I_{IL1}	SCE, SCL, SDI, OSC	V_I=0V	-5.0	-	-	μA
"H" Level Output Voltage	V_{OH1}	S1 to S90	I_O=-20μA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	V_{OH2}	COM1 to COM5	I_O=-100μA, VLCD=1.00*VDD	VDD-0.9	-	-	
	V_{OH3}	P1/G1 to P9/G9	I_O=-1mA	VDD-0.9	-	-	
	V_{OH4}	KS1 to KS6	I_O=-500μA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	V_{OL1}	S1 to S90	I_O=20μA	-	-	0.9	V
	V_{OL2}	COM1 to COM5	I_O=100μA	-	-	0.9	
	V_{OL3}	P1/G1 to P9/G9	I_O=1mA	-	-	0.9	
	V_{OL4}	KS1 to KS6	I_O=25μA	0.2	0.5	1.5	
	V_{OL5}	SDO	I_O=1mA	-	0.1	0.5	
Middle Level Output Voltage	V_{MID1}	S1 to S90	1/2 Bias I_O=±20μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	V
	V_{MID2}	COM1 to COM5	1/2 Bias I_O=±100μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	
	V_{MID3}	S1 to S90	1/3 Bias I_O=±20μA VLCD = 1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID4}	S1 to S90	1/3BiasI_O=±20μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
	V_{MID5}	COM1 to COM5	1/3BiasI_O=±100μA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID6}	COM1 to COM5	1/3BiasI_O=±100μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	

Electrical Characteristics– continued

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Current Consumption	I_{DD1}	VDD	Power-saving mode	-	-	15	µA
	I_{DD2}	VDD	VDD=5.0V Output open 1/2 Bias Frame frequency=80Hz VLCD=1.00*VDD	-	100	200	
	I_{DD3}	VDD	VDD=5.0V Output open 1/3 Bias Frame frequency=80Hz VLCD=1.00*VDD	-	130	250	

Oscillation Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency 1	f_{OSC1}	-	VDD=2.7V to 6.0V	300	-	720	kHz
Oscillator Frequency 2	f_{OSC2}	-	VDD=5V	510	600	690	kHz
External Clock Frequency*(Note)*	f_{OSC3}	OSC/S90	External clock mode (OC = 1)	30	-	1000	kHz
External Clock Rise Time	tr			-	160	-	ns
External Clock Fall Time	tf			-	160	-	ns
External Clock Duty	t_{DTY}			30	50	70	%

(*Note*) Frame frequency is decided external clock and dividing ratio of FC0,FC1,FC2,FC3 setting.

【Reference Data】

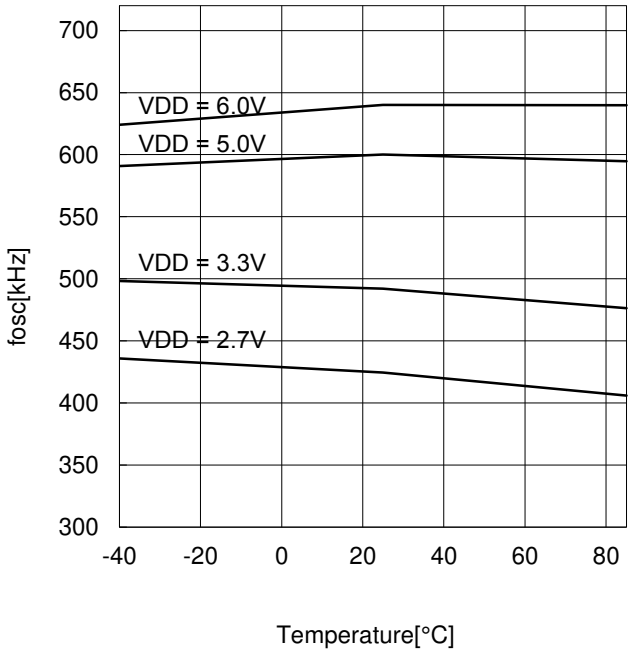
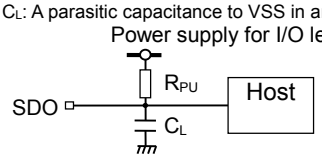


Figure 4. Frame Frequency Typical Temperature Characteristics

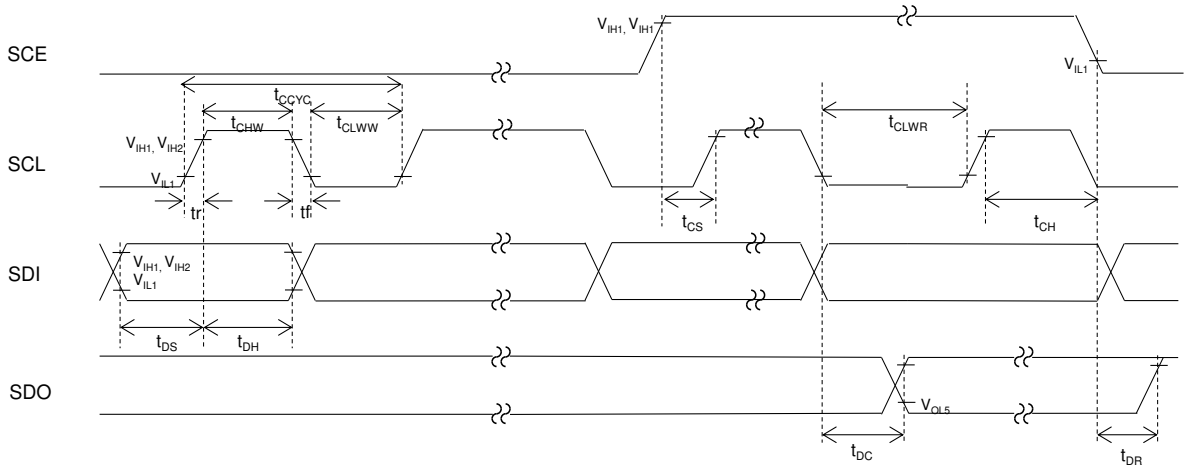
MPU Interface Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	t_{DS}	SCL, SDI	-	120	-	-	ns
Data Hold Time	t_{DH}	SCL, SDI	-	120	-	-	ns
SCE Wait Time	t_{CP}	SCE, SCL	-	120	-	-	ns
SCE Setup Time	t_{CS}	SCE, SCL	-	120	-	-	ns
SCE Hold Time	t_{CH}	SCE, SCL	-	120	-	-	ns
Clock Cycle Time	t_{CCYC}	SCL	-	320	-	-	ns
High-level Clock Pulse Width	t_{CHW}	SCL	-	120	-	-	ns
Low-level Clock Pulse Width (Write)	t_{CLWW}	SCL	-	120	-	-	ns
Low-Level Clock Pulse Width (Read)	t_{CLWR}	SCL	R_{PU}=4.7kΩ C_L=10pF *(Note)*	1.6	-	-	µs
Rise Time	tr	SCE, SCL, SDI	-	-	160	-	ns
Fall Time	tf	SCE, SCL, SDI	-	-	160	-	ns
SDO Output Delay Time	t_{DC}	SDO	R_{PU}=4.7kΩ C_L=10pF *(Note)*	-	-	1.5	µs
SDO Rise Time	t_{DR}	SDO	R_{PU}=4.7kΩ C_L=10pF *(Note)*	-	-	1.5	µs

(*Note*) Since SDO is an open-drain output, "t_{DC}" and "t_{DR}" depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.
R_{PU}: 1kΩ≤R_{PU}≤10kΩ is recommended.
C_L: A parasitic capacitance to VSS in an application circuit. Any component is not necessary to be attached.



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

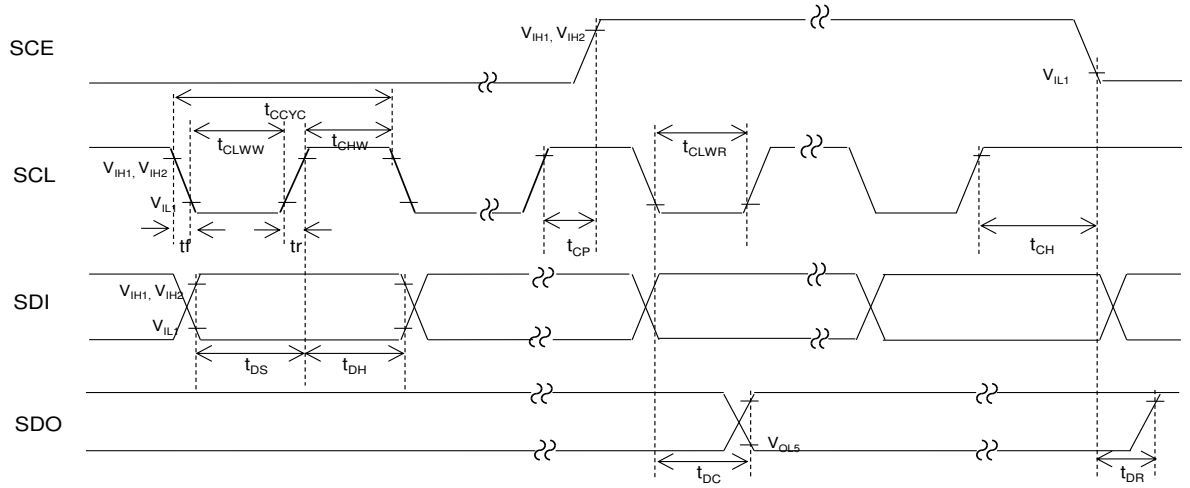


Figure 5.Serial Interface Timing

Pin Description

Pin	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S9/P9/G9	1 to 9	Segment output for displaying the display data transferred by serial data input. The S1/P1/G1 to S9/P9/G9 pins can also be used as General-purpose or PWM outputs when so set up by the control data.	-	O	OPEN
S10 to S77	10 to 77	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S79 to KS6/S84	83 to 88	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S79 to KS6/S84 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
KI1/S85 to KI5/S89	89 to 93	Key scan inputs These pins have built-in pull-down resistors. The KI1/S85 to KI5/S89 pins can be used as segment outputs when so specified by the control data.	-	I O	VSS OPEN
COM1 to COM4	79 to 82	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
COM5/S78	78	Common / Segment output for LCD driving Assigned as Common output in1/5 Duty mode and Segment output in Static, 1/3 Duty and 1/4 Duty modes	-	O	OPEN
OSC/S90	97	Segment output for displaying the display data transferred by serial data input. The pin OSC/S90 can be used as external clock input pin when set up by the control data.	-	I O	VSS OPEN
SCE SCL SDI	98 99 100	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Clock for serial data transfer. SDI: Transfer data	H ↑ -	I I I	VSS VSS VSS
SDO	95	Output data	-	O	OPEN
VDD	94	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	96	Power supply pin. Must be connected to ground.	-	-	-

IO Equivalent Circuit

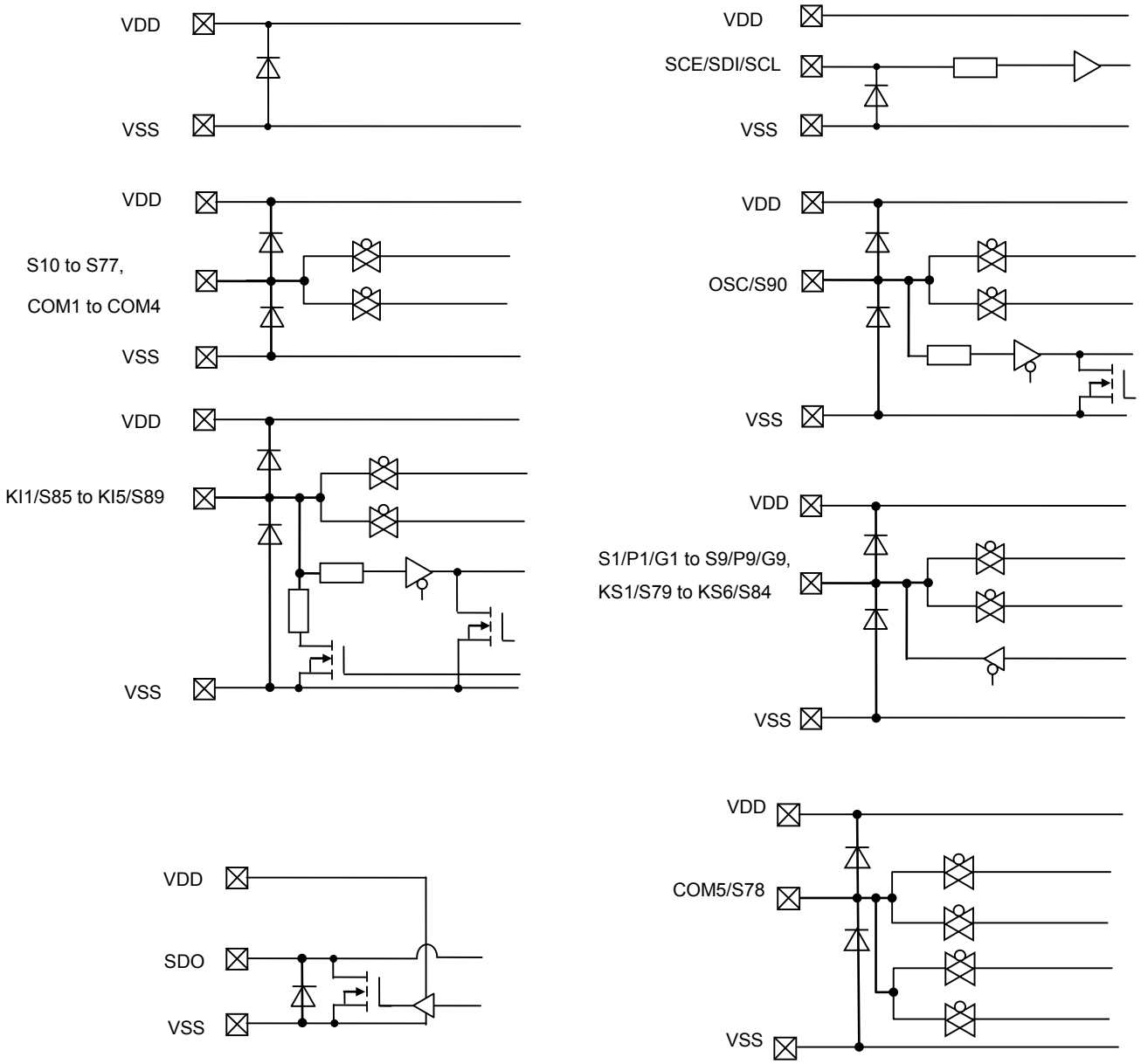


Figure 6. I/O Equivalent Circuit

Serial Data Transfer Formats

1. 1/5 Duty

(1)When SCL is stopped at the low level

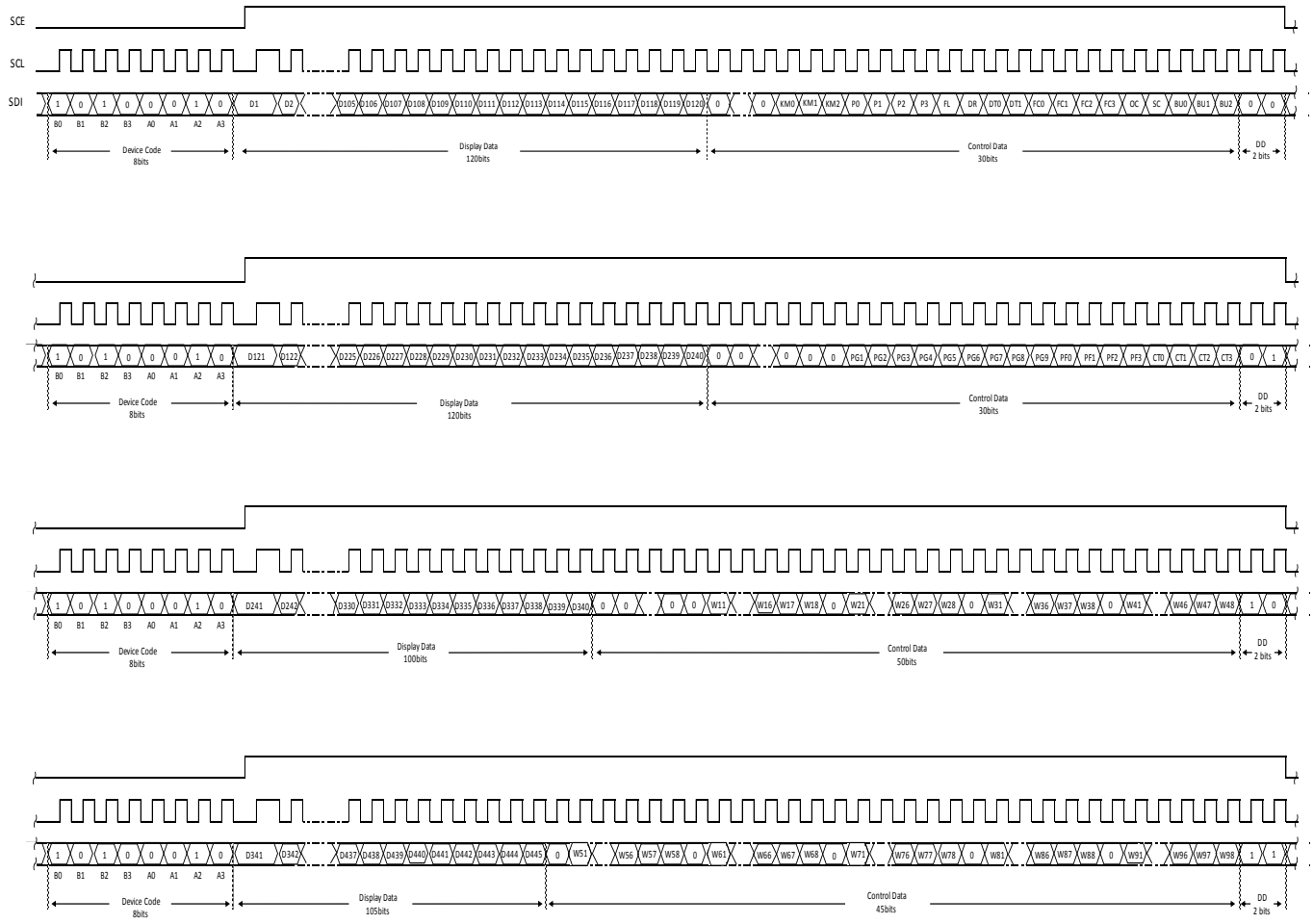


Figure 7. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

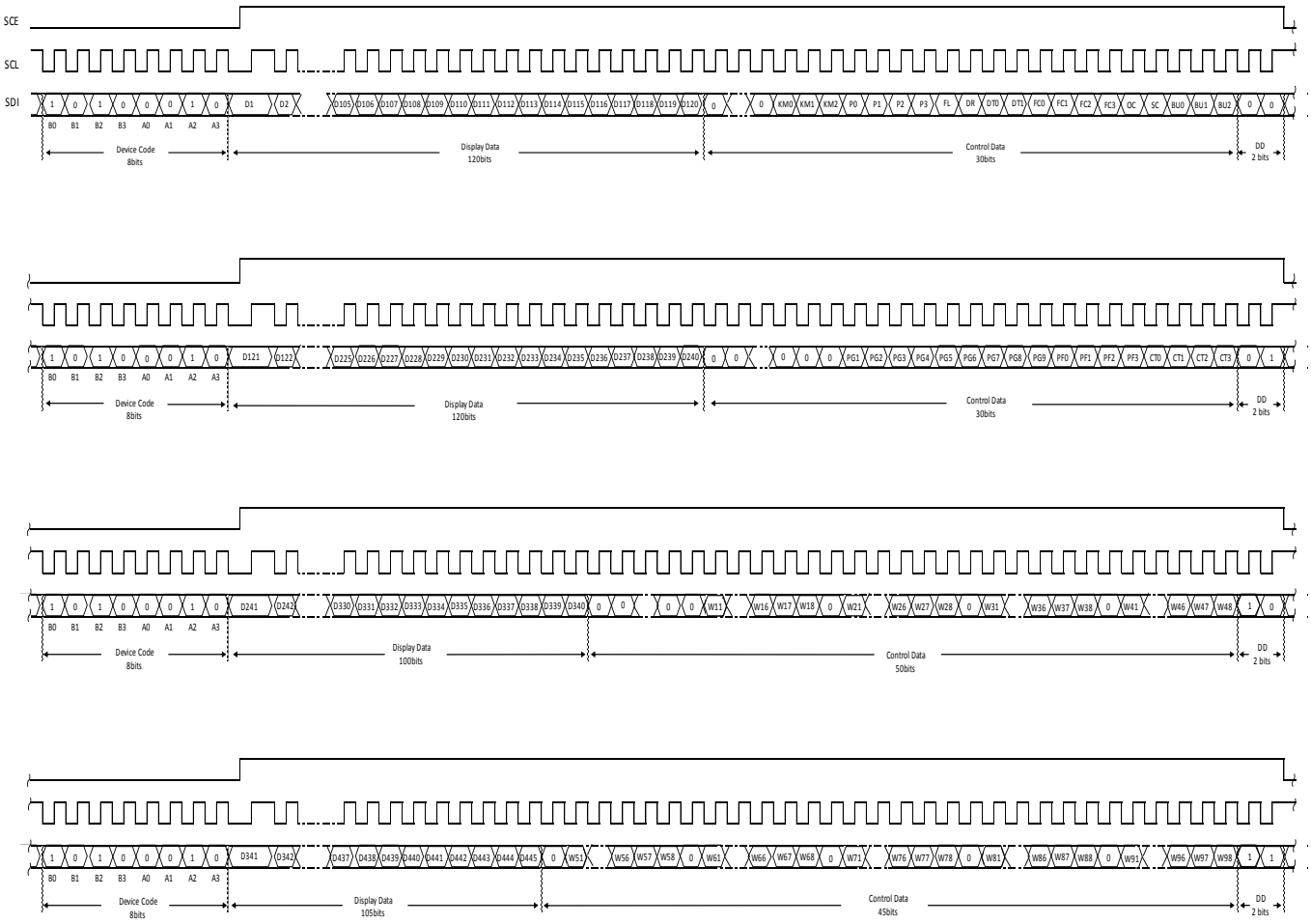


Figure 8. 3-SPI Data Transfer Format

Device code……”45H”
KM0 to KM2……Key Scan output pin / Segment output pin switching control data
D1 to D445 ……Display data
P0 to P3……Segment / PWM / General-purpose output pin switching control data
FL……Line Inversion or Frame Inversion switching control data
DR……1/3 Bias drive or 1/2 Bias drive switching control data
DT0 to DT1……1/5 Duty drive, 1/4 Duty drive, 1/3 Duty drive or Static drive switching control data
FC0 to FC3……Common / Segment output waveform frame frequency switching control data
OC……Internal oscillator operating mode / External clock operating mode switching control data
SC ……Segment on/off switching control data
BU0 to BU2 ……Normal mode/power-saving mode switching control data
PG1 to PG9 ……PWM / General-purpose output switching control data
PF0 to PF3 ……PWM output waveform frame frequency switching control data
CT0 to CT3……LCD display contrast switching control data
W11 to W18, W21 to W28, W31 to W38,W41 to W48, W51 to W58, W61 to W68, W71 to W78, W81 to W88, W91 to W98
……PWM output duty switching control data
DD……Direction data

Serial Data Transfer Formats – continued

2. 1/4 Duty
(1)When SCL is stopped at the low level

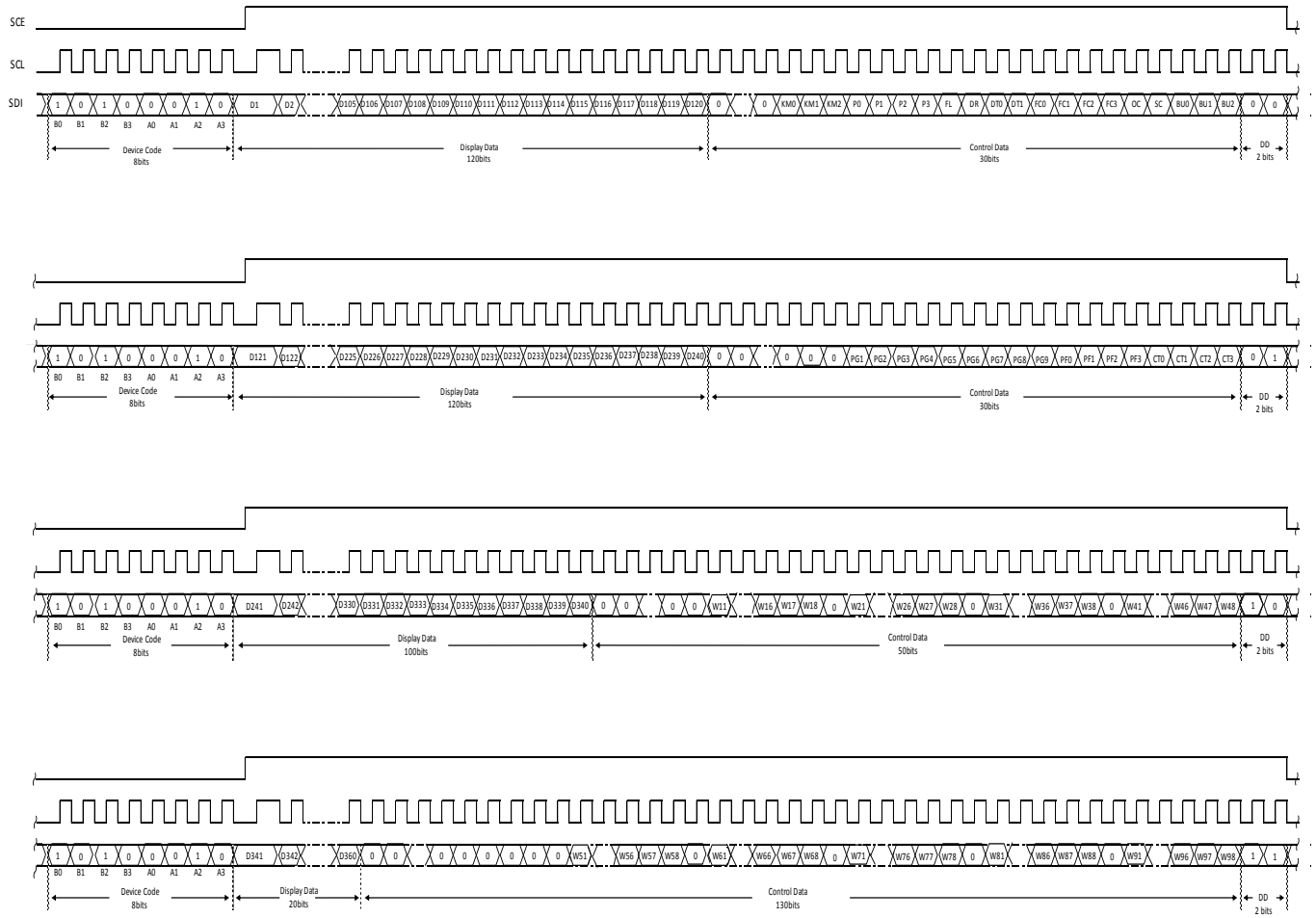


Figure 9. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

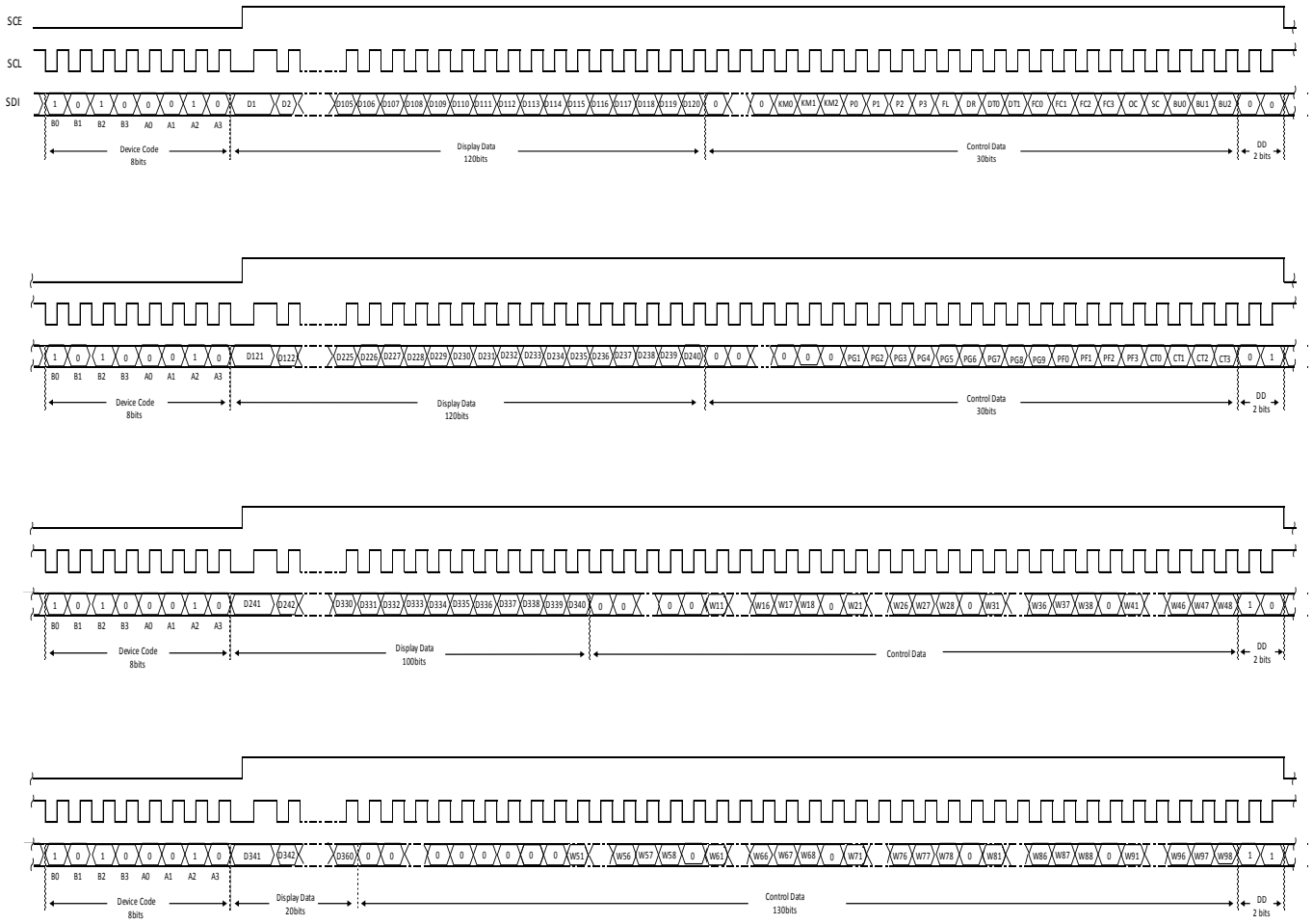


Figure 10. 3-SPI Data Transfer Format

Device code ……"45H"
KM0 to KM2 ……Key Scan output pin / Segment output pint switching control data
D1 to D360 ……Display data
P0 to P3 ……Segment / PWM / General-purpose output pin switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR ……1/3 Bias drive or 1/2 Bias drive switching control data
DT0 to DT1 ……1/5 Duty drive, 1/4 Duty drive, 1/3 Duty drive or Static drive switching control data
FC0 to FC3 ……Common / Segment output waveform frame frequency switching control data
OC ……Internal oscillator operating mode / External clock operating mode switching control data
SC ……Segment on/off switching control data
BU0 to BU2 ……Normal mode / power-saving mode switching control data
PG1 to PG9 ……PWM / General-purpose output switching control data
PF0 to PF3 ……PWM output waveform frame frequency switching control data
CT0 to CT3 ……LCD display contrast switching control data
W11 to W18, W21 to W28, W31 to W38,W41 to W48, W51 to W58, W61 to W68, W71 to W78, W81 to W88, W91 to W98 ……PWM output duty switching control data
DD ……Direction data

Serial Data Transfer Formats – continued

3. 1/3 Duty
(1) When SCL is stopped at the low level

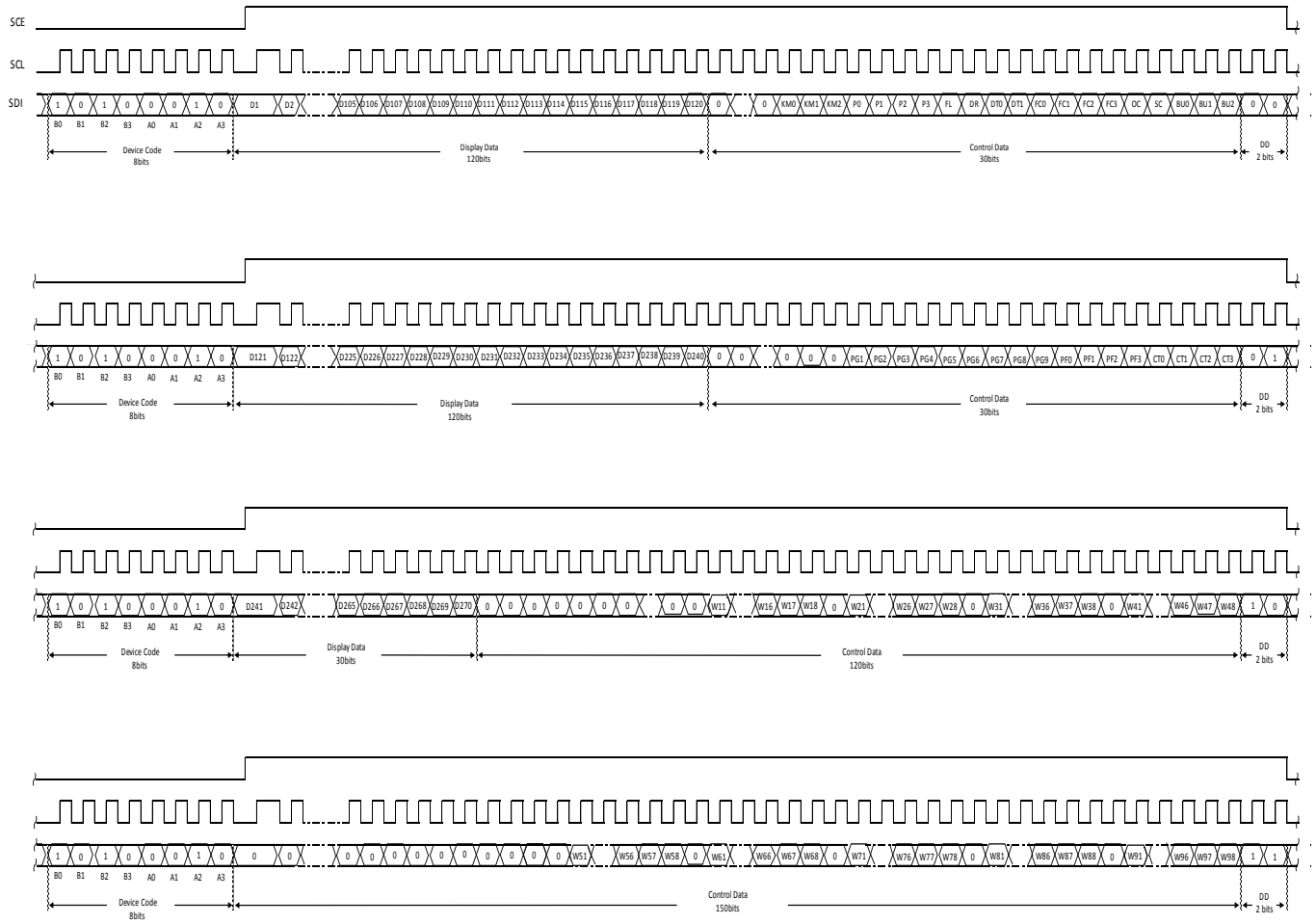


Figure 11. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

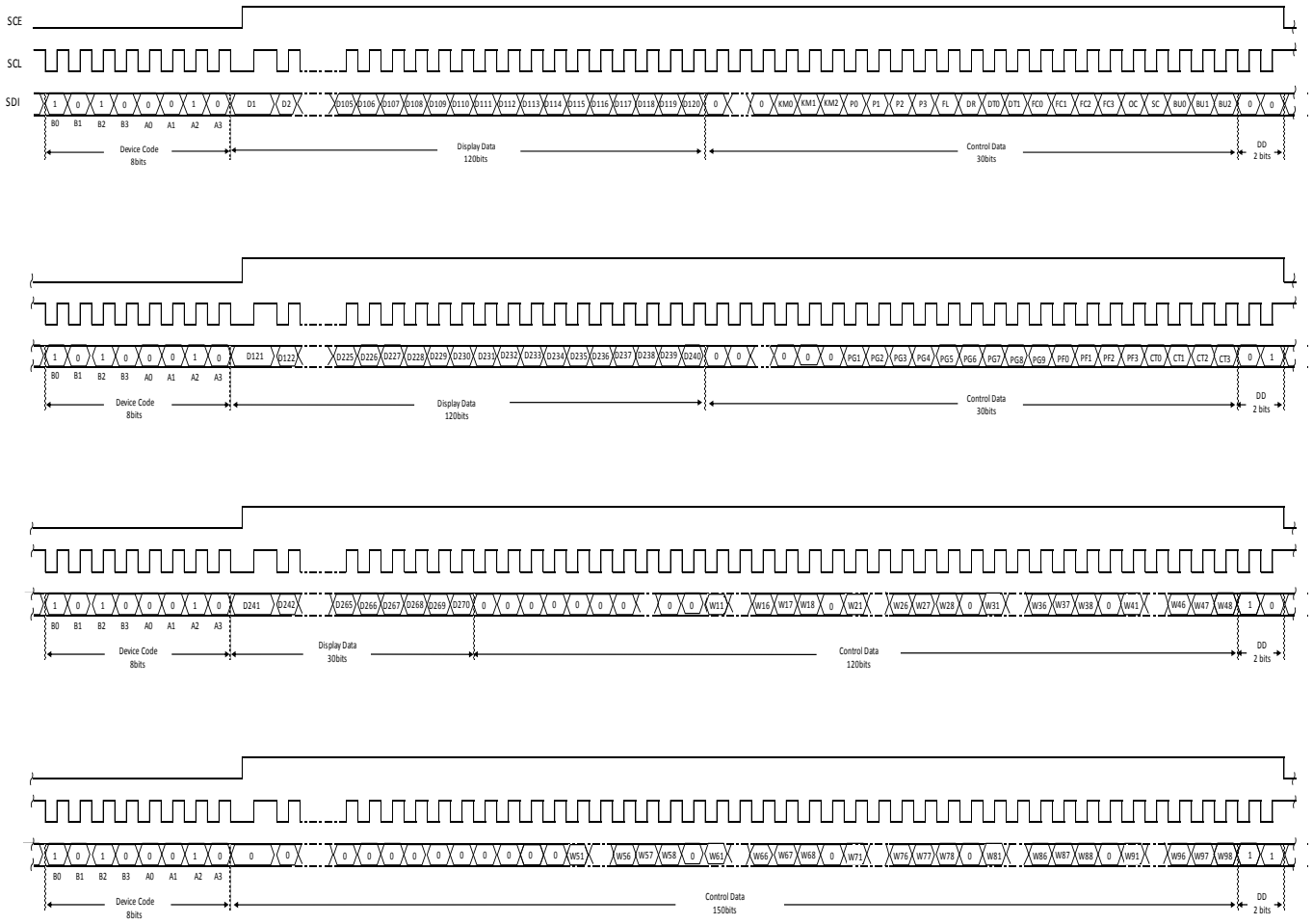


Figure 12. 3-SPI Data Transfer Format

Device code……"45H"
KM0 to KM2……Key Scan output pin / Segment output pin switching control data
D1 to D270 ……Display data
P0 to P3……Segment / PWM / General-purpose output pin switching control data
FL……Line Inversion or Frame Inversion switching control data
DR……1/3 Bias drive or 1/2 Bias drive switching control data
DT0 to DT1……1/5 Duty drive, 1/4 Duty drive, 1/3 Duty drive or Static drive switching control data
FC0 to FC3……Common / Segment output waveform frame frequency switching control data
OC……Internal oscillator operating mode / External clock operating mode switching control data
SC ……Segment on/off switching control data
BU0 to BU2 ……Normal mode / power-saving mode switching control data
PG1 to PG9 ……PWM / General-purpose output switching control data
PF0 to PF3 ……PWM output waveform frame frequency switching control data
CT0 to CT3……LCD display contrast switching control data
W11 to W18, W21 to W28, W31 to W38, W41 to W48, W51 to W58, W61 to W68, W71 to W78, W81 to W88, W91 to W98 ……PWM output duty switching control data
DD……Direction data

Serial Data Transfer Formats – continued

4. Static
(1)When SCL is stopped at the low level

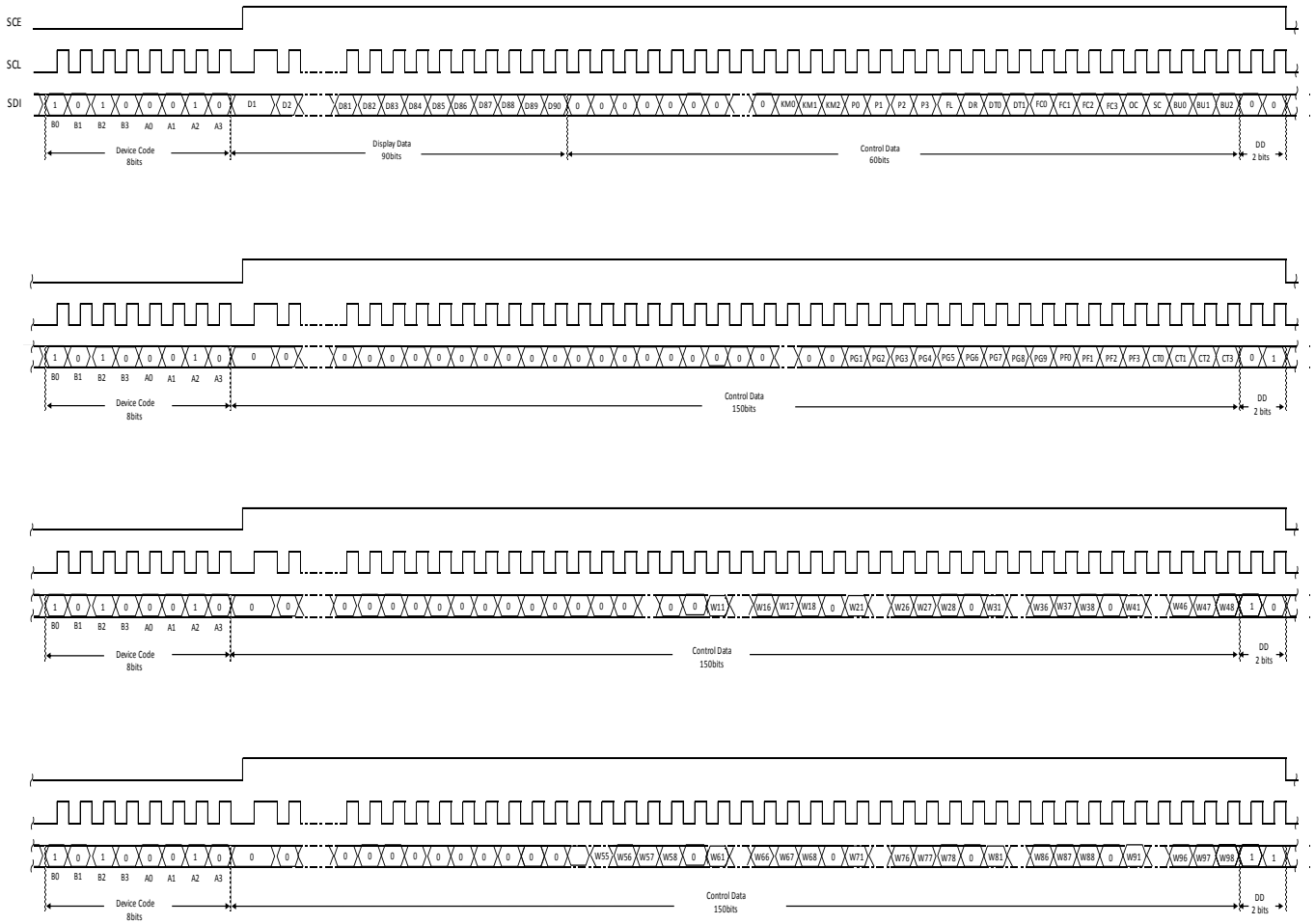


Figure 13. 3-SPI Data Transfer Format

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

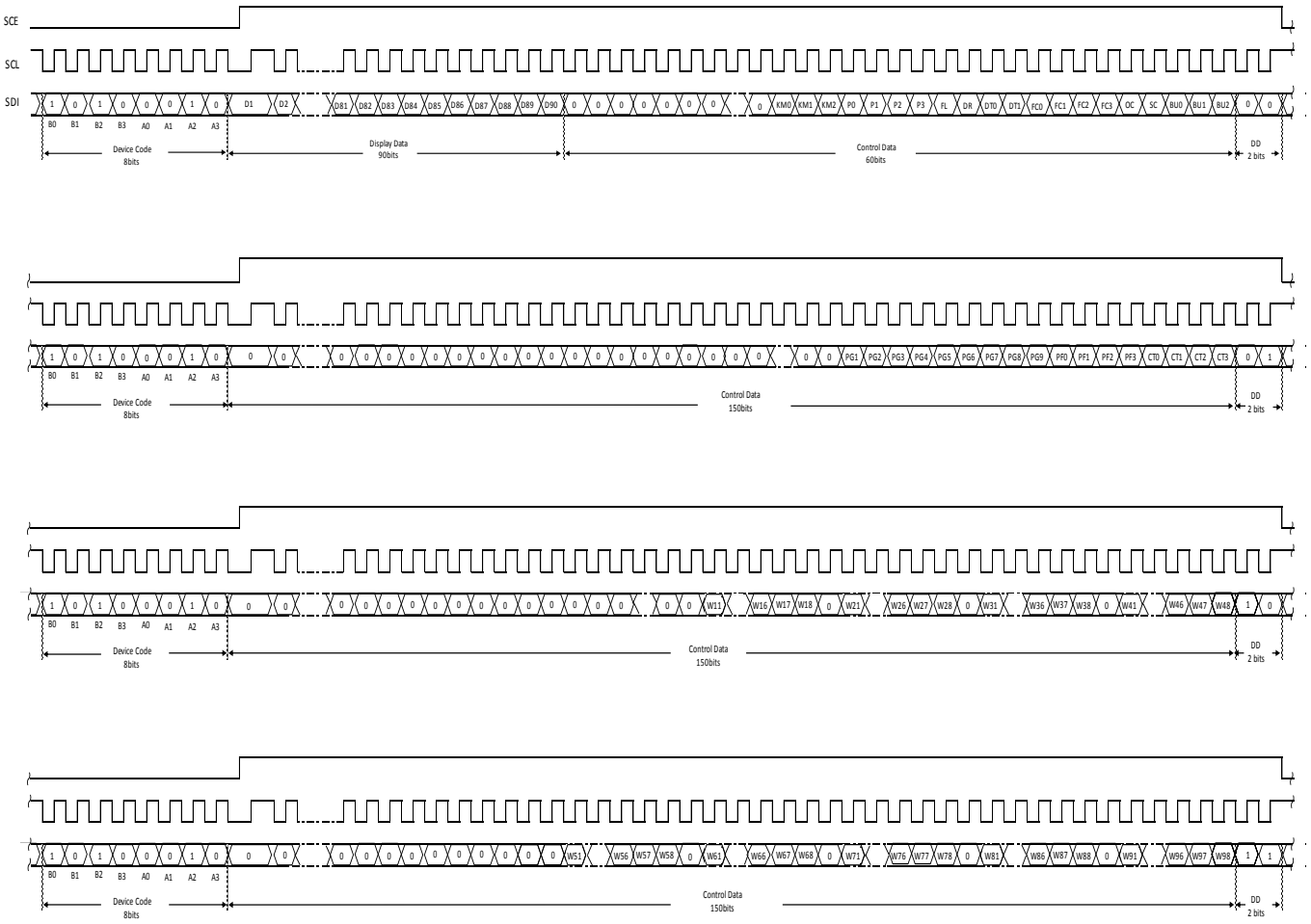


Figure 14. 3-SPI Data Transfer Format

Device code……"45H"
KM0 to KM2……Key Scan output pin / Segment output pin switching control data
D1 to D90……Display data
P0 to P3……Segment / PWM / General-purpose output pin switching control data
FL……Line Inversion or Frame Inversion switching control data
DR……1/3 Bias drive or 1/2 Bias drive switching control data
DT0 to DT1……1/5 Duty drive, 1/4 Duty drive, 1/3 Duty drive or Static drive switching control data
FC0 to FC3……Common / Segment output waveform frame frequency switching control data
OC……Internal oscillator operating mode / External clock operating mode switching control data
SC……Segment on/off switching control data
BU0 to BU2……Normal mode / power-saving mode switching control data
PG1 to PG9……PWM / General-purpose output switching control data
PF0 to PF3……PWM output waveform frame frequency switching control data.
CT0 to CT3……LCD display contrast switching control data.
W11 to W18, W21 to W28, W31 to W38, W41 to W48, W51 to W58, W61 to W68, W71 to W78, W81 to W88, W91 to W98
……PWM output duty switching control data.
DD……Direction data

Control Data Functions

1. KM0,KM1 and KM2: Key Scan output pin / Segment output pin switching control data

These control data bits switch the functions of the KS1/S79 to KS6/S84 output pins between key scan output and segment output.

KM0	KM1	KM2	Output Pin State						Maximum Number of Input Keys	Reset Condition
			KS1/S79	KS2/S80	KS3/S81	KS4/S82	KS5/S83	KS6/S84		
0	0	0	KS1	KS2	KS3	KS4	KS5	KS6	30	-
0	0	1	S79	KS2	KS3	KS4	KS5	KS6	25	-
0	1	0	S79	S80	KS3	KS4	KS5	KS6	20	-
0	1	1	S79	S80	S81	KS4	KS5	KS6	15	-
1	0	0	S79	S80	S81	S82	KS5	KS6	10	-
1	0	1	S79	S80	S81	S82	S83	KS6	5	-
1	1	0	S79	S80	S81	S82	S83	S84	0	-
1	1	1	S79	S80	S81	S82	S83	S84	0	○

2. P0,P1,P2 and P3: Segment / PWM / General-purpose output pin switching control data

These control data bits are used to select the function of the S1/P1/G1 to S9/P9/G9 output pins (Segment Output Pins or PWM Output Pins or General-purpose Output Pins).

P0	P1	P2	P3	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	S7/P7/G7	S8/P8/G8	S9/P9/G9	Reset Condition
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	○
0	0	0	1	P1/G1	S2	S3	S4	S5	S6	S7	S8	S9	-
0	0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	S7	S8	S9	-
0	0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	S7	S8	S9	-
0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	S7	S8	S9	-
0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	S7	S8	S9	-
0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S7	S8	S9	-
0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S8	S9	-
1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	S9	-
1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	P9/S9	-
1	0	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	0	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	0	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	-

PWM output or General-purpose output pin is selected by PGx(x=1 to 9) control data bit.

When the General-purpose Output Pin Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data			
	1/5 Duty Mode	1/4 Duty Mode	1/3 Duty Mode	Static Mode
S1/P1/G1	D1	D1	D1	D1
S2/P2/G2	D6	D5	D4	D2
S3/P3/G3	D11	D9	D7	D3
S4/P4/G4	D16	D13	D10	D4
S5/P5/G5	D21	D17	D13	D4
S6/P6/G6	D26	D21	D16	D5
S7/P7/G7	D31	D25	D19	D7
S8/P8/G8	D36	D29	D22	D8
S9/P9/G9	D41	D33	D25	D9

When the General-purpose Output Pin Function is selected, the respective output pin outputs a “HIGH” level when its corresponding display data is set to “1”. Likewise, it will output a “LOW” level, if its corresponding display data is set to “0”. For example, S4/P4/G4 is used as a General-purpose Output Pin in case of 1/4 Duty, if its corresponding display data – D13is set to “1”, then S4/P4/G4 will output “HIGH(VDD)” level. Likewise, if D13 is set to “0”, then S4/P4/G4 will output “LOW(VSS)” level.

3. FL: Line Inversion or Frame Inversion switching control data

This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion Mode	Reset Condition
0	Line Inversion	○
1	Frame Inversion	-

Typically, when driving large capacitance LCD, Line inversion will increase the influence of crosstalk.
Regarding driving waveform, refer to LCD Driving Waveforms.

Control Data Functions – continued

4. DR: 1/3 Bias drive or 1/2 Bias drive switching control data
This control data bit selects either 1/3 Bias drive or 1/2 Bias drive.

DR	Bias Drive Scheme	Reset Condition
0	1/3 Bias drive	○
1	1/2 Bias drive	-

5. DT: 1/5 Duty drive, 1/4 Duty drive, 1/3 Duty drive or Static drive switching control data
These control data bits select either 1/5 Duty drive, 1/4 Duty drive, 1/3 Duty drive or Static drive

DT0	DT1	Duty Drive Scheme	Reset Condition
0	0	Static drive	○
0	1	1/3 Duty drive	-
1	0	1/4 Duty drive	-
1	1	1/5 Duty drive	-

6. FC0, FC1, FC2 and FC3: Common / Segment output waveform frame frequency switching control data
These control data bits set the display frame frequency.

FC0	FC1	FC2	FC3	Display Frame Frequency fo(Hz)	Reset Condition
0	0	0	0	f_{OSC}*(Note)* / 12288	○
0	0	0	1	f_{OSC} / 10752	-
0	0	1	0	f_{OSC} / 9216	-
0	0	1	1	f_{OSC} / 7680	-
0	1	0	0	f_{OSC} / 6144	-
0	1	0	1	f_{OSC} / 4608	-
0	1	1	0	f_{OSC} / 3840	-
0	1	1	1	f_{OSC} / 3072	-
1	0	0	0	f_{OSC} / 2880	-
1	0	0	1	f_{OSC} / 2688	-
1	0	1	0	f_{OSC} / 2496	-
1	0	1	1	f_{OSC} / 2304	-
1	1	0	0	f_{OSC} / 2112	-
1	1	0	1	f_{OSC} / 1920	-
1	1	1	0	f_{OSC} / 1728	-
1	1	1	1	f_{OSC} / 1536	-

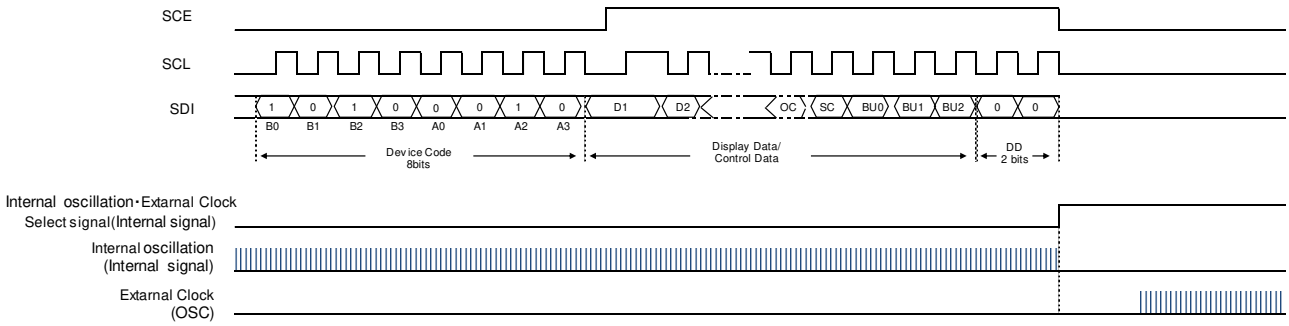
(*Note*) f_{OSC}: Internal oscillation frequency (600 kHz Typ)

7. OC: Internal oscillator operating mode / External clock operating mode switching control data

OC	Operating Mode	In/Out Pin(OSC/S90) Status	Reset Condition
0	Internal oscillator	S90 (segment output)	○
1	External Clock	OSC (clock input)	-

OC=1 : OSC/S90 pin can be used as input clock pin when External Clock is set by the control data.

<External Clock input timing function>
Internal oscillation / external clock select signal behavior is below.
Please input external clock after serial data sending.



8. SC: Segment on/off switching control data
This control data bit controls the on/off state of the segments.

SC	Display State	Reset Condition
0	On	-
1	Off	○

Note that when the segments are turned off by setting SC to “1”, the segments are turned off by outputting segment off waveforms from the segment output pins.

Control Data Functions – continued

9. BU0,BU1 and BU2: Normal mode / Power-saving mode switching control data
These control data bits select either normal mode or power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment Outputs	Output Pin States During Key Scan Standby						Reset Condition
					Common Outputs	KS1	KS2	KS3	KS4	KS5	KS6	
0	0	0	Normal	Operating	Operating	H	H	H	H	H	H	-
0	0	1	Power -saving	Stopped	Low (VSS)	L	L	L	L	L	H	-
0	1	0				L	L	L	L	H	H	-
0	1	1				L	L	L	H	H	H	-
1	0	0				L	L	H	H	H	H	-
1	0	1				L	H	H	H	H	H	-
1	1	0				H	H	H	H	H	H	-
1	1	1				H	H	H	H	H	H	○

Power-saving mode status: S1/P1/G1 to S9/P9/G9=active only General-purpose output
S10 to OSC/S90=low (VSS)
COM1 to COM5=low (VSS)
Stop the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible when at Power-saving mode.

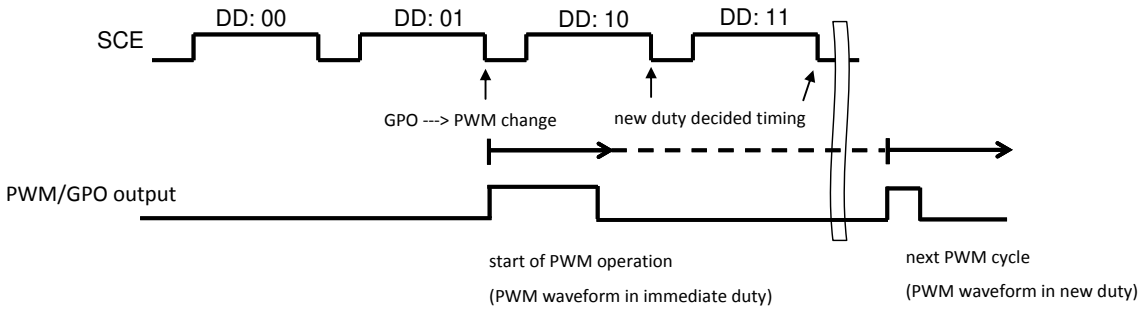
10. PG1, PG2, PG3, PG4, PG5, PG6, PG7, PG8 and PG9: PWM / General-purpose output switching control data
This control data bit select either PWM output or General-purpose output of Sx/Px/Gx pins. (x=1 to 9)

PGx(x=1 to 9)	Mode	Reset Condition
0	PWM output	○
1	General-purpose output	-

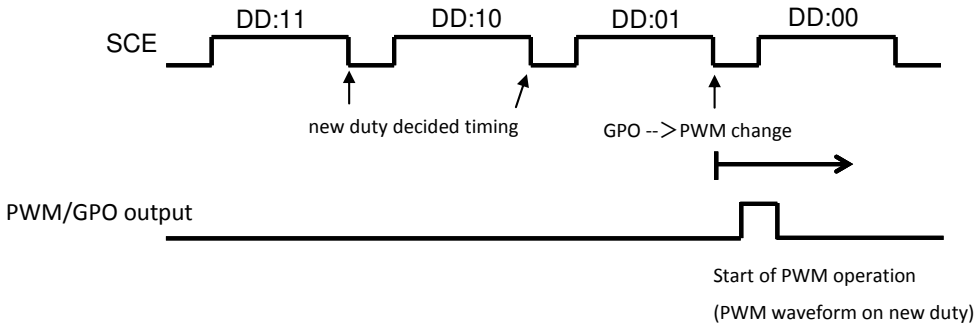
<PWM<->GPO Changing function>

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 01 during GPO -→ PWM change.
- Please take care of reflect timing of new duty setting of DD: 10 and DD: 11 is from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



Control Data Functions – continued

11. PF0, PF1, PF2, and PF3: PWM output waveform frame frequency switching control data
These control data bits set the frame frequency for PWM output waveforms.

PF0	PF1	PF2	PF3	PWM Output Frame Frequency fp(Hz)	Reset Condition
0	0	0	0	f_{OSC}/4096	○
0	0	0	1	f_{OSC}/3840	-
0	0	1	0	f_{OSC}/3584	-
0	0	1	1	f_{OSC}/3328	-
0	1	0	0	f_{OSC}/3072	-
0	1	0	1	f_{OSC}/2816	-
0	1	1	0	f_{OSC}/2560	-
0	1	1	1	f_{OSC}/2304	-
1	0	0	0	f_{OSC}/2048	-
1	0	0	1	f_{OSC}/1792	-
1	0	1	0	f_{OSC}/1536	-
1	0	1	1	f_{OSC}/1280	-
1	1	0	0	f_{OSC}/1024	-
1	1	0	1	f_{OSC}/768	-
1	1	1	0	f_{OSC}/512	-
1	1	1	1	f_{OSC}/256	-

12. CT0, CT1, CT2 and CT3: LCD display contrast switching control data
These control data bits set display contrast

CT0	CT1	CT2	CT3	LCD Drive Bias Voltage for VLCD Level	Reset Condition
0	0	0	0	1.000*VDD	○
0	0	0	1	0.975*VDD	-
0	0	1	0	0.950*VDD	-
0	0	1	1	0.925*VDD	-
0	1	0	0	0.900*VDD	-
0	1	0	1	0.875*VDD	-
0	1	1	0	0.850*VDD	-
0	1	1	1	0.825*VDD	-
1	0	0	0	0.800*VDD	-
1	0	0	1	0.775*VDD	-
1	0	1	0	0.750*VDD	-
1	0	1	1	0.725*VDD	-
1	1	0	0	0.700*VDD	-
1	1	0	1	0.675*VDD	-
1	1	1	0	0.650*VDD	-
1	1	1	1	0.625*VDD	-

This control data bit set VLCD maximum voltage for LCD drive voltage.

Avoid setting VLCD voltage under 2.5V.
And ensure “VDD - VLCD > 0.6” condition is satisfied.
Unstable IC output voltage may result if the above conditions are not satisfied.

The relationship of LCD display contrast setting and VLCD voltage

CT Setting	Formula	VDD=6.000	VDD=5.500	VDD=5.000	VDD= 4.500	VDD= 4.000	VDD= 3.000	Unit
0	VDD	VLCD=6.000	VLCD=5.500	VLCD=5.000	VLCD= 4.500	VLCD= 4.000	VLCD= 3.000	V
1	0.975*VDD	VLCD=5.850	VLCD=5.363	VLCD=4.875	VLCD= 4.388	VLCD= 3.900	VLCD= 2.925	V
2	0.950*VDD	VLCD=5.700	VLCD=5.225	VLCD=4.750	VLCD= 4.275	VLCD= 3.800	VLCD= 2.850	V
3	0.925*VDD	VLCD=5.550	VLCD=5.088	VLCD=4.625	VLCD= 4.163	VLCD= 3.700	VLCD= 2.775	V
4	0.900*VDD	VLCD=5.400	VLCD=4.950	VLCD=4.500	VLCD= 4.050	VLCD= 3.600	VLCD= 2.700	V
5	0.875*VDD	VLCD=5.250	VLCD=4.813	VLCD=4.375	VLCD= 3.938	VLCD= 3.500	VLCD= 2.625	V
6	0.850*VDD	VLCD=5.100	VLCD=4.675	VLCD=4.250	VLCD= 3.825	VLCD= 3.400	VLCD= 2.550	V
7	0.825*VDD	VLCD=4.950	VLCD=4.538	VLCD=4.125	VLCD= 3.713	VLCD= 3.300	VLCD= 2.475	V
8	0.800*VDD	VLCD=4.800	VLCD=4.400	VLCD=4.000	VLCD= 3.600	VLCD= 3.200	VLCD= 2.400	V
9	0.775*VDD	VLCD=4.650	VLCD=4.263	VLCD=3.875	VLCD= 3.488	VLCD= 3.100	VLCD= 2.325	V
10	0.750*VDD	VLCD=4.500	VLCD=4.125	VLCD=3.750	VLCD= 3.375	VLCD= 3.000	VLCD= 2.250	V
11	0.725*VDD	VLCD=4.350	VLCD=3.988	VLCD=3.625	VLCD= 3.263	VLCD= 2.900	VLCD= 2.175	V
12	0.700*VDD	VLCD=4.200	VLCD=3.850	VLCD=3.500	VLCD= 3.150	VLCD= 2.800	VLCD= 2.100	V
13	0.675*VDD	VLCD=4.050	VLCD=3.713	VLCD=3.375	VLCD= 3.038	VLCD= 2.700	VLCD= 2.025	V
14	0.650*VDD	VLCD=3.900	VLCD=3.575	VLCD=3.250	VLCD= 2.925	VLCD= 2.600	VLCD= 1.950	V
15	0.625*VDD	VLCD=3.750	VLCD=3.438	VLCD=3.125	VLCD= 2.813	VLCD= 2.500	VLCD= 1.875	V

Disabled

Control Data Functions – continued

13. W11 to W18[(Note)], W21 to W28, W31 to W38, W41 to W48, W51 to W58, W61 to W68, W71 to W78, W81 to W88 and W91 to W98: PWM output waveform duty setting control data.
These control data bits set the high level pulse width (duty) for PWM output waveforms.

N = 1 to 9 , Tp = 1/fp

Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	Wn8	PWM Duty	Reset Condition
0	0	0	0	0	0	0	0	(0/256) x Tp	○
0	0	0	0	0	0	0	1	(1/256) x Tp	-
0	0	0	0	0	0	1	0	(2/256) x Tp	-
0	0	0	0	0	0	1	1	(3/256) x Tp	-
0	0	0	0	0	1	0	0	(4/256) x Tp	-
0	0	0	0	0	1	0	1	(5/256) x Tp	-
0	0	0	0	0	1	1	0	(6/256) x Tp	-
0	0	0	0	0	1	1	1	(7/256) x Tp	-
0	0	0	0	1	0	0	0	(8/256) x Tp	-
0	0	0	0	1	0	0	1	(9/256) x Tp	-
0	0	0	0	1	0	1	0	(10/256) x Tp	-
0	0	0	0	1	0	1	1	(11/256) x Tp	-
0	0	0	0	1	1	0	0	(12/256) x Tp	-
0	0	0	0	1	1	0	1	(13/256) x Tp	-
0	0	0	0	1	1	1	0	(14/256) x Tp	-
0	0	0	0	1	1	1	1	(15/256) x Tp	-
0	0	0	1	0	0	0	0	(16/256) x Tp	-
0	0	0	1	0	0	0	1	(17/256) x Tp	-
0	0	0	1	0	0	1	0	(18/256) x Tp	-
0	0	0	1	0	0	1	1	(19/256) x Tp	-
0	0	0	1	0	1	0	0	(20/256) x Tp	-
…	…	…	…	…	…	…	…	…	…
1	1	1	0	1	0	1	1	(235/256) x Tp	-
1	1	1	0	1	1	0	0	(236/256) x Tp	-
1	1	1	0	1	1	0	1	(237/256) x Tp	-
1	1	1	0	1	1	1	0	(238/256) x Tp	-
1	1	1	0	1	1	1	1	(239/256) x Tp	-
1	1	1	1	0	0	0	0	(240/256) x Tp	
1	1	1	1	0	0	0	1	(241/256) x Tp	-
1	1	1	1	0	0	1	0	(242/256) x Tp	-
1	1	1	1	0	0	1	1	(243/256) x Tp	-
1	1	1	1	0	1	0	0	(244/256) x Tp	-
1	1	1	1	0	1	0	1	(245/256) x Tp	-
1	1	1	1	0	1	1	0	(246/256) x Tp	-
1	1	1	1	0	1	1	1	(247/256) x Tp	-
1	1	1	1	1	0	0	0	(248/256) x Tp	-
1	1	1	1	1	0	0	1	(249/256) x Tp	-
1	1	1	1	1	0	1	0	(250/256) x Tp	-
1	1	1	1	1	0	1	1	(251/256) x Tp	-
1	1	1	1	1	1	0	0	(252/256) x Tp	-
1	1	1	1	1	1	0	1	(253/256) x Tp	-
1	1	1	1	1	1	1	0	(254/256) x Tp	-
1	1	1	1	1	1	1	1	(255/256) x Tp	-

(*Note*) W11 to W18:S1/P1/G1 pwm duty data
W21 to W28:S2/P2/G2 pwm duty data
W31 to W38:S3/P3/G3 pwm duty data
W41 to W48:S4/P4/G4 pwm duty data
W51 to W58:S5/P5/G5 pwm duty data
W61 to W68:S6/P6/G6 pwm duty data
W71 to W78:S7/P7/G7 pwm duty data
W81 to W88:S8/P8/G8 pwm duty data
W91 to W98:S9/P9/G9 pwm duty data

Display Data and Output Pin Correspondence

1. 1/5 Duty

Output Pin*(Note)*	COM1	COM2	COM3	COM4	COM5
S1/P1/G1	D1	D2	D3	D4	D5
S2/P2/G2	D6	D7	D8	D9	D10
S3/P3/G3	D11	D12	D13	D14	D15
S4/P4/G4	D16	D17	D18	D19	D20
S5/P5/G5	D21	D22	D23	D24	D25
S6/P6/G6	D26	D27	D28	D29	D30
S7/P7/G7	D31	D32	D33	D34	D35
S8/P8/G8	D36	D37	D38	D39	D40
S9/P9/G9	D41	D42	D43	D44	D45
S10	D46	D47	D48	D49	D50
S11	D51	D52	D53	D54	D55
S12	D56	D57	D58	D59	D60
S13	D61	D62	D63	D64	D65
S14	D66	D67	D68	D69	D70
S15	D71	D72	D73	D74	D75
S16	D76	D77	D78	D79	D80
S17	D81	D82	D83	D84	D85
S18	D86	D87	D88	D89	D90
S19	D91	D92	D93	D94	D95
S20	D96	D97	D98	D99	D100
S21	D101	D102	D103	D104	D105
S22	D106	D107	D108	D109	D110
S23	D111	D112	D113	D114	D115
S24	D116	D117	D118	D119	D120
S25	D121	D122	D123	D124	D125
S26	D126	D127	D128	D129	D130
S27	D131	D132	D133	D134	D135
S28	D136	D137	D138	D139	D140
S29	D141	D142	D143	D144	D145
S30	D146	D147	D148	D149	D150
S31	D151	D152	D153	D154	D155
S32	D156	D157	D158	D159	D160
S33	D161	D162	D163	D164	D165
S34	D166	D167	D168	D169	D170
S35	D171	D172	D173	D174	D175
S36	D176	D177	D178	D179	D180
S37	D181	D182	D183	D184	D185
S38	D186	D187	D188	D189	D190
S39	D191	D192	D193	D194	D195
S40	D196	D197	D198	D199	D200
S41	D201	D202	D203	D204	D205
S42	D206	D207	D208	D209	D210
S43	D211	D212	D213	D214	D215
S44	D216	D217	D218	D219	D220
S45	D221	D222	D223	D224	D225
S46	D226	D227	D228	D229	D230
S47	D231	D232	D233	D234	D235
S48	D236	D237	D238	D239	D240
S49	D241	D242	D243	D244	D245
S50	D246	D247	D248	D249	D250
S51	D251	D252	D253	D254	D255
S52	D256	D257	D258	D259	D260
S53	D261	D262	D263	D264	D265
S54	D266	D267	D268	D269	D270
S55	D271	D272	D273	D274	D275
S56	D276	D277	D278	D279	D280
S57	D281	D282	D283	D284	D285
S58	D286	D287	D288	D289	D290
S59	D291	D292	D293	D294	D295
S60	D296	D297	D298	D299	D300
S61	D301	D302	D303	D304	D305
S62	D306	D307	D308	D309	D310
S63	D311	D312	D313	D314	D315

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89, and OSC/S90. Also, COM5/S78 pin is used as Common output.

Display Data and Output Pin Correspondence – continued

Output Pin(Note)	COM1	COM2	COM3	COM4	COM5
S64	D316	D317	D318	D319	D320
S65	D321	D322	D323	D324	D325
S66	D326	D327	D328	D329	D330
S67	D331	D332	D333	D334	D335
S68	D336	D337	D338	D339	D340
S69	D341	D342	D343	D344	D345
S70	D346	D347	D348	D349	D350
S71	D351	D352	D353	D354	D355
S72	D356	D357	D358	D359	D360
S73	D361	D362	D363	D364	D365
S74	D366	D367	D368	D369	D370
S75	D371	D372	D373	D374	D375
S76	D376	D377	D378	D379	D380
S77	D381	D382	D383	D384	D385
KS1/S79	D386	D387	D388	D389	D390
KS2/S80	D391	D392	D393	D394	D395
KS3/S81	D396	D397	D398	D399	D400
KS4/S82	D401	D402	D403	D404	D405
KS5/S83	D406	D407	D408	D409	D410
KS6/S84	D411	D412	D413	D414	D415
KI1/S85	D416	D417	D418	D419	D420
KI2/S86	D421	D422	D423	D424	D425
KI3/S87	D426	D427	D428	D429	D430
KI4/S88	D431	D432	D433	D434	D435
KI5/S89	D436	D437	D438	D439	D440
OSC/S90	D441	D442	D443	D444	D445

(*Note*) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89 and OSC/S90. Also, COM5/S78 pin is used as Common output.

To illustrate further, the states of the S21 output pin is given in the table below.

Display Data					State of S21 Output Pin
D101	D102	D103	D104	D105	
0	0	0	0	0	LCD Segments corresponding to COM1 to COM5 are OFF.
0	0	0	0	1	LCD Segment corresponding to COM5 is ON.
0	0	0	1	0	LCD Segment corresponding to COM4 is ON.
0	0	0	1	1	LCD Segments corresponding to COM4 and COM5 are ON.
0	0	1	0	0	LCD Segment corresponding to COM3 is ON.
0	0	1	0	1	LCD Segments corresponding to COM3 and COM5 are ON.
0	0	1	1	0	LCD Segments corresponding to COM3 and COM4 are ON.
0	0	1	1	1	LCD Segments corresponding to COM3, COM4 and COM5 are ON.
0	1	0	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	0	1	LCD Segments corresponding to COM2 and COM5 are ON.
0	1	0	1	0	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	0	1	1	LCD Segments corresponding to COM2, COM4 and COM5 are ON.
0	1	1	0	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	0	1	LCD Segments corresponding to COM2, COM3, and COM5 are ON.
0	1	1	1	0	LCD Segments corresponding to COM2, COM3, and COM4 are ON.
0	1	1	1	1	LCD Segments corresponding to COM2, COM3, COM4 and COM5 are ON.
1	0	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	0	1	LCD Segments corresponding to COM1 and COM5 are ON.
1	0	0	1	0	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	0	1	1	LCD Segments corresponding to COM1, COM4 and COM5 are ON.
1	0	1	0	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	0	1	LCD Segments corresponding to COM1, COM3 and COM5 are ON.
1	0	1	1	0	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	0	1	1	1	LCD Segments corresponding to COM1, COM3, COM4 and COM5 are ON.
1	1	0	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	0	1	LCD Segments corresponding to COM1, COM2 and COM5 are ON.
1	1	0	1	0	LCD Segments corresponding to COM1, COM2 and COM4 are ON.
1	1	0	1	1	LCD Segments corresponding to COM1, COM2, COM4 and COM5 are ON.
1	1	1	0	0	LCD Segments corresponding to COM1, COM2 and COM3 are ON.
1	1	1	0	1	LCD Segments corresponding to COM1, COM2, COM3 and COM5 are ON.
1	1	1	1	0	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.
1	1	1	1	1	LCD Segments corresponding to COM1, COM2, COM3, COM4 and COM5 are ON.

Display Data and Output Pin Correspondence – continued

2. 1/4 Duty

Output Pin*(Note)*	COM1	COM2	COM3	COM4
S1/P1/G1	D1	D2	D3	D4
S2/P2/G2	D5	D6	D7	D8
S3/P3/G3	D9	D10	D11	D12
S4/P4/G4	D13	D14	D15	D16
S5/P5/G5	D17	D18	D19	D20
S6/P6/G6	D21	D22	D23	D24
S7/P7/G7	D25	D26	D27	D28
S8/P8/G8	D29	D30	D31	D32
S9/P9/G9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, COM5/S78, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89 and OSC/S90.

Display Data and Output Pin Correspondence – continued

Output Pin(Note)	COM1	COM2	COM3	COM4
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S67	D265	D266	D267	D268
S68	D269	D270	D271	D272
S69	D273	D274	D275	D276
S70	D277	D278	D279	D280
S71	D281	D282	D283	D284
S72	D285	D286	D287	D288
S73	D289	D290	D291	D292
S74	D293	D294	D295	D296
S75	D297	D298	D299	D300
S76	D301	D302	D303	D304
S77	D305	D306	D307	D308
COM5/S78	D309	D310	D311	D312
KS1/S79	D313	D314	D315	D316
KS2/S80	D317	D318	D319	D320
KS3/S81	D321	D322	D323	D324
KS4/S82	D325	D326	D327	D328
KS5/S83	D329	D330	D331	D332
KS6/S84	D333	D334	D335	D336
KI1/S85	D337	D338	D339	D340
KI2/S86	D341	D342	D343	D344
KI3/S87	D345	D346	D347	D348
KI4/S88	D349	D350	D351	D352
KI5/S89	D353	D354	D355	D356
OSC/S90	D357	D358	D359	D360

(*Note*) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, COM5/S78, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89 and OSC/S90.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data				State of S21 Output Pin
D81	D82	D83	D84	
0	0	0	0	LCD Segments corresponding to COM1 to COM4 are OFF.
0	0	0	1	LCD Segment corresponding to COM4 is ON.
0	0	1	0	LCD Segment corresponding to COM3 is ON.
0	0	1	1	LCD Segments corresponding to COM3 and COM4 are ON.
0	1	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	1	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	1	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	1	LCD Segments corresponding to COM2, COM3 and COM4 are ON.
1	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	1	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	1	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	1	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	1	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	1	LCD Segments corresponding to COM1, COM2, and COM4 are ON.
1	1	1	0	LCD Segments corresponding to COM1, COM2, and COM3 are ON.
1	1	1	1	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.

Display Data and Output Pin Correspondence – continued

3. 1/3 Duty

Output Pin*(Note)*	COM1	COM2	COM3
S1/P1/G1	D1	D2	D3
S2/P2/G2	D4	D5	D6
S3/P3/G3	D7	D8	D9
S4/P4/G4	D10	D11	D12
S5/P5/G5	D13	D14	D15
S6/P6/G6	D16	D17	D18
S7/P7/G7	D19	D20	D21
S8/P8/G8	D22	D23	D24
S9/P9/G9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D85	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
S56	D166	D167	D168
S57	D169	D170	D171
S58	D172	D173	D174
S59	D175	D176	D177
S60	D178	D179	D180
S61	D181	D182	D183
S62	D184	D185	D186
S63	D187	D188	D189

(Note) The Segment Output Pin function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, COM5/S78, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89 and OSC/S90