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Datasheet

Low Duty LCD Segment Driver for Automotive Application

BU91600xxx-M Series **MAX 148 Segments (37SEG x 4COM)**

General Description

The BU91600FV-M and BU91600FUV-M are a 1/4, 1/3, 1/2duty or Static general-purpose LCD driver that can be used for automotive applications. BU91600FV-M can drive up to 116 LCD Segments and BU91600FUV-M can drive up to 148 LCD Segments.
This product can support VA LCD displays, which has better optical performance with higher LCD voltage driving and higher frame frequency driving.
It can support operating temperature of up to +105°C and is qualified for AEC-Q100 Grade2, as required for automotive applications.
It can control up to 16 general-purpose outputs / 16 PWM output ports for LED backlighting and LED button illumination realizing less flicker by various frequency setting function.
It can also support a key scan function that detects a maximum of 20 key inputs to reduce PCB wiring and to minimize microcontroller size and cost.
It can support LCD contrast adjustment by its EVR function and TTL compatible input interface is also available, these are well-suited for wide-voltage range of MCUs.

Features

- AEC-Q100 Qualified *(Note)*
- 1/4, 1/3, 1/2duty or Static setting selectable
  BU91600FV-M
  1/4duty: Max 116 segments,
  1/3duty: Max 87 segments
  1/2duty: Max 58 segments,
  Static: Max 29 segments
  BU91600FUV-M
  1/4duty: Max 148 segments,
  1/3duty: Max 111 segments
  1/2duty: Max 74 segments,
  Static: Max 37 segments
- 1/3 or 1/2 bias setting selectable
- Support wide range of operation voltage from 2.7V to 6.0V, which can support TN LCD and VA LCD display.
- Integrated LCD voltage driving circuit
- Integrated oscillation circuit for LCD frame frequency
- Line or Frame inversion driving selectable
- Max 16ch external PWM outputs
  (SEG outputs/general purpose outputs selectable)
- Max 6ch internal PWM outputs
  (SEG outputs/general purpose outputs/external PWM outputs selectable)
- Support 256 step PWM function to realize backlight/ button LED illumination
- Support LCD frame frequency from 50Hz to 685Hz, total 128setting.
- Support PWM frequency from 146Hz to 2.34KHz, total 16setting
- Support external PWM input
- Support 3 wire serial interface + KEYOUT
- Support TTL level input to connect 3.3V MCU directly Circuit
- Support Max 20 key input detection (SEG selectable)
- Integrated EVR function to adjust LCD contrast
- Integrated voltage detected type power on reset
- No external components required
- Low power consumption design

(Note) Grade 2

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +105°C
- Max Segments:
  BU91600FV-M 116 Segments
  BU91600FUV-M 148 Segments
- Display Duty Static, 1/2, 1/3, 1/4 Selectable
- Bias: 1/2, 1/3 Selectable
- Interface: 3wire Serial Interface

Special Characteristics

- Electrostatic Discharge Voltage(HBM): ±2000V
- Latch-up Current: ±100mA

Applications

- Instrument Clusters
- Climate Controls
- Car Audios
- Car Radios
- Metering
- White Goods
- Healthcare Products
- Battery operated products

etc.

Package

W (Typ) x D (Typ) x H (Max)

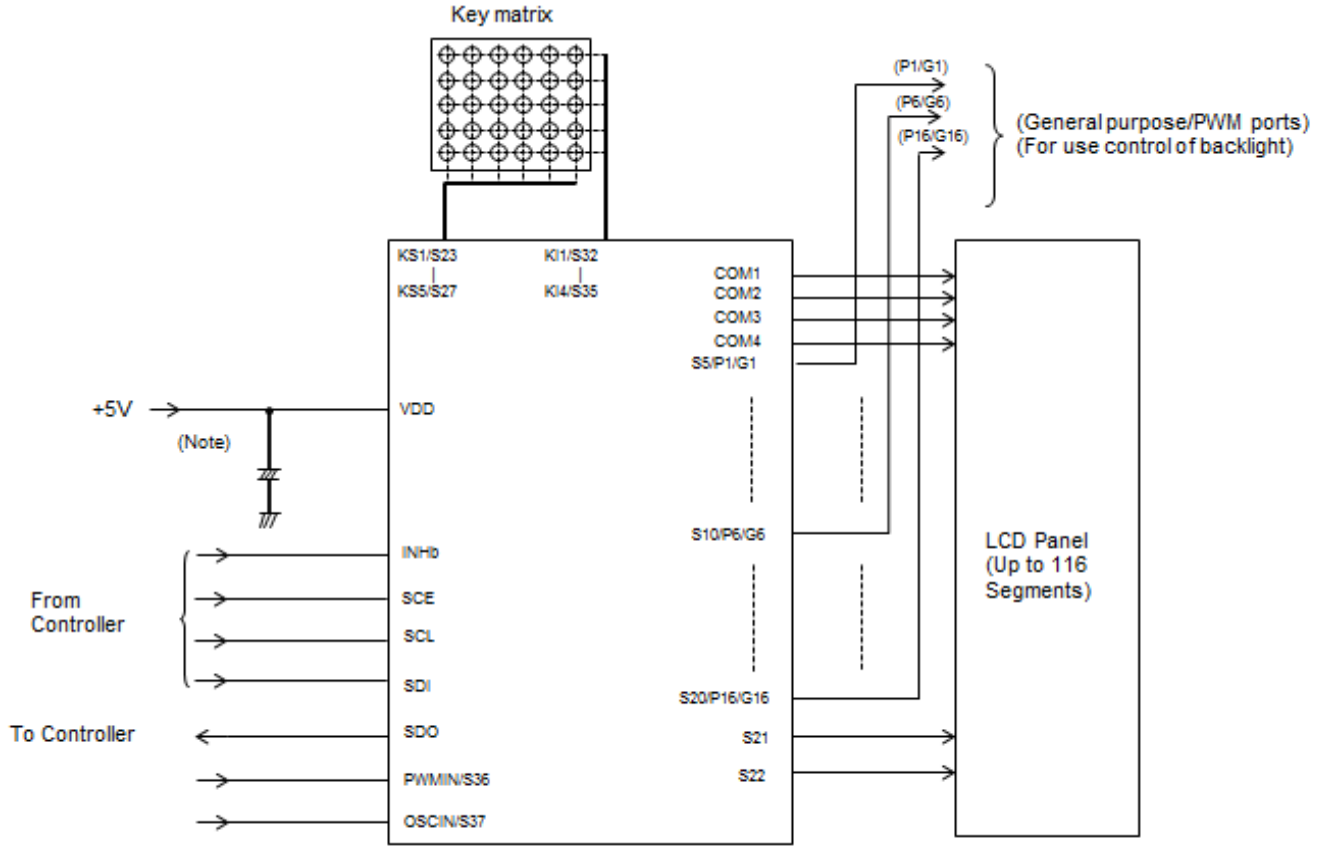
SSOP-B40
13.60mm x 7.80mm x 2.00mm

TSSOP-C48V
12.50mm x 8.10mm x 1.00mm

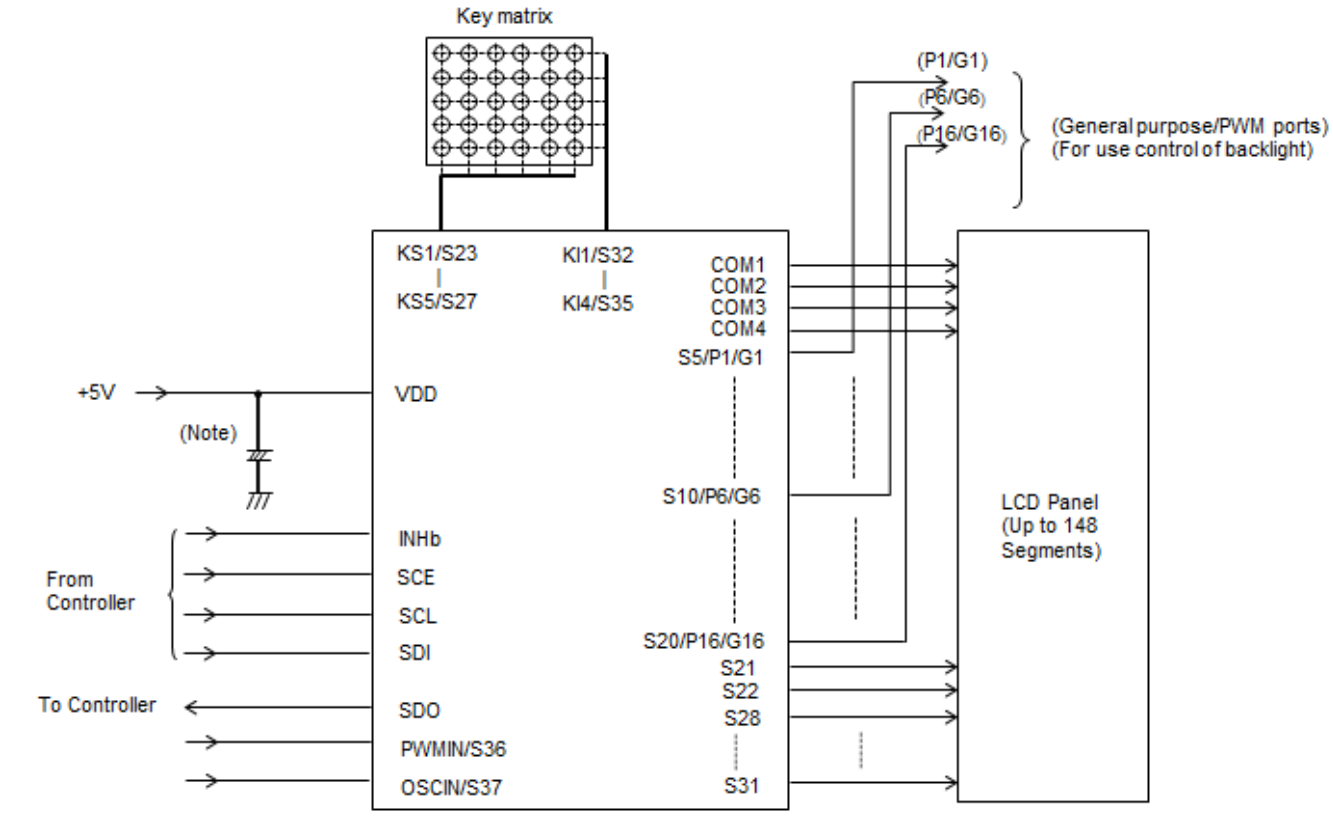
○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Typical Application Circuit

BU91600FV-M



BU91600FUV-M



(Note) Insert capacitors between VDD and VSS C > 0.1µF.

Figure 1. Typical Application Circuit

Block Diagram

BU91600FV-M

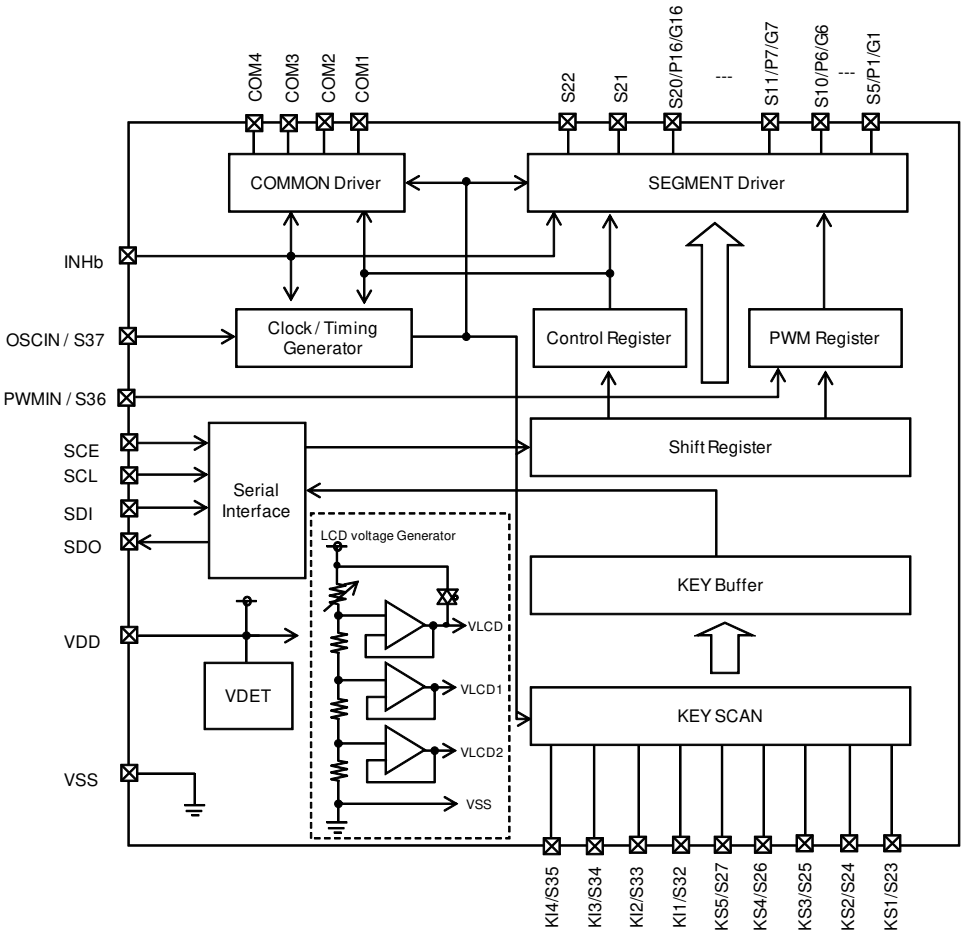


Figure 2. Block Diagram

Pin Arrangement

BU91600FV-M

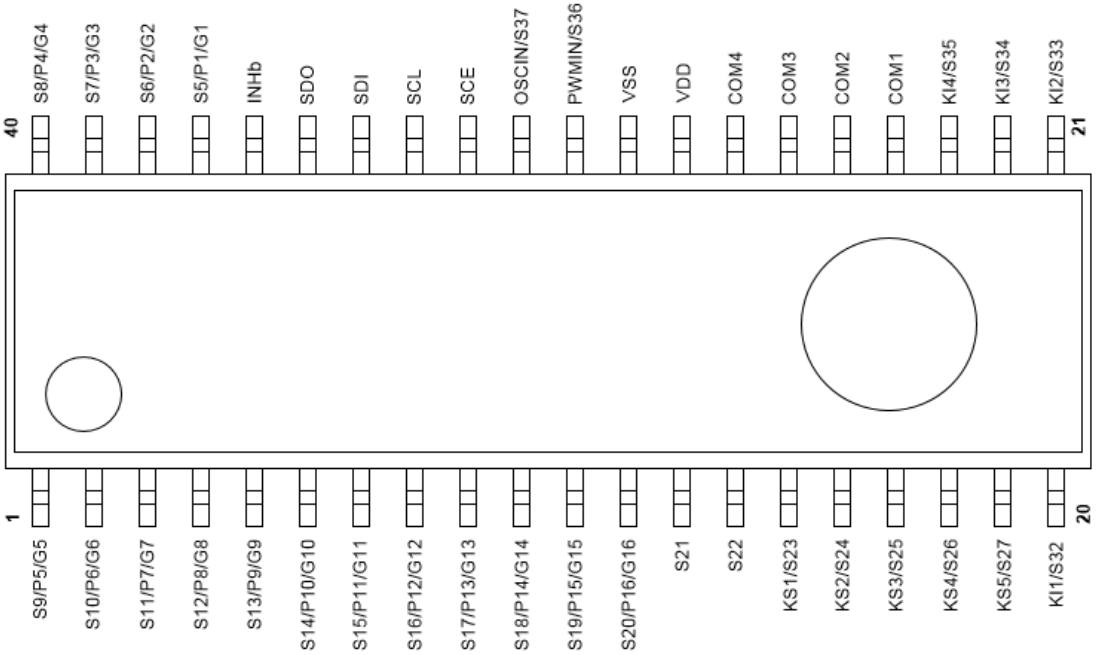


Figure 3. Pin Configuration (TOP VIEW)

Block Diagram

BU91600FUV-M

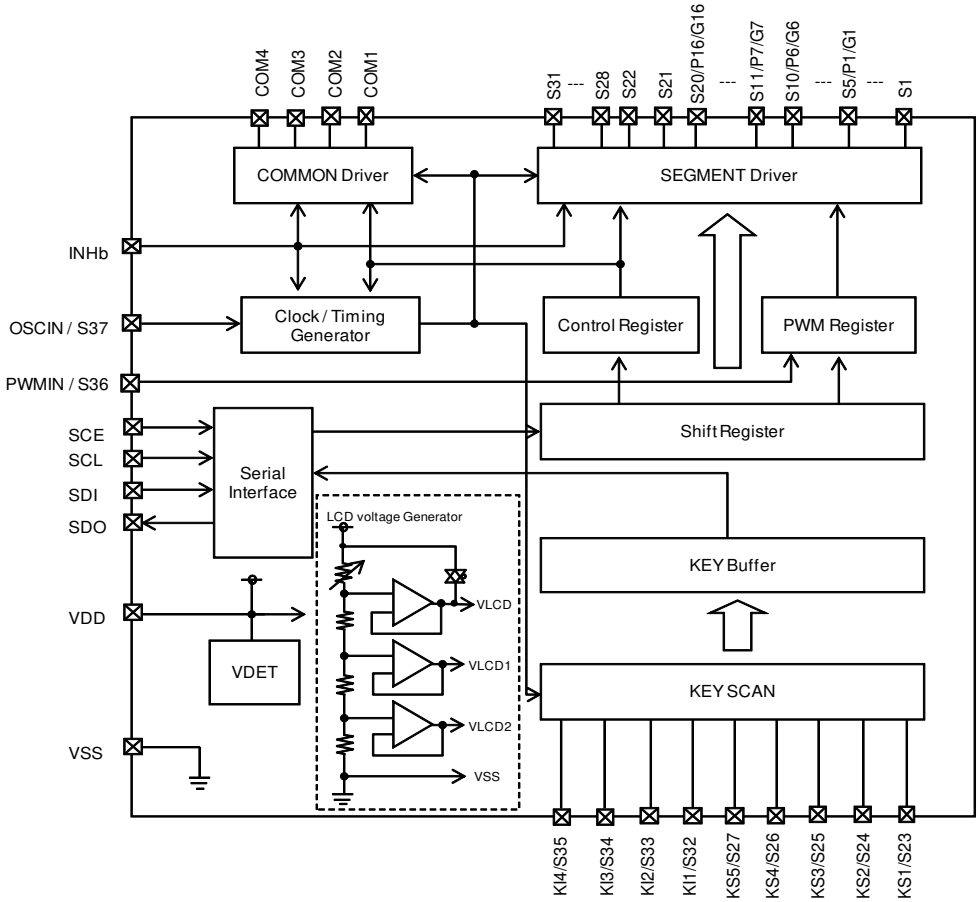


Figure 4. Block Diagram

Pin Arrangement

BU91600FUV-M

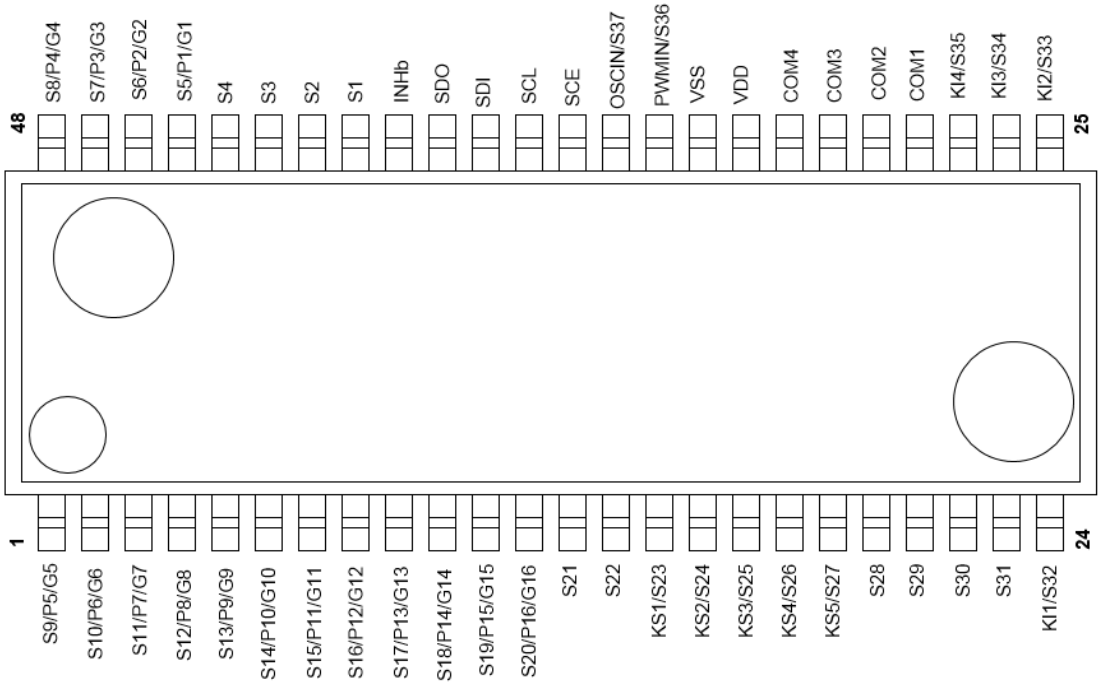


Figure 5. Pin Configuration (TOP VIEW)

Absolute Maximum Ratings(VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum Supply Voltage	VDD	VDD	-0.3 to +7.0	V
Input Voltage	V_{IN1}	SCE, SCL, SDI, INHb, PWMIN*(Note 1)*, OSCIN*(Note 2)*	-0.3 to +7.0	V
	V_{IN2}	KI1 to KI4*(Note 3)*	-0.3 to +7.0	V
Allowable Loss	Pd	BU91600FV-M	0.70*(Note 4)*	W
		BU91600FUV-M	0.64*(Note 4)*	W
Operating Temperature	Topr		-40 to +105	°C
Storage Temperature	Tstg		-55 to +125	°C

(Note 1) In case of External PWM setting.
(Note 2) In case of External clock mode setting.
(Note 3) In case of Key scan setting
(Note 4) Delete by 7.00mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board [BU91600FV-M]).
Delete by 6.40mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board [BU91600FUV-M])
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = -40°C to +105°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Supply Voltage	VDD		2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	V_{H1}	SCE, SCL, SDI, INHb, PWMIN*(Note1)*,OSCIN*(Note 2)*		-	0.03VDD	-	V
	V_{H2}	KI1 to KI4*(Note 3)*		-	0.1VDD	-	V
Power-on Detection Voltage	V_{DET}	VDD		1.3	1.8	2.2	V
"H" Level Input Voltage	V_{IH1}	SCE, SCL, SDI, INHb, PWMIN*(Note 1)*,OSCIN*(Note 2)*	4.5V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	V_{IH2}	SCE, SCL, SDI, INHb, PWMIN*(Note 1)*,OSCIN*(Note 2)*	2.7V ≤ VDD < 4.5V	0.8VDD	-	VDD	V
	V_{IH3}	KI1 to KI4*(Note 3)*		0.7VDD	-	VDD	V
"L" Level Input Voltage	V_{IL1}	SCE,SCL,SDI,INHb, PWMIN*(Note 1)*,OSCIN*(Note 2* KI1 to KI4*(Note 3)*		0	-	0.2VDD	V
Input Floating Voltage	V_{IF}	KI1 to KI4*(Note 3)*		-	-	0.05VDD	V
Pull-down Resistance	R_{PD}	KI1 to KI4*(Note 3)*	VDD=5.0V	50	100	250	kΩ
Output Off Leakage Current	I_{OFFH}	SDO	VO=6.0V	-	-	6.0	µA
"H" Level Input Current	I_{IH1}	SCE, SCL, SDI, INHb, PWMIN*(Note 1)*,OSCIN*(Note 2)*	VI = 5.5V	-	-	5.0	µA
"L" Level Input Current	I_{IL1}	SCE, SCL, SDI, INHb, PWMIN*(Note 1)*,OSCIN*(Note 2)*	VI = 0V	-5.0	-	-	µA
"H" Level Output Voltage	V_{OH1}	S1 to S37	IO = -20µA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	V_{OH2}	COM1 to COM4	IO = -100µA, VLCD=1.00*VDD	VDD-0.9	-	-	
	V_{OH3}	P1/G1 to P16/G16*(Note 5)*	IO = -1mA	VDD-0.9	-	-	
	V_{OH4}	KS1 to KS5*(Note 3)*	IO = -500µA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	V_{OL1}	S1 to S37	IO = 20µA	-	-	0.9	V
	V_{OL2}	COM1 to COM4	IO = 100µA	-	-	0.9	
	V_{OL3}	P1/G1 to P16/G16*(Note 5)*	IO = 1mA	-	-	0.9	
	V_{OL4}	KS1 to KS5*(Note 3)*	IO = 25µA	0.2	0.5	1.5	
	V_{OL5}	SDO	IO = 1mA	-	0.1	0.5	

(Note 5) General –purpose / PWM outputs setting.

Electrical Characteristics – continued

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Middle Level Output Voltage	V_{MID1}	COM1 to COM4	1/2 bias IO = ±100µA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	V
	V_{MID2}	S1 to S37	1/3 bias IO = ±20µA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID3}	S1 to S37	1/3 bias IO = ±20µA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
	V_{MID4}	COM1 to COM4	1/3 bias IO = ±100µA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	V_{MID5}	COM1 to COM4	1/3 bias IO = ±100µA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
Current Consumption	I_{DD1}	VDD	Power-saving mode	-	-	15	µA
	I_{DD2}	VDD	VDD = 5.0V Output open, 1/2 bias Frame frequency=80Hz VLCD=1.00*VDD	-	100	210	µA
	I_{DD3}	VDD	VDD = 5.0V Output open, 1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	120	250	µA

Oscillation Characteristics (Ta = -40°C to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency 1	f_{OSC1}	-	VDD = 2.7V to 6.0V	360	-	720	kHz
Oscillator Frequency 2	f_{OSC2}	-	VDD = 5V	540	600	660	kHz
External Clock Frequency *(Note 1)*	f_{OSC3}	OSCIN	External clock mode (OC=1)	30	-	1000	kHz
External Clock Rise Time	tr			-	160	-	ns
External Clock Fall Time	tf			-	160	-	ns
External Clock Duty	tdty			30	50	70	%

(Note 1) Frame frequency is decided external frequency and dividing ratio of FC0, FC1, FC2, FC3, FC4, FC5, FC6 setting.

[Reference Data]

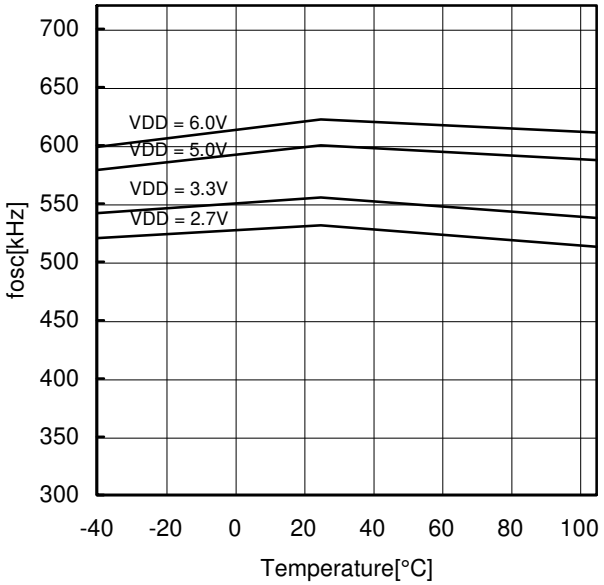


Figure 6. Frame Frequency Typical Temperature Characteristics

External PWM Clock Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

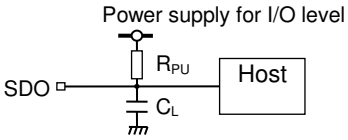
Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
External PWM Frequency	f_{PWM}	PWMIN	External PWM mode *(Note 2)*	30	-	5000	Hz
External PWM Input Rise Time	tr_{PWM}			-	160	-	ns
External PWM Input Fall Time	tf_{PWM}			-	160	-	ns
External PWM Pulse Width	pw_{PWM}			780	-	-	ns

(Note 2) About External PWM mode setting, please refer to "Control Data Functions".

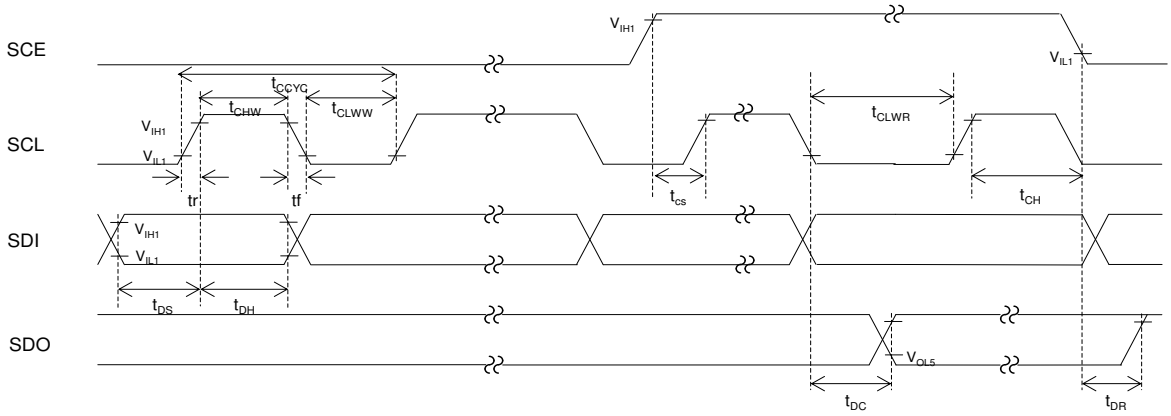
MPU Interface Characteristics (Ta = -40 to +105°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	t_{DS}	SCL, SDI		120	-	-	ns
Data Hold Time	t_{DH}	SCL, SDI		120	-	-	ns
SCE Wait Time	t_{CP}	SCE, SCL		120	-	-	ns
SCE Setup Time	t_{CS}	SCE, SCL		120	-	-	ns
SCE Hold Time	t_{CH}	SCE, SCL		120	-	-	ns
Clock Cycle Time	t_{CCYC}	SCL		320	-	-	ns
High-level Clock Pulse Width	t_{CHW}	SCL		120	-	-	ns
Low-level Clock Pulse Width (Write)	t_{CLWW}	SCL		120	-	-	ns
Low-level Clock Pulse Width (Read)	t_{CLWR}	SCL	R_{PU} =4.7kΩ C_L =10pF*(Note)*	1.6	-	-	µs
Rise Time	tr	SCE, SCL, SDI,		-	160	-	ns
Fall Time	tf	SCE, SCL, SDI,		-	160	-	ns
INH Switching Time	tc	INHb, SCE		10	-	-	µs
SDO Output Delay Time	t_{DC}	SDO	R_{PU} =4.7kΩ C_L =10pF*(Note)*	-	-	1.5	µs
SDO Rise Time	t_{DR}	SDO	R_{PU} =4.7kΩ C_L =10pF*(Note)*	-	-	1.5	µs

(Note) Since SDO is an open-drain output, "t_{DC}" and "t_{DR}" depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.
R_{PU}: 1kΩ≤ R_{PU} ≤10kΩ is recommended.
C_L: A parasitic capacitance to VSS in an application circuit. Any component is not necessary to be attached.



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

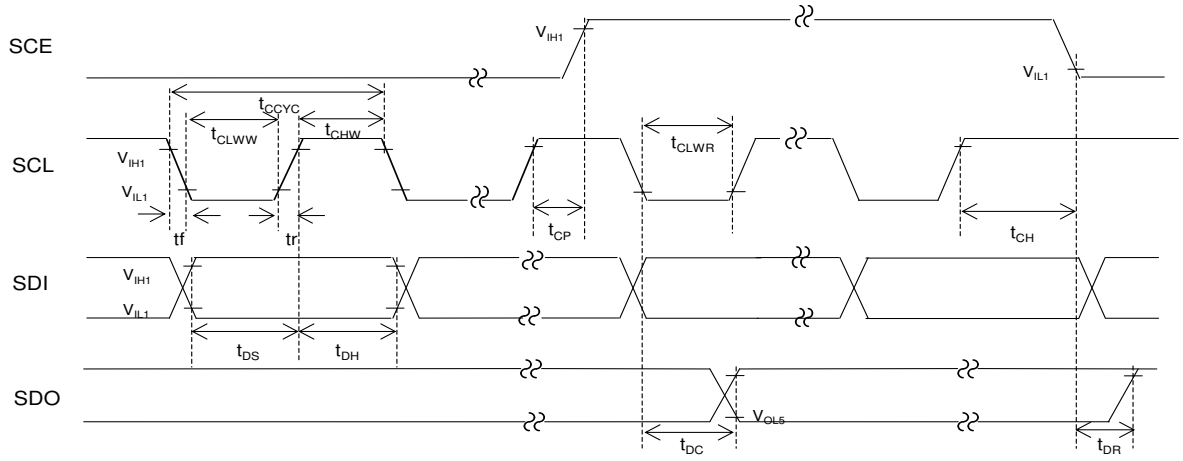


Figure 7. Serial Interface Timing

Pin Description

BU91600FV-M

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S5/P1/G1 to S10/P6/G6	1 to 2 37 to 40	Segment output for displaying the display data transferred by serial data input. The S5/P1/G1 to S10/P6/G6 pins can also be used as General –purpose / PWM outputs when set by the control data.	-	O	OPEN
S11/P7/G7 to S20/P16/G16	3 to 12	Segment output for displaying the display data transferred by serial data input. The S11/P7/G7 to S20/P16/G16 pins can also be used as General –purpose outputs / PWM outputs (by External PWM only) when set by the control data.	-	O	OPEN
S21 to S22	13 to14	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S23 to KS5/S27	15 to 19	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S23 to KS5/S27 pins can be used as segment outputs when specified by the control data.	-	O	OPEN
KI1/S32 to KI4/S35	20 to 23	Key scan inputs. These pins have built-in pull-down resistors. The KI1/S32 to KI4/S35 pins can be used as segment outputs when specified by the control data.	-	I O	VSS OPEN
COM1 to COM4	24 to 27	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
PWMIN/S36	30	Segment output for displaying the display data transferred by serial data input. The pin PWMIN/S36 can be used external PWM input pin or segment output when set by the control data.	-	I O	VSS OPEN
OSCIN/S37	31	Segment output for displaying the display data transferred by serial data input. The pin OSCIN/S37 can be used as external frequency input pin or segment output when set by the control data.	-	I O	VSS OPEN
SCE SCL SDI	32 33 34	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Synchronization clock SDI: Transfer data	 H ↑ -	 I I I	VSS
SDO	35	Output data	-	O	OPEN
INHb	36	Display off control input. When INHb = low (VSS), Display forced off S5/P1/G1 to S10/P6/G6 = low (VSS) S11/P7/G7 to S20/P16/G16 = low (VSS) S21 to S22 = low (VSS) KS1/S23 to KS5/S27 = low (VSS) KI1/S32 to KI4/S35 = low (VSS) PWMIN/S36 = low (VSS) OSCIN/S37 = low (VSS) COM1 to COM4 = low (VSS) Stop the LCD drive bias voltage generation divider resistors. Stop the internal oscillation circuit. When INHb = high (VDD), Display on However, serial data transfer is possible when the display is forced off.	L	I	VDD
VDD	28	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	29	Power supply pin. Must be connected to ground.	-	-	-

Pin Description – continued

BU91600FUV-M

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S5/P1/G1 to S10/P6/G6	1 to 2 45 to 48	Segment output for displaying the display data transferred by serial data input. The S5/P1/G1 to S10/P6/G6 pins can also be used as General –purpose / PWM outputs when set by the control data.	-	O	OPEN
S11/P7/G7 to S20/P16/G16	3 to 12	Segment output for displaying the display data transferred by serial data input. The S11/P7/G7 to S20/P16/G16 pins can also be used as General –purpose outputs / PWM outputs (by External PWM only) when set by the control data.	-	O	OPEN
S1 to S4 S21 to S22 S28 to S31	41 to 44 13 to 14 20 to 23	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S23 to KS5/S27	15 to 19	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S23 to KS5/S27 pins can be used as segment outputs when specified by the control data.	-	O	OPEN
KI1/S32 to KI4/S35	24 to 27	Key scan inputs. These pins have built-in pull-down resistors. The KI1/S32 to KI4/S35 pins can be used as segment outputs when specified by the control data.	-	I O	VSS OPEN
COM1 to COM4	28 to 31	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
PWMIN/S36	34	Segment output for displaying the display data transferred by serial data input. The pin PWMIN/S36 can be used external PWM input pin or segment output when set by the control data.	-	I O	VSS OPEN
OSCIN/S37	35	Segment output for displaying the display data transferred by serial data input. The pin OSCIN/S37 can be used as external frequency input pin or segment output when set by the control data.	-	I O	VSS OPEN
SCE SCL SDI	36 37 38	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Synchronization clock SDI: Transfer data	 H ↑ -	 I I I	VSS
SDO	39	Output data	-	O	OPEN
INHb	40	Display off control input. When INHb = low (VSS), Display forced off S5/P1/G1 to S10/P6/G6 = low (VSS) S11/P7/G7 to S20/P16/G16 = low (VSS) S1 to S4, S21 to S22, S28 to S31 = low (VSS) KS1/S23 to KS5/S27 = low (VSS) KI1/S32 to KI4/S35 = low (VSS) PWMIN/S36 = low (VSS) OSCIN/S37 = low (VSS) COM1 to COM4 = low (VSS) Stop the LCD drive bias voltage generation divider resistors. Stop the internal oscillation circuit. When INHb = high (VDD), Display on However, serial data transfer is possible when the display is forced off.	L	I	VDD
VDD	32	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	33	Power supply pin. Must be connected to ground.	-	-	-

IO Equivalence Circuit

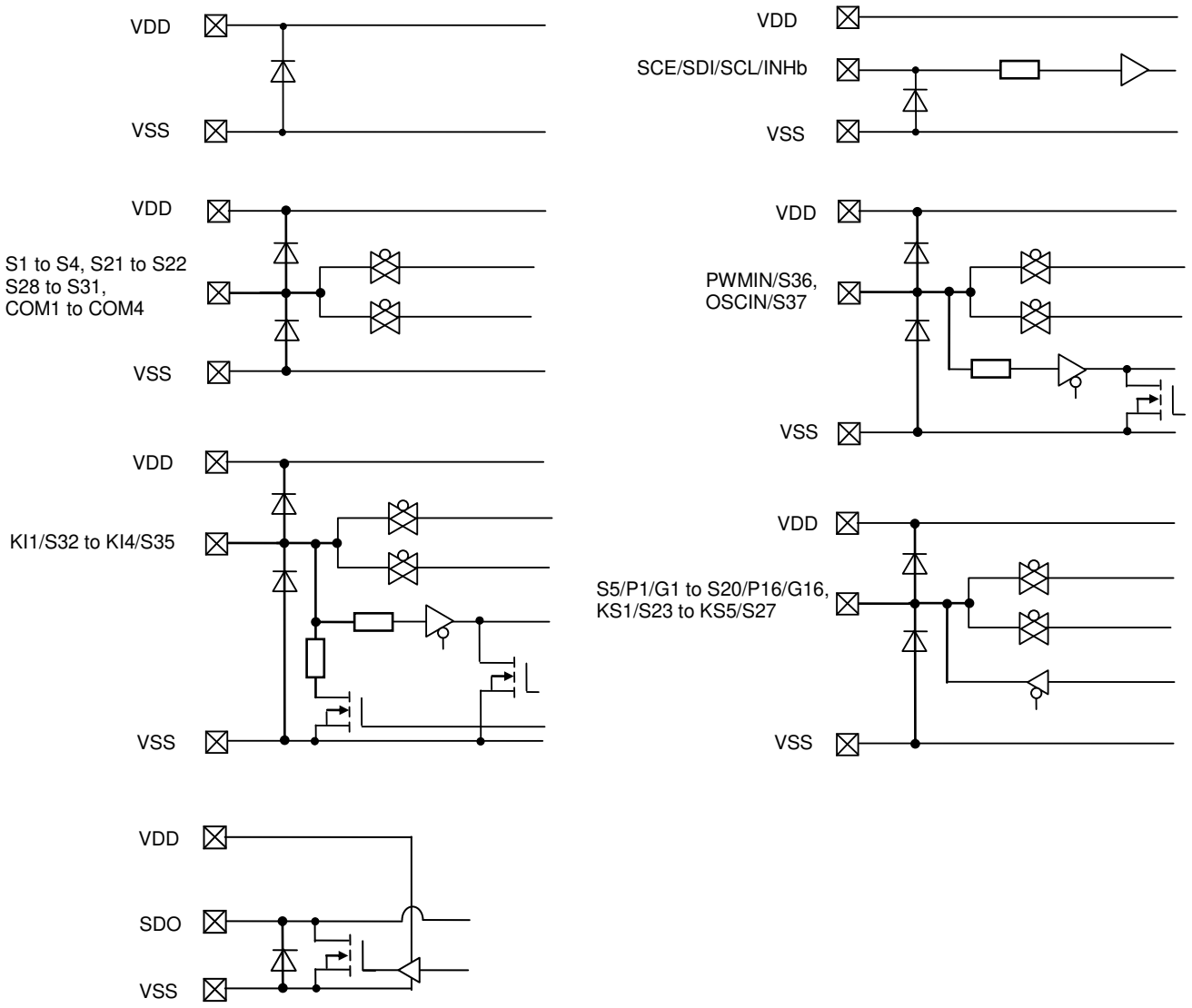


Figure 8. I/O Equivalent Circuit

Serial Data Transfer Formats

1. 1/4-Duty

(1)When SCL is stopped at the low level

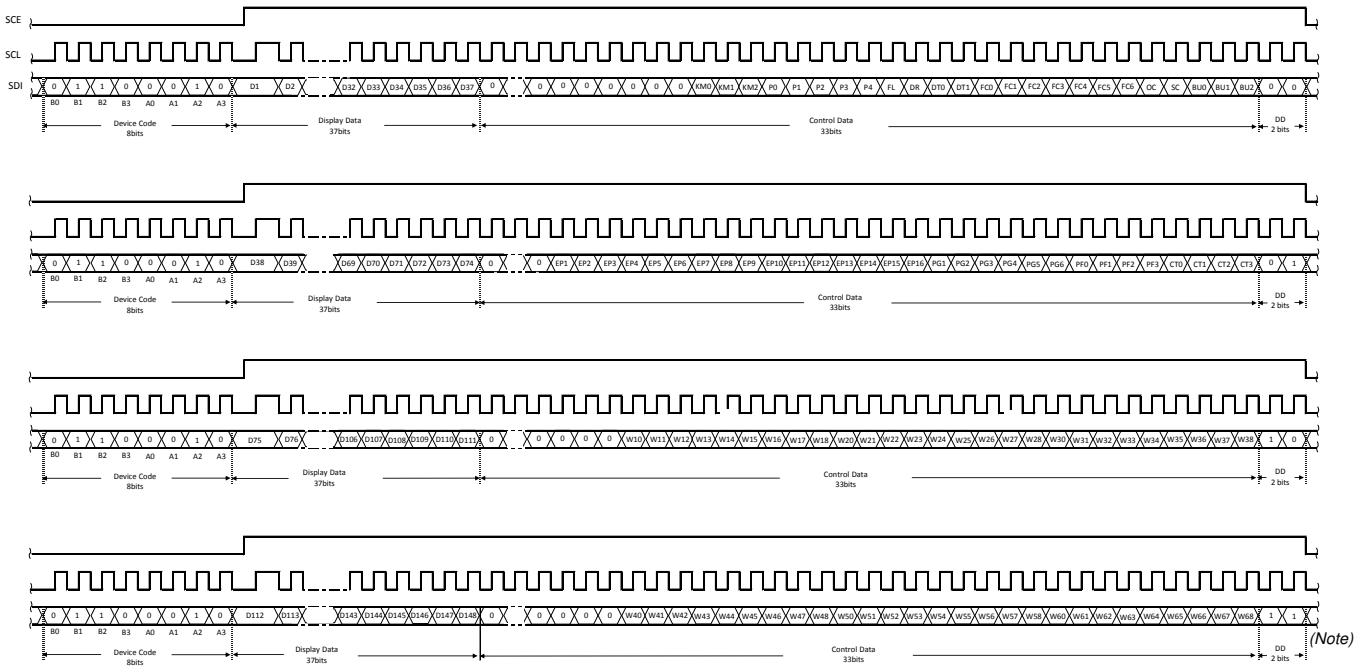


Figure 9. 3-SPI Data Transfer Format

(Note) DD is direction data.

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

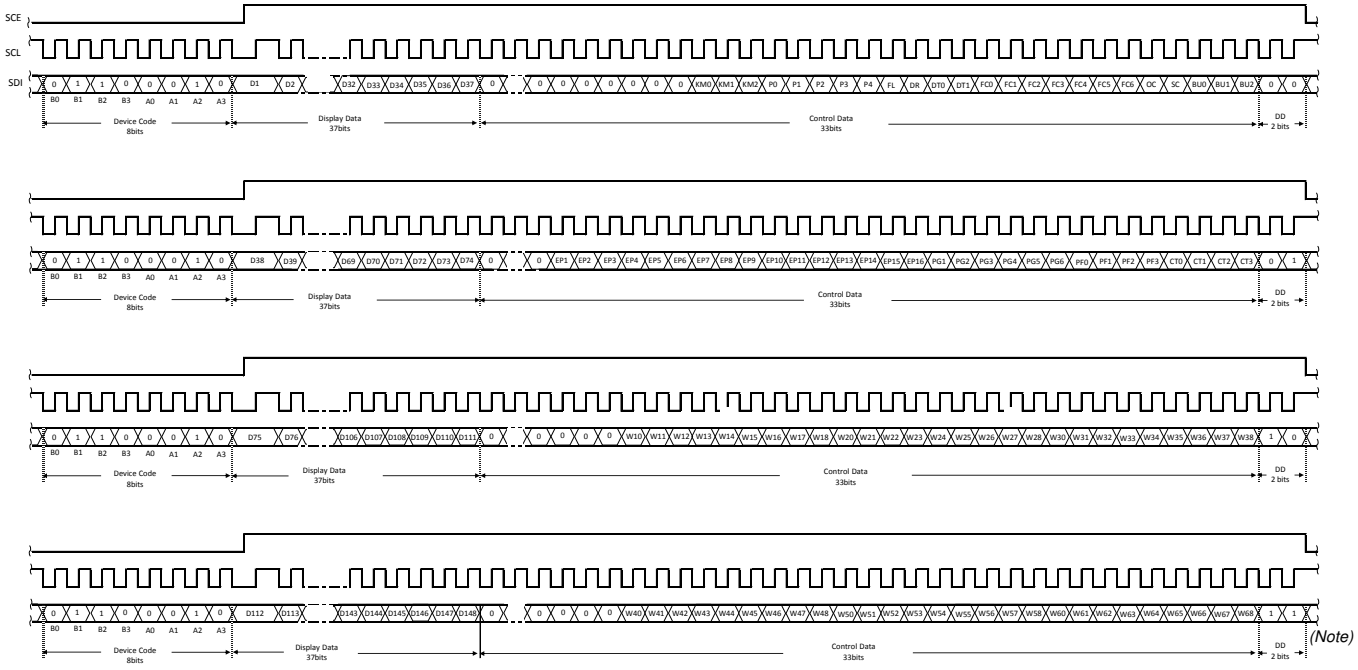


Figure 10. 3-SPI Data Transfer Format

(Note) DD is direction data.

Device code·····”46H”
KM0 to KM2·····Key Scan output port/Segment output port switching control data
D1 to D148·····Display data
P0 to P4·····Segment / PWM / General Purpose output port switching control data
FL·····Line Inversion or Frame Inversion switching control data
DR·····1/3 bias drive or 1/2 bias drive switching control data
DT0 to DT1·····1/4 duty drive, 1/3 duty drive, 1/2 duty drive or Static drive switching control data
FC0 to FC6·····Common/Segment output waveform frame frequency switching control data
OC····· Internal oscillator operating mode/External clock operating mode switching control data
SC·····Segment on/off switching control data
BU0 to BU2·····Normal mode/power-saving mode switching control data
PG1 to PG6·····PWM/General Purpose Output(GPO) switching control data
EP1 to EP16·····Internal PWM/External PWM switching control data (EP1-EP6),
GPO/External PWM switching control data (EP7-EP16)
PF0 to PF3·····PWM output waveform frame frequency switching control data.
CT0 to CT3·····LCD display contrast switching control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68
·····PWM output duty switching control data

Serial Data Transfer Formats – continued

2. 1/3-Duty

(1) When SCL is stopped at the low level

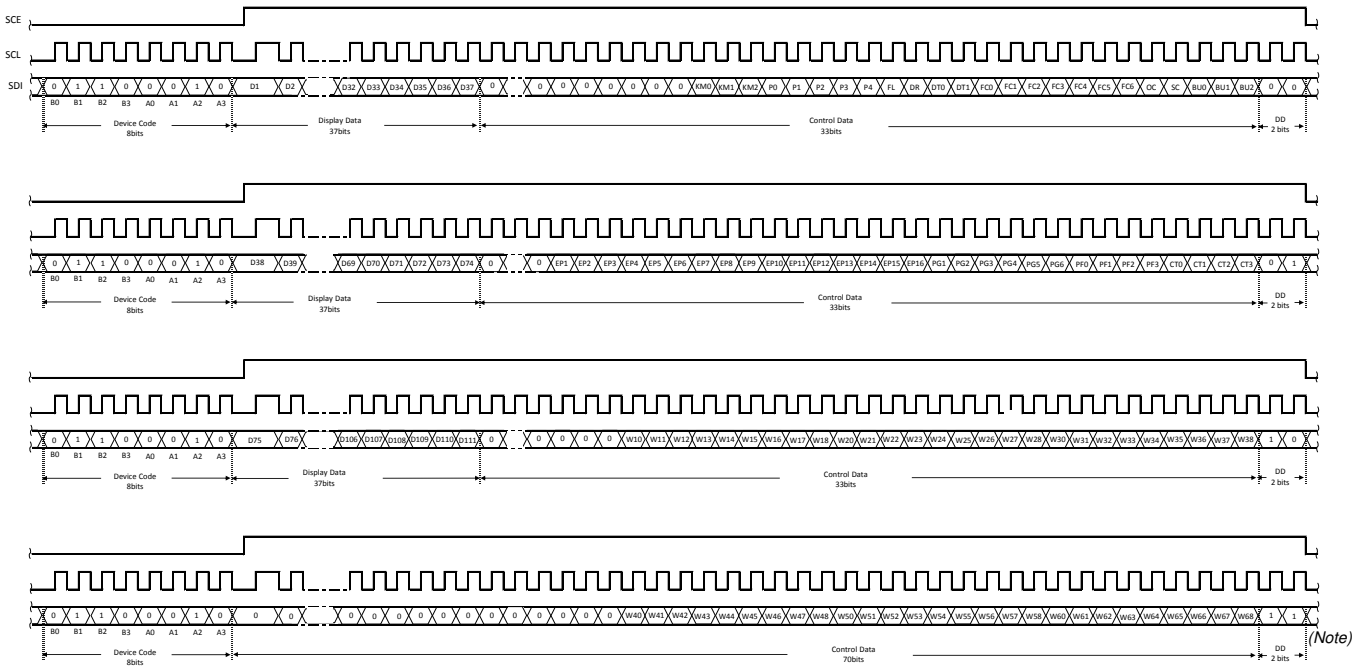


Figure 11. 3-SPI Data Transfer Format

(Note) DD is direction data.

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

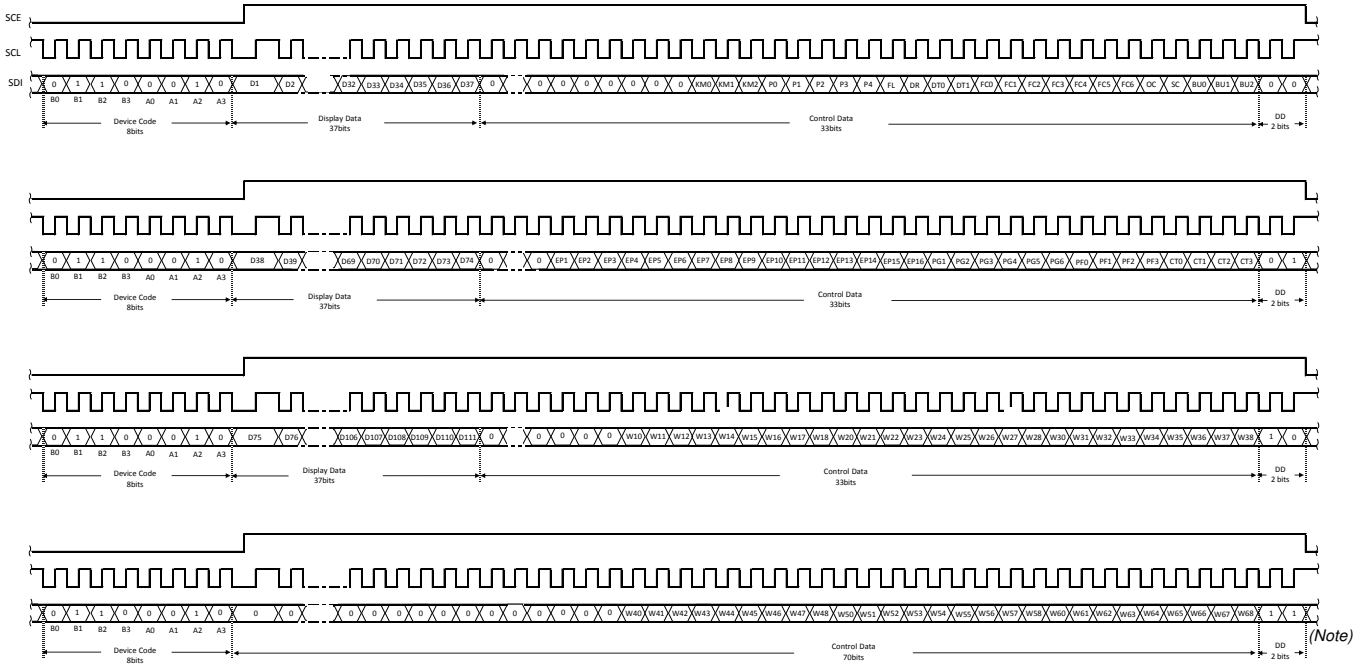


Figure 12. 3-SPI Data Transfer Format

(Note) DD is direction data.

Device code·····”46H”
KM0 to KM2·····Key Scan output port/Segment output port switching control data
D1 to D111·····Display data
P0 to P4·····Segment / PWM / General Purpose output port switching control data
FL·····Line Inversion or Frame Inversion switching control data
DR·····1/3 bias drive or 1/2 bias drive switching control data
DT0 to DT1·····1/4 duty drive, 1/3 duty drive, 1/2 duty drive or Static drive switching control data
FC0 to FC6·····Common/Segment output waveform frame frequency switching control data
OC····· Internal oscillator operating mode/External clock operating mode switching control data
SC·····Segment on/off switching control data
BU0 to BU2·····Normal mode/power-saving mode switching control data
PG1 to PG6·····PWM/General Purpose Output(GPO) switching control data
EP1 to EP16·····Internal PWM/External PWM switching control data (EP1-EP6),
GPO/External PWM switching control data (EP7-EP16)
PF0 to PF3·····PWM output waveform frame frequency switching control data.
CT0 to CT3·····LCD display contrast switching control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68
·····PWM output duty switching control data

Serial Data Transfer Formats – continued

3. 1/2-Duty

(1) When SCL is stopped at the low level

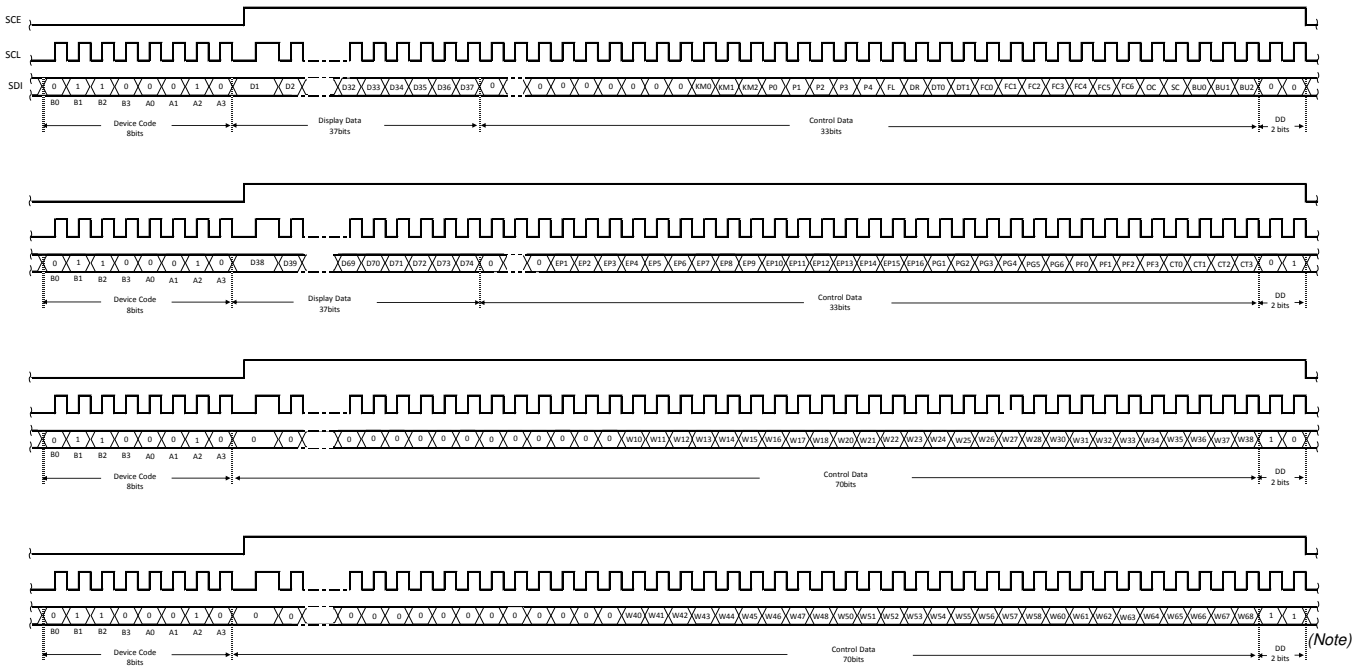


Figure 13. 3-SPI Data Transfer Format

(Note) DD is direction data.

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

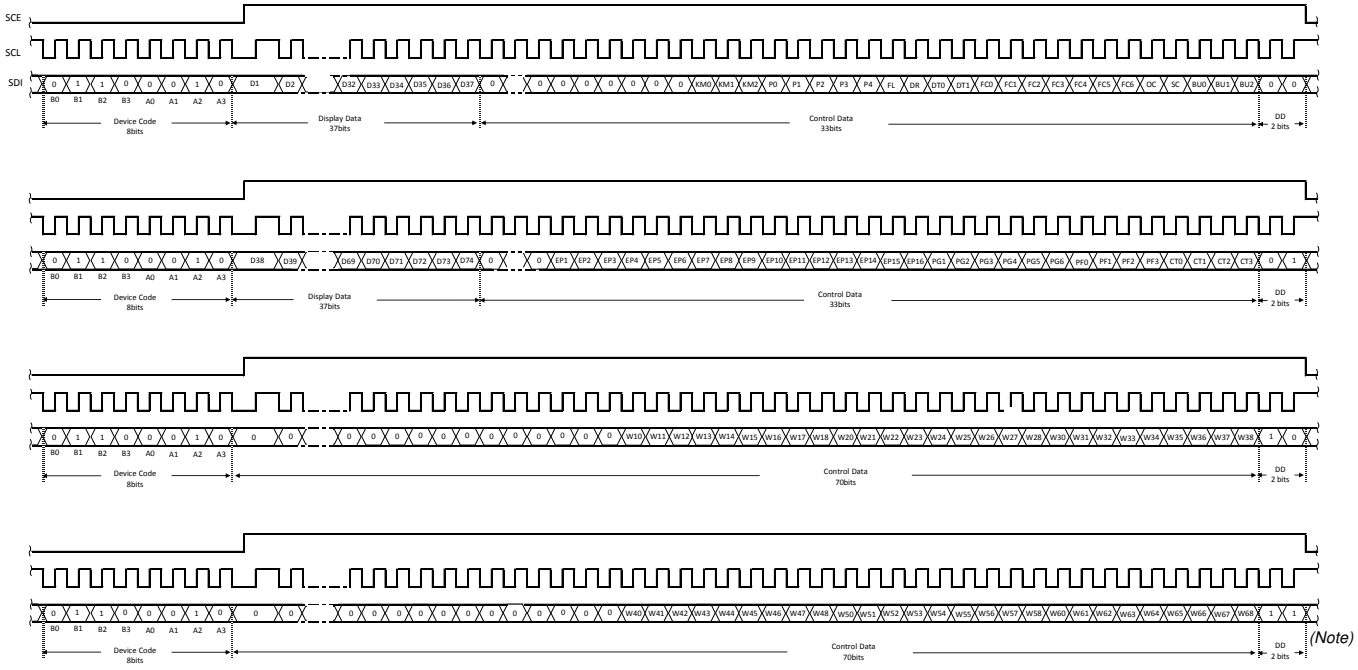


Figure 14. 3-SPI Data Transfer Format

(Note) DD is direction data.

Device code·····”46H”
KM0 to KM2·····Key Scan output port/Segment output port switching control data
D1 to D74·····Display data
P0 to P4·····Segment / PWM / General Purpose output port switching control data
FL·····Line Inversion or Frame Inversion switching control data
DR·····1/3 bias drive or 1/2 bias drive switching control data
DT0 to DT1·····1/4 duty drive, 1/3 duty drive, 1/2 duty drive or Static drive switching control data
FC0 to FC6·····Common/Segment output waveform frame frequency switching control data
OC····· Internal oscillator operating mode/External clock operating mode switching control data
SC·····Segment on/off switching control data
BU0 to BU2·····Normal mode/power-saving mode switching control data
PG1 to PG6·····PWM/General Purpose Output(GPO) switching control data
EP1 to EP16·····Internal PWM/External PWM switching control data (EP1-EP6),
GPO/External PWM switching control data (EP7-EP16)
PF0 to PF3·····PWM output waveform frame frequency switching control data.
CT0 to CT3·····LCD display contrast switching control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68
·····PWM output duty switching control data

Serial Data Transfer Formats – continued

4. Static

(1)When SCL is stopped at the low level

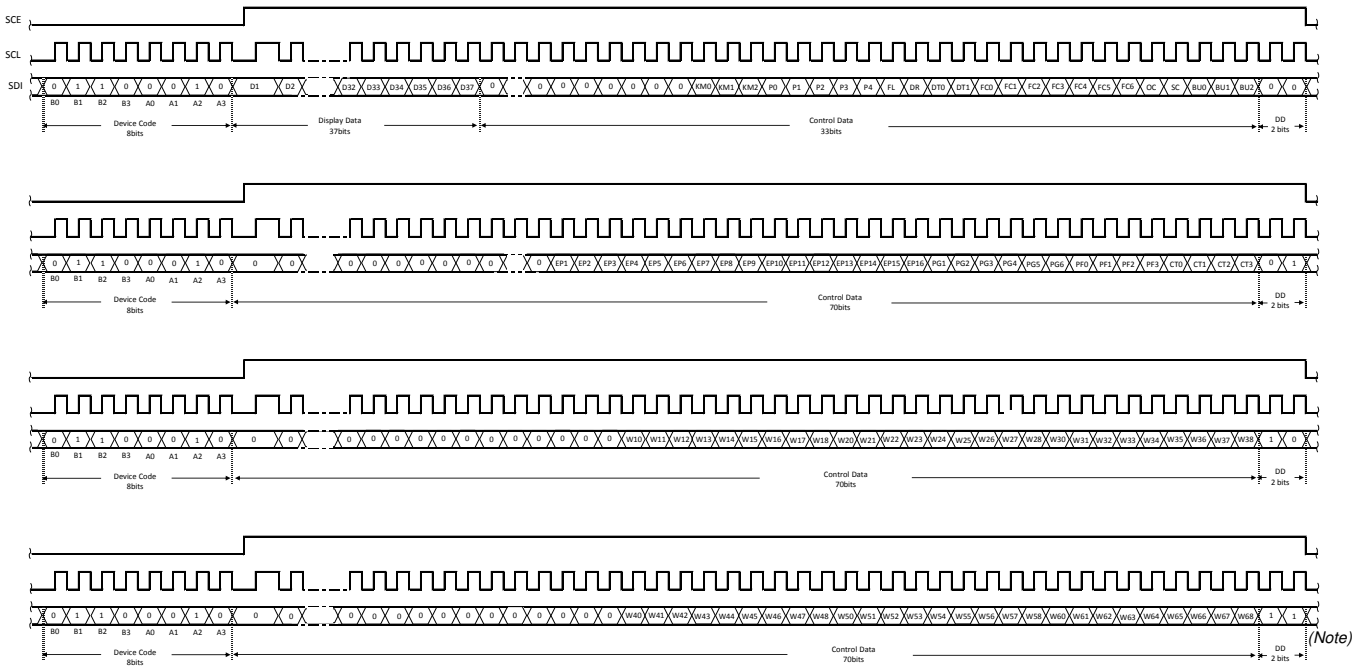


Figure 15. 3-SPI Data Transfer Format

(Note) DD is direction data.

Serial Data Transfer Formats – continued

(2)When SCL is stopped at the high level

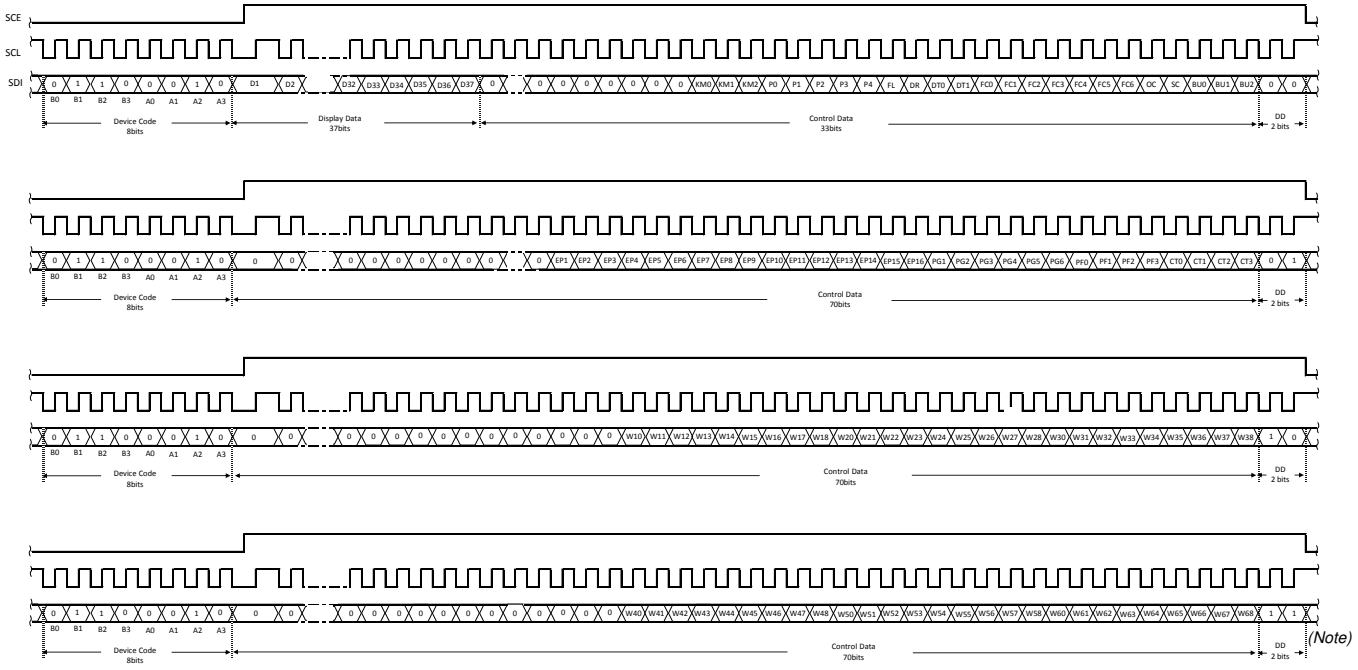


Figure 16. 3-SPI Data Transfer Format

(Note) DD is direction data.

Device code·····”46H”
KM0 to KM2·····Key Scan output port/Segment output port switching control data
D1 to D37·····Display data
P0 to P4·····Segment / PWM / General Purpose output port switching control data
FL·····Line Inversion or Frame Inversion switching control data
DR·····1/3 bias drive or 1/2 bias drive switching control data
DT0 to DT1·····1/4 duty drive, 1/3 duty drive, 1/2 duty drive or Static drive switching control data
FC0 to FC6·····Common/Segment output waveform frame frequency switching control data
OC····· Internal oscillator operating mode/External clock operating mode switching control data
SC·····Segment on/off switching control data
BU0 to BU2·····Normal mode/power-saving mode switching control data
PG1 to PG6·····PWM/General Purpose Output(GPO) switching control data
EP1 to EP16·····Internal PWM/External PWM switching control data (EP1-EP6),
GPO/External PWM switching control data (EP7-EP16)
PF0 to PF3·····PWM output waveform frame frequency switching control data.
CT0 to CT3·····LCD display contrast switching control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68
·····PWM output duty switching control data

Control Data Functions

1. KM0,KM1 and KM2: Key Scan output port/Segment output port switching control data

These control data bits switch the functions of the KS1/S23 to KS5/S27 output pins between key scan output and segment output.

KM0	KM1	KM2	Output Pin State					Maximum Number of Input keys	Reset condition
			KS1/S23	KS2/S24	KS3/S25	KS4/S26	KS5/S27		
0	0	0	KS1 *(Note 1)*	KS2	KS3	KS4	KS5	20	-
0	0	1	S23 *(Note 2)*	KS2	KS3	KS4	KS5	16	-
0	1	0	S23	S24	KS3	KS4	KS5	12	-
0	1	1	S23	S24	S25	KS4	KS5	8	-
1	0	0	S23	S24	S25	S26	KS5	4	-
1	0	1	S23	S24	S25	S26	S27	0	-
1	1	0	S23	S24	S25	S26	S27	0	-
1	1	1	S23	S24	S25	S26	S27	0	○

(Note 1) KSx :Key scan Output(x=1 to 5)
(Note 2) Sx :Segment Output(x=23 to 27)

2. P0,P1,P2,P3 and P4: Segment / PWM / General Purpose output port switching control data

These control bits are used to select the function of the S5/P1/G1 to S20/P16/G16 output pins (Segment Output Pins or PWM Output Pins or General Purpose Output Pins).

P0	P1	P2	P3	P4	S5/ P1/ G1	S6/ P2/ G2	S7/ P3/ G3	S8/ P4/ G4	S9/ P5/ G5	S10/ P6/ G6	S11/ P7/ G7	S12/ P8/ G8	Reset condition
0	0	0	0	0	S5	S6	S7	S8	S9	S10	S11	S12	○
0	0	0	0	1	P1/G1 *(Note 3)*	S6	S7	S8	S9	S10	S11	S12	-
0	0	0	1	0	P1/G1	P2/G2	S7	S8	S9	S10	S11	S12	-
0	0	0	1	1	P1/G1	P2/G2	P3/G3	S8	S9	S10	S11	S12	-
0	0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S9	S10	S11	S12	-
0	0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S10	S11	S12	-
0	0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S11	S12	-
0	0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S12	-
0	1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
0	1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
0	1	0	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
0	1	0	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
0	1	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
0	1	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
0	1	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
0	1	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	0	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	0	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	0	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	0	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-
1	1	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	-

(Note 3) Px/Gx : PWM output or General Purpose output (x=1 to 16)

Control Data Functions – continued

P0	P1	P2	P3	P4	S13/ P9/ G9	S14/ P10/ G10	S15/ P11/ G11	S16/ P12/ G12	S17/ P13/ G13	S18/ P14/ G14	S19/ P15/ G15	S20/ P16 G16	Reset condition
0	0	0	0	0	S13	S14	S15	S16	S17	S18	S19	S20	○
0	0	0	0	1	S13	S14	S15	S16	S17	S18	S19	S20	-
0	0	0	1	0	S13	S14	S15	S16	S17	S18	S19	S20	-
0	0	0	1	1	S13	S14	S15	S16	S17	S18	S19	S20	-
0	0	1	0	0	S13	S14	S15	S16	S17	S18	S19	S20	-
0	0	1	0	1	S13	S14	S15	S16	S17	S18	S19	S20	-
0	0	1	1	0	S13	S14	S15	S16	S17	S18	S19	S20	-
0	0	1	1	1	S13	S14	S15	S16	S17	S18	S19	S20	-
0	1	0	0	0	S13	S14	S15	S16	S17	S18	S19	S20	-
0	1	0	0	1	P9/G9	S14	S15	S16	S17	S18	S19	S20	-
0	1	0	1	0	P9/G9	P10/G10	S15	S16	S17	S18	S19	S20	-
0	1	0	1	1	P9/G9	P10/G10	P11/G11	S16	S17	S18	S19	S20	-
0	1	1	0	0	P9/G9	P10/G10	P11/G11	P12/G12	S17	S18	S19	S20	-
0	1	1	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	S18	S19	S20	-
0	1	1	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	S19	S20	-
0	1	1	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	S20	-
1	0	0	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	0	0	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	0	0	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	0	0	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	0	1	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	0	1	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	0	1	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	0	1	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	0	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	0	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	0	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	0	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	1	0	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	1	0	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	1	1	0	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-
1	1	1	1	1	P9/G9	P10/G10	P11/G11	P12/G12	P13/G13	P14/G14	P15/G15	P16/G16	-

PWM or General Purpose output is selected by PGx(x=1 to 6) control data bit
Internal PWM, External PWM output or General Purpose output is selected by EPx(x=1 to 6).
External PWM or General Purpose output is selected by EPx(x=7 to 16).

When the General Purpose Output Port Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data			
	1/4 Duty mode	1/3 Duty mode	1/2 Duty mode	Static mode
S5/P1/G1	D17	D13	D9	D5
S6/P2/G2	D21	D16	D11	D6
S7/P3/G3	D25	D19	D13	D7
S8/P4/G4	D29	D22	D15	D8
S9/P5/G5	D33	D25	D17	D9
S10/P6/G6	D37	D28	D19	D10
S11/P7/G7	D41	D31	D21	D11
S12/P8/G8	D45	D34	D23	D12
S13/P9/G9	D49	D37	D25	D13
S14/P10/G10	D53	D40	D27	D14
S15/P11/G11	D57	D43	D29	D15
S16/P12/G12	D61	D46	D31	D16
S17/P13/G13	D65	D49	D33	D17
S18/P14/G14	D69	D52	D35	D18
S19/P15/G15	D73	D55	D37	D19
S20/P16/G16	D77	D58	D39	D20

When the General Purpose Output Port Function is selected, the respective output pin outputs a “HIGH” level when its corresponding display data is set to “1”. Likewise, it will output a “LOW” level, if its corresponding display data is set to “0”. For example, at 1/4 Duty mode, S8/P4/G4 is used as a General Purpose Output Port, if its corresponding display data D29 is set to “1”, then S8/P4/G4 will output “HIGH” level. Likewise, if D29 is set to “0”, then S8/P4/G4 will output “LOW” level.

Control Data Functions – continued

3. FL: Line Inversion or Frame Inversion switching control data

This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion mode	Reset condition
0	Line Inversion	○
1	Frame Inversion	-

Typically, when driving large capacitance LCD, Line inversion will increase the influence of crosstalk.
Regarding driving waveform, refer to LCD driving waveforms.

4. DR: 1/3 bias drive or 1/2 bias drive switching control data

This control data bit selects either 1/3 bias drive or 1/2 bias drive.

DR	Bias drive scheme	Reset condition
0	1/3 bias drive	○
1	1/2 bias drive	-

The settings take effect if except Static are already set by DT0 and DT1 control bits.

5. DT: 1/4 duty drive, 1/3 duty drive, 1/2 duty drive or Static drive switching control data

These control data bits select either 1/4 duty drive, 1/3 duty drive, 1/2 duty drive or Static drive

DT0	DT1	Duty drive scheme	Reset condition
0	0	Static drive	-
0	1	1/2 duty drive	-
1	0	1/3 duty drive	-
1	1	1/4 duty drive	○

6. FC0, FC1, FC2, FC3, FC4, FC5, and FC6: Common/Segment output waveform frame frequency switching control data

These control data bits set the frame frequency for common and segment output waveforms.

FC0	FC1	FC2	FC3	FC4	FC5	FC6	Frame Frequency fo(Hz)	Reset condition
0	0	0	0	0	0	0	fosc*(Note)* /12000	○
0	0	0	0	0	0	1	fosc /10908	-
0	0	0	0	0	1	0	fosc /10000	-
0	0	0	0	0	1	1	fosc /9230	-
0	0	0	0	1	0	0	fosc /8572	-
0	0	0	0	1	0	1	fosc /8000	-
0	0	0	0	1	1	0	fosc /7500	-
0	0	0	0	1	1	1	fosc /7058	-
0	0	0	1	0	0	0	fosc /6666	-
0	0	0	1	0	0	1	fosc /6316	-
0	0	0	1	0	1	0	fosc /6000	-
0	0	0	1	0	1	1	fosc /5714	-
0	0	0	1	1	0	0	fosc /5454	-
0	0	0	1	1	0	1	fosc /5218	-
0	0	0	1	1	1	0	fosc /5000	-
0	0	0	1	1	1	1	fosc /4800	-
0	0	1	0	0	0	0	fosc /4616	-
0	0	1	0	0	0	1	fosc /4444	-
0	0	1	0	0	1	0	fosc /4286	-
0	0	1	0	0	1	1	fosc /4138	-
0	0	1	0	1	0	0	fosc /4000	-
0	0	1	0	1	0	1	fosc /3870	-
0	0	1	0	1	1	0	fosc /3750	-
0	0	1	0	1	1	1	fosc /3636	-
0	0	1	1	0	0	0	fosc /3530	-
0	0	1	1	0	0	1	fosc /3428	-
0	0	1	1	0	1	0	fosc /3334	-
0	0	1	1	0	1	1	fosc /3244	-
0	0	1	1	1	0	0	fosc /3158	-
0	0	1	1	1	0	1	fosc /3076	-

(Note) fosc: Internal oscillation frequency (600 kHz typ)

Control Data Functions – continued

FC0	FC1	FC2	FC3	FC4	FC5	FC6	Frame Frequency fo(Hz)	Reset condition
0	0	1	1	1	1	0	fosc*(Note)* /3000	-
0	0	1	1	1	1	1	fosc /2926	-
0	1	0	0	0	0	0	fosc /2858	-
0	1	0	0	0	0	1	fosc /2790	-
0	1	0	0	0	1	0	fosc /2728	-
0	1	0	0	0	1	1	fosc /2666	-
0	1	0	0	1	0	0	fosc /2608	-
0	1	0	0	1	0	1	fosc /2554	-
0	1	0	0	1	1	0	fosc /2500	-
0	1	0	0	1	1	1	fosc /2448	-
0	1	0	1	0	0	0	fosc /2400	-
0	1	0	1	0	0	1	fosc /2352	-
0	1	0	1	0	1	0	fosc /2308	-
0	1	0	1	0	1	1	fosc /2264	-
0	1	0	1	1	0	0	fosc /2222	-
0	1	0	1	1	0	1	fosc /2182	-
0	1	0	1	1	1	0	fosc /2142	-
0	1	0	1	1	1	1	fosc /2106	-
0	1	1	0	0	0	0	fosc /2068	-
0	1	1	0	0	0	1	fosc /2034	-
0	1	1	0	0	1	0	fosc /2000	-
0	1	1	0	0	1	1	fosc /1968	-
0	1	1	0	1	0	0	fosc /1936	-
0	1	1	0	1	0	1	fosc /1904	-
0	1	1	0	1	1	0	fosc /1874	-
0	1	1	0	1	1	1	fosc /1846	-
0	1	1	1	0	0	0	fosc /1818	-
0	1	1	1	0	0	1	fosc /1792	-
0	1	1	1	0	1	0	fosc /1764	-
0	1	1	1	0	1	1	fosc /1740	-
0	1	1	1	1	0	0	fosc /1714	-
0	1	1	1	1	0	1	fosc /1690	-
0	1	1	1	1	1	0	fosc /1666	-
0	1	1	1	1	1	1	fosc /1644	-
1	0	0	0	0	0	0	fosc /1622	-
1	0	0	0	0	0	1	fosc /1600	-
1	0	0	0	0	1	0	fosc /1578	-
1	0	0	0	0	1	1	fosc /1558	-
1	0	0	0	1	0	0	fosc /1538	-
1	0	0	0	1	0	1	fosc /1518	-
1	0	0	0	1	1	0	fosc /1500	-
1	0	0	0	1	1	1	fosc /1482	-
1	0	0	1	0	0	0	fosc /1464	-
1	0	0	1	0	0	1	fosc /1446	-
1	0	0	1	0	1	0	fosc /1428	-
1	0	0	1	0	1	1	fosc /1412	-
1	0	0	1	1	0	0	fosc /1396	-
1	0	0	1	1	0	1	fosc /1380	-
1	0	0	1	1	1	0	fosc /1364	-
1	0	0	1	1	1	1	fosc /1348	-

(Note) fosc: Internal oscillation frequency (600 kHz typ)

Control Data Functions – continued

FC0	FC1	FC2	FC3	FC4	FC5	FC6	Frame Frequency fo(Hz)	Reset condition
1	0	1	0	0	0	0	fosc(Note) /1334	-
1	0	1	0	0	0	1	fosc /1318	-
1	0	1	0	0	1	0	fosc /1304	-
1	0	1	0	0	1	1	fosc /1290	-
1	0	1	0	1	0	0	fosc /1276	-
1	0	1	0	1	0	1	fosc /1264	-
1	0	1	0	1	1	0	fosc /1250	-
1	0	1	0	1	1	1	fosc /1238	-
1	0	1	1	0	0	0	fosc /1224	-
1	0	1	1	0	0	1	fosc /1212	-
1	0	1	1	0	1	0	fosc /1200	-
1	0	1	1	0	1	1	fosc /1188	-
1	0	1	1	1	0	0	fosc /1176	-
1	0	1	1	1	0	1	fosc /1166	-
1	0	1	1	1	1	0	fosc /1154	-
1	0	1	1	1	1	1	fosc /1142	-
1	1	0	0	0	0	0	fosc /1132	-
1	1	0	0	0	0	1	fosc /1122	-
1	1	0	0	0	1	0	fosc /1112	-
1	1	0	0	0	1	1	fosc /1100	-
1	1	0	0	1	0	0	fosc /1090	-
1	1	0	0	1	0	1	fosc /1082	-
1	1	0	0	1	1	0	fosc /1072	-
1	1	0	0	1	1	1	fosc /1062	-
1	1	0	1	0	0	0	fosc /1052	-
1	1	0	1	0	0	1	fosc /1044	-
1	1	0	1	0	1	0	fosc /1034	-
1	1	0	1	0	1	1	fosc /1026	-
1	1	0	1	1	0	0	fosc /1016	-
1	1	0	1	1	0	1	fosc /1008	-
1	1	0	1	1	1	0	fosc /1000	-
1	1	0	1	1	1	1	fosc /992	-
1	1	1	0	0	0	0	fosc /984	-
1	1	1	0	0	0	1	fosc /976	-
1	1	1	0	0	1	0	fosc /968	-
1	1	1	0	0	1	1	fosc /960	-
1	1	1	0	1	0	0	fosc /952	-
1	1	1	0	1	0	1	fosc /944	-
1	1	1	0	1	1	0	fosc /938	-
1	1	1	0	1	1	1	fosc /930	-
1	1	1	1	0	0	0	fosc /924	-
1	1	1	1	0	0	1	fosc /916	-
1	1	1	1	0	1	0	fosc /910	-
1	1	1	1	0	1	1	fosc /902	-
1	1	1	1	1	0	0	fosc /896	-
1	1	1	1	1	0	1	fosc /888	-
1	1	1	1	1	1	0	fosc /882	-
1	1	1	1	1	1	1	fosc /876	-

(Note) fosc: Internal oscillation frequency (600 kHz typ)

Control Data Functions – continued

7. OC: Internal oscillator operating mode/External clock operating mode switching control data

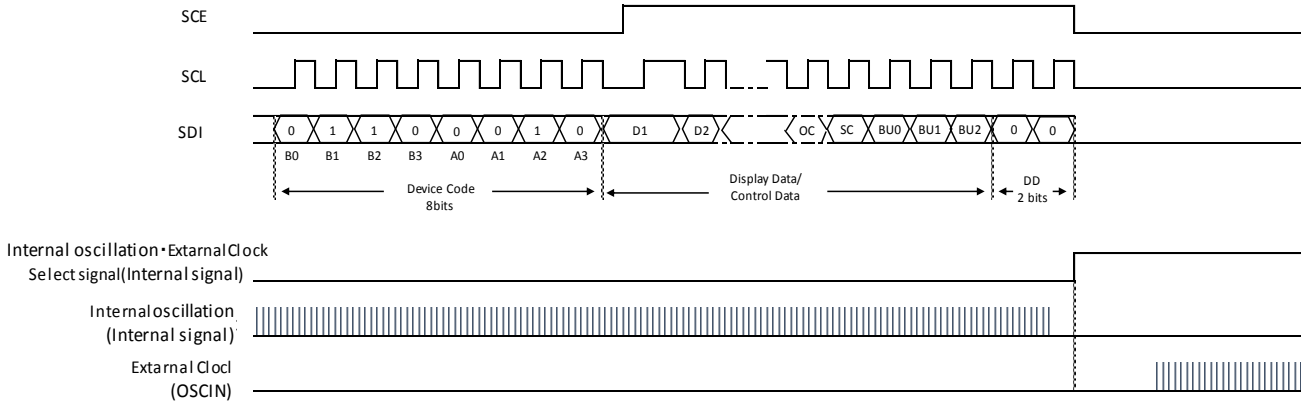
These control data bits select either Internal oscillator operating or External clock operating mode.

OC	Operating mode	In/Out pin(OSCIN/S37) status	Reset condition
0	Internal oscillator	S37 (segment output)	○
1	External Clock	OSCIN (clock input)	-

OC=1 : OSCIN/S37 pin can be used as input clock pin when External Clock is set by the control data.

<External Clock input timing function>

Internal oscillation / external clock select signal behavior is below.
Please input external clock after serial data sending.



8. SC: Segment on/off switching control data

This control data bit controls the on/off state of the segments.

SC	Display state	Reset condition
0	On	-
1	Off	○

Note that when the segments are turned off by setting SC to "1", the segments are turned off by outputting segment off waveforms from the segment output pins.

9. BU0,BU1 and BU2: Normal mode/power-saving mode switching control data

These control data bits select either normal mode or power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment outputs Common outputs	Output Pin States During Key Scan Standby KS1	KS2	KS3	KS4	KS5	Reset condition
0	0	0	Normal	Operating	Operating	H	H	H	H	H	-
0	0	1	Power -saving	Stopped	Low(VSS)	L	L	L	L	H	-
0	1	0				L	L	L	H	H	-
0	1	1				L	L	H	H	H	-
1	0	0				L	H	H	H	H	-
1	0	1				H	H	H	H	H	-
1	1	0				H	H	H	H	H	-
1	1	1				H	H	H	H	H	○

Power-saving mode status: S5/P1/G1 to S20/P16/G16 = active only General Purpose output
S1 to S4, S21 to S22, S28 to S31 = low (VSS)
KS1/S23 to KS5/S27 = low (VSS)
KI1/S32 to KI4/S35 = low (VSS)
PWMIN/S36 = low (VSS)
OSCIN/S37 = low (VSS)
COM1 to COM4 = low (VSS)
Stop the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible.