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Digital Sound Processors for FPD TVs

32bit Audio DSP with Built-in 4ch DAC and ASRC

BU9408KS2

No.12083EAT02

●General Description

This LSI is the digital sound processor which made
the use digital signal processing for FPD TVs.
DSP of ROHM original is used for the TV sound processor unit, and it excels in cost performance. A selection input of two lines is possible from four digital inputs. An asynchronous sampling rate converter(ASRC) is built in one line. Three digital outputs are built in.
Two audio DA converters are built in.

●Features

■Digital Signal Processor unit

Word length: 32bit (Data RAM)
The fastest machine cycle: 40.7ns (512fs, fs = 48kHz)
Multiplier: 32 x 24 → 56bit
Adder: 32 + 32 → 32bit
Data RAM: 256 x 32bit
Coefficient RAM: 128 x 24bit
Sampling frequency: fs = 48kHz
Master clock : 512fs（24.576MHz,fs=48kHz）

■Digital signal input (Stereo4lines):
16/20/24bit (I^2S, Left-Justified, Right-Justified)
Digital signal output (Stereo 3 lines):
16/20/24bit (I^2S, Left-Justified, Right-Justified, S/PDIF)

■.Asynchronous sampling rate converter
（one line at stereo）: 32kHz/44.1kHz/48kHz/88.2kHz/96kHz/176.4kHz/192kHz → 48kHz

■Audio DAC : One stereo output
24bit 8 x Over-sampling digital filter + 1 bit delta sigma DAC
S/N : 96dB
THD+N : 0.005%（Sine-wave 1kHz,0dB）

■Audio 16bit DAC : One stereo output
24bit 8 x Over-sampling digital filter + Audio 16bit DAC
S/N : 90dB
THD+N : 0.03%（Sine-wave 1kHz,0dB）

■The sound signal processing function for FPD TVs
Pre-Scaler, DC cut HPF, Channel Mixer, *P^2Volume*(Perfect Pure Volume), BASS, MIDDLE, TREBLE, Simulated-Stereo, Surround, *P^2Bass*, *P^2Treble*, 7Band Parametric EQ, Master Volume, L/R balance, Post-Scaler, Output signal clipper
(*P^2Volume*, *P^2Bass*, and *P^2Treble* are the sound effect functions of ROHM original.)

●Applications

Flat Panel TVs (LCD, Plasma)

●Absolute Maximum Ratings

Items	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	4.5	V
Power dissipation	P_d	850(*1)	mW
Operating temp. range	T_{opr}	-25～+85	°C
Storage temp. range	T_{stg}	-55～+125	°C

*1Use of this processor at Ta = 25°C and over is subject to reduction of 8.5mW per 1°C.
Operation is not guaranteed.

●Recommended Operating Rating(s)

Items	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	3.0～3.6	V

*1 This product is not designed for protection against radioactive rays.

●Electrical Characteristics(Digital system)

V_{DD}=3.3V (Unless otherwise specified Ta = 25°C)

Items		Symbol	Limit			Unit	Conditions	Adaptive terminal
			MIN	TYP	MAX			
Input voltage	H-level voltage	V_{IH}	2.3	-	-	V		*1
	L-level voltage	V_{IL}	-	-	1.0	V		*1
Hysteresis input voltage	H-level voltage	V_{IH}	2.5	-	-	V		*2,3,4
	L-level voltage	V_{IL}	-	-	0.8	V		*2,3,4
Input current		I_I	-1	-	+1	μA	V_{IN}=0~3.3V	*1,2
Input L current to Pull-up resistor		I_{IL}	-150	-100	-50	μA	V_{IN}=0V	*3
Input H current to Pull-down resistor		I_{IH}	35	70	105	μA	V_{IN}=3.3V	*4
Output voltage	H-level voltage	V_{OH}	2.75	-	-	V	I_O=-0.6mA	*5
	L-level voltage	V_{OL}	-	-	0.55	V	I_O=0.6mA	*5
SDA Output voltage	L-level voltage	V_{OL}	-	-	0.4	V	I_O=3mA	*6

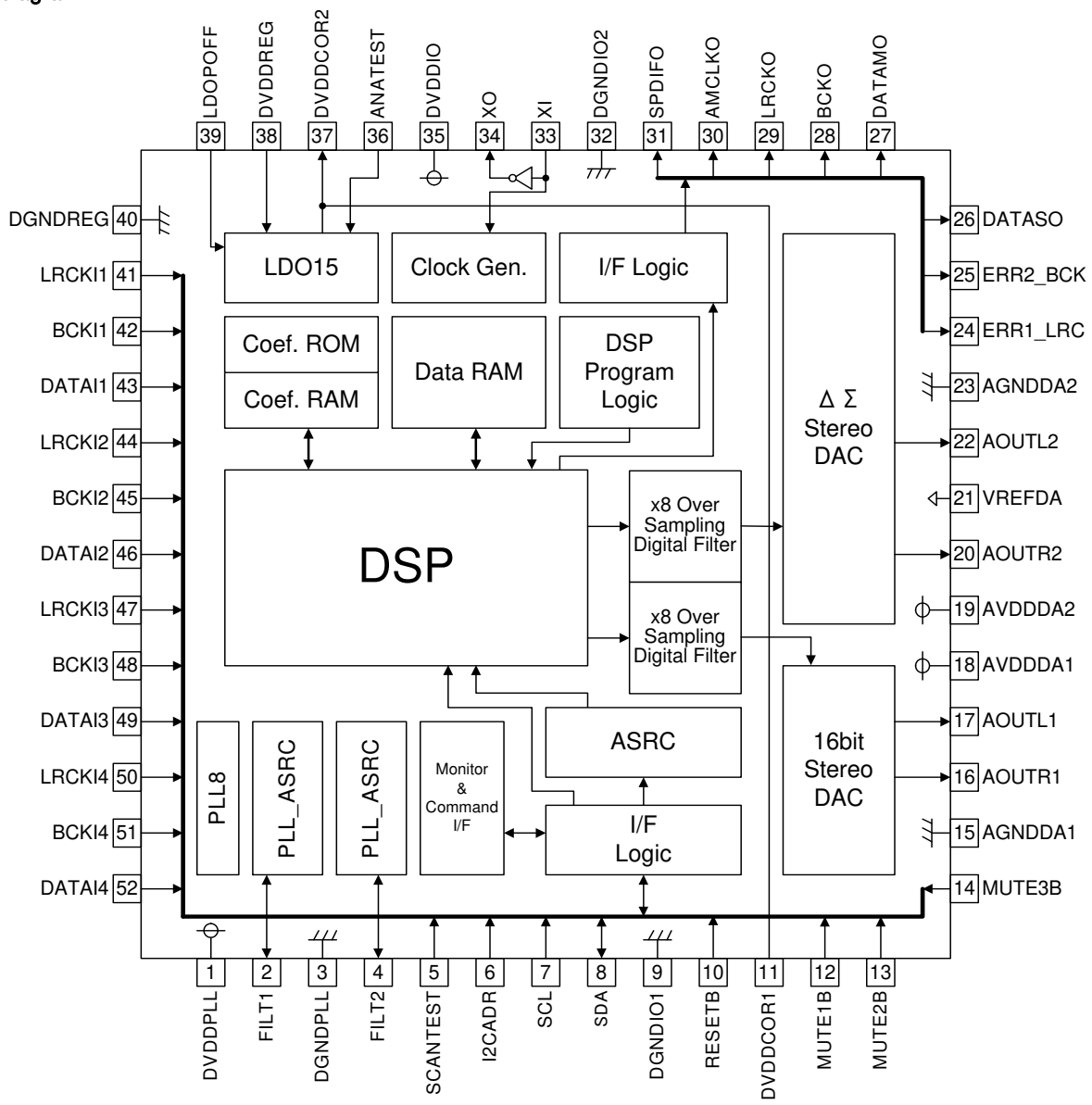
Adaptive terminal
*1 CMOS input terminal
XI(33pin)
*2 CMOS hysteresis input terminal
SCANTEST(5pin), SCL(7pin), SDA(8pin)
*3 CMOS hysteresis input terminal with a built-in pull-up resistor
LRCKI1(41pin), BCKI1(42pin), DATAI1(43pin), LRCKI2(44pin), BCKI2(45pin), DATAI2(46pin), LRCKI3(47pin), BCKI3(48pin), DATAI3(49pin), LRCKI4(50pin), BCKI4(51pin), DATAI4(52pin)
*4 CMOS input terminal with a built-in pull down resistor
I2CADR(6pin), RESETB(10pin), MUTE1B(12pin), MUTE2B(13pin), MUTE3B(14pin)
*5 CMOS output terminal
ERR1_LRC(24pin), ERR2_BCK(25pin), DATASO(26pin), DATAMO(27pin), BCKO(28pin), LRCKO(29pin), AMCLKO(30pin), SPDIFO(31pin), XO(34pin),
*6 Open drain output terminal
SDA(8pin)

●Electrical Characteristics (Analog system)

V_{DD}=3.3V (Unless otherwise specified Ta = 25°C, R_L=10kΩ, standard V_C)

Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
Total						
Circuit current	I_Q	-	40	70	mA	DVDDIO,DVDDPLL,AVDDDA1, AVDDDA2
Regulator						
Output voltage	V_{REG}	1.3	1.5	1.7	V	I_O=100mA
PLLA						
Lock frequency	f_{PA8}	-	24.576	-	MHz	BCK=3.072MHz (fs=48kHz)
Audio DAC						
Max-output amplitude	V_{OMAX}	0.63	0.75	0.86	Vrms	
THD+N	THD_{DA}	-	0.005	0.03	%	0dB,1kHz
S/N	S/N_{DA}	-	96	-	dB	0dB,1kHz,A-weighted
16bitDAC						
Max-output amplitude	V_{OMAX}	0.65	0.77	0.88	Vrms	
THD+N	THD_{DA}	-	0.03	-	%	0dB,1kHz
S/N	S/N_{DA}	-	90	-	dB	0dB,1kHz,A-weighted

●Block diagram

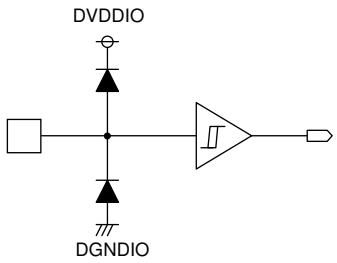
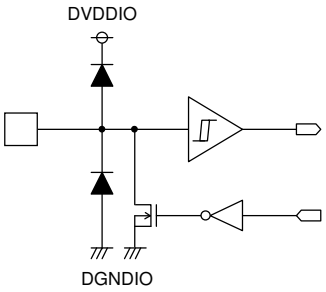
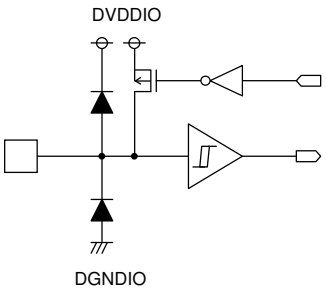
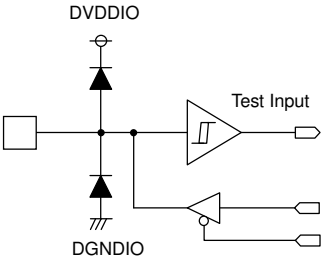
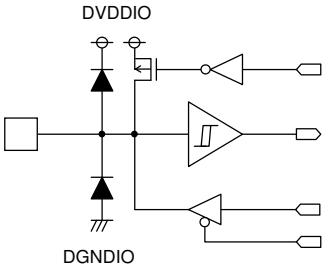
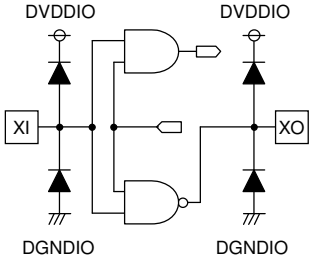
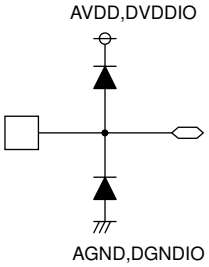
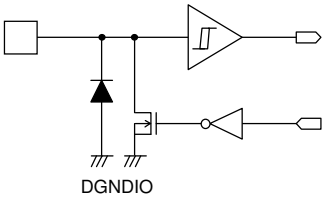
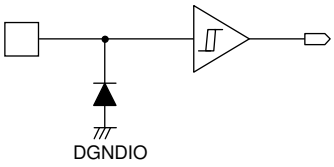


●Pin Description(s)

No.	Name	Description of terminals	Type
1	DVDDPLL	Power supply for PLL	—
2	FILT1	PLLA filter connect terminal 1	G
3	DGNDPLL	GND for PLL	-
4	FILT2	PLLA filter connect terminal 2	G
5	SCANTEST	Test mode select pin	A
6	I2CADR	I^2C slave address select pin	B
7	SCL	I^2C transfer clock input pin	I
8	SDA	I^2C data I/O pin	H
9	DGNDIO1	Digital I/O GND	-
10	RESETB	“L” → reset condition	B
11	DVDDCOR1	Power supply for Digital core 1	-
12	MUTE1B	“L” → Digital-out mute	B
13	MUTE2B	“L” → Audio DAC mute	B
14	MUTE3B	“L” → 16bit DAC mute	B
15	AGNDDA1	GND for DAC 1	-
16	AOUTR1	Audio DAC Rch output 1	G
17	AOUTL1	Audio DAC Lch output 1	G
18	AVDDDA1	Power supply for DAC 1	-
19	AVDDDA2	Power supply for DAC 2	-
20	AOUTR2	Audio DAC Rch output 2	G
21	VREFDA	Reference voltage only for DAC	G
22	AOUTL2	Audio DAC Lch output 2	G
23	AGNDDA2	GND for DAC 2	-
24	ERR1_LRC	PLL1 Error / LRCK output	D
25	ERR2_BCK	PLL2 Error / BCK output	D
26	DATASO	I^2S audio SUB data output	D

No.	Name	Description of terminals	Type
27	DATAMO	I^2S audio Main data output	D
28	BCKO	I^2S audio bit transfer clock output	D
29	LRCKO	I^2S audio LR sampling clock output	D
30	AMCLKO	I^2S audio Synchronous clock output	D
31	SPDIFO	S/PDIF output	D
32	DGNDIO2	Digital I/O GND 2	-
33	XI	X’tal 24.576MHz input	F
34	XO	X’tal 24.576MHz output	F
35	DVDDIO	Digital I/O power supply	-
36	ANATEST	Analog test mode select pin	G
37	DVDDCOR2	Power supply for Digital core 2	-
38	DVDDREG	power supply for Regulator	-
39	LDOPOFF	Regulator POFF signal	G
40	DGNDREG	GND for Regulator	-
41	LRCKI1	I^2S audio LR sampling clock input 1	C
42	BCKI1	I^2S audio bit transfer clock input 1	C
43	DATAI1	I^2S audio data input 1	C
44	LRCKI2	I^2S audio LR sampling clock input 2	C
45	BCKI2	I^2S audio bit transfer clock input 2	C
46	DATAI2	I^2S audio data input 2	C
47	LRCKI3	I^2S audio LR sampling clock input 3	C
48	BCKI3	I^2S audio bit transfer clock input 3	C
49	DATAI3	I^2S audio data input 3	C
50	LRCKI4	I^2S audio LR sampling clock input 4	C
51	BCKI4	I^2S audio bit transfer clock input 4	C
52	DATAI4	I^2S audio data input 4	C

●Terminal equal circuit figure

A	B	C
		
D	**E**	**F**
		
G	**H**	**I**
		

1. Command Interface

BU9408KS2 uses I^2C-bus system for the command interface with a host CPU.

The register of BU9408KS2 has Write-mode and Read-mode.

BU9408KS2 specifies a slave address and 1 byte of selection address, and it performs writing and read-out.

The slave mode format of I^2C bus is shown below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

S : Start condition

Slave Address : After the slave address (7 bits) set up by I2CADR, bit of a read-mode (H") and a write-mode (L") is attached, and a total of 8-bit data is sent. (MSB first)

A: Acknowledge An acknowledge bit is added on to each bit of data transmitted.

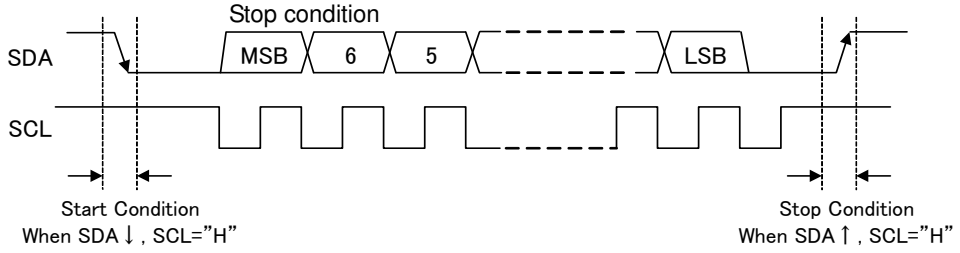
When data transmission is being done correctly, “L” is transmitted.

“H” transmission means there was no acknowledge.

Select Address: BU9408KS2 uses a 1-byte select address. (MSB first)

Data: Data byte, transmitted data (MSB first)

P: Stop condition



1-1. Data Write-In

S	Slave Address	A	Select Address	A	Data	A	P

: Master to Slave : Slave to Master

ADDR=0

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

ADDR=1

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	0

Setting of BU9408KS2 slave address

Terminal setting ADDR	Write-mode Slave-address
0	80h
1	82h

S	Slave Address	A	Select Address	A	Data	A	Data	A	Data	A	P
（例）	80h		20h		00h		00h		00h		

: Master to Slave : Slave to Master

Write-in Procedure

Step	Clock	Master	Slave(BU9408KS2)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Select Address		Write-in target register: 8bit
6	1		Acknowledge	
7	8	Data		8bit write-in data
8	1		Acknowledge	
9		Stop Condition		

○When transmitting continuous data, the auto-increment function moves the select address up by one.
Repeat steps 7 and 8.

1-2. Data Read-out

During read-out, the corresponding read-out address is first written into the &hD0 address register (&h20h in the example). In the following stream, the data is read out after the slave address. Do not return an acknowledge after completing the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P
(ex.)	80h		D0h		20h		

S	Slave Address	A	Data 1	A	Data 2	A		A	Data N	Ā	P
(ex.)	81h		**h		**h				**h		

: Master to Slave, : Slave to Master, A: With acknowledge, Ā: Without acknowledge

Read-out Procedure

Step	Clock	Master	Slave(BU9408KS2)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Req_Addr		I^2C read-out address &hD0
6	1		Acknowledge	
7	8	Select Address		Read-out target register: 8bit
8	1		Acknowledge	
9	1	Stop Condition		
10	1	Start Condition		
11	7	Slave Address		&h81 (&h83)
12	1	R/W (1)		
13	1		Acknowledge	
14	8		Data	8bit read-out data
15	1	Acknowledge		
16		Stop Condition		

○When transmitting continuous data, the auto-increment function moves up the select address by one.
Repeat steps 14 and 15.

1-3. Control Signal Specifications

○ Electrical Characteristics and Timing for Bus Line and I/O Stage

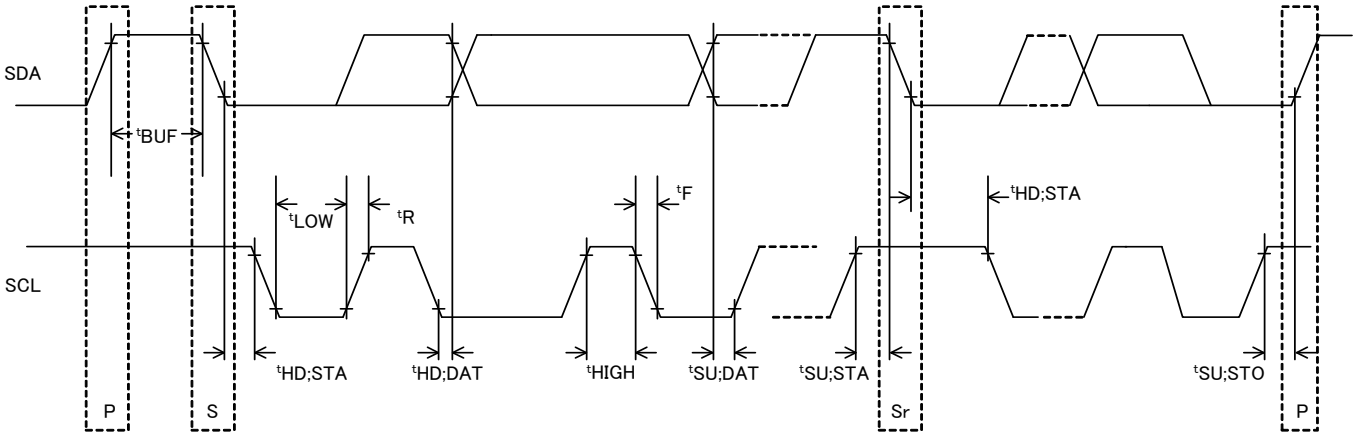


Fig.1-1: Timing Chart

Table 1-1: SDA and SCL Bus Line Characteristics (Ta=25℃ and V_{DD}=3.3V)

Parameters		Symbol	High-Speed Mode		Unit
			Min.	Max.	
1	SCL clock frequency	fSCL	0	400	kHz
2	Bus free time between “stop” condition and “start” condition	^{t}BUF	1.3	—	μS
3	Hold time (re-transmit) “start” condition. After this period, the first clock pulse is generated.	^{t}HD;STA	0.6	—	μS
4	SCL clock LOW state hold time	^{t}LOW	1.3	—	μS
5	SCL clock HIGH state hold time	^{t}HIGH	0.6	—	μS
6	Re-transmit set-up time of “start” condition	^{t}SU;STA	0.6	—	μS
7	Data hold time	^{t}HD;DAT	0[1)]	—	μS
8	Data setup time	^{t}SU;DAT	100	—	ns
9	SDA and SCL signal stand-up time	^{t}R	20+Cb	300	ns
10	SDA and SCL signal stand-down time	^{t}F	20+Cb	300	ns
11	Set-up time for “stop” condition	^{t}SU;STO	0.6	—	μS
12	Each bus line’s capacitive load	Cb	—	400	pF

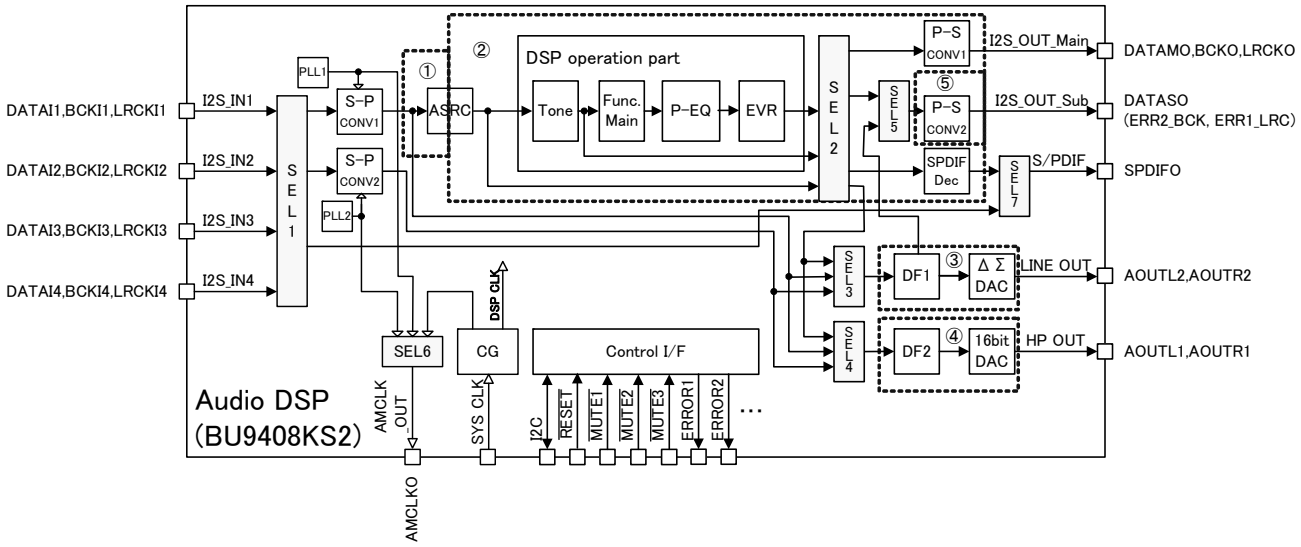
The values above correspond with $V_{IH\ min}$ and $V_{IL\ max}$ levels.

1) Because the transmission device exceeds the undefined domain of the SCL fall edge, it is necessary to internally provide a minimum 300ns
hold time for the SDA signal (of $V_{IH\ min}$ of SCL signal).

The above-mentioned characteristic is a theory value in IC design and it doesn't be guaranteed by shipment inspection.
When problem occurs by any chance, we talk in good faith and correspond.
Neither terminal SCLI nor terminal SDAI correspond to 5V tolerant. Please use it within absolute maximum rating 4.5V.

2. Data and System-clock setting

The input-and-output distribution diagram of the audio data of BU9408KS2 is shown below.



BU9408KS2 has a 4-line digital stereo input, 3-line digital stereo output and 2-line analog stereo output.
The digital data input to the DSP operation part is first changed to fs=48kHz data at the ASRC (asynchronous sampling rate converter).
DSP operation part output is changed to either I^2S format digital output, S/PDIF format digital serial output or analog output.

2-1. Input data selection to S-P Conversion 1 (SEL1)

Default = 0

Select Address	Value	Operation Description
&h03 [1:0]	0	Input data from I2S_IN1
	1	Input data from I2S_IN2
	2	Input data from I2S_IN3
	3	Input data from I2S_IN4

2-2. Input data selection to S-P Conversion 2 (SEL1)

Default = 0

Select Address	Value	Operation Description
&h03 [5:4]	0	Input data from I2S_IN1
	1	Input data from I2S_IN2
	2	Input data from I2S_IN3
	3	Input data from I2S_IN4

2-3. Output data selection P-S Conversion 1 for DATAMO terminal (SEL2)

Default = 0

Select Address	Value	Operation Description
&h04 [1:0]	0	Main data output after DSP operation
	1	Sub data output after DSP operation
	2	Data output before DSP operation

2-4. Output data selection P-S Conversion 2 for DATASO terminal (SEL2, SEL5)

Default = 0

Select Address	Value	Operation Description
&h04 [5:4]	0	Sub data output after DSP operation
	1	Main data output after DSP operation
	2	Data output before DSP operation
	3	Data output from DF1

2-5. P-S Conversion 2 output data option (DATASO, ERR1_LRC, ERR2_BCK)

Usually, from a DATASO terminal, the result of the Sub output process of DSP is outputted to the timing (LRCKO, BCKO) which synchronized with DATAMO.

Moreover, if this output option is set up, it will enable DATAMO to output the data of DF1 as independent data from a DATASO terminal as a 3 line serial output with ERR1_LRC (LRCK) and ERR2_BCK (BCK).

This function is used when doing a line out output using external DAC.

Default = 0

Select Address	Value	Operation Description
&h0E [7]	0	Synchronous output with DATAMO (LRCKO, BCKO)
	1	Asynchronous output with DATAMO (ERR1_LRC, ERR2_BCK)

If this function is used, the monitor of the error flag from ERROR1 and ERROR2 terminal will not be made.

2-6. Output data selecting of SPDIFO terminal (SEL1, SEL7)

Default = 0

Select Address	Value	Operation Description
&h05 [3:0]	0	Data output before DSP operation
	1	Main data output after DSP operation
	2	Sub data output after DSP operation
	3	Output data from I2S_IN1 (Only data of S/PDIF form)
	4	Output data from I2S_IN2 (Only data of S/PDIF form)
	5	Output data from I2S_IN3 (Only data of S/PDIF form)
	6	Output data from I2S_IN4 (Only data of S/PDIF form)

2-7. Output data selecting DF1＋ΔΣDAC (SEL3)

Default = 0

Select Address	Value	Operation Description
&h06 [2:0]	0	Output data from S-P conversion 1 (Refer to &h03 [5:4])
	1	Output data from S-P conversion 2 (Refer to &h03 [1:0])
	2	Data output before DSP operation
	3	Main data output after DSP operation
	4	Sub data output after DSP operation

2-8. Output data selecting DF2+16bitDAC (SEL4)

Default = 0

Select Address	Value	Operation Description
&h06 [6:4]	0	Output data from S-P conversion 1 (Refer to &h03 [5:4])
	1	Output data from S-P conversion 2 (Refer to &h03 [1:0])
	2	Data output before DSP operation
	3	Main data output after DSP operation
	4	Sub data output after DSP operation

2-9. Output clock selecting AMCLKO terminal (SEL8)

Default = 0

Select Address	Value	Operation Description
&h07 [3:0]	0	Output the 256fs (12.288MHz) clock of an input from the XI terminal.
	1	Output the 256fs clock made from PLL1
	2	Output the 256fs clock made from PLL2
	3	Output the 512fs (24.576MHz) clock of an input from the XI terminal.
	4	Output the 512fs clock made from PLL1
	5	Output the 512fs clock made from PLL2
	6	Output the 128fs (6.144MHz) clock of an input from the XI terminal.
	7	Output the 128fs clock made from PLL1
	8	Output the 128fs clock made from PLL2

There are three system clocks used by ASRC of BU9408KS2, DSP, the P-S conversion 1, the P-S conversion 2, a SPDIF output part, DF1+sigma-delta DAC, and DF2+16bit DAC.
One is a 24.576MHz (512fs) system clock from XI terminal, and other two are a clock of 512fs made from PLL1 or PLL2.

2-10. System Clock Selecting of Input Part of ASRC (it is Used for up sampling) (Dotted line ①)

Default = 0

Select Address	Value	Operation Description
&h08 [0]	0	The 24.576MHz (512fs) system clock from the XI terminal
	1	The clock of 512fs made from PLL1 of the S-P conversion 1

2-11. The output part of ASRC (it is used for down sampling), DSP, P-S conversion 1, system clock selecting of a SPDIF output part (Dotted line ②)

Default = 0

Select Address	Value	Operation Description
&h08 [4]	0	The 24.576MHz (512fs) system clock from the XI terminal
	1	The clock of 512fs made from PLL1 of the S-P conversion 1

2-12. System Clock Selecting of DF1＋ΔΣDAC (Dotted line ③)

Default = 0

Select Address	Value	Operation Description
&h0A [1:0]	0	The 24.576MHz (512fs) system clock from the XI terminal
	1	The clock of 512fs made from PLL1 of the S-P conversion 1
	2	The clock of 512fs made from PLL2 of the S-P conversion 2

2-13. System Clock Selecting DF2＋16bit DAC (Dotted line ④)

Default = 0

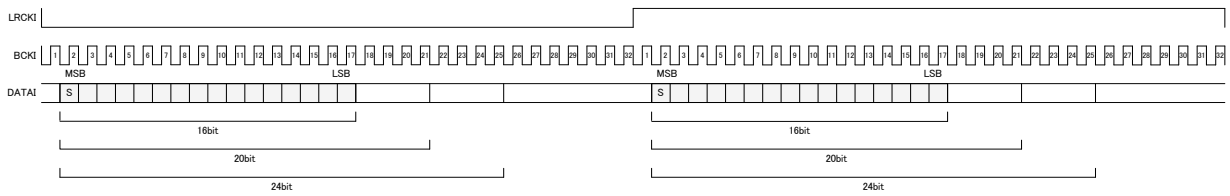
Select Address	Value	Operation Description
&h0A [5:4]	0	The 24.576MHz (512fs) system clock from the XI terminal
	1	The clock of 512fs made from PLL1 of the S-P conversion 1
	2	The clock of 512fs made from PLL2 of the S-P conversion 2

When using DATASO as an asynchronous output to DATAMO, it sets up system clock selecting of the P-S conversion 2 by this command. (Dotted line ⑤)

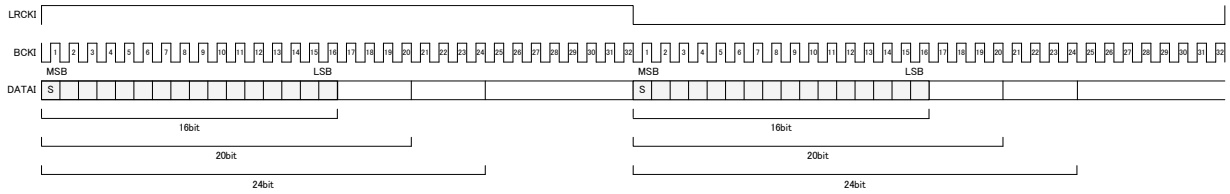
3. S-P Conversion 1 and S-P Conversion 2

BU9408KS2 has two built-in serial-parallel conversion circuits. (S-P Conversion 1 and S-P Conversion 2)
S-P conversions 1 and 2 are blocks which receive 3-line serial input audio data from pins and convert it to parallel data.
Input from DATAI1, BCKI1 and LRCKI1 (pins 43, 42 and 41), DATAI2, BCKI2 and LRCKI2 (pins 46, 45, and 44), DATAI3, BCKI3 and LRCKI3 (pins 49, 48 and 47), and DATAI4, BCKI4 and LRCKI4 (pins 52, 51 and 50) are selected.
The three input formats are IIS, left-justified and right-justified. The bit clock frequency may be selected from either 64fs or 48fs, but when 48fs is selected, the input format is always right-justified. 16bit, 20bit and 24bit output may be selected for each format.
Below are the timing charts for each transfer format.

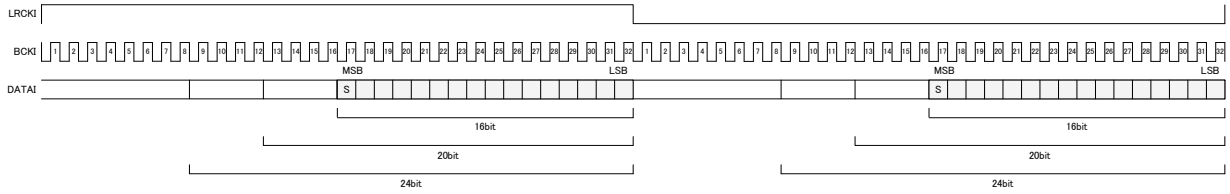
IIS Format



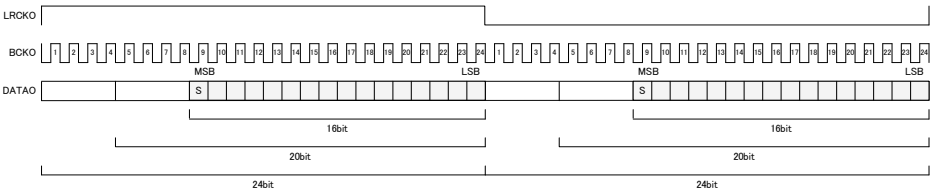
Left-Justified Format



Right-Justified Format



48fs



3-1. Bit Clock Frequency Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0B [4]	0	64fs format
S-P Conversion 2 &h0C [4]	1	48fs format

3-2. Format Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0B [3:2]	0	IIS format
S-P Conversion 2 &h0C [3:2]	1	Left-justified format
	2	Right-justified format

3-3. Data Bit Width Configuration for 3-line Serial Input

Default = 0

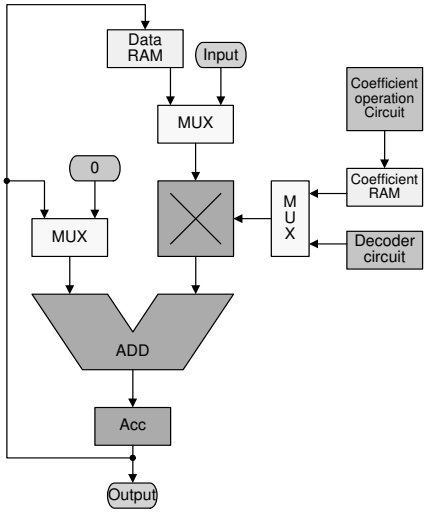
Select Address	Value	Operation Description
S-P Conversion 1 &h0B [1:0]	0	16 bit
S-P Conversion 2 &h0C [1:0]	1	20 bit
	2	24 bit

4. Digital Sound Processing (DSP)

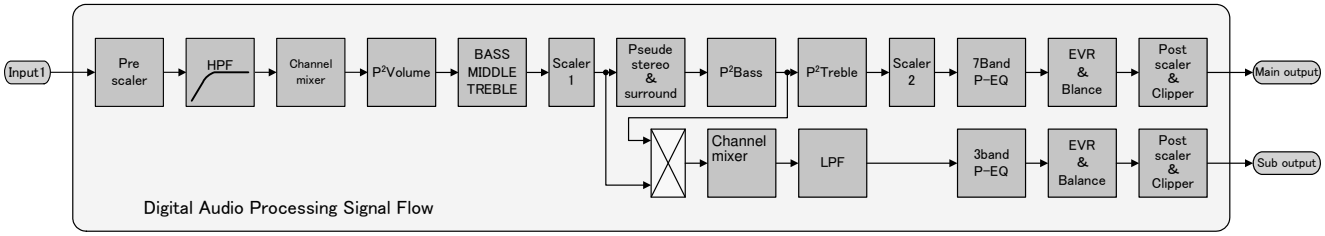
BU9408KS2's Digital Sound Processing (DSP) consists of special hardware most suitable to Thin TV.
BU9408KS2 uses this special DSP to perform the following processing.
Prescaler, DC cut HPF, Channel Mixer, P^2Volume (Perfect Pure Volume), BASS, MIDDLE, TREBLE,
Pseudo Stereo, Surround, P^2Bass, P^2Treble, 7 Band Parametric Equalizer, Master Volume, L/R Balance, PostScaler, Output Clipper, Sub-woofer output Processing.

DSP Outline and Signal Flow

Data width:	32 bit (DATA RAM)
Machine cycle:	40.7ns (512fs, fs=48kHz)
Multiplier:	32×24 → 56 bit
Adder:	32+32 → 32 bit
Data RAM:	256×32 bit
Coefficient RAM:	128×24 bit
Sampling frequency:	fs=48kHz
Master clock:	512fs (24.576MHz, fs=48kHz)



Digital signal from 16bit to 24bit is inputted to DSP,
and it is extended by +8bit (+42dB) as overflow margin on the upper side.
The clip process is performed in DSP when the process exceeding this range is performed.



4-1. Prescaler

When digital signal is inputted to audio DSP, if the level is full scale input and the process of surround or equalizer is performed, then it overflows, therefore the input gain is adjusted by prescaler.
Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.
Prescaler does not incorporate the smooth transition function.

Default = 30h

Select Address	Operational explanation
&h20 [7:0]	command / gain 00 / +24dB 01 / +23.5dB ⋮ / ⋮ 30 / 0dB 31 / −0.5dB 32 / −1dB ⋮ / ⋮ FE / −103dB FF / −∞

4-2. DC cut HPF

The DC offset component of digital signal inputted to the audio DSP is cut by this HPF.

The cut off frequency (fc) of HPF is 1Hz, and first-order filter is used.

Default = 0

Select Address	Value	Operational explanation
&h21 [0]	0	Not using the DC cut HPF
	1	Using the DC cut HPF

4-3. Channel mixer

It performs the setting of mixing the sounds of left channel & right channel of digital signal inputted to the audio DSP.

Here the stereo signal is made to be monaural.

The data inputted to Lch of DSP is mixed.

Default = 0

Select Address	Value	Operational explanation
&h22 [7:6]	0	Inputting the Lch data
	1	Inputting the data of (Lch + Rch) / 2
	2	Inputting the data of (Lch + Rch) / 2
	3	Inputting the Rch data

The data inputted to Rch of DSP is mixed.

Default = 0

Select Address	Value	Operational explanation
&h22 [5:4]	0	Inputting the Rch data
	1	Inputting the data of (Lch + Rch) / 2
	2	Inputting the data of (Lch + Rch) / 2
	3	Inputting the Lch data

4-4. P^2Volume （Perfect Pure Volume）

There are some scenes in which sound suddenly becomes large like plosive sound in TV Commercial or Movie.

P^2Volume function automatically controls the volume and adjusts the output level.

In addition, it also adjusts in such a way that a whispery sound can be heard easily.

P^2Volume function operates in the fields of (1), (2) & (3) divided according to input level.

(1) at the time of $V_{I\,inf}(-\infty) \sim V_{I\,min}$

Noise is prevented from being lifted by P^2Volume function.

(2) When input level is over $V_{I\,min}$ and output is below V_{Omax}

$$V_O = V_I + \alpha$$

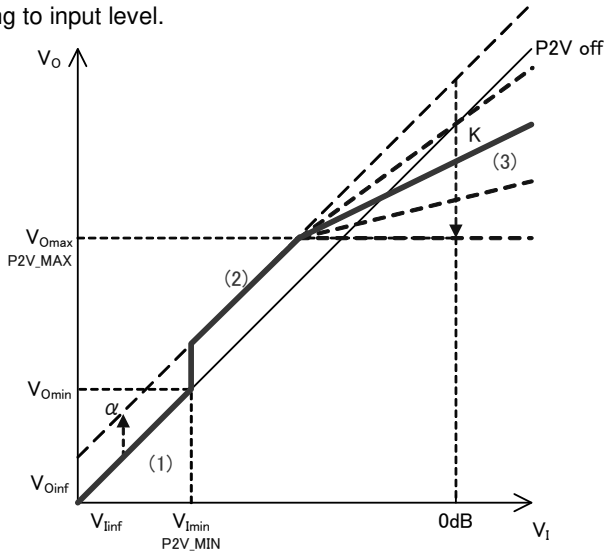
α： Lifting the Whole output level by the offset value α

(3) When output level V_O exceeds V_{Omax}

$$V_O = K \cdot V_I + \alpha$$

K： Slope for suppressing of D range （P2V_K）

It is also possible to set an output level constant.



Selection of using the P^2Volume function.

Default = 0

Select Address	Value	Operational explanation
&h33 [7]	0	Not using the P^2Volume function
	1	Using the P^2Volume function

Setting of $V_{I\,min}$

In order to cancel that noise etc. is lifted by P^2Volume, the P2V_MIN sets the minimum level at which (to the minimum) the P^2Volume functions.

command

Default = 00h

Select Address	Operational explanation
&h34 [4:0]	

command	gain	command	gain	command	gain	コマンド値	ゲイン
00	−∞	08	−44dB	10	−60dB	18	−76dB
01	−30dB	09	−46dB	11	−62dB	19	−78dB
02	−32dB	0A	−48dB	12	−64dB	1A	−80dB
03	−34dB	0B	−50dB	13	−66dB	1B	−82dB
04	−36dB	0C	−52dB	14	−68dB	1C	−84dB
05	−38dB	0D	−54dB	15	−70dB	1D	−86dB
06	−40dB	0E	−56dB	16	−72dB	1E	−88dB
07	−42dB	0F	−58dB	17	−74dB	1F	−90dB

Setting of V_{Omax}

P2V_MAX sets the output suppression level. It represents the output level V_{Omax} at the time of input level V_I = 0dB in the case of setting of P2V_K = “0h” (slope is 0).

Default = 00h

Select Address	Operational explanation
&h35 [4:0]	

command	gain	command	gain	command	gain	command	gain
00	0dB	08	−8dB	10	−16dB	18	−24dB
01	−1dB	09	−9dB	11	−17dB	19	−25dB
02	−2dB	0A	−10dB	12	−18dB	1A	−26dB
03	−3dB	0B	−11dB	13	−19dB	1B	−27dB
04	−4dB	0C	−12dB	14	−20dB	1C	−28dB
05	−5dB	0D	−13dB	15	−21dB	1D	−29dB
06	−6dB	0E	−14dB	16	−22dB	1E	−30dB
07	−7dB	0F	−15dB	17	−23dB	1F	−

Setting of K

P2V_K sets the slop of D range. It sets the P2V_MAX = “1Eh” (-30dB) and represents the output level V_{Omax} at the time of input level V_I = 0dB.

Default = 00h

Select Address	Operational explanation
&h36 [3:0]	

command	gain	comman	gain
0	−30dB	8	−14dB
1	−28dB	9	−12dB
2	−26dB	A	−10dB
3	−24dB	B	−8dB
4	−22dB	C	−6dB
5	−20dB	D	−4dB
6	−18dB	E	−2dB
7	−16dB	F	0dB

Setting of α

P2V_OFS makes small voice easy to be heard because the whole output level is lifted.

Default = 00h

Select Address	Operational explanation
&h37 [4:0]	

command	gain	command	gain	command	gain	command	gain
00	0dB	08	+8dB	10	+16dB	18	+24dB
01	+1dB	09	+9dB	11	+17dB	19	−
02	+2dB	0A	+10dB	12	+18dB	1A	−
03	+3dB	0B	+11dB	13	+19dB	1B	−
04	+4dB	0C	+12dB	14	+20dB	1C	−
05	+5dB	0D	+13dB	15	+21dB	1D	−
06	+6dB	0E	+14dB	16	+22dB	1E	−
07	+7dB	0F	+15dB	17	+23dB	1F	−

Setting 1 of transition time at the time of attack

A_RATE is the setting of transition time when the state of P^2Volume function is transited to (2)→(3).

Default = 0

Select Address	Operational explanation
&h38 [6:4]	

command	A_RATE time	command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

Setting 1 of transition time at the time of recovery

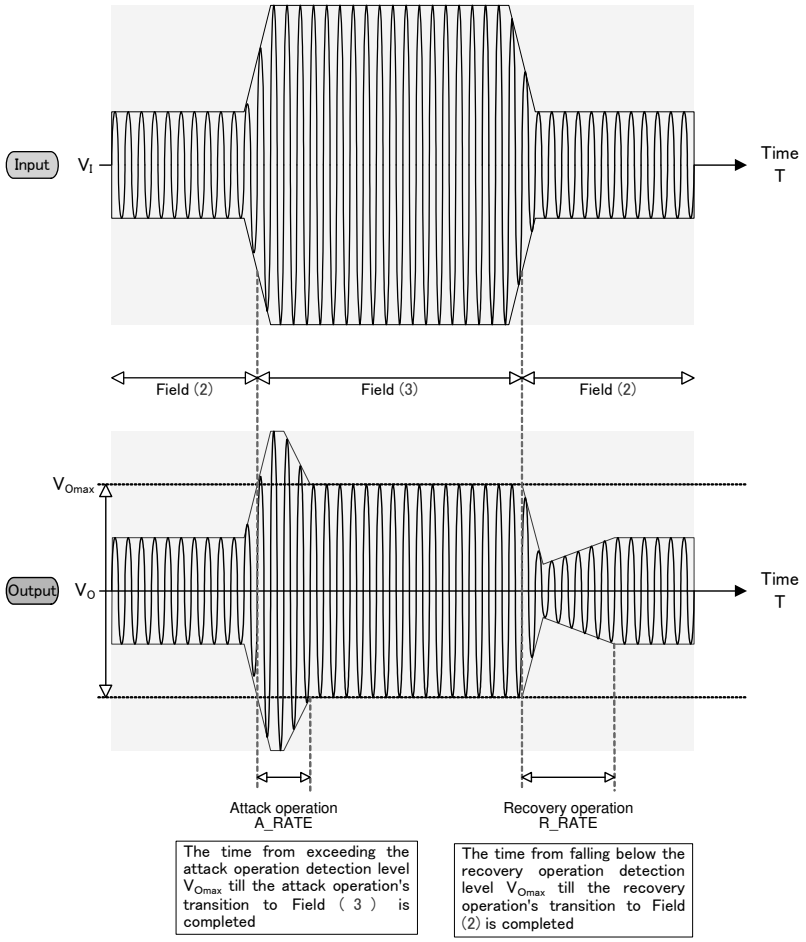
R_RATE is the setting of transition time when the state of P^2Volume function is transited to (3)→(2).

Default = 0h

Select Address	Operational explanation
&h38 [3:0]	

command	R_RATE time	command	R_RATE time
0	0.25s	8	3s
1	0.5s	9	4s
2	0.75s	A	5s
3	1s	B	6s
4	1.25s	C	7s
5	1.5s	D	8s
6	2s	E	9s
7	2.5s	F	10s

Explanation of A_RATE,R_RATE(field transition of (2)<->(3))



Setting 1 of attack detection time

A_TIME is the setting of the initiation of P^2Volume function's transition operation. If output level at the time of transiting to (2)→(3) continues for more then A_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

Select Address	Operational explanation
&h39 [6:4]	

command	A_TIME	command	A_TIME
0	0.5ms	4	3ms
1	1ms	5	4ms
2	1.5ms	6	5ms
3	2ms	7	6ms

Setting 1 of recovery detection time

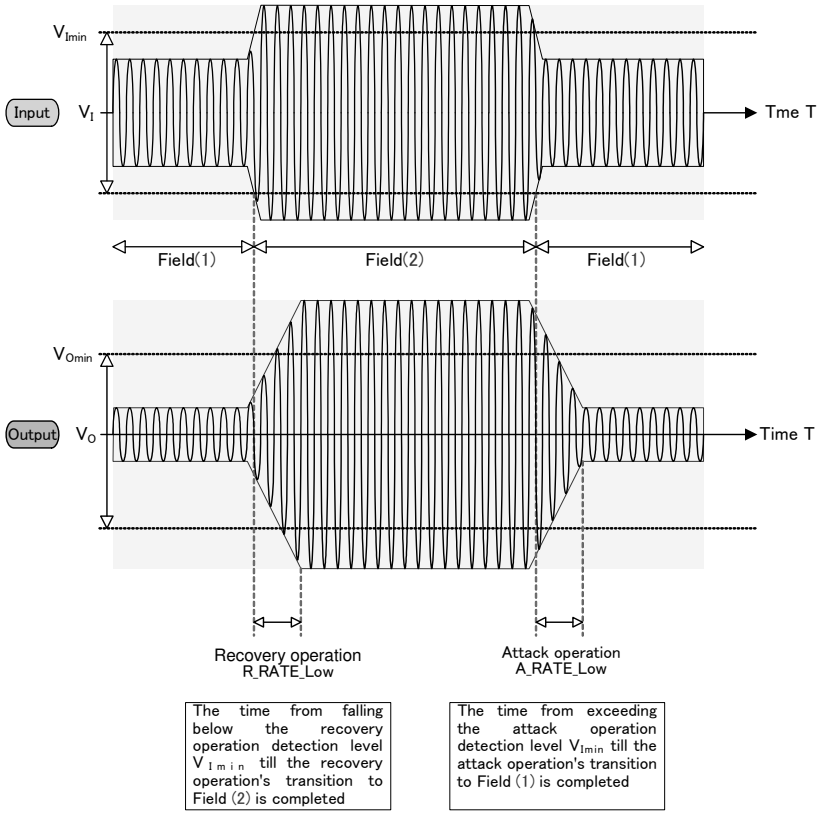
R_TIME is the setting of the initiation of P^2Volume function's transition operation. If output level at the time of transiting to (3)→(2) continues for more then R_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

Select Address	Operational explanation
&h39 [2:0]	

command	R_TIME	command	R_TIME
0	50ms	4	300ms
1	100ms	5	400ms
2	150ms	6	500ms
3	200ms	7	600ms

Explanation of A_RATE_Low,R_RATE_Low(field transition of (1)<->(2))



Setting 2 of the transition time at the time of attack

A_RATE_LOW is the setting of transition time when the state of P^{2}Volume function is transited to (2)→(1).

Default = 0

Select Address	Operational explanation

Command	A_RATE_LOW Time	Command	A_RATE_LOW Time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

&h3A [6:4]

Setting 2 of the transition time at the time of recovery

R_RATE_LOW is the setting of transition time when the state of P^{2}Volume function is transited to (1)→(2).

Default = 0 (Caution) This setting value is not reflected in BU9408KS2. The value of &h38 [3:0] is set up.

Select Address	Operational explanation

Command	R_RATE_LOW Time	Command	R_RATE_LOW Time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

&h3A [2:0]

Setting 2 of attack recovery detection time

AR_TIME_LOW is the setting of the initiation of P^{2}Volume function's transition operation. If output level at the time of transiting to (1)<->(2) continues for more then AR_TIME time in succession, then the state transition of P^{2}Volume is started.

Default = 0

Select Address	Operational explanation

Command	AR_TIME_LOW	Command	AR_TIME_LOW
0	0.5ms	4	3ms
1	1ms	5	4ms
2	1.5ms	6	5ms
3	2ms	7	6ms

&h3B [6:4]

○Pulse sound detection and High-speed recovery function（functioning only at the time of transition of (2)<->(3)）

P^2Volume function makes the P^2Volume also compatible with large pulse sounds (clapping of hands, fireworks & shooting etc.) in addition to normal P^2Volume operation. When large pulse sound is inputted, attack operation (A_RATE) or recovery operation (R_RATE) is performed at 4 or 8 times the speed of normal attack operation or recovery operation.

Selection of using the pulse sound detection function.

Default = 0

Select Address	Value	Operational explanation
&h3BC [7]	0	Not using of pulse sound detection function
	1	Using of pulse sound detection function

Selection of operating times of Recovery Time (R_RATE) in the case of using the pulse sound detection function

Default = 0

Select Address	Value	Operational explanation
&h3C [3]	0	Operating at 4 times the speed corresponding to the setting time of R_RATE
	1	Operating at 8 times the speed corresponding to the setting time of R_RATE

Selection of pulse sound detection time

Default = 0

Select Address	Operational explanation
&h3C [6:4]	See table below

Command	Detection time	Command	Detection time
0	100us	4	2ms
1	200us	5	5ms
2	400us	6	10ms
3	1ms	7	20ms

Setting of operating level of pulse sound detection function

Operation is started by the difference between the presently detected value and the last value as a standard.

Default = 0

Select Address	Operational explanation
&h3C [2:0]	See table below

Command	Detection level	Command	Detection level
0	Over 1.002	4	Over 0.251
1	Over 0.709	5	Over 0.178
2	Over 0.502	6	Over 0.126
3	Over 0.355	7	Over 0.089

Example） Present detection level A : -10dB → 10^(-10/20) = 0.32

The last detection level B : -30dB → 10^(-30/20) = 0.032

A – B : 0.32 – 0.032 = 0.288 → Operating by the setting of command ”4” to ”7”.

4-5. BASS

BASS of TONE Control can use Peaking filter or Low-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients (b0, b1, b2, a1, a2)by selecting the F_0, Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○BASS Control

Selection of filter types

Default = 0

Select Address	Value	Operational explanation
&h40 [7]	0	Peaking filter
	1	Low-shelf filter

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h40 [6]	0	Using BASS smooth transition function
	1	Not BASS using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h40 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h40[0] command, to the coefficient RAM for smooth transition, the alteration of BASS's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [0]	0	BASS smooth transition stop
	1	BASS smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of Bass smooth transition time, from the time the BASS smooth transition start (&h4C[0] = "1") is executed until the following command is sent. Please make sure to perform the Bass smooth transition stop (&h4C[0] = "0") after the smooth transition is completed.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted directly to the coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h40 [0]	0	BASS coefficient transmission stop
	1	BASS coefficient transmission start

Selection of frequency (F_0)

Default = 0Eh

Select Address: &h41 [5:0]

Operational explanation

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	–
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	–
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	–

Selection of quality factor (Q)

Default = 4h

Select Address: &h42 [3:0]

Operational explanation

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address: &h43 [6:0]

Operational explanation

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-6. MIDDLE

MIDDLE of TONE Control uses Peaking filter.

The setting is converted, in the IC, into digital filter's coefficients (b0, b1, b2, a1, a2)by selecting the F, Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○MIDDLE Control

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h44 [6]	0	Using MIDDLE smooth transition function
	1	Not MIDDLE using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h44 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h44[0] command, to the coefficient RAM for smooth transition, the alteration of MIDDLE's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [1]	0	MIDDLE smooth transition stop
	1	MIDDLE smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of MIDDLE smooth transition time, from the time the MIDDLE smooth transition start (&h4C[1] = "1") is executed until the following command is sent. Please make sure to perform the MIDDLE smooth transition stop (&h4C[1] = "0") after the smooth transition is completed.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted to the direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h44 [0]	0	MIDDLE coefficient transmission stop
	1	MIDDLE coefficient transmission start