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Digital Sound Processors for FPD TVs

32bit Audio DSP

BU9414FV

No.12083EAT04

●General Description

This LSI is the digital sound processor which made the use digital signal processing for FPD TVs.
DSP of ROHM original is used for the TV sound processor unit, and it excels in cost performance.
There are two digital input systems. An output is a digital output corresponding to 2.1ch.

●Features

■ Digital Signal Processor unit

Word length:	32bit (Data RAM)
The fastest machine cycle:	40.7ns (512fs, fs = 48kHz)
Multiplier:	32 x 24 → 56bit
Adder:	32 + 32 → 32bit
Data RAM:	256 x 32bit
Coefficient RAM:	128 x 24bit
Sampling frequency:	fs = 48kHz
Master clock :	512fs (It is a slave to 256fs of fs = 48kHz, 44.1 kHz, and 32 kHz)

■ Digital signal input (Stereo 2 lines): 16/20/24bit(I2S, Left-Justified, Right-Justified)
Digital signal output (Stereo 2 lines): 16/20/24bit(I2S, Left-Justified, Right-Justified, S/PDIF)

■The sound signal processing function for FPD TVs

Pre-Scaler, DC cut HPF, Channel Mixer, P^2Volume(Perfect Pure Volume), BASS, MIDDLE, TREBLE, Pseudo BASS, Surround, P^2Bass, P^2Treble, 7Band Parametric EQ, Master Volume, L/R balance, Post-Scaler, Output signal clipper
(P^2Volume, P^2Bass, and P^2Treble are the sound effect functions of ROHM original.)

●Applications

Flat Panel TVs (LCD, Plasma)

●Absolute maximum rating（Ta=25°C）

Item	Symbol	Rating	Unit
Power-supply voltage	V_{DD}	4.5	V
Allowable dissipation	P_d	700 (*1)	mW
operating temperature range	T_{opr}	-25～+85	°C
Storage temperature range	T_{stg}	-55～+125	°C

*1： 7mW is decreased for 1°C when using it with Ta=25°C or more.
*Operation can't be guaranteed.

●Operating condition（Ta=-25～+85°C）

Item	Symbol	Rating	Unit
Power-supply voltage	V_{DD}	3.0～3.6	V

* It isn't Radiation-proof designed for the product.

●**Electric characteristic(Digital serial)**

V_{DD}=3.3V unless specified, Ta=25°C

Item		Symbol	Rating value			Unit	Terms	Adaptive terminal
			Min.	Standard	Max.			
Hysteresis Input voltage	H Level voltage	V_{IH}	2.5	-	-	V		*1,2,3
	L Level voltage	V_{IL}	-	-	0.8	V		*1,2,3
Input current		I_I	-1	-	+1	μA	V_{IN}=0～3.3V	*1
Pull-up resistor input L current		I_{IL}	-150	-100	-50	μA	V_{IN}=0V	*2
Pull-down resistor input H current		I_{IH}	35	70	105	μA	V_{IN}=3.3V	*3
Output voltage	H Level voltage	V_{OH}	2.75	-	-	V	I_O=-0.6mA	*4
	L Level voltage	V_{OL}	-	-	0.55	V	I_O=0.6mA	*4
SDA terminal Output voltage	L Level voltage	V_{OL}	-	-	0.4	V	I_O=3mA	*5

Adaptive terminal

*1 CMOS hysteresis input terminal
SCLI(8pin), SDAI(9pin), MODE(20pin)

*2 Pull-up resistor built-in CMOS hysteresis input terminal
LRCKI(2pin), SDATA1(3pin), SDATA2(4pin), MCLK(39pin), BCKI(40pin)

*3 Pull-down resistor built-in CMOS hysteresis input terminal
RESETX(5pin), MUTEX_SP(6pin), MUTEX_DAC(7pin), ADDR(21pin)

*4 CMOS output terminal
SPDIFO(22pin), SDAO(28pin), SCLO(29pin), MUTEX_DACO(30pin), MUTEX_SPO(31pin), RESETXO(32pin), DATAO2(33pin), DATAO1(34pin), LRCKO(35pin), BCKO(36pin), SYSCKO(37pin)

*5 Open drain output terminal
SDAI(9pin)

・Electric characteristic(Analogue serial)

V_{DD}=3.3V Unless specified, Ta=25°C,R_L=10kΩ, V_C standard

Item	Symbol	Rating Value			Unit	Object pin/Condition
		Min	Standard	Max		
whole						
Circuit current	I_Q	-	15	30	mA	VDD
Regulator part						
Output voltage	V_{REG}	1.3	1.5	1.7	V	I_O=100mA
PLL part						
Lock frequency	F_{LK8}	-	24.576	-	MHz	256fs(fs=48kHz) input

●Block diagram

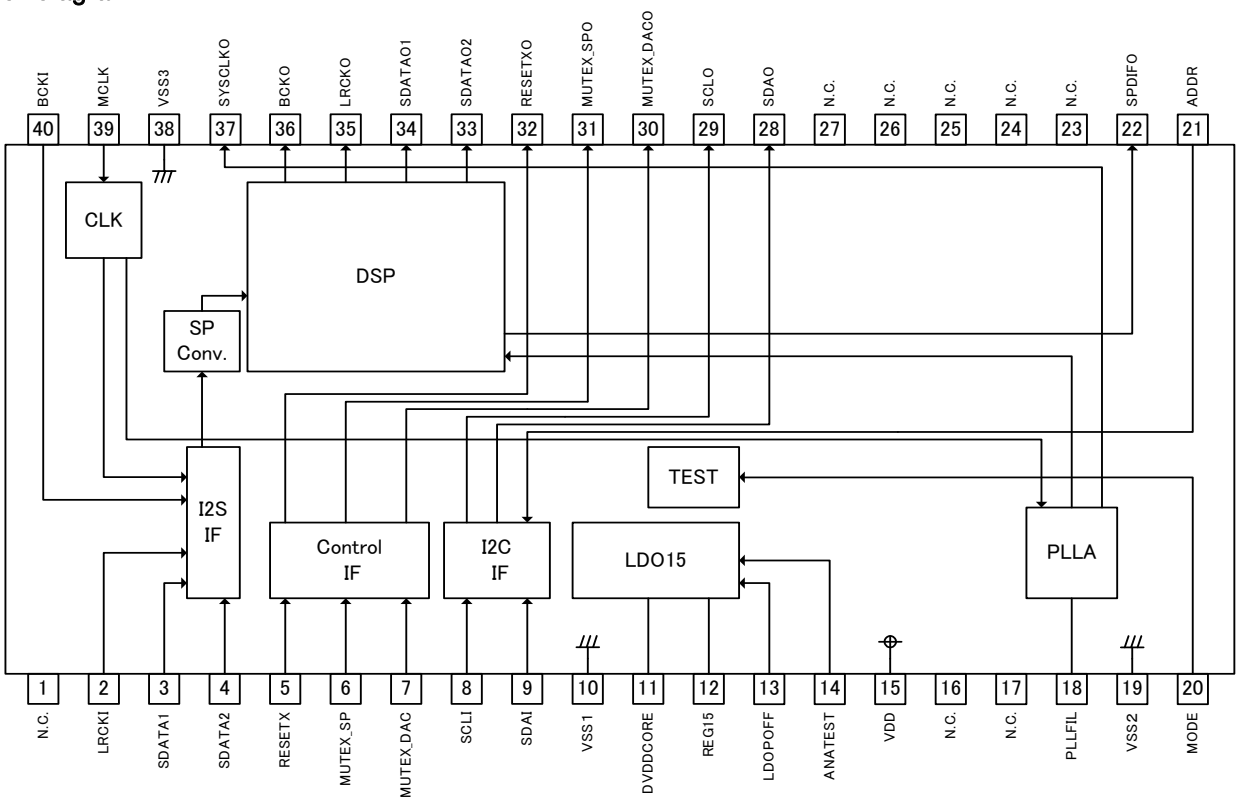


Fig.2 Block diagram

●Pin Description(s)

No.	Name	Description of terminals	Type
1	N.C	(*2)	-
2	LRCKI	I^2S Audio LR signal input	D
3	SDATA1	I^2S Audio data input 1	D
4	SDATA2	I^2S Audio data input 2	D
5	RESETX	Reset status with “L”	B
6	MUTEX_SP	DAC mute signal input(*1)	B
7	MUTEX_DAC	SP mute signal input(*1)	B
8	SCLI	I^2C Forwarding clock input	F
9	SDAI	I^2C Data input output	E
10	VSS1	Digital I/O GND	-
11	DVDDCORE	Connect to REG15 terminal	-
12	REG15	Built-in regulator voltage output	G
13	LDOPOFF	Built-in regulator POFF signal input	G
14	ANATEST	Analog test monitor terminal	G
15	VDD	Digital I/O power supply	-
16	N.C		-
17	N.C		-
18	PLLFIL	Filter connection terminal for PLL	G
19	VSS2	Digital I/O GND	-
20	MODE	Test mode selection input	A

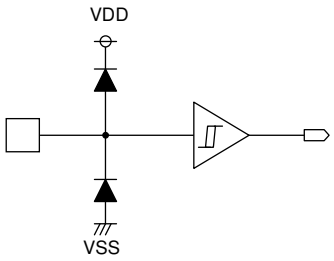
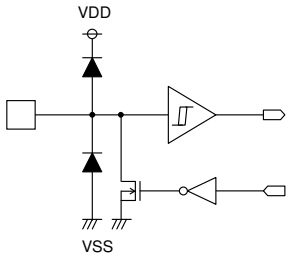
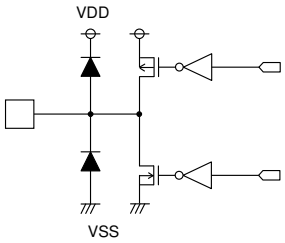
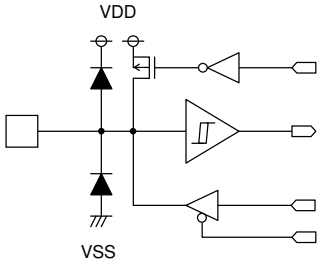
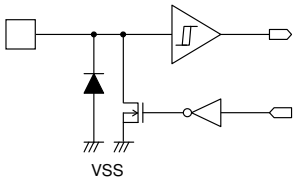
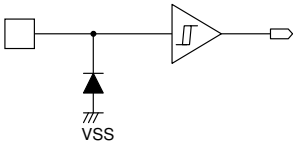
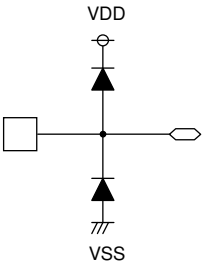
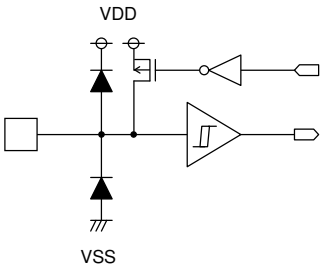
No.	Name	Description of terminals	Type
21	ADDR	I^2C Slave address selection terminal	B
22	SPDIFO	S/PDIF Signal output	C
23	N.C		-
24	N.C		-
25	N.C		-
26	N.C		-
27	N.C		-
28	SDAO	2 line serial data output（*1）	C
29	SCLO	2 line serial clock output（*1）	C
30	MUTEX_DACO	DAC mute signal output(*1)	C
31	MUTEX_SPO	SP mute signal output(*1)	C
32	RESETXO	Reset signal output(*1)	C
33	SDATAO2	I^2S Audio data output 2	C
34	SDATAO1	I^2S Audio data output 1	C
35	LRCKO	I^2S Audio LR signal output 1	C
36	BCKO	I^2S Audio clock output 1	C
37	SYSCLKO	System clock output（*1）	C
38	VSS3	Digital I/O GND	-
39	MCLK	Master clock input	H
40	BCKI	I^2S Audio clock input	D

N.C.：Non Connection

(*1)：signal terminal is used with D class amplifier IC (BD5446EFV etc.) for input I2S made by Rohm.

(*2) ：It connects with the lead frame of a package. Please use by OPEN or GND connection.

● Pin Equivalent Circuit Diagrams

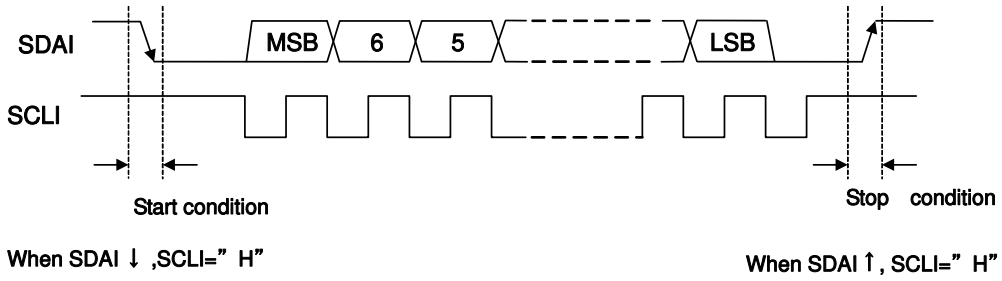
A	B	C
		
D	**E**	**F**
		
G	**H**	
		

1.Command interface

I²C bus method is used in command interface with host CPU on BU9414FV.
In BU9414FV, not only writing but read-out is possible except for some registers.
Besides the slave address in BU9414FV, one byte select address can be Specified, written and readout.
The format of I²C bus slave mode is shown below.

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Select Address	A	Data	A	P

S: Start condition
Slave Address: Putting up the bit of read mode (H") or write mode (L") after slave address (7bit) set with ADDR, the data of eight bits in total will be sent. (MSB first)
A: The acknowledge bit in each byte adds into the data when acknowledge is sent and received.
When data is correctly sent and received, "L" will be sent and received.
There was no acknowledge for "H".
Select Address: 1 byte select address is used in BU9414FV. (MSB first)
Data: Data-byte, data(MSB first)sent and received
P: Stop Condition



1-1. Data writing

S	Slave Address	A	Select Address	A	Data	A	P

: From master to slave : From slave to master

ADDR=0

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

ADDR=1

MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	0

Setting of BU9414FV slave address

Terminal setting	Write-mode
ADDR	Slave-address
0	80h
1	82h

S	Slave Address	A	Select Address	A	Data	A	Data	A	Data	A	P
(example)	80h		20h		00h		00h		00h		

: From master to slave : From slave to master

Writing procedure

Step	Clock	Master	Slave(BU9414FV)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Select Address		Writing object register 8 bit
6	1		Acknowledge	
7	8	Data		Writing data 8 bit
8	1		Acknowledge	
9		Stop Condition		

- The select address add +1 by auto increment function when the data is transferred continuously.
  Repeat of Step 7~8.

1-2. Data readout

First of all, the readout target address(ex.&h20h) is written in &hD0 address register at the time of readout.
In the following stream, data is read out after the slave address. Please do not return the acknowledge when ending the reception.

S	Slave Address	A	Req_Addr	A	Select Address	A	P

(example) 80h D0h 20h

S	Slave Address	A	Data 1	A	Data 2	A	...	A	Data N	Ā	P

(example) 81h **h **h **h

: Master to slave, : Slave to master, A : With acknowledge, Ā : without acknowledge

Readout Procedure

Step	Clock	Master	Slave(BU9414FV)	Note
1		Start Condition		
2	7	Slave Address		&h80 (&h82)
3	1	R/W (0)		
4	1		Acknowledge	
5	8	Req_Addr		Address for I^2C readout &hD0
6	1		Acknowledge	
7	8	Select Address		Readout object register 8 bit
8	1		Acknowledge	
9	1	Stop Condition		
10	1	Start Condition		
11	7	Slave Address		&h81 (&h82)
12	1	R/W (1)		
13	1		Acknowledge	
14	8		Data	Readout data 8 bit
15	1	Acknowledge		
16		Stop Condition		

○ The select address adds +1 by auto increment function when continuous data is transferred.
  Repeat Step14~15.

1-3. Control signal specification

○ Bus line, I/O stage electrical specification and timing.

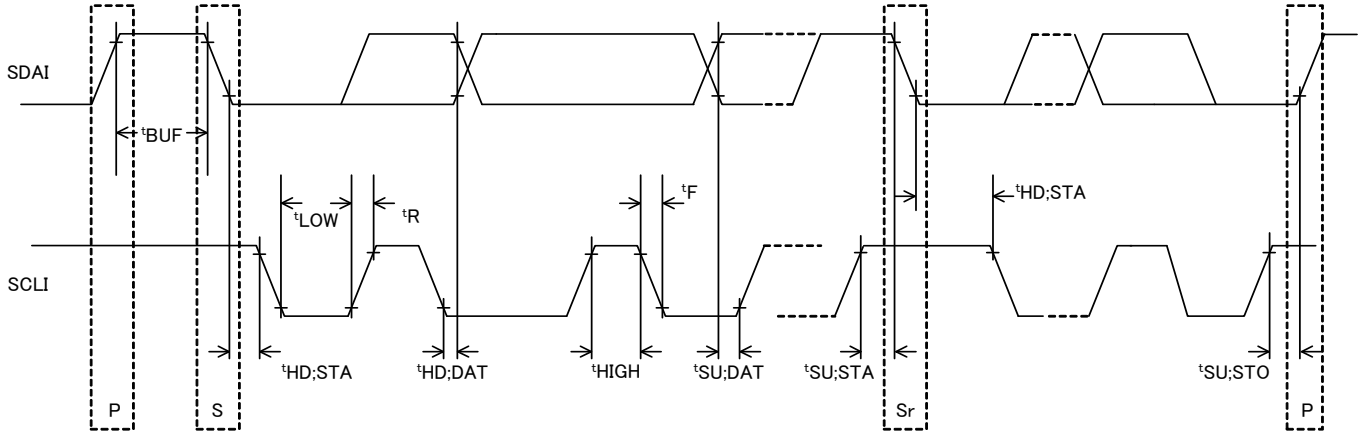


Fig.1-1: Timing chart

Table 1-1: SDAI and SCLI bus-line characteristic (Unless specified, Ta=25°C, Vcc=3.3V)

Parameter		Code	High-speed mode		Unit
			Min.	Max.	
1	SCLI clock frequency	fSCL	0	400	kHz
2	Bus-free-time between "Stop" condition and "Start" condition	^{t}BUF	1.3	—	μS
3	"Start" condition of hold-time (resending). After this period, the first clock-pulse is generated.	^{t}HD;STA	0.6	—	μS
4	LOW status hold-time of SCLI clock	^{t}LOW	1.3	—	μS
5	HIGH status hold-time of SCLI clock	^{t}HIGH	0.6	—	μS
6	Setup time of resending “Start” condition	^{t}SU;STA	0.6	—	μS
7	Data-hold-time	^{t}HD;DAT	0[1)]	—	μS
8	Data-setup time	^{t}SU;DAT	500/250/150	—	ns
9	Rising time of SDAI and SCL signal	^{t}R	20+Cb	300	ns
10	Fall time of SDAI and SCL signal	^{t}F	20+Cb	300	ns
11	Setup time of "Stop" condition	^{t}SU;STO	0.6	—	μS
12	Capacitive load of each bus-line	Cb	—	400	pF

The above-mentioned numerical values are all the values corresponding to $V_{IH\ min}$ and $V_{IL\ max}$ level.

1) To exceed an undefined area on falling edged of SCLI, transmission device should internally offer the hold-time of 300ns or more for SDAI signal($V_{IH\ min}$ of SCLI signal).

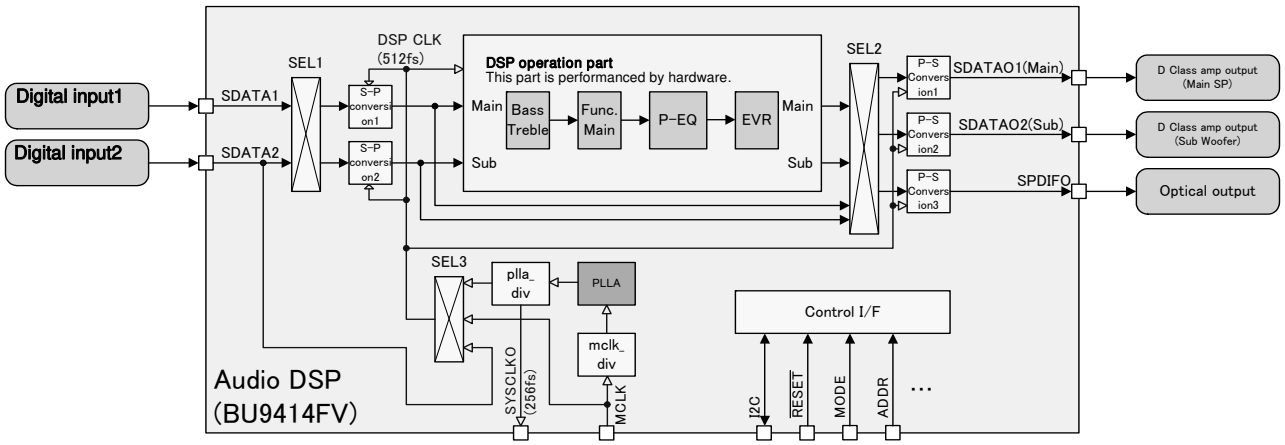
2) Data-setup time changes with setup of MCLK. In MCLK=512fs, data setup time is 150ns. In MCLK=256fs, data setup time is 250ns. In MCLK=128fs, data setup time is 500ns.

The above-mentioned characteristic is a theory value in IC design and it doesn't be guaranteed by shipment inspection. When problem occurs by any chance, we talk in good faith and correspond.

Neither terminal SCLI nor terminal SDAI correspond to 5V tolerant. Please use it within absolute maximum rating 4.5V.

2.Switching of data and clock

I/O system chart of BU9414FV audio data is shown below.



BU9414FV has 2 digital stereo input and 3 digital stereo output with the same sampling rate.
Output from DSP operation part is converted into I^2S mode digital output or S/PDIF mode digital serial output.
System clock uses master clock input from MCLK terminal, makes 512fs multiplying clock in PLL block. Moreover, 256fs synchronous clock can be output from terminal SYSCLKO, and the clock is supplied to external DAC or D class SP amplifier.

SPDIFO and output data selection of SDATAO1 and SDATAO2 should unify the DSP processing after (post) or processing before (pre) with all outputs.

2-1. S-P conversion1 input data selection(SEL1)

Default = 0

Select Address	Value	Operating Description
&h03 [0]	0	Input data from SDATA1
	1	Input data from SDATA2

2-2. S-P conversion2 input data selection(SEL1)

Default = 0

Select Address	Value	Operating Description
&h03 [4]	0	Input data from SDATA1
	1	Input data from SDATA2

2-3. Output data selection(SEL2) to P-S conversion1 (SDATAO1 Terminal)

Default = 0

Select Address	Value	Operating Description
&h04 [1 : 0]	0	Main data output after DSP is processed.
	1	Sub data output after DSP is processed.
	2	Main data output before DSP is processed.
	3	Sub data output before DSP is processed.

2-4. Output data selection(SEL2) to P-S conversion2 (SDATAO2 Terminal)

Default = 0

Select Address	Value	Operating Description
&h04 [5 : 4]	0	Sub data output after DSP is processed.
	1	Main data output after DSP is processed.
	2	Sub data output before DSP is processed.
	3	Main data output before DSP is processed.

2-5. SPDIFO Terminal output data selection（SEL2）

Default = 0

Select Address	Value	Operating Description
&h05 [1 : 0]	0	Main data output after DSP is processed.
	1	Sub data output after DSP is processed.
	2	Main data output before DSP is processed.
	3	Sub data output before DSP is processed.

2-6. System clock selection（SEL3）

Select the DSP clock supplied to S-P conversion1、S-P conversion2、DSP、P-S conversion1、P-S conversion2、S/PDIF output part.

Default = 0

Select Address	Value	Operating Description
&h08 [5 : 4]	0	Chose the input from a MCLK terminal as a clock.
	1	Chose the PLL output as a clock.
	2	Chose the input from a SDATA2terminal as a clock. (used for IC test).
	3	

After power on or reset released, system block selection uses clock(even if not 512fs is ok) input from terminal MCLK to receive I2C command and initialize BU9414. Then set the dividing frequency ratio of PLL block (mclk_div, pll_div) that is suitable for the clock frequency from terminal MCLK , when PLL_512fs clock from PLL is steady, set &h08 = 10h.

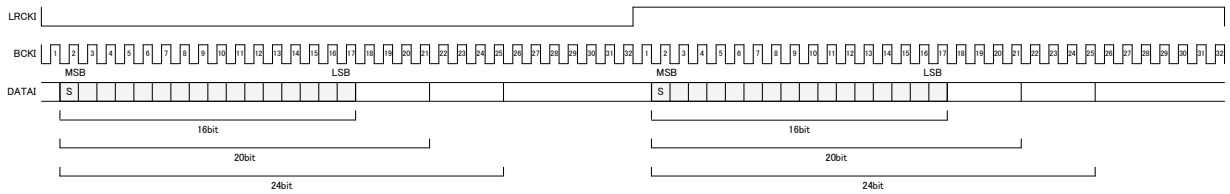
2-7. Dividing frequency ratio setting of PLL block which corresponding to input clock from terminal MCLK

Sampling rate of input clock	Setting of mclk_div &hF3	Setting of pll_div &hF5	PLL initialization &hF6
512fs（24.576MHz、fs=48kHz）	10h	01h	00h
256fs（12.288MHz、fs=48kHz）	08h	01h	00h
128fs（6.144MHz、fs=48kHz）	04h	01h	00h

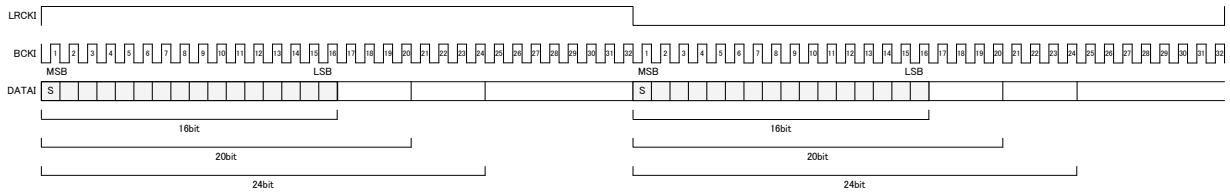
3. S-P Conversion 1, S-P Conversion 2

BU9414FV has two serial-parallel conversion circuits. （S-P conversion 1, S-P conversion 2）
S-P conversion 1 & 2 receives the audio data of three-wire serial input from terminal and converts it into parallel data.
They select the inputs from LRCKI (2pin), BCKI (40pin), SDATA1 (3pin), and SDATA2(4pin).
Input format has IIS method, left-justified method and right-justified method. Moreover, for bit clock frequency, 64fs or 48fs can be selected, and when 48fs is selected, the input format becomes the fixed right-justification. In addition, 16bit, 20bit and 24bit inputs can be selected respectively.
Timing chart of each transmission method is shown in the diagram below.

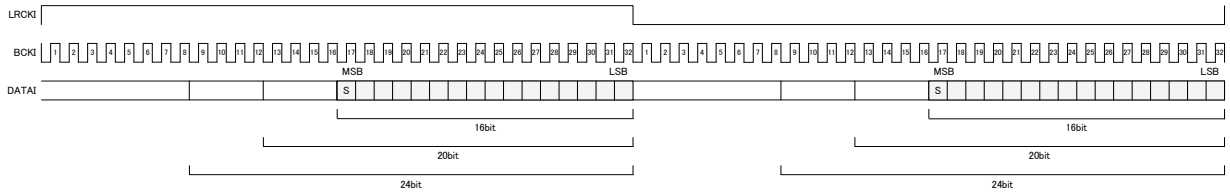
IIS method



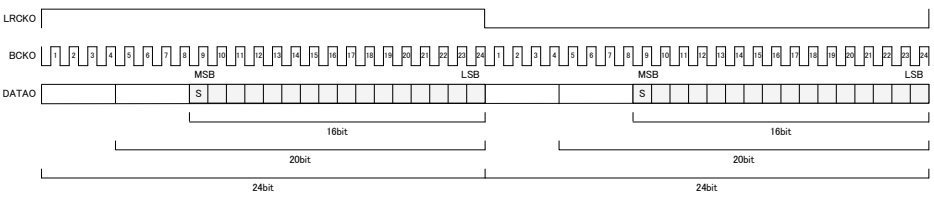
Left-justified method



Right-justified method



48fs



3-1. Three-wire serial input's bit clock frequency setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1, S-Pconversion2 &h0B [4]	0	64fs method
	1	48fs method

3-2. Three-wire serial input's format setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1 &h0B [3 : 2]	0	IIS method
S-P conversion2 &h0C [3 : 2]	1	left-justified method
	2	right-justified method

3-3. Three-wire serial input's data bit width setting

Default = 0

Select Address	Value	Operational explanation
S-P conversion1 &h0B [1 : 0]	0	16 bit
S-P conversion2 &h0C [1 : 0]	1	20 bit
	2	24 bit

4. Digital sound processing（DSP）

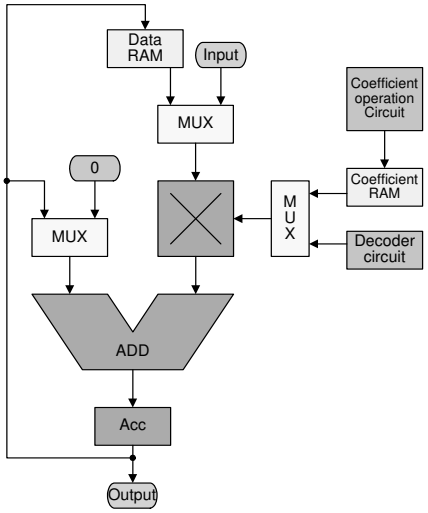
BU9414FV's Digital Sound Processing（DSP） consists of special hardware most suitable to Thin TV.

BU9414FV uses this special DSP to perform the following processing.

Prescaler, DC Cut HPF, Channel Mixer, P^2Volume（Perfect Pure Volume）, BASS, MIDDLE, TREBLE, Pseudo Stereo, Surround, P^2Bass, Pseudo Bass, P^2Treble, 7 Band・Parametric Equalizer, Master Volume, L/R Balance, PostScaler, Output Clipper.

DSP Outline and Signal Flow

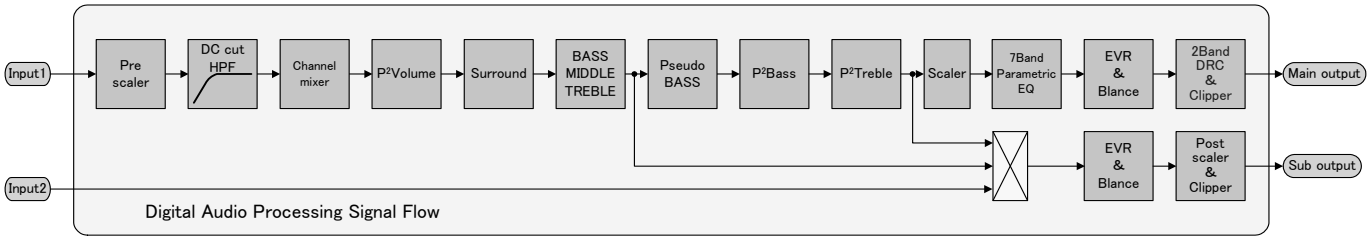
Data width：	32 bit （DATA RAM）
Machine cycle：	40.7ns （512fs, fs=48kHz）
Multiplier：	32×24 → 56 bit
Adder：	32＋32 → 32 bit
Data RAM：	256×32 bit
Coefficient RAM：	128×24 bit
Sampling frequency：	fs=48kHz
Master clock：	512fs （24.576MHz, fs=48kHz）



Digital signal from 16bit to 24bit is inputted to DSP,

and it is extended by +8bit（+42dB） as overflow margin on the upper side.

The clip process is performed in DSP when the process exceeding this range is performed.



4-1. Prescaler

When digital signal is inputted to audio DSP, if the level is full scale input and the process of surround or equalizer is performed, then it overflows, therefore the input gain is adjusted by prescaler.

Adjustable range is +24dB to -103dB and can be set by the step of 0.5dB.

Prescaler does not incorporate the smooth transition function.

Default = 30h

Select Address	Operational explanation
&h20 [7 : 0]	command / gain 00 / +24dB 01 / +23.5dB ⋮ / ⋮ 30 / 0dB 31 / −0.5dB 32 / −1dB ⋮ / ⋮ FE / −103dB FF / −∞

4-2. DC Cut HPF

The DC offset component of digital signal inputted to the audio DSP is cut by this HPF.

The cutoff frequency fc of HPF is 1Hz, and first-order filter is used.

Default = 0

Select Address	Value	Operational explanation
&h21 [0]	0	Not using the DC Cut HPF
	1	Using the DC Cut HPF

4-3. Channel mixer

It performs the setting of mixing the sounds of left channel & right channel of digital signal inputted to the audio DSP.

Here the stereo signal is made to be monaural.

The data inputted to Lch of DSP is mixed.

Default = 0

Select Address	Value	Operational explanation
&h22 [7 : 6]	0	Inputting the Lch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Rch data

The data inputted to Rch of DSP is mixed.

Default = 0

Select Address	Value	Operational explanation
&h22 [5 : 4]	0	Inputting the Rch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of（Lch + Rch） / 2
	3	Inputting the Lch data

4-4. P^2Volume （Perfect Pure Volume）

There are some scenes in which sound suddenly becomes large like plosive sound in TV Commercial or Movie.

P^2Volume function automatically controls the volume and adjusts the output level.

In addition, it also adjusts in such a way that a whispery sound can be heard easily.

P^2Volume function operates in the fields of (1), (2) & (3) divided according to input level.

(1) at the time of $V_{I\,inf}(-\infty) \sim V_{I\,min}$

Noise is prevented from being lifted by P^2Volume function.

(2) When input level is over $V_{I\,min}$ and output is below V_{Omax}

$V_O = V_I + \alpha$

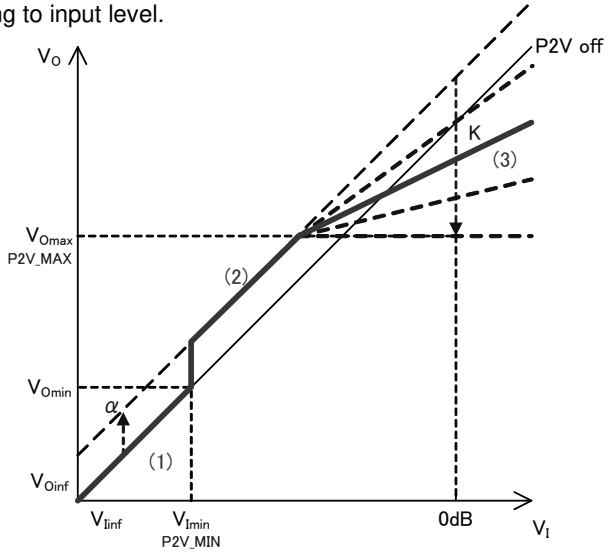
α： Lifting the Whole output level by the offset value α

(3) When output level V_O exceeds V_{Omax}

$V_O = K \cdot V_I + \alpha$

K： Slope for suppressing of D range （P2V_K）

It is also possible to set an output level constant.



Selection of using the P^2Volume function.

Default = 0

Select Address	Value	Operational explanation
&h33 [7]	0	Not using the P^2Volume function
	1	Using the P^2Volume function

Setting of $V_{I\,min}$

In order to cancel that noise etc. is lifted by P^2Volume, the P2V_MIN sets the minimum level at which (to the minimum) the P^2Volume functions.

Default = 00h

Select Address	Operational explanation
&h34 [4:0]	command / gain / command / gain / command / gain / コマンド値 / ゲイン 00 / −∞ / 08 / −44dB / 10 / −60dB / 18 / −76dB 01 / −30dB / 09 / −46dB / 11 / −62dB / 19 / −78dB 02 / −32dB / 0A / −48dB / 12 / −64dB / 1A / −80dB 03 / −34dB / 0B / −50dB / 13 / −66dB / 1B / −82dB 04 / −36dB / 0C / −52dB / 14 / −68dB / 1C / −84dB 05 / −38dB / 0D / −54dB / 15 / −70dB / 1D / −86dB 06 / −40dB / 0E / −56dB / 16 / −72dB / 1E / −88dB 07 / −42dB / 0F / −58dB / 17 / −74dB / 1F / −90dB

Setting of V_{Omax}

P2V_MAX sets the output suppression level. It represents the output level V_{Omax} at the time of input level V_I = 0dB in the case of setting of P2V_K = “0h”（slope is 0）.

Default = 00h

Select Address	Operational explanation
&h35 [4:0]	command / gain / command / gain / command / gain / command / gain 00 / 0dB / 08 / −8dB / 10 / −16dB / 18 / −24dB 01 / −1dB / 09 / −9dB / 11 / −17dB / 19 / −25dB 02 / −2dB / 0A / −10dB / 12 / −18dB / 1A / −26dB 03 / −3dB / 0B / −11dB / 13 / −19dB / 1B / −27dB 04 / −4dB / 0C / −12dB / 14 / −20dB / 1C / −28dB 05 / −5dB / 0D / −13dB / 15 / −21dB / 1D / −29dB 06 / −6dB / 0E / −14dB / 16 / −22dB / 1E / −30dB 07 / −7dB / 0F / −15dB / 17 / −23dB / 1F / −

Setting of K

P2V_K sets the slop of D range. It sets the P2V_MAX = “1Eh”（-30dB） and represents the output level V_{Omax} at the time of input level V_I = 0dB.

Default = 00h

Select Address	Operational explanation
&h36 [3:0]	

command	gain	comman	gain
0	−30dB	8	−14dB
1	−28dB	9	−12dB
2	−26dB	A	−10dB
3	−24dB	B	−8dB
4	−22dB	C	−6dB
5	−20dB	D	−4dB
6	−18dB	E	−2dB
7	−16dB	F	0dB

Setting of α

P2V_OFS makes small voice easy to be heard because the whole output level is lifted.

Default = 00h

Select Address	Operational explanation
&h37 [4:0]	

command	gain	command	gain	command	gain	command	gain
00	0dB	08	+8dB	10	+16dB	18	+24dB
01	+1dB	09	+9dB	11	+17dB	19	−
02	+2dB	0A	+10dB	12	+18dB	1A	−
03	+3dB	0B	+11dB	13	+19dB	1B	−
04	+4dB	0C	+12dB	14	+20dB	1C	−
05	+5dB	0D	+13dB	15	+21dB	1D	−
06	+6dB	0E	+14dB	16	+22dB	1E	−
07	+7dB	0F	+15dB	17	+23dB	1F	−

Setting 1 of transition time at the time of attack

A_RATE is the setting of transition time when the state of P^2Volume function is transited to (2)→(3).

Default = 0

Select Address	Operational explanation
&h38 [6:4]	

command	A_RATE time	command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

Setting 1 of transition time at the time of recovery

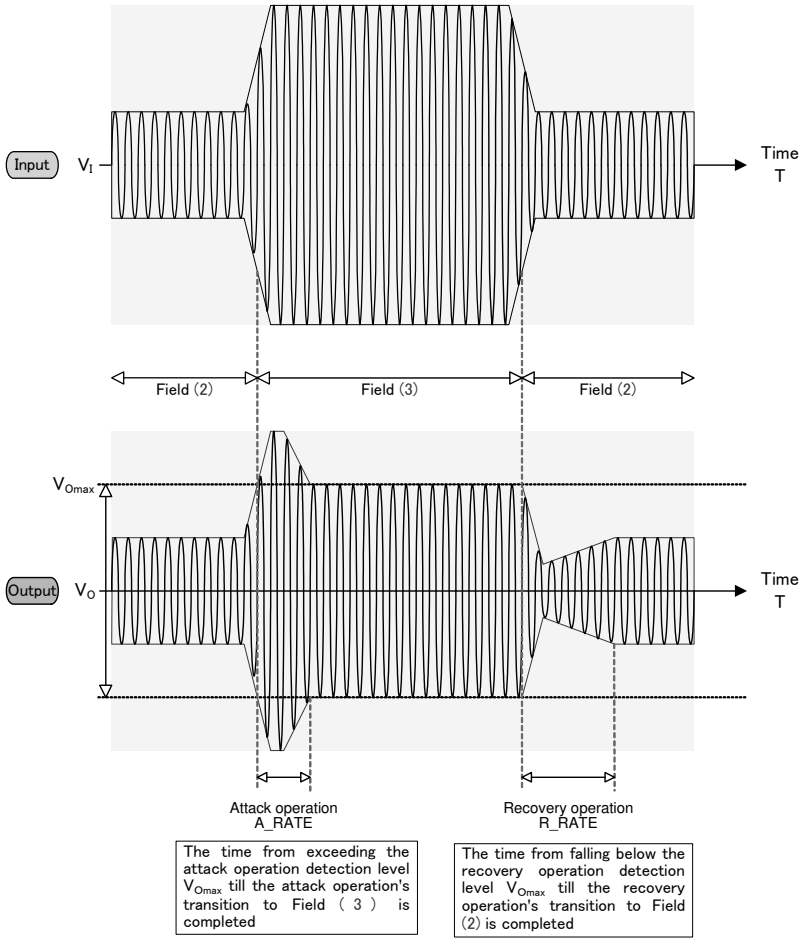
R_RATE is the setting of transition time when the state of P^2Volume function is transited to (3)→(2).

Default = 0h

Select Address	Operational explanation
&h38 [3:0]	

command	R_RATE time	command	R_RATE time
0	0.25s	8	3s
1	0.5s	9	4s
2	0.75s	A	5s
3	1s	B	6s
4	1.25s	C	7s
5	1.5s	D	8s
6	2s	E	9s
7	2.5s	F	10s

Explanation of A_RATE,R_RATE(field transition of (2)<->(3))



Setting 1 of attack detection time

A_TIME is the setting of the initiation of P^2Volume function's transition operation. If output level at the time of transiting to (2)→(3) continues for more then A_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

Select Address	Operational explanation

command	A_TIME	command	A_TIME
0	0.5ms	4	3ms
1	1ms	5	4ms
2	1.5ms	6	5ms
3	2ms	7	6ms

Setting 1 of recovery detection time

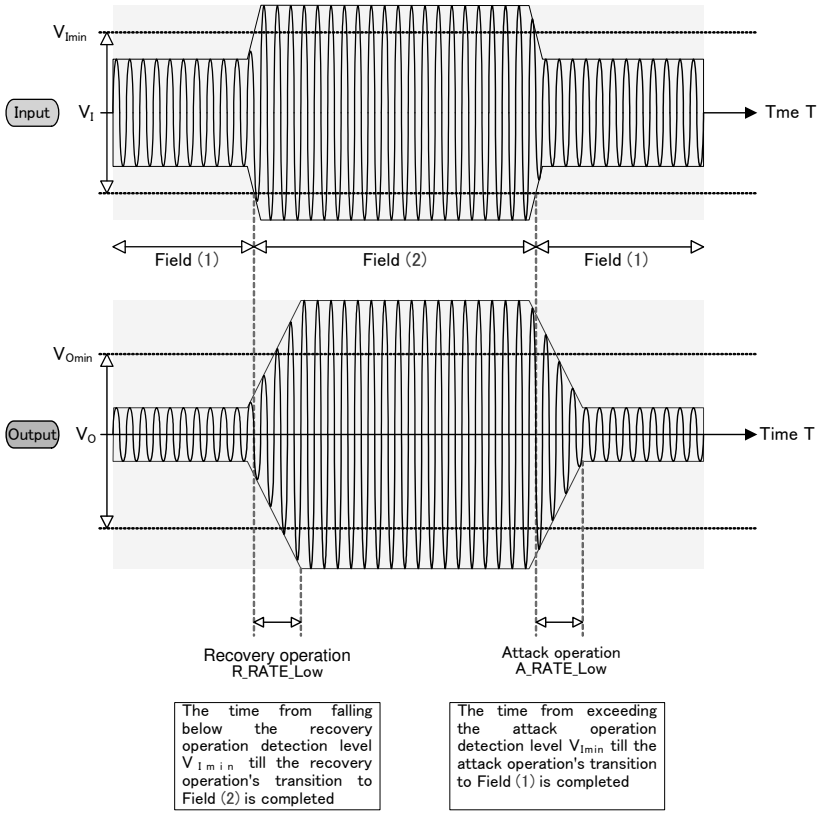
R_TIME is the setting of the initiation of P^2Volume function's transition operation. If output level at the time of transiting to (3)→(2) continues for more then R_TIME time in succession, then the state transition of P^2Volume is started.

Default = 0

Select Address	Operational explanation

command	R_TIME	command	R_TIME
0	50ms	4	300ms
1	100ms	5	400ms
2	150ms	6	500ms
3	200ms	7	600ms

Explanation of A_RATE_Low,R_RATE_Low(field transition of (1)<->(2))



Setting 2 of the transition time at the time of attack

A_RATE_LOW is the setting of transition time when the state of P^{2}Volume function is transited to (2)→(1).

Default = 0

Select Address	Operational explanation

Command	A_RATE_LOW Time	Command	A_RATE_LOW Time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

&h3A [6:4]

Setting 2 of the transition time at the time of recovery

R_RATE_LOW is the setting of transition time when the state of P^{2}Volume function is transited to (1)→(2).

Default = 0

Select Address	Operational explanation

Command	R_RATE_LOW Time	Command	R_RATE_LOW Time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

&h3A [2:0]

Setting 2 of attack recovery detection time

A_TIME_LOW is the setting of the initiation of P^{2}Volume function's transition operation. If the input level below A continues more than continuation A_TIME_LOW in the state of (2) or (3), state transition of P2Volume will be started toward the state of (1).

Default = 0

Select Address	Operational explanation

Command	A_TIME_LOW	Command	A_TIME_LOW
0	50ms	4	300ms
1	100ms	5	400ms
2	150ms	6	500ms
3	200ms	7	600ms

&h3B [6:4]

Setting 3 of attack recovery detection time

R_TIME_LOW is the setting of the initiation of P^{2}Volume function's transition operation. If the input level above A continues more than continuation R_TIME_LOW in the state of (1), state transition of P2Volume will be started toward the state of (2) or (3).

Default = 0

Select Address	Operational explanation
&h3B [6:4]	

Command	R_TIME_LOW	Command	R_TIME_LOW
0	0.5ms	4	3ms
1	1ms	5	4ms
2	1.5ms	6	5ms
3	2ms	7	6ms

○Scene change detection and High-speed recovery function（functioning only at the time of transition of (2)<->(3)）

P^{2}Volume function makes the P^{2}Volume also compatible with large pulse sounds (clapping of hands, fireworks & shooting etc.) in addition to normal P^{2}Volume operation. When large pulse sound is inputted, attack operation (A_RATE) or recovery operation (R_RATE) is performed at 4 or 64 times the speed of normal attack operation or recovery operation.

Selection of using the scene change detection function.

Default = 0

Select Address	Value	Operational explanation
&h3C[7]	0	Not using of pulse sound detection function
	1	Using of pulse sound detection function

Selection of operating times of Recovery Time (R_RATE) in the case of using the scene change detection function. (Operating-time selection at the time of R_RATE / scene detection) serves as a recovery time.

Default = 0

Select Address	Value Operational explanation
&h3D [1:0]	

Command	Value
0	4
1	8
2	16
3	64

Selection of scene change detection time

Default = 0

Select Address	Operational explanation
&h3C [6:4]	

Command	Time	Command	Time
0	50ms	4	300ms
1	100ms	5	400ms
2	150ms	6	500ms
3	200ms	7	600ms

Setting of operating level of scene change detection function

Operation is started by the difference between the presently detected value and the last value as a standard.

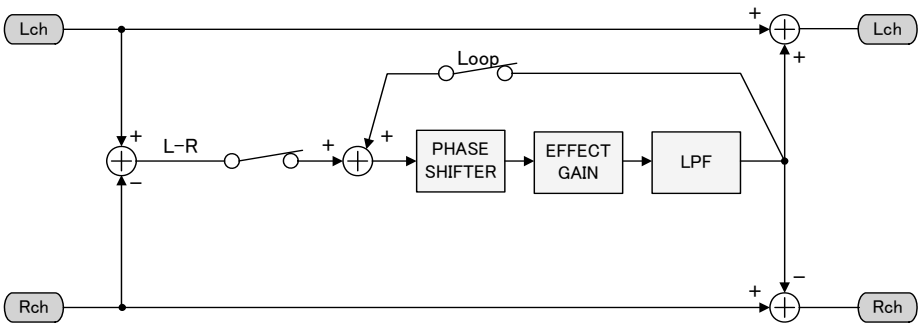
Default = 0

<table>
<tr><th>Select Address</th><th>Operational explanation</th></tr>
<tr><td>&h3C [2:0]</td><td>
<table>
<tr><th>Command</th><th>Detection level</th><th>Command</th><th>Detection level</th></tr>
<tr><td>0</td><td>Over 1.002</td><td>4</td><td>Over 0.251</td></tr>
<tr><td>1</td><td>Over 0.709</td><td>5</td><td>Over 0.178</td></tr>
<tr><td>2</td><td>Over 0.502</td><td>6</td><td>Over 0.126</td></tr>
<tr><td>3</td><td>Over 0.355</td><td>7</td><td>Over 0.089</td></tr>
</table>
</td></tr>
</table>

4-5. Surround （Matrix Surround 3D）

It realizes the Surround with little feeling of fatigue even after wide seat spot and long-time watching & listening to. It reproduces the feeling of broadening of the natural sounds in medium & high bands and realizes the sound field that do no damage to the feeling of locating of the vocal.

If loop is used, then the number of stages of phase shifter can be increased in a pseudo way.



ON/OFF of Surround function

Default = 0

Select Address	Value	Operational explanation
&h70 [7]	0	Turning the Surround effect OFF
	1	Turning the Surround effect ON

Setting of using the LOOP

Default = 0

Select Address	Value	Operational explanation
&h70 [5]	0	Not using of LOOP
	1	Using of LOOP

Setting of Surround gain

Default = Fh

Select Address	Operational explanation
&h70 [3 : 0]	

Command	Gain	Command	Gain
0	0dB	8	−8dB
1	−1dB	9	−9dB
2	−2dB	A	−10dB
3	−3dB	B	−11dB
4	−4dB	C	−12dB
5	−5dB	D	−13dB
6	−6dB	E	−14dB
7	−7dB	F	−15dB

4-6. BASS

BASS of TONE Control can use Peaking filter or Low-shelf filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F_0, Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○BASS Control

Selection of filter types

Default = 0

Select Address	Value	Operational explanation
&h40 [7]	0	Peaking filter
	1	Low-shelf filter

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h40 [6]	0	Using BASS smooth transition function
	1	Not BASS using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h40 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h40[0] command, to the coefficient RAM for smooth transition, the alteration of BASS's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [0]	0	BASS smooth transition stop
	1	BASS smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of Bass smooth transition time, from the time the BASS smooth transition start （&h4C[0] = "1"） is executed until the following command is sent. Please make sure to perform the Bass smooth transition stop（&h4C[0] = "0"） after the smooth transition is completed.

&h4D [0] and &hF4 [0] are set to H during soft transition.

(Refer to Chapter 15)

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted directly to the coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h40 [0]	0	BASS coefficient transmission stop
	1	BASS coefficient transmission start

selection of frequency（F_0）

Default = 0Eh

Select Address: &h41 [5:0]

Operational explanation

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	–
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	–
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	–

Selection of quality factor （Q）

Default = 4h

Select Address: &h42 [3:0]

Operational explanation

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address: &h43 [6:0]

Operational explanation

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

4-7. MIDDLE

MIDDLE of TONE Control uses Peaking filter.

The setting is converted, in the IC, into digital filter's coefficients （b0, b1, b2, a1, a2）by selecting the F，Q and Gain, and transmitted to coefficient RAM. The switching shock noise at the time of alteration of setting can be prevented by the smooth transition function.

○MIDDLE Control

Selection of smooth transition function

Default = 0

Select Address	Value	Operational explanation
&h44 [6]	0	Using MIDDLE smooth transition function
	1	Not MIDDLE using smooth transition function

Selection of smooth transition time

Default = 0

Select Address	Value	Operational explanation
&h44 [5:4]	0	21.4ms
	1	10.7ms
	2	5.4ms
	3	2.7ms

Setting of smooth transition start

In the case of using the smooth transition function, after being transmitted, by the &h44[0] command, to the coefficient RAM for smooth transition, the alteration of MIDDLE's coefficients is completed by using this command.

Default = 0

Select Address	Value	Operational explanation
&h4C [1]	0	MIDDLE smooth transition stop
	1	MIDDLE smooth transition start

What is necessary is the time of waiting, which is more than the time selected by the setting of MIDDLE smooth transition time, from the time the MIDDLE smooth transition start （&h4C[1] = "1"） is executed until the following command is sent. Please make sure to perform the MIDDLE smooth transition stop（&h4C[1] = "0"） after the smooth transition is completed.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted to the direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h44 [0]	0	MIDDLE coefficient transmission stop
	1	MIDDLE coefficient transmission sart