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Datasheet

USB Audio Decoder LSI Series

AAC/WMA/MP3 +SD Memory Card + iPod

BU94502Cxxx Series

Description

BU94502Cxxx series are WAV/AAC/WMA/MP3 decoder LSI which contains USB host, SD card I/F, audio DAC, system controller, regulator for internal CORE power supply.

Features

- USB2.0 Full Speed host I/F function contained.
- SD card I/F function contained.
- I^2C format I/F function contained.
- Protocol conversion from I^2C to USB HID or from USB HID to I^2C.
- MP3 decode function contained.

(Available for MPEG1, 2 and 2.5, Layer 1, 2 and 3)

- WMA decode function contained.

(Available for WMA9 standard and not available for DRM)

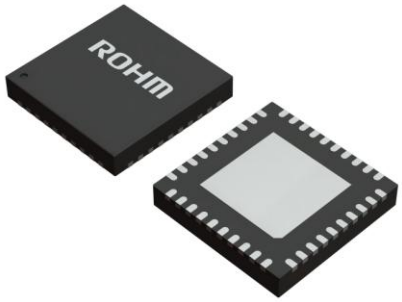
- AAC decode function contained.

(Available for MPEG4 AAC-LC and not available for DRM)

- WAV format file playing function contained.
- Sample Rate Converter contained.
- System Controller contained.
- FAT analysis function contained.
- Folder pass table making function contained.
- ID3TAG and WMATAG and AACTAG Analysis.
- Fast forward playing and fast backward playing function contained.
- Resume function contained.
- Reading a specified file data is possible from connected memory.
- LUN is selectable.
- Sound Effect function contained.
- Digital Audio Out function contained. (I^2S, EIAJ, S/PDIF)
- Audio DAC contained.
- Regulator for internal CORE power supply contained.

Package

W(Typ) x D(Typ) x H(Max)



VQFN040V6060
6.00mm x 6.00mm x 1.00mm

SQFP-T52
12.00mm x 12.00mm x 1.50mm

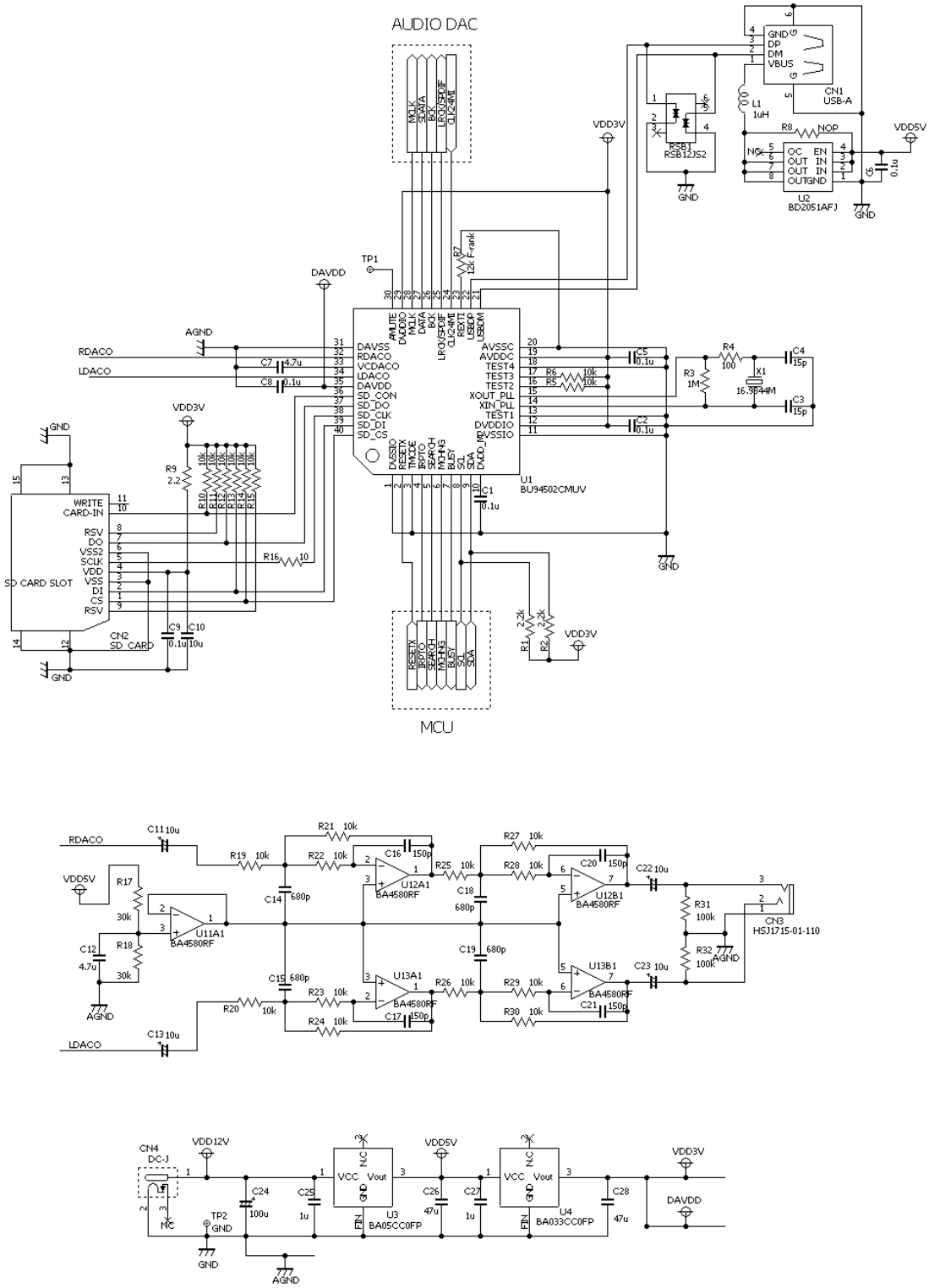
Applications

Audio products, etc

Line up

Part number	Package		Ordering part number
BU94502CMUV	VQFN040V6060	Reel of 2000	BU94502CMUV-E2
BU94502CKS2	SQFP-T52	Tray of 1000	BU94502CKS2

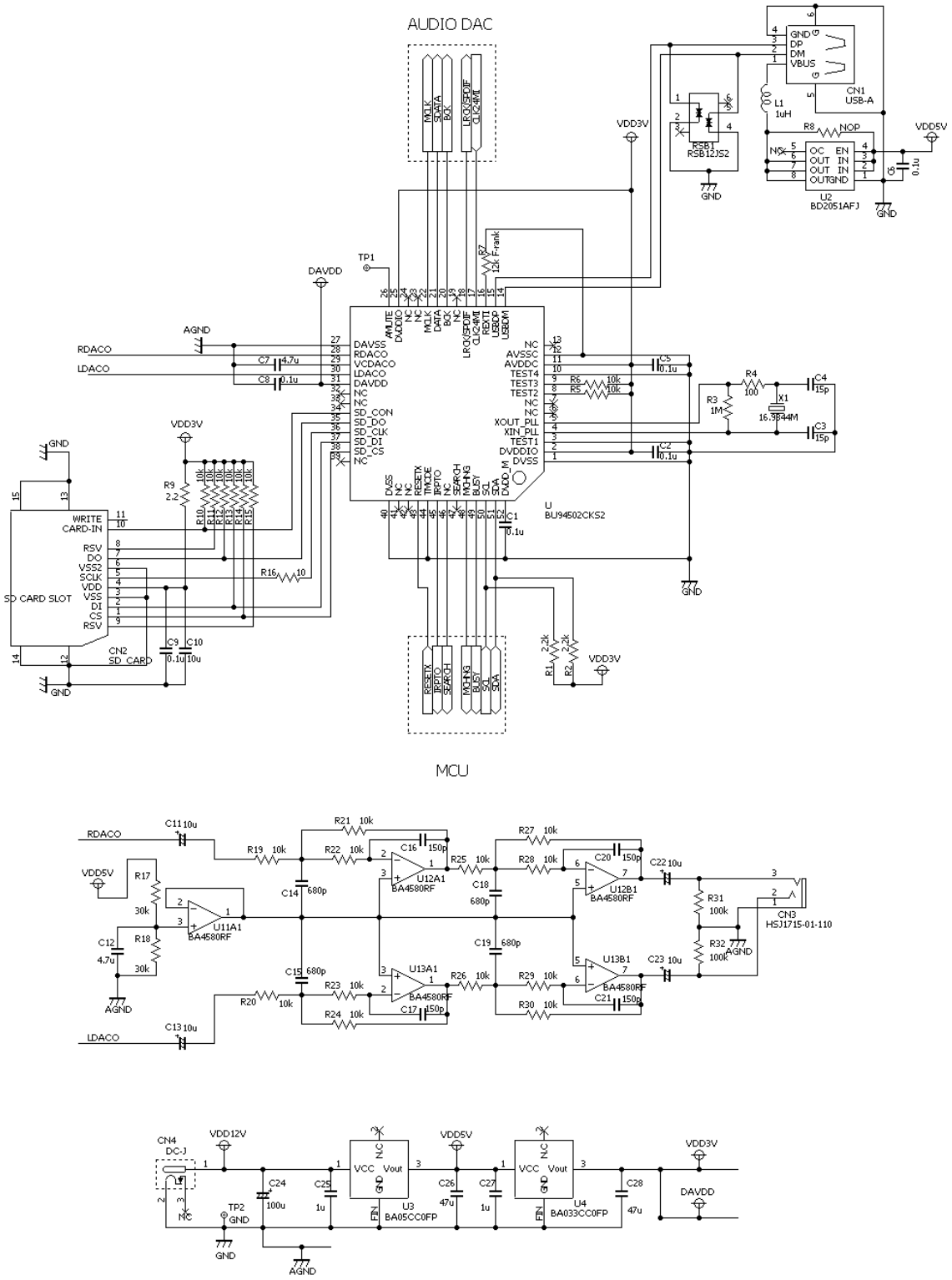
Basic circuit application diagram -part1



This LSI builds in regulator for internal CORE power supply (1.5V).
DVDD_M terminal of 10PIN connect to bypass condenser and don't connect to power supply (3.3V)
Please confirm the optimal oscillation circuit parameters applicable to your systems or products with the oscillator manufacturer in advance.
VQFN040V6060 package exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.

Figure 1. an example of connection circuit application(BU94502CMUV)

Basic circuit application diagram -part2



This LSI builds in regulator for internal CORE power supply (1.5V).
DVDD_M terminal of 52PIN connect to bypass condenser and don't connect to power supply (3.3V)
Please confirm the optimal oscillation circuit parameters applicable to your systems or products with the oscillator manufacturer in advance.

Figure 2. an example of connection circuit application(BU94502CKS2)

Difference of BU94502Cxxx Series features

Item	BU94502CMUV	BU94502CKS2
Package	VQFN040V6060	SQFP-T52
Number of pins	40pin	52pin
Power supply	3.3V (inner 1.5V regulator)	3.3V (inner 1.5V regulator)
USB Host I/F	USB Full speed(12Mbps), USB mass storage class	USB Full speed(12Mbps), USB mass storage class
SD card I/F	SPI mode SD, SDHC, MMC, mini-SDcard	SPI mode SD, SDHC, MC, mini-SDcard
Protocol conversion from I2C to USB HID or from USB HID to I2C	Supported	Supported
I^2C command I/F (Slave)	Supported	Supported
Patch cord download	Supported	Supported
Change the Setting of timeout and retry mode in USB memory or SD card mount operation	Supported	Supported
Audio line output	Supported	Supported
Digital audio output	I^2S, EIAJ, SPDIF	I^2S, EIAJ, SPDIF
Sample rate convertor	Supported	Supported
clock	16.9344MHz (Note 1)	16.9344MHz (Note 1)
Playable MP3 files	*.mp3, *.mp2, *.mp1	*.mp3, *.mp2, *.mp1
Playable WMA files	*.asf, *.wma	*.asf, *.wma
Playable AAC files	*.m4a, *.3gp, *.mp4	*.m4a, *.3gp, *.mp4
Playable WAV files	*.wav	*.wav

Block diagram

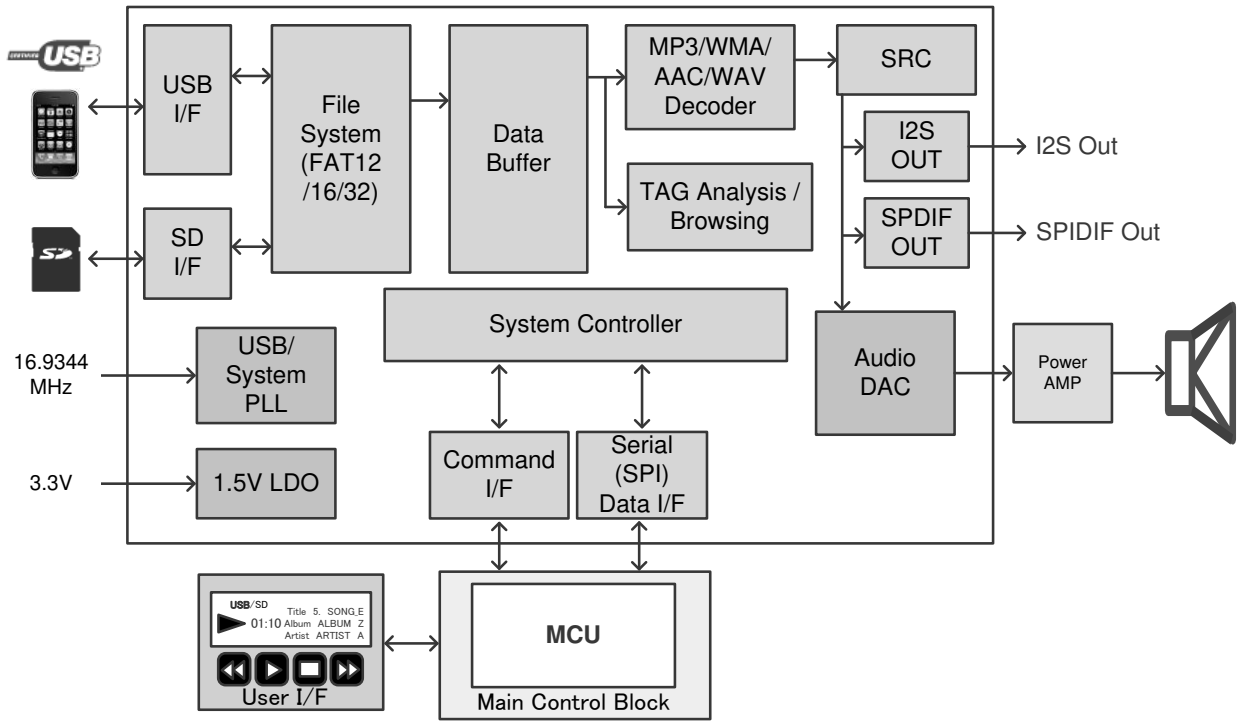


Figure 3. Block diagram

Arrangement of Terminals

BU94502CMUV

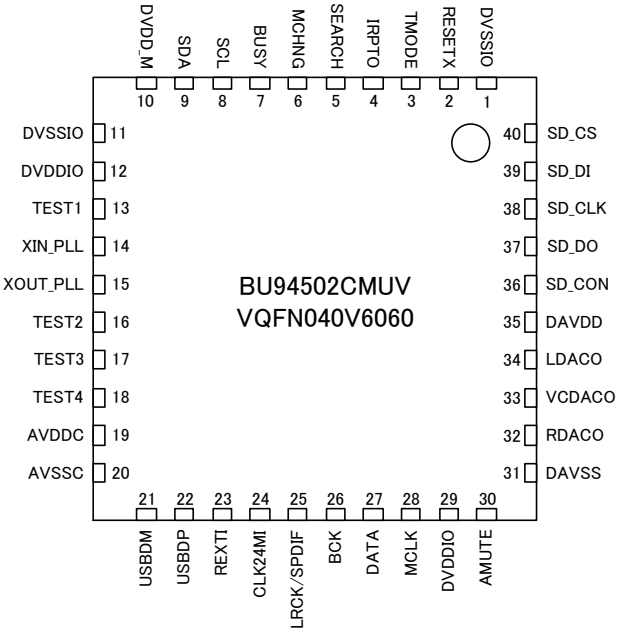


Figure 4. Arrangement of Terminals (BU94502CMUV)

BU94502CKS2

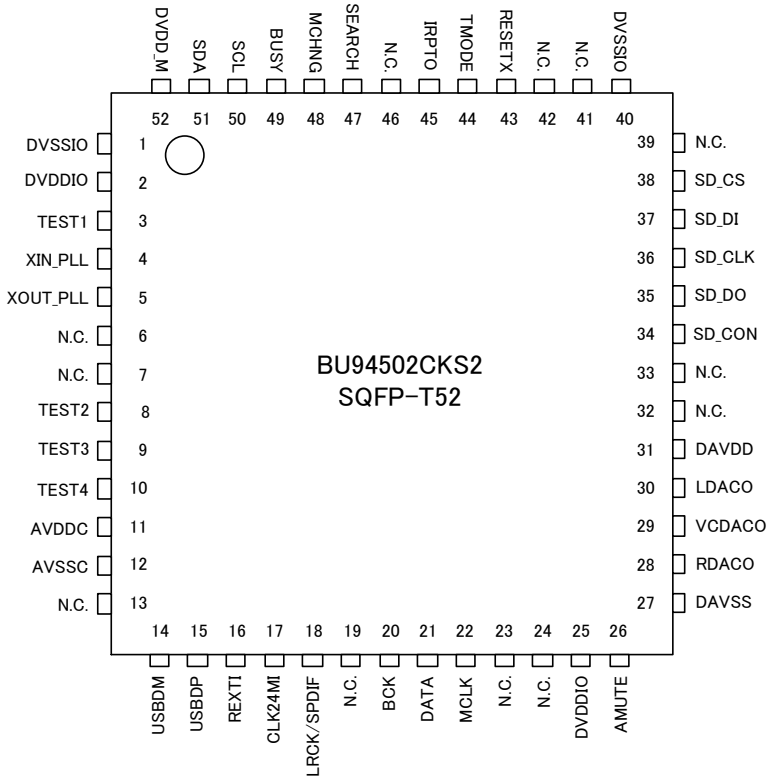


Figure 5. Arrangement of Terminals (BU94502CKS2)

Description of Terminals -part1

BU94502CMUV

No	Pin Name	IO Cir	IO	PU	Function
1	DVSSIO	—	—	—	GND terminal
2	RESETX	A	I	PU(Note 3)	H: Release RESET, L: RESET
3	TMODE	H	I	—	Test mode terminal. Connect it to GND.
4	IRPTO	B	O	—	Connection interrupt output terminal
5	SEARC	B	O	—	Search flag output terminal
6	MCHNG	B	O	—	File play end flag output terminal
7	BUSY	B	O	—	Command analysis BUSY output temrinal
8	SCL	I	I	(Note 2)	I^2C slave clock input terminal
9	SDA	I	I/O	(Note 2)	I^2C slave data I/O terminal
10	DVDD_M	—	—	—	CORE power (VDD2) monitor terminal. Connect it to bypass capacitor.
11	DVSSIO	—	—	—	GND terminal
12	DVDDIO	—	—	—	IO power (VDD1) terminal
13	TEST1	—	I	—	Test mode terminal. Connect it to GND.
14	XIN_PLL	E	I	—	X'tal (16.9344MHz) connection input terminal.
15	XOUT_PLL	E	O	—	X'tal (16.9344MHz) connection output terminal.
16	TEST2	H	I	PU	Pull it up at VDD1 power.
17	TEST3	H	I	PU	Pull it up at VDD1 power.
18	TEST4	H	I	PU (Note 1) (Note 3)	Test mode terminal. Connect it to GND.
19	AVDDC	—	—	—	USB Power supply (VDD1) terminal
20	AVSSC	—	—	—	USB GND terminal
21	USB_DM	C	I/O	—	USB D−I/O terminal
22	USB_DP	C	I/O	—	USB D+ I/O terminal
23	REXTI	D	O	—	USB bias resistor (12kΩ) connecting terminal Arrange the resistance of 12kΩ near PIN, and wiring on the PIN side doesn't cross with other signal lines.
24	CLK24MI	B	I/O	PU(Note 3)	24MHz clock input terminal at SRC through mode
25	LRCK/SPDIF	B	O	—	Digital Audio channel clock or SPDIF output terminal
26	BCK	B	O	—	Digital Audio bit clock output terminal
27	DATA	B	O	—	Digital Audio data output terminal
28	MCLK	B	O	—	Audio Master clock (12.288MHz/16.9344MHz) output terminal
29	DVDDIO	—	—	—	IO Power supply (VDD1) terminal
30	AMUTE	G	O	—	Audio Mute output terminal (H : MUTE OFF, L : MUTE ON)
31	DAVSS	—	—	—	Audio DAC GND terminal
32	RDACO	F	O	—	Audio DAC Rch Line output terminal
33	VCDACO	J	O	—	Audio DAC Reference voltage output terminal
34	LDACO	F	O	—	Audio DAC Lch Line output terminal
35	DAVDD	B	—	—	Audio DAC Power supply (VDD1) terminal
36	SD_CON	B	I	PU(Note 3)	SD card Connect terminal
37	SD_DO	B	I	—	SD card Data In terminal
38	SD_CLK	B	O	—	SD card Clock terminal
39	SD_DI	B	O	—	SD card Data Out terminal
40	SD_CS	B	O	—	SD card Chip select terminal

(Note 1) Pull-Up turns OFF when L is input.
(Note 2) An external pull-up resistor is required because of Open Drain IO
(Note 3) please input L level directly without resistance when you input L to the terminal with Pull-Up (about 33 kΩ)

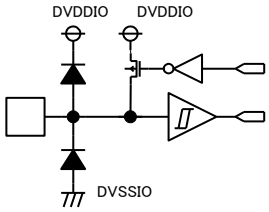
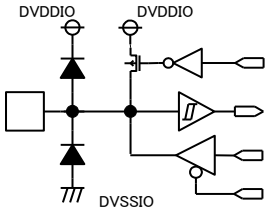
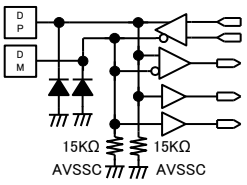
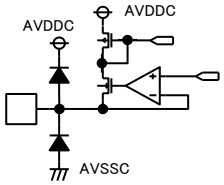
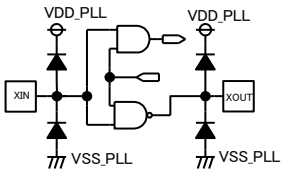
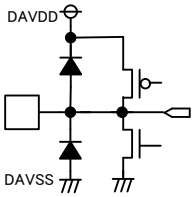
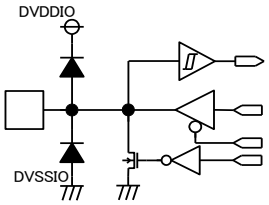
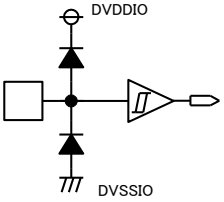
Description of Terminals -part2

BU94502CKS2

No	Pin Name	IO Cir	IO	PU	Function
1	DVSSIO	—	—	—	GND terminal
2	DVDDIO	—	—	—	IO power (VDD1) terminal
3	TEST1	—	I	—	Test mode terminal. Connect it to GND.
4	XIN_PLL	E	I	—	X'tal (16.9344MHz) connection input terminal.
5	XOUT_PLL	E	O	—	X'tal (16.9344MHz) connection output terminal.
6	N.C.	—	—	—	Non Connection
7	N.C.	—	—	—	Non Connection
8	TEST2	H	I	PU	Pull it up at VDD1 power.
9	TEST3	H	I	PU	Pull it up at VDD1 power.
10	TEST4	H	I	PU (Note 1) (Note 3)	Test mode terminal. Connect it to GND.
11	AVDDC	—	—	—	USB Power supply (VDD1) terminal
12	AVSSC	—	—	—	USB GND terminal
13	N.C.	—	—	—	Non Connection
14	USB_DM	C	I/O	—	USB D−I/O terminal
15	USB_DP	C	I/O	—	USB D+ I/O terminal
16	REXTI	D	O	—	USB bias resistor (12kΩ) connecting terminal Arrange the resistance of 12kΩ near PIN, and wiring on the PIN side doesn't to cross with other signal lines.
17	CLK24MI	B	I	PU(Note 3)	24MHz clock input terminal at SRC through mode
18	LRCK/SPDIF	B	O	—	Digital Audio channel clock or SPDIF output terminal
19	N.C.	—	—	—	Non Connection
20	BCK	B	O	—	Digital Audio bit clock output terminal
21	DATA	B	O	—	Digital Audio data output terminal
22	MCLK	B	O	—	Audio Master clock (12.288MHz/16.9344MHz) output terminal
23	N.C.	—	—	—	Non Connection
24	N.C.	—	—	—	Non Connection
25	DVDDIO	—	—	—	IO Power supply (VDD1) terminal
26	AMUTE	G	O	—	Audio Mute output terminal (H : MUTE OFF, L : MUTE ON)
27	DAVSS	—	—	—	Audio DAC GND terminal
28	RDACO	F	O	—	Audio DAC Rch Line output terminal
29	VCDACO	J	O	—	Audio DAC Reference voltage output terminal
30	LDACO	F	O	—	Audio DAC Lch Line output terminal
31	DAVDD	B	—	—	Audio DAC Power supply (VDD1) terminal
32	N.C.	—	—	—	Non Connection
33	N.C.	—	—	—	Non Connection
34	SD_CON	B	I	PU(Note 3)	SD card Connect terminal
35	SD_DO	B	I	—	SD card Data In terminal
36	SD_CLK	B	O	—	SD card Clock terminal
37	SD_DI	B	O	—	SD card Data Out terminal
38	SD_CS	B	O	—	SD card Chip select terminal
39	N.C.	—	—	—	Non Connection
40	DVSSIO	—	—	—	GND terminal
41	N.C.	—	—	—	Non Connection
42	N.C.	—	—	—	Non Connection
43	RESETX	A	I	PU(Note 3)	H: Release RESET, L: RESET
44	TMODE	H	I	—	Test mode terminal. Connect it to GND.
45	IRPTO	B	O	—	Connection interrupt output terminal
46	N.C.	—	—	—	Non Connection
47	SEARCH	B	O	—	Search flag output terminal
48	MCHNG	B	O	—	File play end flag output terminal
49	BUSY	B	O	—	Command analysis BUSY output terminal
50	SCL	I	I	(Note 2)	I^2C slave clock input terminal
51	SDA	I	I/O	(Note 2)	I^2C slave data I/O terminal
52	DVDD_M	—	—	—	CORE power (VDD2) monitor terminal Connect it to bypass capacitor.

(Note 1) Pull-Up turns OFF when L is input.
(Note 2) An external pull-up resistor is required because of Open Drain IO
(Note 3) please input L level directly without resistance when you input L to the terminal with Pull-Up (about 33 kΩ)

Terminal equivalent circuit diagram

A	B	C	D
			
E	**F**	**G**	**H**
			
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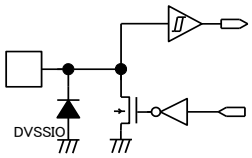	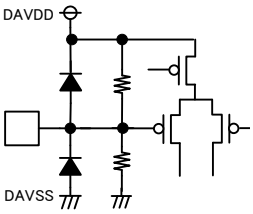		

Description of each block's movement -part1

1. USB host interface

- Builds in the USB Full speed (12Mbps) HOST control function.
- Supports the USB mass storage class.
- Converts the protocol from I^2C to USB (HID) or vice versa during communications with the master microcomputer.*
- Builds in isochronous transmission functions up to 192byte/Frame. *
- Builds in the interrupt IN transfer function. *
- Doesn't support external HUB.
- Doesn't support MTP.

*These functions are available for a device having two or more configurations.

2. SD card interface

- Supports the SPI mode.
- Supports SDHC memory cards.
- Supports MMC, mini-SD and micro-SD cards.
- Does not support CPRM.

3. I^2C command interface (Slave I/F)

- Communicates with the master microcomputer using the I^2C interface format.
- Operates as I^2C slave I/F.
- Supports the standard mode (100kbps) and the fast mode (400kbps).
- Supports 7-bit addresses.

4. Audio output

- Supports audio line outputs from built-in 1bit-DAC.
- Builds in the digital soft mute function. *
- Supports digital audio outputs of the I^2S format, the EIAJ format and those and the digital audio interface (SPDIF).
- Builds in sound effects including POPS, JAZZ, ROCK, CLASSIC, R&B and Bass Boost. *

*This is available for audio line outputs only.

5. Sample rate converter

- Converts all support sample rates to 44.1 kHz based on the polyphase calculation.
- Selection of sample rate converter ON / OFF is possible by the command configuration.

* Supports only digital audio outputs of the I^2S and EIAJ format and

- When sample rate converter is used in off, enter the clock of 24.576 MHz synchronizing with the clock of 16.9344 MHz (enter XIN_PLL terminal) to the CLK24MI terminal.

6. System controller

- Control all operations including interface control to the master microcomputer, USB device access, SD card access, FAT analysis, sort function, decoding, encoding and audio output.

7. FAT analysis

Supports FAT32, FAT16 and FAT12 file system.
Supports VFAT (long file name).
Supports multi-partition up to 1 partition.
Supports multi-drive up to 1 drive.
Supports changeover of LUN (Logical Unit Number) and possible that Test Unit Ready of other LUN is confirmed during the playback.
Supports playable folder hierarchies up to 16 hierarchies whose full path including the file name is within 260 characters.
Supports playable file extension of *.wav for WAV files.
Supports playable file extensions of *.m4a, *.3gp and *.mp4 for AAC files.
Supports playable file extensions of *.asf and *.wma for WMA files.
Supports playable file extensions of *.mp3, *.mp2 and*.mp1 for MP3 files. For *.mp2 and *.mp1, the function allows you to select whether to play. Does not extinguish between upper case letters and lower case letters of file extensions.
Up to 256 folders and 256 files can be sorted and played in the order of UNICODE when sorting functional effective.
Can obtain 5 file names ahead from current music file.
Can obtain a folder name or file name within 128 bytes.
Supports 512, 1024, 2048 and 4096 bytes per sector.
Playable file size up to 2G-1 byte. A file over 2Gbyte is recognized as a playable file, too. But, it is for 2Gbyte -1byte that it can play.
Supports the device size up to FAT specification (2T byte).

Description of each block's movement -part2

8. Control from master microcomputer (little endian order)

Can control from the master microcomputer using the I^2C interface.

Controllable using commands of play, pause, stop, tune skip, tune forward, folder move, device change, volume setting, repeat change, random play, digital audio output setting, sound effect setting and etc.

Can read information on internal status during play or stop, folder number, file number within the folder, play time, total number of folders, total number of files, name of folder being played, name of file being played and TAG (title, artist, album, genre), and etc.

9. MP3 decoder

- Supports MPEG audio 1, 2 and 2.5.
- Supports Layer1, 2 and 3.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k, 12 k, 24 k and 48 kHz.
- Supports bit rate of 8 to 320 kbps and VBR (Variable Bit Rate). *Excluding the free format
- Supports ID3TAG V1.0, V.1, 1, V2.2, V2.3 and V2.4.
  (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)

10. WMA decoder

- Supports Windows Media Audio 9 standard.
- Not supports DRM files.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k and 48 kHz.
- Supports bit rate of 5 to 384 kbps and VBR (Variable Bit Rate).
- Supports WMA-TAG.
- (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)

11. AAC decoder

- Supports MPEG4 AAC-LC (Audio stream).
- Based on 3GPP TS 26.244 and iTunes.
- Supports File Type of m4a, mp4 and 3gpX. (X stands for any numeric value.)
- Not supports DRM files.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k, 12 k, 24 k and 48 kHz.
- Supports bit rate of 8 to 320kbps and VBR (Variable Bit Rate).
- Supports AACTAG (iTunes Meta-data and 3GP Meta-data).
  (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)
  *For files other than those encoded by iTunes, sound interruption may occur when skipping or forwarding to the next tune if streams such as gaps and video data are contained in the file.

12. WAV play

- Supports WAV format.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k, 12 k, 24 k and 48 kHz.
- Supports 16-bit PCM data.
- Supports RIFF TAG.
  (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)

13. Repeat and random play

- Supports repeat within the memory, repeat within folder and repeat with single tune.
- Supports random play in the whole memory or the playing Folder.
- Can select auto-play of next music or stop playing at the end of current music playing.

14. Read from files within memory

- Can read the data from specified file stored in the specified folder within the memory.

Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage(Analog, I/O)	VDD1MAX	-0.3 to 4.5	V	DVDDIO, DAVDD, AVDDC
Input voltage	VIN	-0.3 to VDD1 + 0.3	V	
Storage temperature range	TSTG	-55 to 125	˚C	
Operating temperature range	TOPR	-40 to 85	˚C	
VQFN040V6060 Package Power dissipation (Note 1)	PD1	800	mW	BU94502CMUV
SQFP-T52 Package Power dissipation (Note 1)	PD2	850	mW	BU94502CKS2

(Note 1) : 74.2mm × 74.2mm × 1.6mm, FR4, 1-layer glass epoxy board (Copper area 23.69mm2)
In the case of use at Ta=25℃ or more, 8mW should be reduced per 1℃.
(Note 2) : In the case of use at Ta=25℃ or more, 8.5mW should be reduced per 1℃.

Operating conditions (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage(Analog, I/O)	VDD1	3.0 to 3.6	V	DVDDIO, DAVDD, AVDDC

Electrical characteristics

(Unless specified, Ta=25℃VDD1=3.3V, DVSS=AVSSC=VSS_PLL=DAVSS=0V, XIN_PLL=16.9344MHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
<Total >						
Circuit current (VDD1 USB1)	IDD1USB1	-	51.0	75.0	mA	When USB memory is played. (Note 1)
Circuit current (VDD1 SD1)	IDD1SD1	-	26.0	45.0	mA	When SD card is played. (Note 1)
<Digital block>						
H-Level input voltage	VIH	VDD1*0.7	—	VDD1	V	(Note 2)
L-Level input voltage	VIL	DVSS	—	VDD1*0.3	V	(Note 2)
H-Level output voltage1	VOH1	VDD1-0.4	—	VDD1	V	IOH=-1.6mA (Note 3)
L-Level output voltage1	VOL1	0	—	0.4	V	IOL=1.6mA (Note 3)
L-Level output voltage2	VOL2	0	—	0.4	V	IOL=3.6mA (Note 4)
H-Level output voltage3	VOH3	VDD1-0.4	—	VDD1	V	IOH=-0.6mA (Note 5)
L-Level output voltage3	VOL3	0	—	0.4	V	IOL=0.6mA (Note 5)
H-Level output voltage4	VOH4	VDD1-1.0	—	VDD1	V	IOH=-1.6mA (Note 6)
L-Level output voltage4	VOL4	0	—	1.0	V	IOL=1.6mA (Note 6)
<USB-HOST >						
H-Level input voltage	VIHUSB	VDD1*0.6	—	VDD1	V	(Note 7)
L-Level input voltage	VILUSB	AVSSC	—	VDD1*0.3	V	(Note 7)
Output impedance(H)	ZOH	22.0	45.0	60.0	Ω	(Note 7)
Output impedance(L)	ZOL	22.0	45.0	60.0	Ω	(Note 7)
H-Level output voltage	VOHUSB	VDD1-0.5	—	VDD1	V	(Note 7)
L-Level output voltage	VOLUSB	0	—	0.3	V	(Note 7)
Rise/Fall time	Tr/Tf	—	11	—	ns	Output capacity 50pF (Note 7)
Voltage of crossing point	VCRS	—	VDD1/2	—	V	Output capacity 50pF (Note 7)
Range of differential input	VDIFF	0.8	—	2.5	V	(Note 7)
Differential input sensitivity	VSENS	0.2	—	—	V	(Note 7)
Pull-down resistance	RPD	14.25	20.0	24.8	kΩ	(Note 7)
<Audio DAC>						
Distortion rate	THD	—	0.005	0.05	%	1kHz, 0dB, sine, (Note 8)
Dynamic range	DR	—	90	—	dB	1kHz, -60dB, sine, (Note 8)
S/N ratio	S/N	66	96	—	dB	1kHz, 0dB, A-weighted, (Note 8)
Max output level	VSMAX	0.60	0.75	—	Vrms	1kHz, 0dB, sine, (Note 8)

BU94502CMUV

(Note 1) 3.3V system I/O, Analog Power supply(VDD1), 1kHz, 0dB, sine-wave playing
(Note 2) 2, 3, 7-9, 13, 14, 16-18, 24, 36, 37 pin
(Note 3) 4-7, 24-28, 30 pin
(Note 4) 9 pin
(Note 5) 38-40 pin
(Note 6) 15 pin
(Note 7) 21, 22 pin
(Note 8) 32, 34 pin output no-load

BU94502CKS2

(Note 1) 3.3V system I/O, Analog Power supply(VDD1), 1kHz, 0dB, sine-wave playing
(Note 2) 3, 4, 8-10, 17, 34, 35, 43, 44, 49-51 pin
(Note 3) 45,47-49,17,18,20-22,26 pin
(Note 4) 51 pin
(Note 5) 36-38 pin
(Note 6) 5 pin
(Note 7) 14, 15 pin
(Note 8) 28, 30 pin output no-load

Application Information

1. Clock and Reset

Clock

Clock name	I/O	Function	Remarks
XIN_PLL	I	X'tal (16.9344MHz) connection input terminal	-
XOUT_PLL	O	X'tal (16.9344MHz) connection terminal	-

Reset

Signal name	I/O	Function	Remarks
RESETX	I	System reset input terminal	-

Please release the reset signal continue L input for more than 100 us after clock input from the oscillation I/O terminal becomes stable. (See Figure 6.)

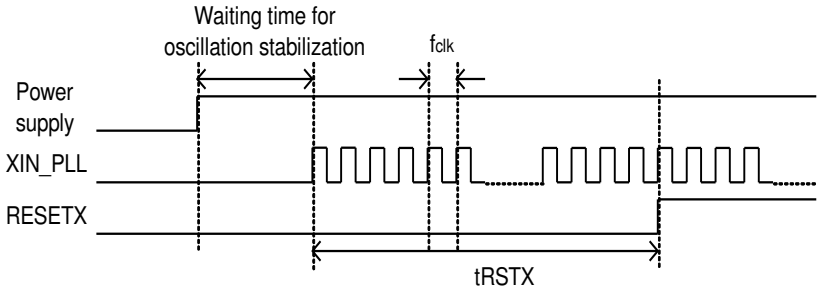

Figure 6. Reset Timing

Item	Code	Rating			Unit	Remarks
		min	typ	max		
Clock frequency	f_{CLK}	16.9302	16.9344	16.9386	MHz	-
Reset L interval	t_{RSTX}	100	-	-	us	-

2. USB I/F

USB I/O interface

Signal name	I/O	Function	Remarks
USB_DP	I/O	USB D+ I/O terminal	-
USB_DM	I/O	USB D- I/O terminal	-
REXTI	O	USB bias resistor connection terminal	Connect a resistor of 12 kΩ±1% to GND.

This interface communicates with the USB device using USB_DP and USB_DM differential signals.
REXTI terminal is used to connect to the bias resistor in the USB-PHY block.

3. SD I/F

SD memory card SPI interface

Signal name	I/O	Function	Remarks
SD_CS	O	SD chip select	-
SD_CLK	O	SPI clock	-
SD_DI	O	SPI data input	-
SD_DO	I	SPI data output	-
SD_CON	I	SD card connect detection terminal	H: Do not detect SD card connect, L: Detect SD card connect

This interface connects to the SD memory card slot to communicate with the SD memory device.
Supports the SPI mode.
Supports SD, SDHC memory cards and MMC, mini-SD and micro-SD cards.
Does not supports CPRM.
Since the SD memory card slot needs to detect the insertion status of the SD memory device, be sure to use the slot having the SD memory card insertion status detection terminal. The SD_CON terminal is pulled up within the device and detects “SD card connect” when L is input.
The SD_CON terminal is pulled up within the device and detects “SD card connect” when L is input.

3.1 Timing
(Unless specified, Ta=25℃, VDD1=3.3V, Load=20pF, 10kΩ)

Item	Symbol	Rating			Unit	Remarks
		min	typ	max		
SD_CS Setup time	Tcss	-	5	-	us	
SD_CS Hold time	Tcsh	-	15	-	us	
SD_CLK Clock Frequency	Tclk	-	13.5	-	MHz	
SD_DI Output delay	Tod	-20	-	20	ns	
SD_DO Data in Setup time	Tds	18	-	-	ns	
SD_DO Data in Hold time	Tdh	5	-	-	ns	
Output High Voltage	Voh	0.625*VDD1	-	-	V	
Output Low Voltage	Vol	-	-	0.25*VDD1	V	

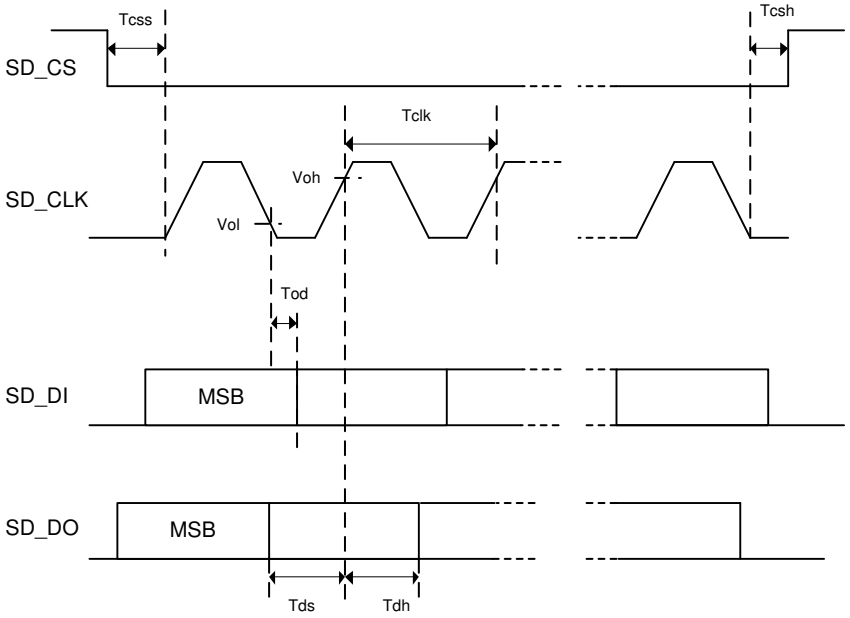

Figure 7. SPI I/F Timing

4. Audio line output

Audio line output

Signal name	I/O	Function	Remarks
LDACO	O	Lch audio line output	-
RDACO	O	Rch audio line output	-

This is a line output of decoded music data.
When a sample rate converter is used in on, data on the sample rate 48kHz, 32kHz are changed into 44.1kHz and outputted.
It turns ON when line output is selected by a command.
Figure 8. shows the relationship between audio outputs and volume steps.
The initial value is –24.1dB at power ON.

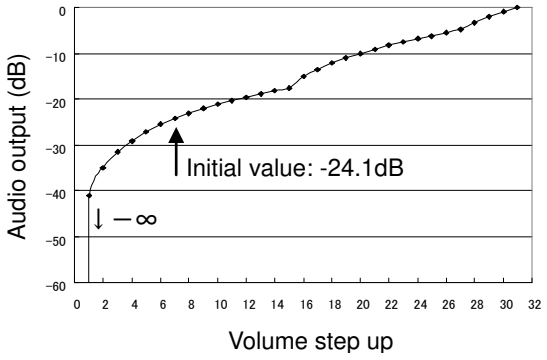

Figure 8. Volume Step Function

5. Equalizers

Selectable audio line output from 5 types of equalizers and 2 types of bus boosts, using commands.
You can use a combination of an equalizer and bus boost 1.
Even when line output is not selected, the equalizer setting is valid. However, for digital output, the equalizer cannot change the sound quality.
Figure 9. - Figure 14.show frequency characteristics of each filter.
Clipping may occur by the combination of volume and equalizer setting.

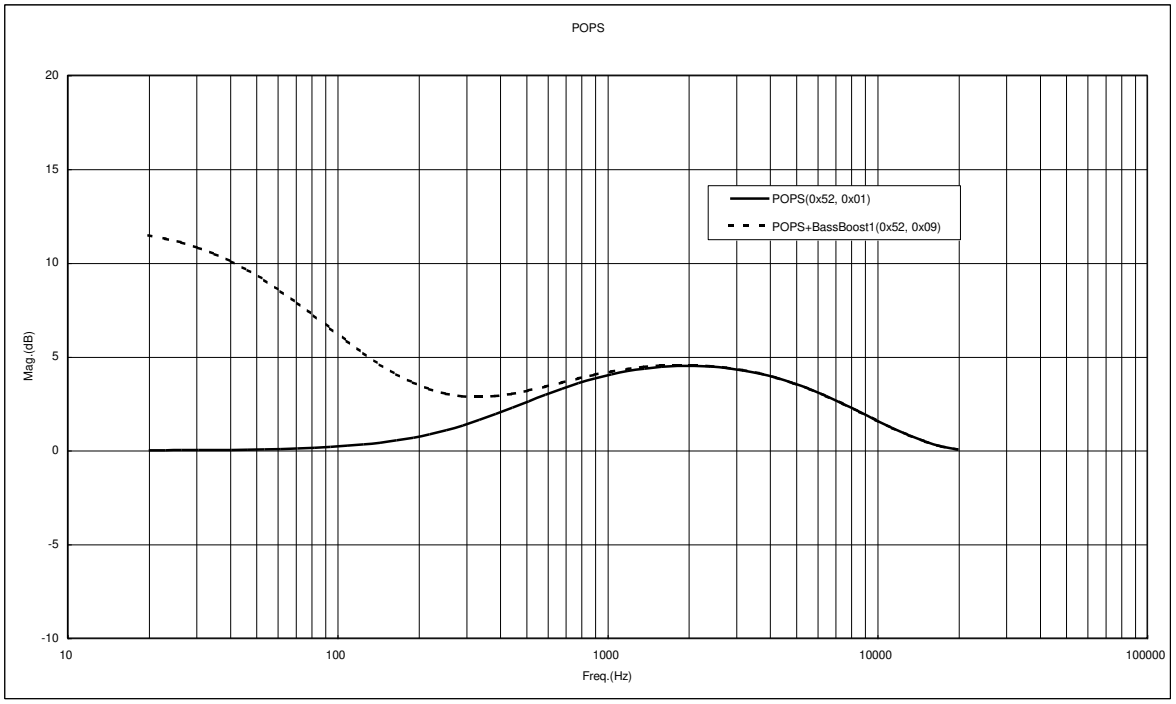

Figure 9. POPS Frequency Characteristics

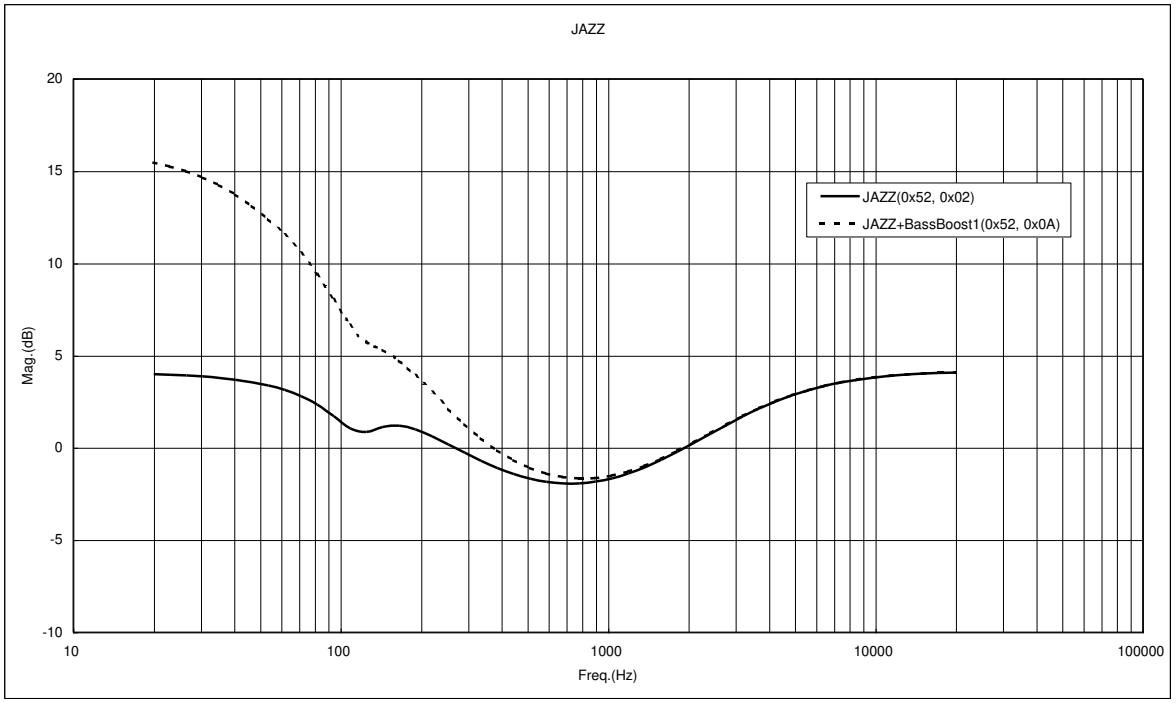

Figure 10. JAZZ Frequency Characteristics

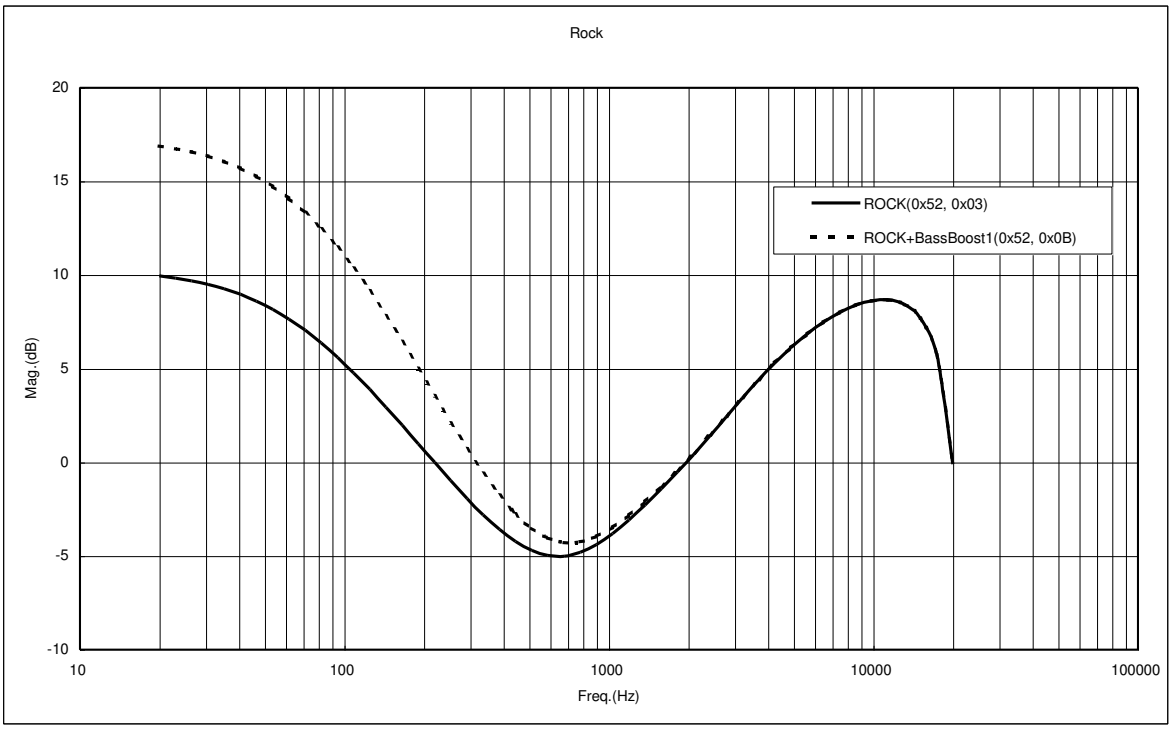

Figure 11. ROCK Frequency Characteristics

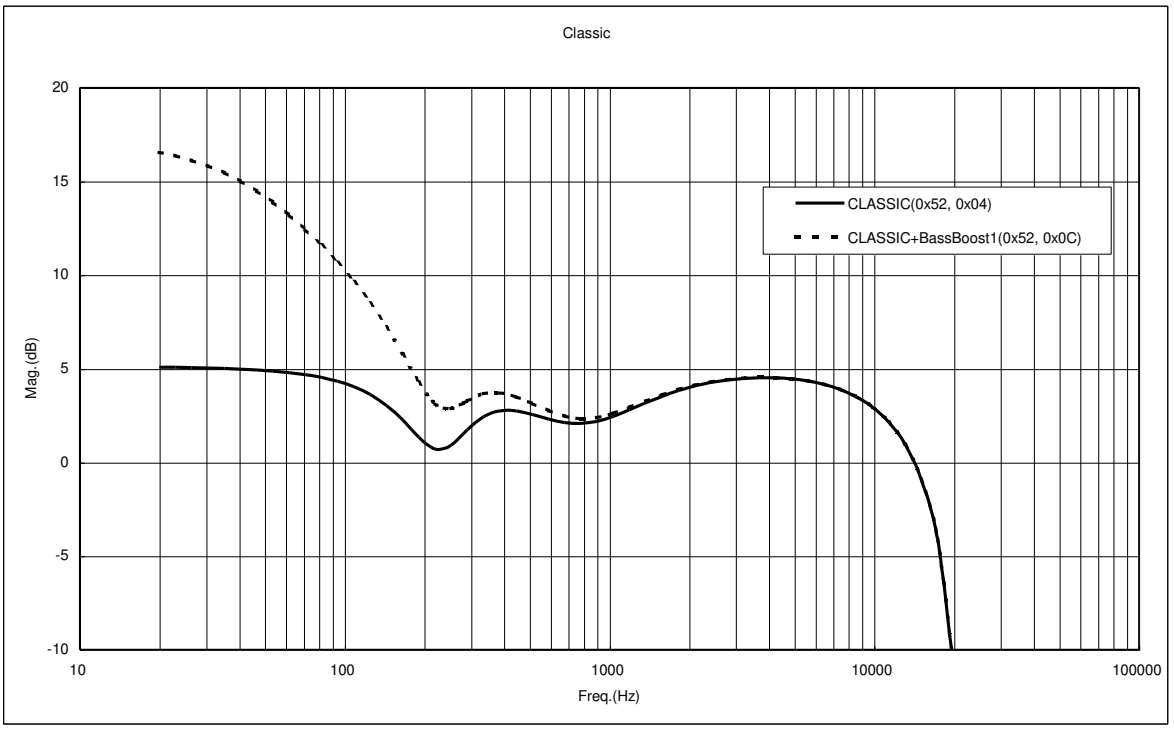

Figure 12. CLASSIC Frequency Characteristics

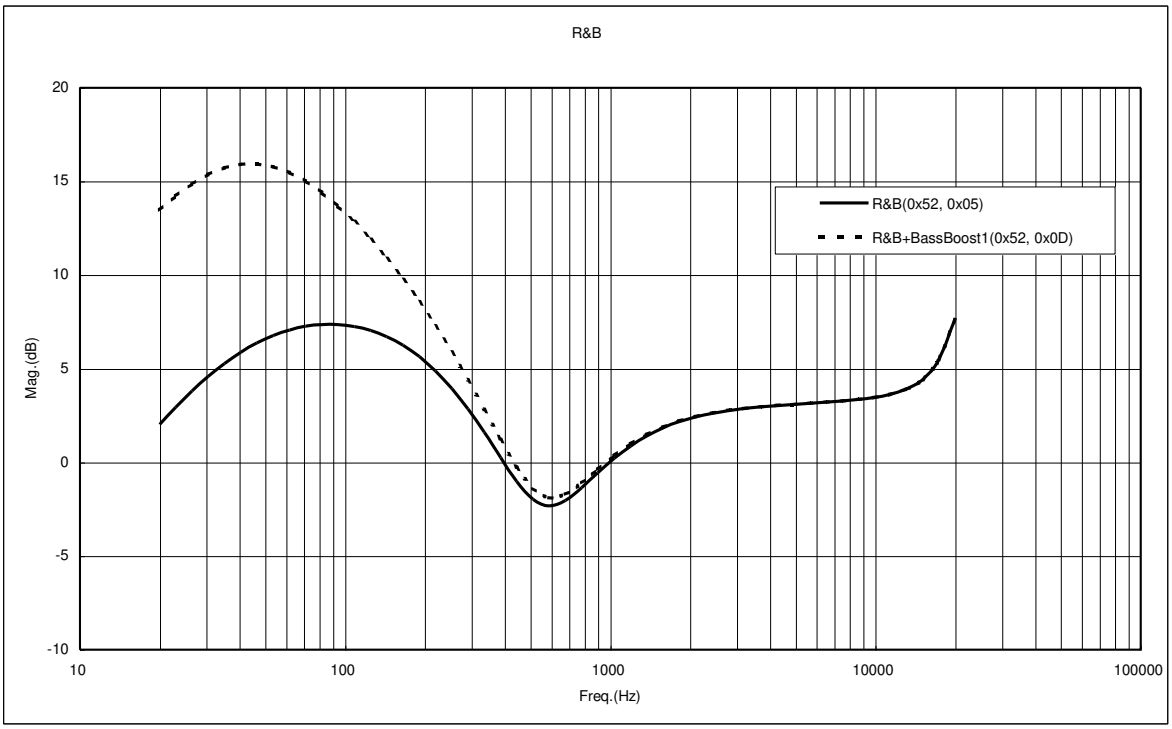

Figure 13. R&B

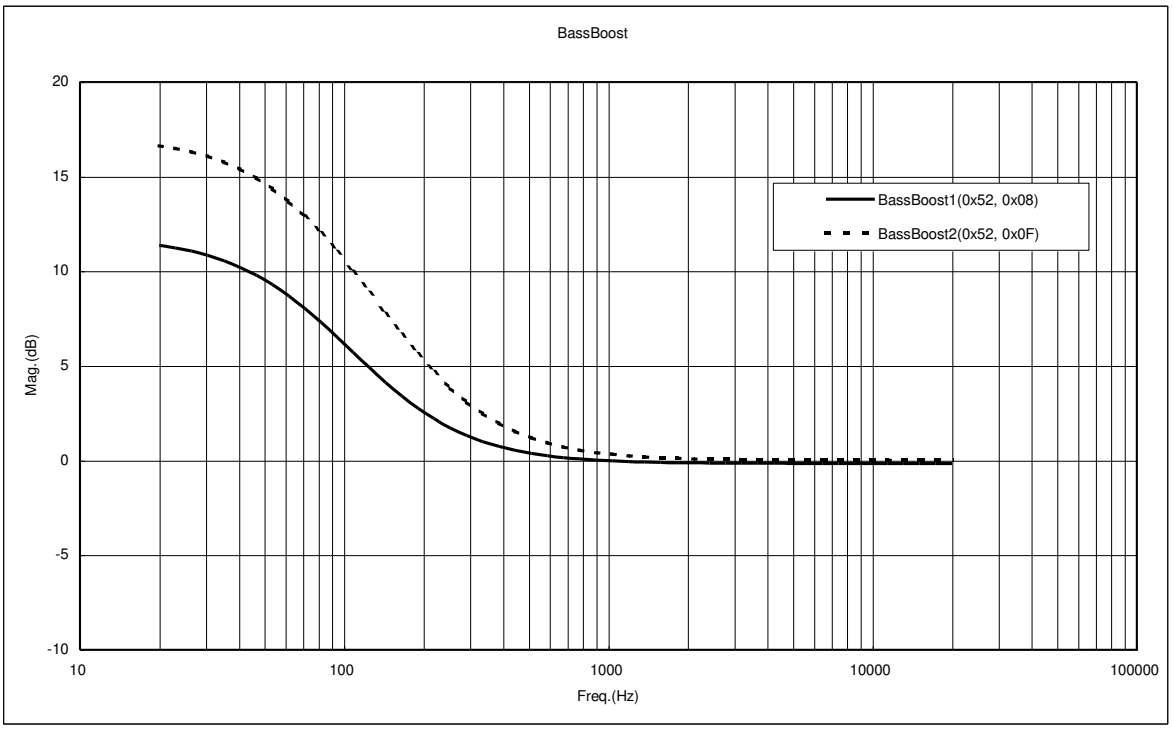

Figure 14. Bass Boost

6. MUTE control output

Audio MUTE

Signal name	I/O	Function	Remarks
AMUTE	O	Audio mute control terminal	H: At audio output , L: At mute

It outputs H at audio output and L at mute.
When power is ON or in the silence mode such as FF or FB, This control terminal is used to mute audio output
It can be used for the flag to do mute with the amplifier of the rear step and so on.
Figure 15. shows the operation waveforms.

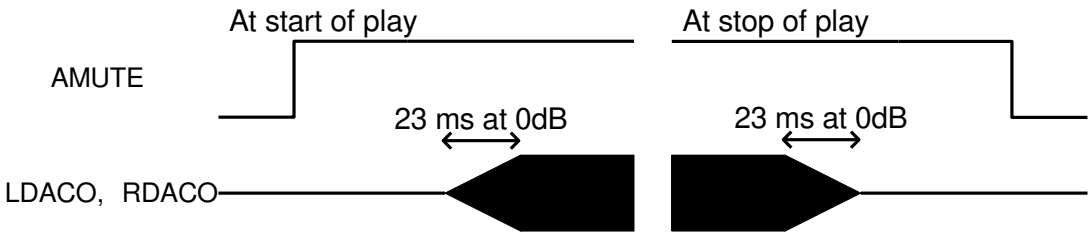

Figure 15. Waveform at Audio Mute

7. Digital audio output (I^2S, EIAJ)

The analog audio system line output by the built-in DAC and the change of the digital audio output signal are possible by a command.
Audio outputs are shown in Table 1. “Audio Output”.
Because TEST terminal is an output terminal, use it as OPEN.

Table 1. Audio Output

PIN	ANALOG output mode	DIGTAL output mode	
		SPDIF OFF	SPDIF ON
RDACO	Line Out Rch	HiZ	HiZ
LDACO	Line Out Lch	HiZ	HiZ
LRCK	TEST terminal	LR CLOCK	SPDIF
BCK	TEST terminal	BIT CLOCK	TEST terminal
DATA	TEST terminal	LR DATA	TEST terminal
MCLK	TEST terminal	MASTER CLOCK	TEST terminal

Digital audio interface (I^2S, EIAJ)

Signal name	I/O	Function	Remarks
LRCK	O	LR clock output (fs=44.1kHz)	-
BCK	O	Bit clock output	-
DATA	O	Data output	-
MCLK	O	Masterxlock output	At fs=32kHz 12.288MHz (384fs) At fs=44.1kHz 16.9344MHz (384fs) At fs=48kHz 12.288MHz (256fs)

This is a digital audio output interface terminal.
It becomes enabled by using the appropriate command.
When serial audio output is selected, The output format can be selected from the EIAJ format or I^2S format of 32fs, 48fs or 64fs .
Selectable With the mode that the sample rate of the playback tune is outputted and the mode fixed on 44.1 kHz by sample rate converter.
Figure 16. - Figure 21. show the output formats.

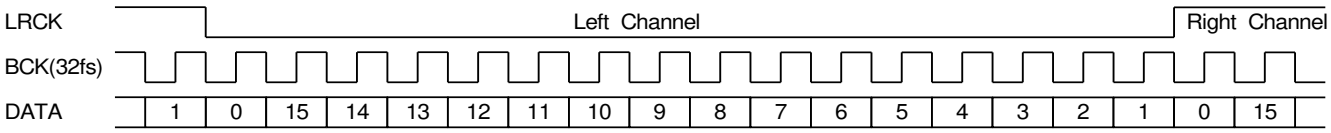

Figure 16. I²S Output Timing (32fs)

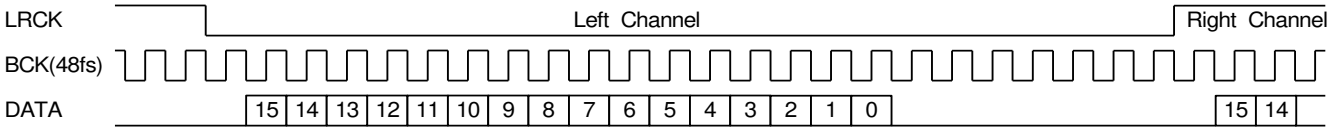

Figure 17. I²S Output Timing (48fs)

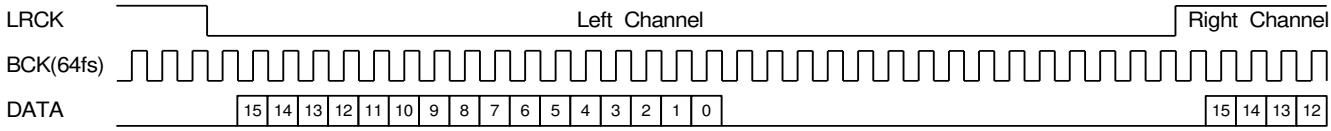

Figure 18. I²S Output Timing (64fs)

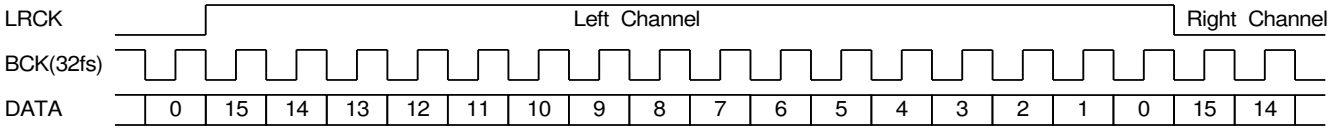

Figure 19. EIAJ Output Timing (32fs)

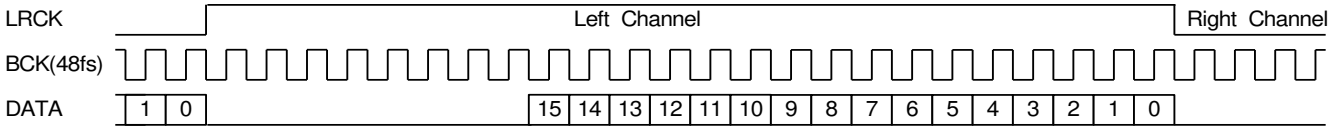

Figure 20. EIAJ Output Timing (48fs)

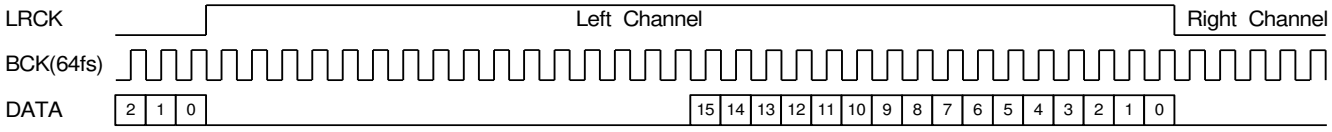

Figure 21. EIAJ Output Timing (64fs)

7.1 I^2S, EIAJ Output Timing

48fs I^2S format(Unless specified, Ta=25℃, VDD1=3.3V, Load=20pF)

Item	Symbol	Rating			Unit	Remarks
		min	typ	max		
BCK Clock Frequency	Tbck	-	472.4	-	ns	
BCK Low time	Tbck1	216	236	-	ns	
BCK High time	Tbck2	216	236	-	ns	
LRCK Clock Frequency	Tlrck	-	44.1	-	kHz	
LRCK Output delay	Tlrck1	-20	0	20	ns	
DATA Output delay	Tda1	-20	0	20	ns	
Output High Voltage	Toh	VDD1-0.4	-	-	V	
Output Low Voltage	Vol	-	-	0.4	V	

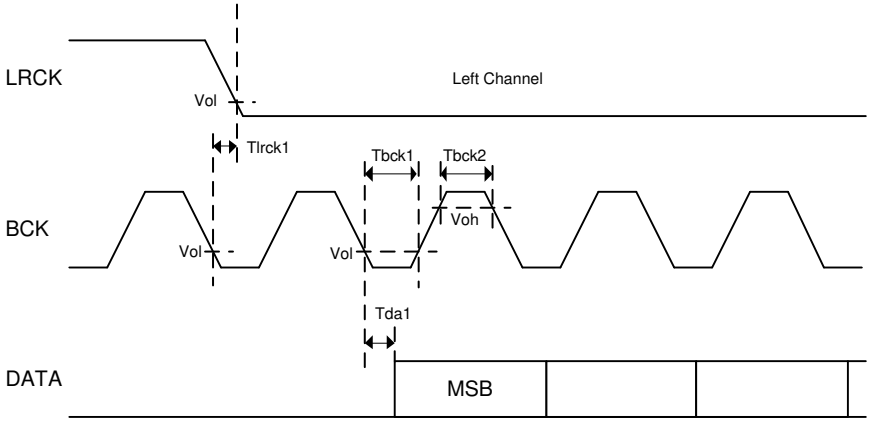

Figure 22. I^2S, EIAJ Output Timing

8. Digital audio output (SPDIF)

Digital audio interface

Signal Name	I/O	Function	Remarks
SPDIF	O	SPDIF output	-

SPDIF output become enabled by setting it using the appropriate command.
Figure 23. shows the digital audio signal output format.

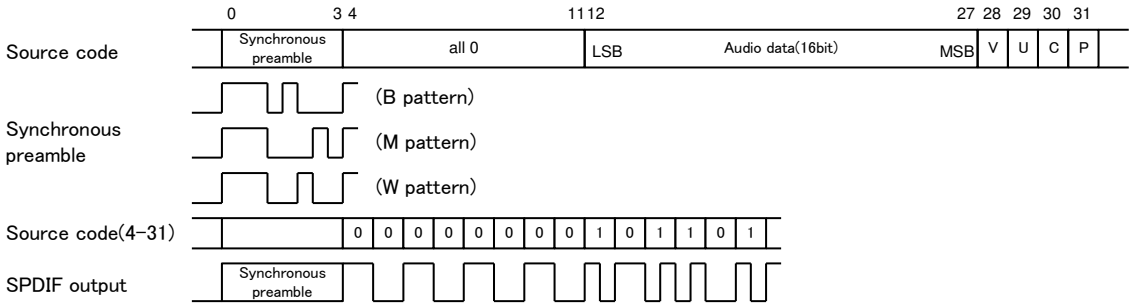

Figure 23. SPDIF Output Format

One sub frame of SPDIF consists of synchronous preambles, 16-bit audio data, V bit (validity flag), U bit (user data), C bit (channel status) and P bit (parity bit).
Output rate is fixed to 1X speed.
SPDIF outputs synchronous preambles (source code 0-3) as they are, and other elements (source code 4-31) as the biphase output. While the operation stops, L output is enabled.
Synchronous preambles and C bit use 32 frames (≈4.4 ms) for one cycle. The data formats are shown in Tables.2 and 3 V bit is fixed to L. U bit uses 98 frames (≈13.3 ms) for one cycle

Table 2. Synchronous Preamble Pattern

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	B	W	M	W	M	W	M	W	M	W	M	W
1	M	W	M	W	M	W	M	W	M	W	M	W
:	:	:	:	:	:	:	:	:	:	:	:	:
31	M	W	M	W	M	W	M	W	M	W	M	W

Table 3. C Bit Format

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	0		0		Copy		0		0		0	
1	0		0		1		0		0		0	
2	0		0		0		Lbit		0		0	
3	0		0		1	0	0	1	0		0	
4	0		0		0		0		0		0	
5	0		0		0		0		0		0	
:	:		:		:		:		:		:	
31	0		0		0		0		0		0	

Table 4. U Bit Format

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:	:
97	1	0	0	0	0	0	0	0	0	0	0	0

P bit is set to 1 if the number of “1” contained in source codes 4-30 is odd, and set to 0 if the number is even. Therefore, the number of source codes to be set to 1 for one data must be even, SPDIF ends with L output, and preamble output always starts in the same direction.

8.1 SPDIF Output Timing

(Unless specified, Ta=25℃, VDD1=3.3V, Load=20pF)

Item	Symbol	Rating			Unit	Remarks
		min	typ	max		
SPDIF Clock Frequency	Tck	-	2.822	-	MHz	
SPDIF Clock High time	Tck1	157	177	-	ns	
SPDIF Clock Low time	Tck2	157	177	-	ns	
Output High Voltage	Voh	VDD1-0.4	-	-	V	
Output Low Voltage	Vol	-	-	0.4	V	

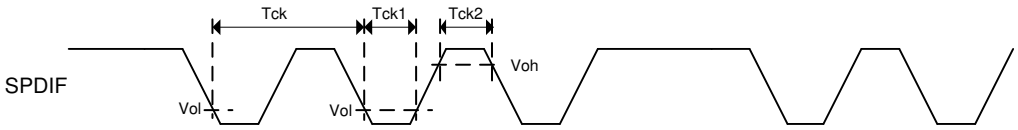

Figure 24. SPDIF Output Timing

9. I²C command interface

Slave I²C serial interface

Signal name	I/O	Function	Remarks
SCL	I	I²C interface clock input	External pull-up resistor is required.
SDA	I/O	I²C interface data I/O	External pull-up resistor is required.

This is an I²C serial interface terminal to communicate with the microcomputer (master).
It supports slave I²C operations.

9.1 I²C protocol

When the I2C bus is in the IDLE state, SDA and SCL are set to H by the external Pull-up resistor.
To start communications, the master sets SDA to L while SCL set to H (Start condition).
To finish communications, the master sets SDA to H while SCL set to H (Stop condition). During transfer, the master changes SDA only while SCL is L. Figure 25. shows Start condition and Stop condition of I²C.

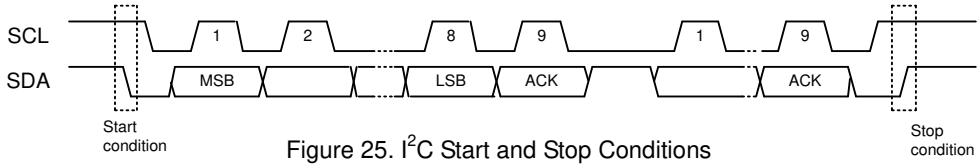

Figure 25. I²C Start and Stop Conditions

9.2 Slave address

I²C bus slave addresses support the 7-bit addressing mode.
Figure 26. shows the slave address transfer format.

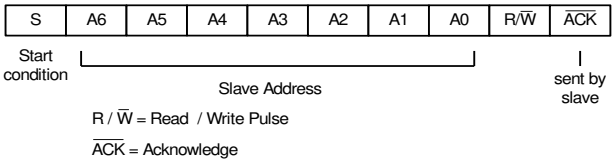

Figure 26. Slave Address Transfer Format

Table 5. Settable Slave Addresses

MSB	A5	A4	A3	A2	A1	LSB A0
1	0	0	0	0	1	1

9.3 Protocol to write from the master

When sending commands from the master using the I²C bus, be sure to conform to the transfer protocol shown in Figure 27.

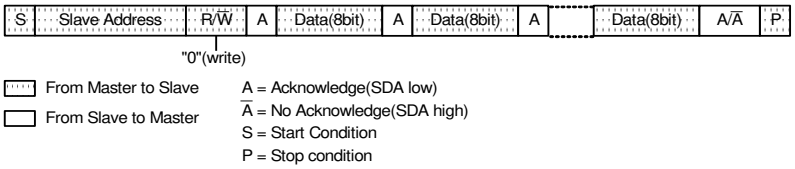

Figure 27. Command Send Protocol