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Datasheet

USB Audio Decoder LSI Series

AAC/WMA/MP3 +SD Memory Card + iPod

BU94601KV BU94603KV BU94604BKV

●Description

BU94601KV / BU94603KV / BU94604BKV are AAC+ WMA + MP3 decoder IC which contains USB host, SD card I/F, audio DAC, system controller, and regulator for internal CORE power supply.

●Features

- USB2.0 Full Speed host I/F function contained.
- Protocol conversion from I²C to USB HID or from USB HID to I²C. (Only BU94604BKV)
- SD card I/F function contained.
- I²C I/F function contained.
- FAT analysis function contained.
- MP3 decode function contained. (available for MPEG1, 2 and 2.5, Layer 1, 2 and 3)
- WMA decode function contained.
  (Except BU94601KV)
  Available for WMA9 standard and not available for DRM
- AAC decode function contained.
  (Except BU94601KV)
  Available for MPEG4 AAC-LC and not available for DRM
- Sample Rate Converter contained.
- System Controller contained.
- LED Controller contained.
- KEY matrix Controller contained.
- Stand Alone mode contained.
- External processor can control. (Slave mode)
- Audio DAC contained.
- Sound Effect function contained.
- Digital Audio Output(I²S, S/PDIF) function contained.
- File Name, Folder Name Sorting.
- ID3TAG and WMATAG and AACTAG Analysis.
- Reading a specified file data is possible from USB memory.
- LUN is selectable.
- Regulator for internal CORE power supply contained.
- VQFP64pin(0.5mm pitch)

●Package W(Typ.) x D(Typ.) x H(Max.)

VQFP64
12.00mm x 12.00mm x 1.60mm

●Applications

Audio products, etc

●Line up

Part number	Format	iPod	Package		Ordering part number
BU94601KV	MP3	Not supported	VQFP64	Reel of 2000	BU94601KV-ZAE2
BU94603KV	AAC/WMA/MP3		VQFP64	Reel of 2000	BU94603KV-ZAE2
BU94604BKV	AAC/WMA/MP3	Supported	VQFP64	Reel of 2000	BU94604BKV-ZAE2

●**Basic circuit application diagram-part1**

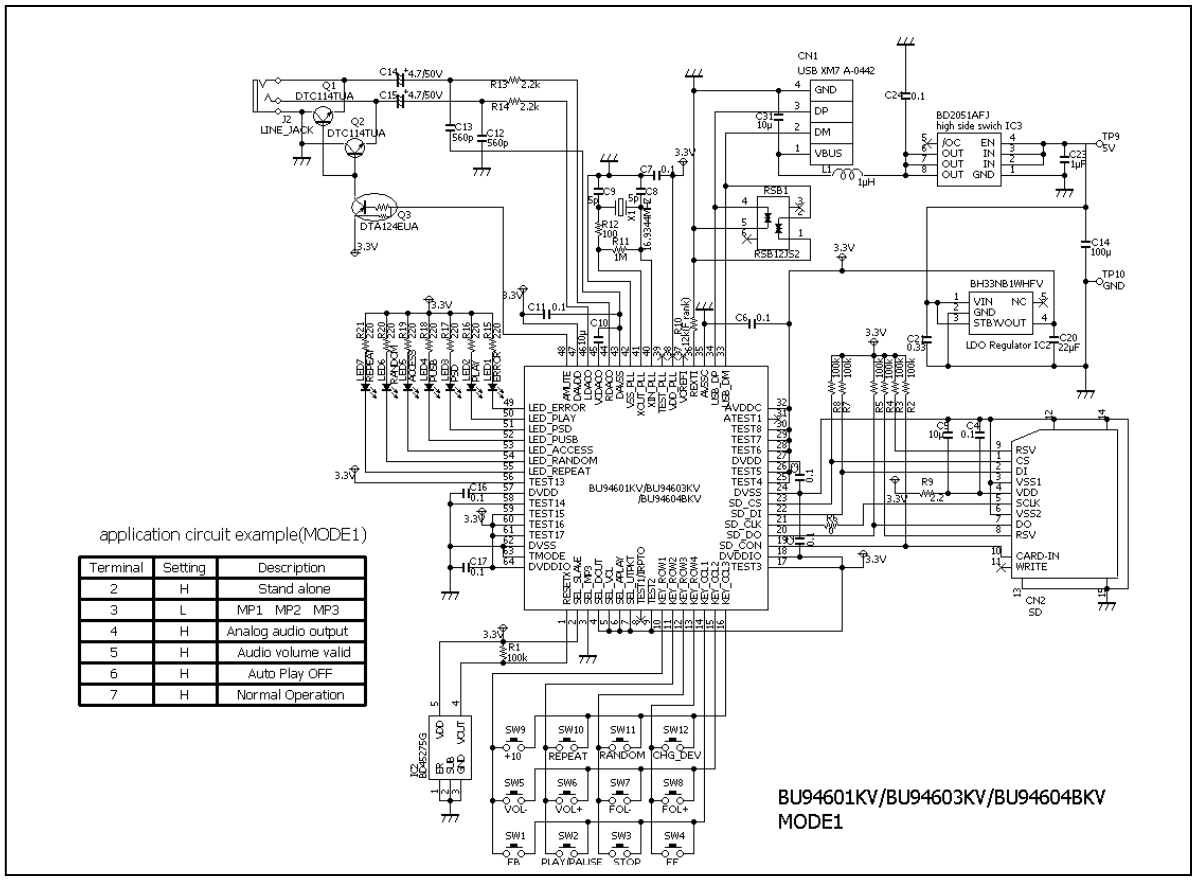


Figure 1. an example of connection circuit application (BU94601KV/BU94603KV/BU94604BKV MODE1) *

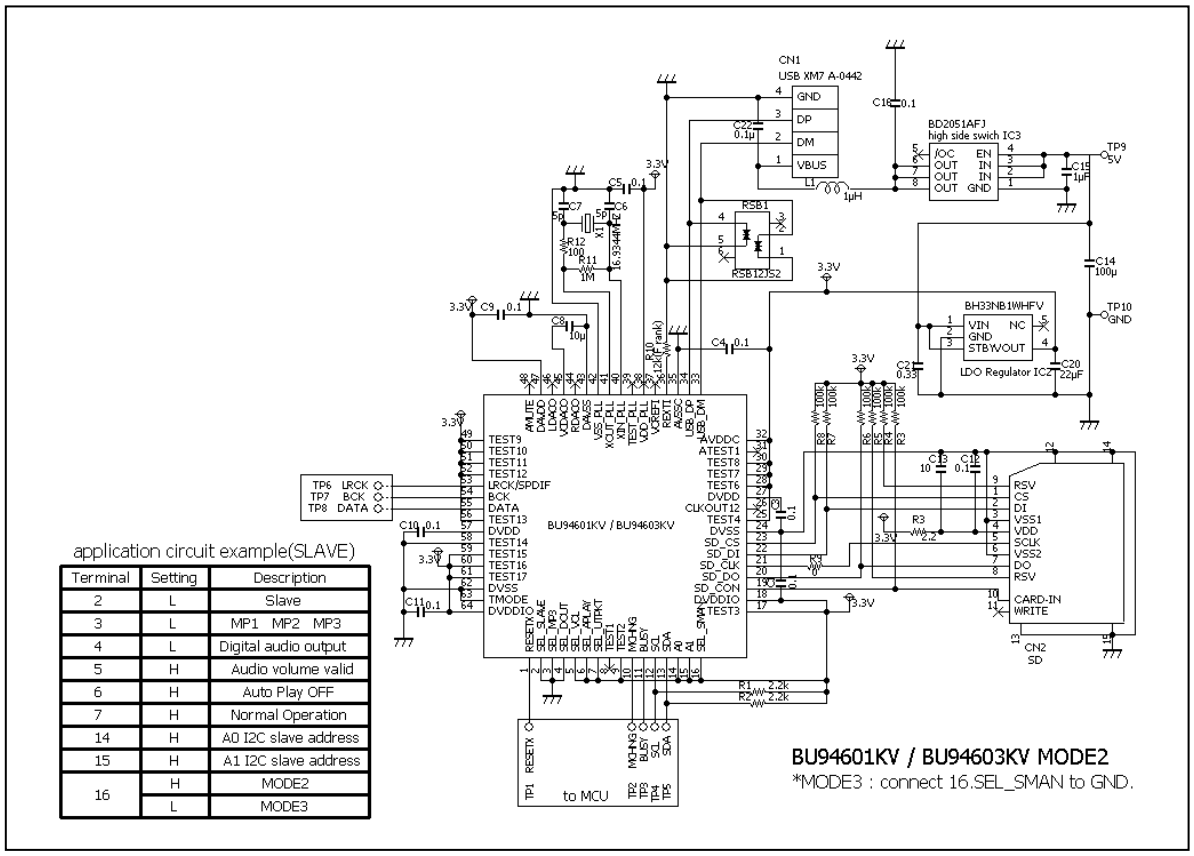
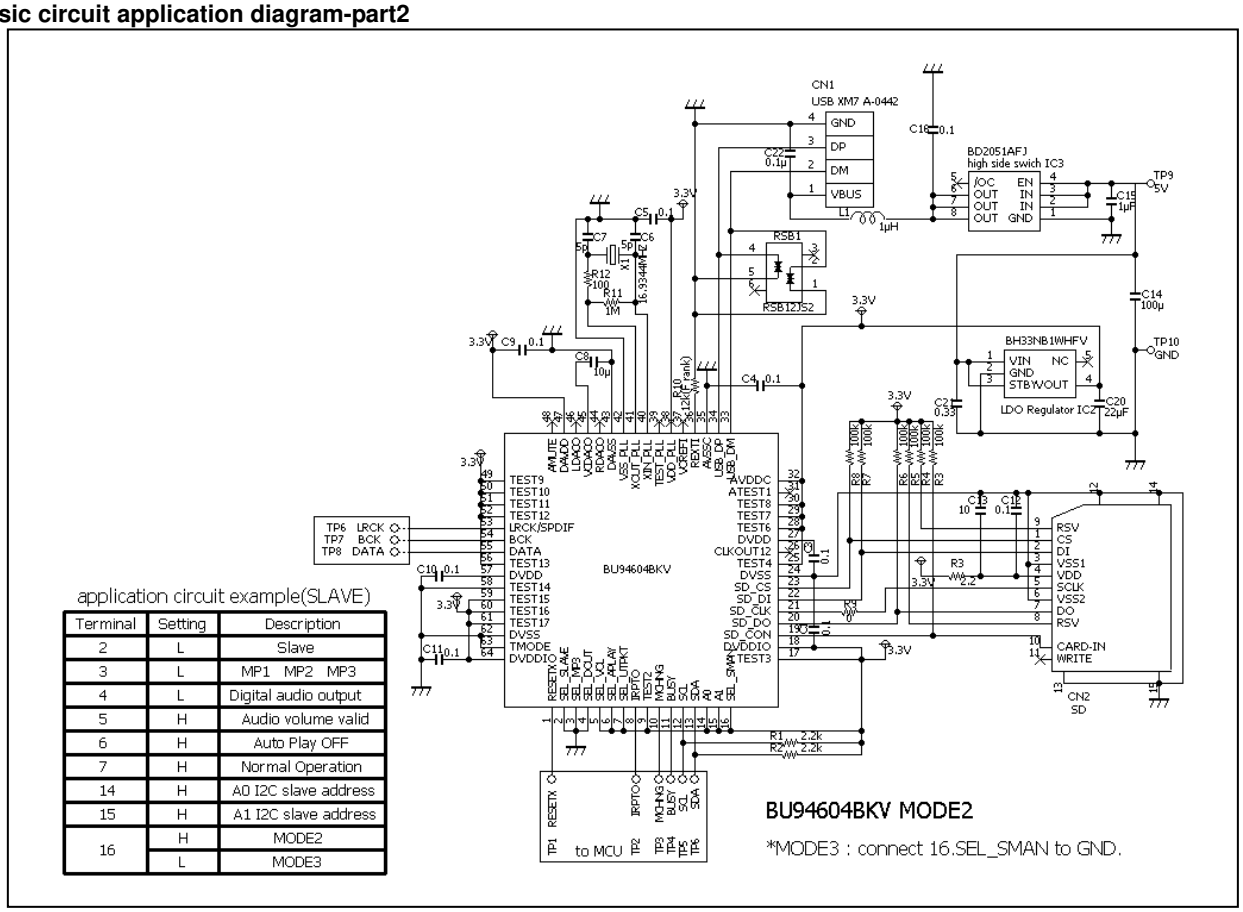


Figure 2. an example of connection circuit application (BU94601KV/BU94603KV MODE2/3) *

●**Basic circuit application diagram-part2**



application circuit example(SLAVE)

Terminal	Setting	Description
2	L	Slave
3	L	MP1 MP2 MP3
4	L	Digital audio output
5	H	Audio volume valid
6	H	Auto Play OFF
7	H	Normal Operation
14	H	A0 I2C slave address
15	H	A1 I2C slave address
16	H	MODE2
	L	MODE3

Figure 3. an example of connection circuit application (BU94604BKV MODE2/3) *

This LSI has built in regulator for internal CORE power supply. DVDD terminal of 27PIN and 57PIN connect to bypass condenser. DVDD terminal of 27PIN and 57PIN don't connect to power supply.

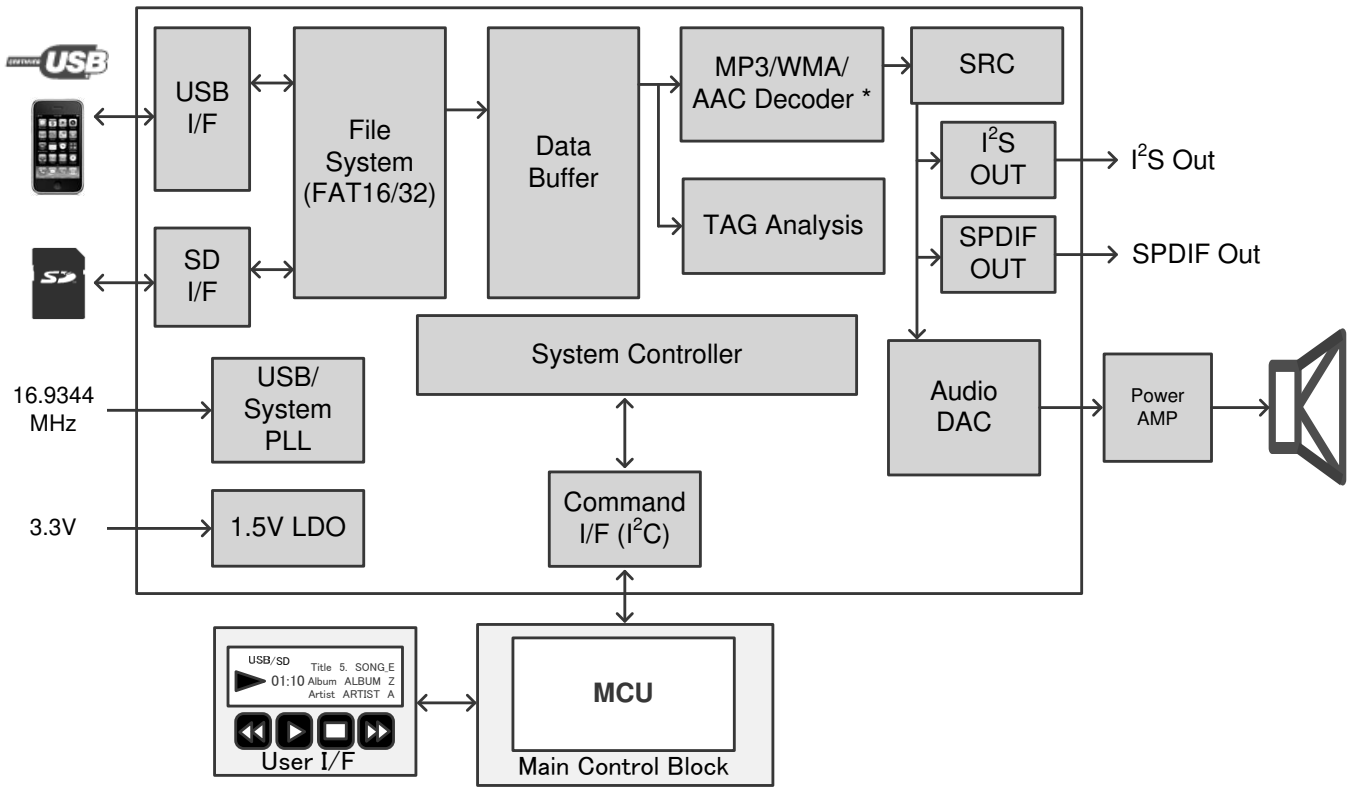
The reference circuit and reference circuit parameters for crystal oscillator are shown above. The circuit parameters introduced above is not taking into consideration the environment in customer's systems or set's board. Therefore, ROHM is not guaranteed this content in any circuits. Please check the optimal circuit parameter in customer's actual systems or products with the oscillator manufacturer.

●Difference of BU94601KV/BU94603KV/BU94604BKV features

Item	BU94601KV	BU94603KV	BU94604BKV
Package	VQFP64		
Number of pins	64pin		
Power supply	3.3V (inner 1.5V regulator)		
USB Host I/F	USB Full speed(12Mbps) USB mass storage class		
SD Card I/F	SPI mode SD, SDHC, MMC, mini-SDcard		
I^2C command I/F(Slave)	Supported		
Audio line output	Supported		
Digital audio output	I^2S SPDIF		
Sample rate converter	Supported		
clock	16.9344MHz		
Playable MP3 files	*.mp3,*.mp2,*.mp1		
Playable WMA files	Not supported	*.asf,*.wma	
Playable AAC files	Not supported	*.m4a,*.3gp,*.mp4	
iPod	Not supported		Supported*1

*1 For using of BU94604BKV, It is necessary to become a licensee of Apple Inc. regarding "Made for iPod/iPhone/iPad License".

●**Block diagram**



*BU94601KV contains only MP3 decoder

Figure 4. Block diagram

●Arrangement of Terminals

BU94601KV / BU94603KV / BU94604BKV

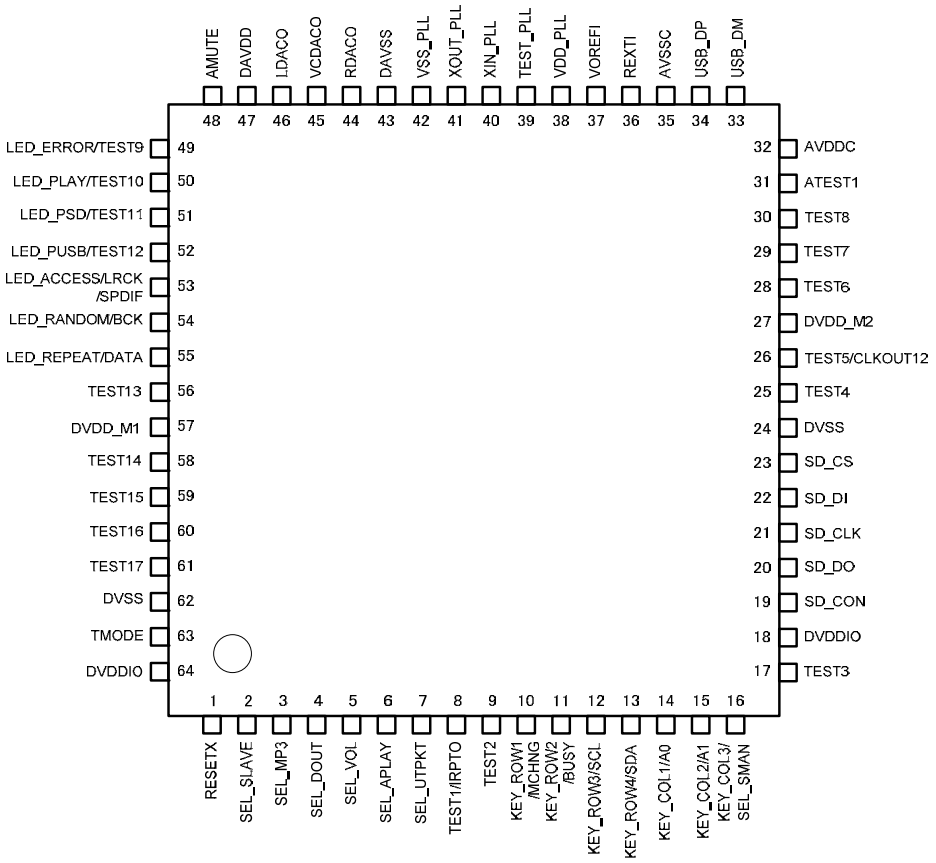


Figure 5. Arrangement of Terminals

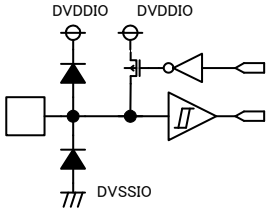
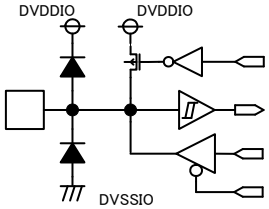
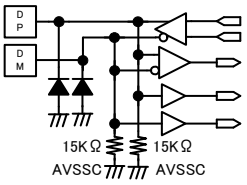
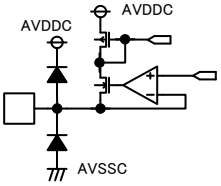
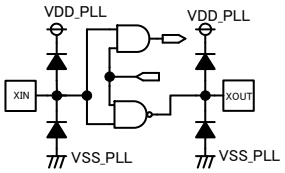
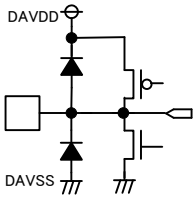
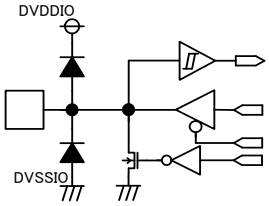
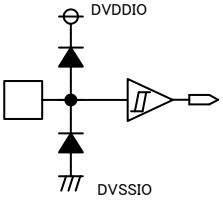
●**Description of Terminals**

	STAND ALONE MODE (MODE1)					SLAVE MODE (MODE2,MODE3)			
Pin No.	Signal Name	I/O Cir	I/O	Pull-Up/ Down (*7)	Function	Signal Name	I/O	Pull-Up/ Down (*7)	Function
1	RESETX	A	I	PU	H: Release RESET, L: RESET	←			
2	SEL_SLAVE	B	I	PU(*1)	H: STAND ALONE, L:SLAVE	←			
3	SEL_MP3	B	I	PU(*1)	H: PLAY MP3 ONLY, L: PLAY MP1,MP2 and MP3	←			
4	SEL_DOUT	B	I	PU(*1)	H: Audio Line Output, L: Digital Audio Output	←			
5	SEL_VOL	B	I	PU(*1)	H: Volume control valid, L: Volume control invalid	←			
6	SEL_APLAY	B	I	PU(*1)	H: Auto Play OFF , L: Auto Play	←			
7	SEL_UTPKT	B	I	PU(*1)	H: Normal Operation L: USB Test Packet Output	←			
8	TEST1 (*2)	B	O	-	OPEN (for TEST)	←			
	IRPTO (*3)	B	O	-	Device (Have 2 configuration or more) connection's interruption output terminal	←			
9	TEST2	-	I	PU	Pull-up to 3.3V system power supply (for TEST)	←			
10	KEY_ROW1	B	I	PU	KEY Input ROW1	MCHNG	O	-	Music change Output
11	KEY_ROW2	B	I	PU	KEY Input ROW2	BUSY	O	-	Command Operation Busy Flag
12	KEY_ROW3	B	I	PU	KEY Input ROW3	SCL	I	-	I^2C I/F Clock Input
13	KEY_ROW4	B	I	PU	KEY Input ROW4	SDA	I/O	-	I^2C I/F Data Input/Output
14	KEY_COL1	B	O	-	KEY Input COLUMN1	A0	I	-	I^2C I/F Slave Address Set0
15	KEY_COL2	B	O	-	KEY Input COLUMN2	A1	I	-	I^2C I/F Slave Address Set1
16	KEY_COL3	B	O	-	KEY Input COLUMN3	SEL_SMAN	I	PU(*1)	H: MODE2, L: MODE3
17	TEST3	B	I	PU	Pull-up to 3.3V system power supply (for TEST)	←			
18	DVDDIO	-	-	-	Connect to 3.3V System Power Supply	←			
19	SD_CON	B	I	-	SD I/F (*4)	←			
20	SD_DO	B	I	-	SD I/F (*4)	←			
21	SD_CLK	B	O	-	SD I/F	←			
22	SD_DI	B	O	-	SD I/F	←			
23	SD_CS	B	O	-	SD I/F	←			
24	DVSS	-	-	-	Connect to GND	←			
25	TEST4	-	I	PU	Pull-up to 3.3V system power supply (for TEST)	←			
26	TEST5	-	I	PU	Pull-up to 3.3V system power supply (for TEST)	CLKOUT12(*5)	I/O (*5)	PU(*5)	12MHz CLK Output.
27	DVDD_M2	-	-	-	Connect to 57PIN	←			
28	TEST6	-	I	-	Pull-up to 3.3V system power supply (for TEST)	←			
29	TEST7	-	I	-	Pull-up to 3.3V system power supply (for TEST)	←			
30	TEST8	-	I	-	Pull-up to 3.3V system power supply (for TEST)	←			
31	ATEST1	-	O	-	OPEN (for TEST)	←			
32	AVDDC	-	-	-	Connect to 3.3V System Power Supply	←			
33	USB_DM	C	I/O	-	USB DATA-	←			
34	USB_DP	C	I/O	-	USB DATA+	←			
35	AVSSC	-	-	-	Connect to GND	←			
36	REXTI	D	O	-	USB bias resistor(12kΩ) connecting terminal. Arrange the resistance of 12kΩ near PIN, and wiring on the PIN side doesn't cross with other signal lines.	←			

37	VOREFI	-	O	-	OPEN (for TEST)	←			
38	VDD_PLL	-	-	-	Connect to 3.3V System Power Supply	←			
39	TEST_PLL	-	I	-	OPEN (for TEST)	←			
40	XIN_PLL	E	I	-	X'tal Input 16.9344MHz	←			
41	XOUT_PLL	E	O	-	Connect to X'tal 16.9344MHz	←			
42	VSS_PLL	-	-	-	Connect to GND	←			
43	DAVSS	-	-	-	Connect to GND	←			
44	RDACO	F	O	-	Audio DAC Line Output Rch	←			
45	VCDACO	I	O	-	Audio DAC Reference Voltage Output	←			
46	LDACO	F	O	-	Audio DAC Line Output Lch	←			
47	DAVDD	-	-	-	Connect to 3.3V System Power Supply	←			
48	AMUTE	G	O	-	Audio Mute Output (H:Mute Cancel, L:Mute)	←			
49	LED_ERROR	B	O	-	Error LED Output	TEST9	I	PU	Pull-up to 3.3V system power supply
50	LED_PLAY	B	O	-	Play LED Output	TEST10	I	PU	Pull-up to 3.3V system power supply
51	LED_PSD	B	O	-	Play SD Card LED Output	TEST11	I	PU	Pull-up to 3.3V system power supply
52	LED_PUSB	B	O	-	Play USB LED Output	TEST12	I	PU	Pull-up to 3.3V system power supply
53	LED_ACCESS	B	O	-	Memory Access LED Output	LRCK /SPDIF(*4)	I/O (*6)	PU(*6)	I²S Output LR Clock / SPDIF Output
54	LED_RANDOM	B	O	-	Random Play LED Output	BCK(*4)	I/O (*6)	PU(*6)	I²S Output Bit Clock
55	LED_REPEAT	B	O	-	Repeat Play LED Output	DATA(*4)	I/O (*6)	PU(*6)	I²S Output LR DATA
56	TEST13	-	I	PU	Pull-up to 3.3V system power supply (for TEST)	←			
57	DVDD_M1	-	-	-	Connect to Bypass Condenser	←			
58	TEST14	F	I	-	Connect to GND	←			
59	TEST15	-	I	-	Pull-up to 3.3V system power supply (for TEST)	←			
60	TEST16	-	I	-	Pull-up to 3.3V system power supply (for TEST)	←			
61	TEST17	-	I	-	Pull-up to 3.3V system power supply (for TEST)	←			
62	DVSS	-	-	-	Connect to GND	←			
63	TMODE	H	I	-	Connect to GND	←			
64	DVDDIO	-	-	-	Connect to 3.3V System Power Supply	←			

*1 When L is input, Pull-UP turns OFF.
*2 BU94601KV / BU94603KV
*3 BU94604BKV
*4 When SD I/F is disused, pull-up to 3.3V system power supply.
*5 Enabled/Disabled can be selected using commands.
This pin becomes output and pull-up is OFF, only when 12MHz clock output is enable.
*6 In STAND ALONE MODE (MODE1),
When Audio Line output is selected (SEL_DOUT=H), LED output is enabled.
When the Digital Audio output is selected (SEL_DOUT=L), the I^2S format audio output is enabled.
In SLAVE MODE (MODE2, MODE3),
When the Analog Line output is selected (SEL_DOUT=H), these pins are TEST terminals.
When the Digital Audio output is selected (SEL_DOUT=L), I^2S or SPDIF is selectable.
See Chapter 4 . SEL_DOUT for further information.
*7 Input L level directly without resistance when you input L to the terminal with Pull-Up (about 33 kΩ).

●**Terminal equivalent circuit diagram**

A	B	C	D
			
E	F	G	H
			
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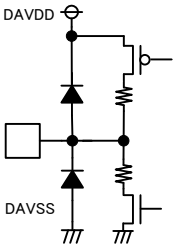			

●Description of each block's movement-part1

- BU94601KV/BU94603KV/BU94604BKV are AAC+WMA+MP3 decoder IC in which a USB host I/F, SD memory card I/F, audio DAC and system control functions are built. Using a KEY or I²C interface command, the IC reads out a MP3 file written to a memory device having a USB I/F or a SD memory card. All the operations required before the data can be output to audio devices are incorporated into one chip. *BU94601KV supports only MP3.
- Supporting STAND ALONE MODE which is enabled by commands entered from the keyboard (hereinafter referred to as MODE1), AUTO SLAVE MODE which is enabled by commands entered from the master microcomputer, same as those entered from the keyboard, via the built-in I²C interface (hereinafter referred to as MODE2) and MANUAL SLAVE MODE which can send the memory device information to the master microcomputer via the I²C interface and completely control sequences such as a play sequence by the master microcomputer (hereinafter referred to as MODE3).
- I²C bus <-> USB protocol conversion function built into. *Only MODE2 and MODE3 of BU94604BKV.
- Supporting fast forward playing and fast backward playing with music.
- Supporting outputs folder names, file names, ID3TAG (V1.0, V1.1 V2.2 V2.3 and V2.4) information and WMA-TAG information and AAC-TAG(iTunes Meta-data) information via the I²C interface. This function is enabled only in MODE 2 and MODE 3.
- Supporting audio line output, digital audio output (I²S, SPDIF).
- Reading a specified file data is possible from USB memory. *Only a file that exists in root folder corresponds.

1. USB host I/F
   - Builds in the USB Full speed (12 Mbps) HOST control function.
   - Supports the USB mass storage class.
   - Convert the protocol from I²C from USB(HID) and USB(HID) to I²C when communicating with the master microcomputer.*
   - An isochronous IN transfer function to 192 byte/Frame is built into.*
   - Interrupt IN transfer function is built into.*
   - It doesn't correspond to external HUB.

   * Only the device with two CONFIGURATIONS or more. Only BU94604BKV.

2. SD card I/F
   - Supports the SPI mode.
   - Supports the MMC and mini-SD cards.
   - Supports the SDHC cards.
   - Supports the SD ver1.01 (file system).
   - Does not support CPRM.

3. I²C I/F
   - Communicates with the master microcomputer using an I²C interface format.
   - Supports the standard mode (100 kbps) and fast mode (400 kbps).
   - Supports a 7-bit address.
   - Can select four types of slave addresses.

4. Audio output
   - 1bit-DAC output
   - Builds in the digital soft mute function.
   - Supports digital audio output (I²S, SPDIF).
   - Builds in sound effects of POPS, JAZZ, ROCK, CLASSIC, R&B and BassBoost.*

   * Only audio line output is enabled.

●Description of each block's movement-part2

5. FAT analysis
   - Supports FAT16 and FAT 32.
   - Supports VFAT (long file name).
   - Supports multi-partition up to 1.
   - The maximum number of playable folders within each folder is 65534.
   - The maximum number of playable files within each folder is 65534.
   - The maximum number of playable folders within each device is 65534.
   - The playable folder hierarchy is up to 8 layers containing the root directory.
   - The playable file extension supports *.m4a, *.3gp, and *.mp4 for AAC, *.wma and *.asf for WMA, *.mp3, *.mp2, and *.mp1 for MP3. For *.mp2 and *.mp1, play enabled/disabled can be selected. Upper case letters and lower case letters are not distinguished in the file extension. (BU94601KV supports only *.mp3, *.mp2, and *.mp1.)
   - Sorts and plays up to 100 folders and 100 files in the order of UNICODE.
   - Possible to obtain up to 64 bytes as the folder name or file name.
   - Supports 1 sector of 512, 1024, 2048 and 4096 bytes.
   - Playable file size is up to 2Gbyte-1 byte. Although a file over 2Gbyte is recognized as a playable file, 2Gbyte -1byte part of the file is playable.

6. MP3 decoder
   - Supports MPEG audio 1, 2 and 2.5.
   - Supports Layer 1, 2 and 3.
   - Supports sample rates 8k, 16k, 32k, 11.025k, 22.05k, 44.1k, 12k, 24k and 48kHz.
   - Supports bit rate 8 to 320 kbps and VBR (Variable Bit Rate). *Except free format.
   - Supports ID3TAG V1.0, V1.1, V2.2, V2.3 and V2.4.
     (Up to 64 bytes can be obtained for the names of album, artist, and title.)

7. WMA decoder (BU94601KV doesn't support.)
   - Supports Windows Media Audio 9 standard.
   - Not supports DRM.
   - Supports sample rates 8k, 16k, 32k, 11.025k, 22.05k, 44.1k, and 48kHz.
   - Supports bit rate 5 to 384 kbps and VBR (Variable Bit Rate). *Except free format.
   - Supports WMA-TAG.
     (Up to 64 bytes can be obtained for the names of album, artist, and title.)

8. AAC decoder (BU94601KV doesn't support.)
   - Supports MPEG4 AAC-LC encoded by iTunes.
   - Not supports DRM.
   - Supports sample rates 8k, 16k, 32k, 11.025k, 22.05k, 44.1k, 12k, 24k and 48kHz.
   - Supports bit rate 8 to 320 kbps and VBR (Variable Bit Rate).
   - Supports AAC-TAG(iTunes Meta-data).
     (Up to 64 bytes can be obtained for the names of album, artist, and title.)
   - The playable file extension supports *.m4a, *.3gp, and *.mp4
   - Based on 3GPP TS 26.244.
   - Supports file type of m4a, mp42, and 3gpX (numbers with arbitrary X).

   *About except for the file encoded by iTunes, when the stream of a gap or video data is included in the file, it may skip to the following music or skipping may be carried out.

9. Sample rate converter
   - Converts all the supported sample rates to 44.1 kHz using a poly-phase operation.

10. System controller
    - Controls all the system operations including KEY input, LED output, interface control with the master microcomputer, USB device access, SD card access, FAT analysis, sort function, MP3 decode, WMA decode and audio output.

●Description of each block's movement-part3

11. KEY matrix controller
    - Controls 12 types of KEY inputs: play/pause, stop, tune forward/fast forward playing, tune backward/fast backward playing, folder forward, folder backward, 10-tune forward, volume up, volume down, repeat play, random play and device selection.

12. LED controller
    - Controls 7 types of LED outputs: play/pause, error, memory accessing, random playing, repeat playing, USB selection and SD selection

13. Control from the master microcomputer
    - Control from the master microcomputer is enabled using the I^2C interface.
    - Through the command operations, the following can be controlled: play, pause, stop, tune forward, tune backward, fast forward playing, fast backward playing, folder forward, folder backward, 10-tune forward, 10-tune backward, volume up, volume down, device selection, volume setting, repeat selection, random play, digital audio output setting, sound effect setting, resume data setting and direct tune selection data setting.
    - Controls the following: playing status output, pause, stop, searching, error, folder number, file number within folder, play time information, number of total folders, number of total files, name of folder being played, name of file being played, ID3TAG (title, artist and album) , WMATAG (title, artist and album), AACTAG (title, artist and album),resume data and direct tune selection data (MODE3).

14. Function selection
    - Selects MODE1 or MODE2/3 (SEL_SLAVE=H: MODE1, L: MODE2/3).
    - Selects MPEG Audio Layer (SEL_MP3=H: play MP3 only, L: play MP1/MP2/MP3)
    - Digital audio output selection (SEL_DOUT=H: output OFF, L: output ON)
    - Sound volume operation selection (SEL_VOL=H: volume adjustable, L: volume not adjustable MAX output)
    - Selects operation at power ON to check device (SEL_APLAY=H: stop, L: play). *Enabled in MODE 1 only.
    - Selects MODE2 or MODE3 (SEL_SMAN=H: MODE2, L: MODE3). *Enabled in MODE 2/3 only.

15. File Read function in USB memory
    - The specified data of file that exists in the root folder of the USB memory reading is possible.

    * The file name corresponds only by 8.3 forms. (The wild-card cannot be used.)

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage(Analog, I/O)	VDD1MAX	-0.3 to 4.5	V	DVDDIO, VDD_PLL, DAVDD, AVDDC
Input voltage	VIN	-0.3 to VDD1 + 0.3	V	
Storage temperature range	TSTG	-55 to 125	℃	
Operating temperature range	TOPR	-40 to 85	℃	
Power dissipation *1	PD	750	mW	

*1 : In the case of use at Ta=25℃ or more, 7.5mW should be reduced per 1℃.
Radiation resistance design is not arranged.

●Operating conditions (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage(Analog, I/O)	VDD1	3.0 to 3.6	V	DVDDIO,VDD_PLL, DAVDD, AVDDC

●Electrical characteristics

(Unless specified, Ta=25℃,VDD1=3.3V, DVSS=AVSSC=VSS_PLL=DAVSS=0V, XIN_PLL=16.9344MHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
<Total >						
Circuit current (VDD1 USB1)	IDD1USB1	-	65	80	mA	*1 When USB memory is played.
Circuit current (VDD1 SD1)	IDD1SD1	-	35	50	mA	*1 When SD card is played.
<Digital block>						
H-Level input voltage	VIH	VDD1*0.7	—	VDD1	V	*3
L-Level input voltage	VIL	DVSS	—	VDD1*0.3	V	*3
H-Level output voltage1	VOH1	VDD1-0.4	—	VDD1	V	IOH=-1.6mA, *4
L-Level output voltage1	VOL1	0	—	0.4	V	IOL=1.6mA. *4
H-Level output voltage2	VOH2	VDD1-0.4	—	VDD1	V	IOH=-3.6mA, *5
L-Level output voltage2	VOL2	0	—	0.4	V	IOL=3.6mA, *5
H-Level output voltage3	VOH3	VDD1-0.4	—	VDD1	V	IOH=-0.6mA, *6
L-Level output voltage3	VOL3	0	—	0.4	V	IOL=0.6mA, *6
H-Level output voltage4	VOH4	VDD1-1.0	—	VDD1	V	IOH=-0.6mA, *7
L-Level output voltage4	VOL4	0	—	1.0	V	IOL=0.6mA, *7
<USB-HOST >						
H-Level input voltage	VIHUSB	VDD1*0.6	—	VDD1	V	*8
L-Level input voltage	VILUSB	AVSSC	—	VDD1*0.3	V	*8
Output impedance(H)	ZOH	22.0	45.0	60.0	Ω	*8
Output impedance(L)	ZOL	22.0	45.0	60.0	Ω	*8
H-Level output voltage	VOHUSB	VDD1-0.5	—	VDD1	V	*8
L-Level output voltage	VOLUSB	0	—	0.3	V	*8
Rise/Fall time	Tr/Tf	—	11	—	ns	*8, Output capacity 50pF
Voltage of crossing point	VCRS	—	VDD1/2	—	V	*8, Output capacity 50pF
Range of differential input	VDIFF	0.8	—	2.5	V	*8
Differential input sensitivity	VSENS	0.2	—	—	V	*8
Pull-down resistance	RPD	14.25	15.0	24.8	kΩ	*8
<Audio DAC>						
Distortion rate	THD	—	0.02	—	%	1kHz, 0dB, sine, *9
Dynamic range	DR	—	88	—	dB	1kHz, -60dB, sine, *9
S/N ratio	S/N	—	96	—	dB	*9
Max output level	VSMAX	—	0.92	—	Vrms	1kHz, 0dB, sine, no load, *9

*1 3.3V system I/O, Analog Power supply(VDD1), 1kHz, 0dB, sine-wave playing
*3 1-7, 9-17, 19-20, 25-26, 28-30, 40, 49-52, 56, 58-61, 63 pin
*4 8, 10-11, 14-16, 48-55 pin
*5 13 pin
*6 21-23, 26 pin
*7 41 pin
*8 33, 34 pin
*9 44, 46 pin

●Application Information

1. Clock and reset

Clock

Signal name	I/O	Function	Remarks
XIN_PLL	I	X'tal (16.9344 MHz) connection input terminal	
XOUT_PLL	O	X'tal (16.9344 MHz) connection terminal	

Reset

Signal name	I/O	Function	Remarks
RESETX	I	System reset input terminal	

To disable a reset signal, continue L input for more than 5 us after all of the supply voltage reach the specified value and clock input from the oscillation I/O terminal becomes stable. (See Figure 6.)

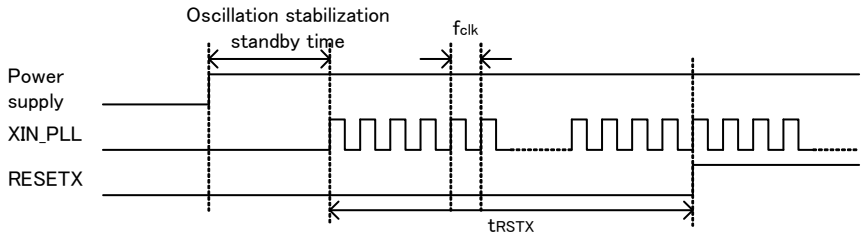

Figure 6 Reset Timing

Item	Symbol	Specification			Unit	Remarks
		min	typ	max		
Clock frequency	f_{CLK}	16.9302	16.9344	16.9386	MHz	
Reset L interval	t_{RSTX}	5	-	-	us	

2. SEL_SLAVE

MODE1/MODE2, 3 selection input signal

Signal name	I/O	Function	Remarks
SEL_SLAVE	I	Selects MODE1 or MODE2, 3.	H: MODE1, L: MODE2, 3

SEL_SLAVE selects MODE1 (STAND ALONE MODE) or MODE 2/3 (SLAVE MODE).
By selecting SEL_SLAVE, SLAVE mode terminal setting is enabled.
SEL_SLAVE is set only at power ON. Note that change of selection after power ON is ignored.

3. SEL_MP3

MPEG Audio Layer 1, 2, 3 play selection signal

Signal name	I/O	Function	Remarks
SEL_MP3	I	MPEG Audio Layer selection	H: Can play MP3 only.L: Can play MP1, MP2 and MP3.

SEL_MP3 allows you to select the layer of the MPEG audio to be played. When enabling all the files having mp1, mp2 or mp3 as the file extension to be played, enter L. When enabling mp3 only, enter H.
SEL_MP3 is set only at power ON. Note that change of election after power ON is ignored.

4. SEL_DOUT

Audio output selection signal

Signal name	I/O	Function	Remarks
SEL_DOUT	I	Audio output selection	H: Line output, L: Digital output(I²S, SPDIF)

This SEL_DOUT selects audio output signal.

Table 1. “Audio output” shows the audio outputs for each MODE.

Also table 2. ”I²S_fs” shows the I²S output formats for each MODE.

For command, see Chapter VII

"TEST terminal" needs to be pull-up to 3.3V power supply.

Table 1. Audio output

Pin No.	MODE1						MODE2,3								
	SEL_DOUT=H			SEL_DOUT=L			SEL_DOUT=H			SEL_DOUT=L					
										I2S			SPDIF ON		
	function	I/O	PU	function	I/O	PU	function	I/O	PU	function	I/O	PU	function	I/O	PU
44	Line Out Rch	O	OFF	HiZ	O	OFF	Line Out Rch	O	OFF	HiZ	O	OFF	HiZ	O	OFF
46	Line Out Lch	O	OFF	HiZ	O	OFF	Line Out Lch	O	OFF	HiZ	O	OFF	HiZ	O	OFF
53	LED_ACCESS	O	OFF	I2S LR CLOCK	O	OFF	TEST terminal	I	ON	I2S LR CLOCK	O	OFF	SPDIF	O	OFF
54	LED_RANDOM	O	OFF	I2S BIT CLOCK	O	OFF	TEST terminal	I	ON	I2S BIT CLOCK	O	OFF	TEST terminal	I	OFF
55	LED_REPEAT	O	OFF	I2S LRDATA	O	OFF	TEST terminal	I	ON	I2S LRDATA	O	OFF	TEST terminal	I	OFF

*PU・・・Pull-Up

Table 2. I²S_fs

MODE1	32fs
MODE2/3	Can select 32fs, 48fs, 64fs by command.

SEL_DOUT is set only at power ON. Note that change of selection after power ON is ignored.

5. SEL_VOL

Sound volume operation selection signal

Signal name	I/O	Function	Remarks
SEL_VOL	I	Sound volume operation	H: Sound volume operation enabled, L: Sound volume operation disabled

SEL_VOL selects whether sound volume operation is to be enabled or disabled.

Sound volume operation is enabled when SEL_VOL=H.

Initial value of audio output is -24.1dB at power ON.

Sound volume operation is disabled when SEL_VOL=L. Audio output is fixed to 0dB.

Figure 7 shows the relationship between audio output and sound volume step.

SEL_VOL is set only at power ON. Note that change of selection after power ON is ignored.

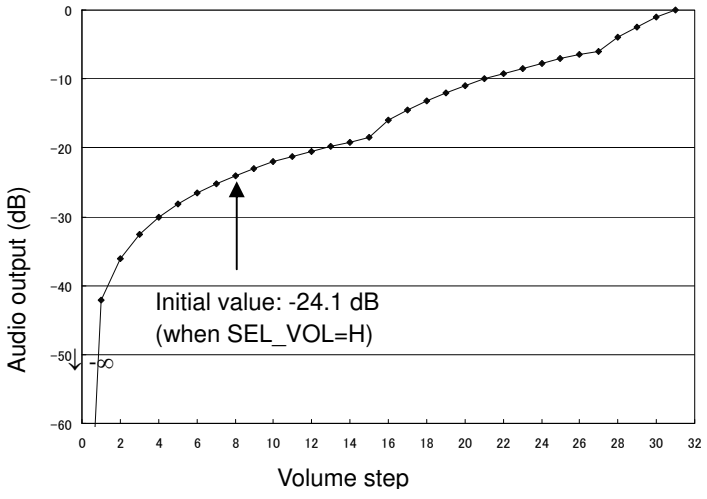

Figure 7 Volume Step Function

6. SEL_APLAY

Auto play selection signal at power ON/device recognition

Signal name	I/O	Function	Remarks
SEL_APLAY	I	Auto play selection signal at device recognition	H: Stop after recognizing device, L: Play after recognizing device

SEL_APLAY selects whether the audio data in the memory is to be automatically played when a memory device (USB memory or SD card) is inserted at power ON or when the system recognizes the memory device inserted. SEL_APLAY can be selected only in MODE1. Since selection of SEL_APLAY is ignored in MODE2/3, select it from Pull-up. When MODE2/3 is selected, audio data is halted after the system recognizes a device.

7. SEL_UTPKT

USB test packet

Signal name	I/O	Function	Remarks
SEL_UTPKT	I	USB test packet send	H: Disabled, L: USB test packet send

A test packet signal is output from USB_DP terminal or USB_DM terminal when L is set to SEL_UTPKT at power ON.
Once enabled, SEL_UTPK keeps that state regardless of operation modes and sends out a test packet.
A test packet signal is continuously output until power turns OFF. Use SEL_UTPKT when evaluating the USB terminal. In other cases, use it from Pull-up.

8. Audio line output

Audio line output

Signal name	I/O	Function	Remarks
LDACO	O	Lch audio line output	-
RDACO	O	Rch audio line output	-

These signals are decoded MP3 music audio data line outputs.
They turn ON when the line output is selected by SEL_DOUT terminal.
Sample rate converter converts the sample rate 48kHz and 32kHz to 44.1kHz and outputted.

9. MUTE control output

Audio MUTE

Signal name	I/O	Function	Remarks
AMUTE	O	Audio mute control terminal	H: At audio output, L: At mute

This terminal outputs H at audio output and L at mute.
This signal can be used as flag for external amplifier when mute audio output at power ON or FF/FB (silence).
Figure 8 shows the operation waveform.

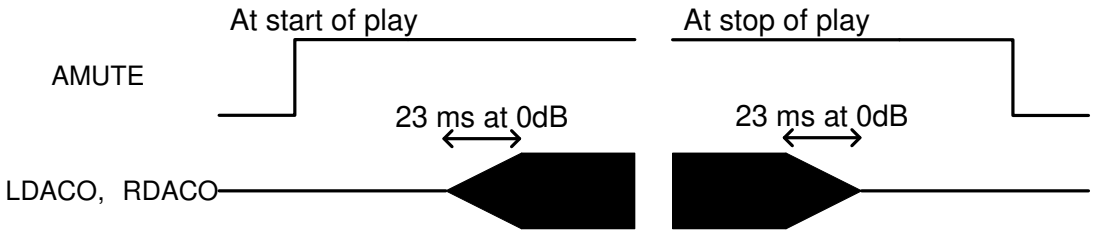

Figure 8 Waveform at Audio Mute

10. KEY input format

3x4 matrix command input

Signal name	I/O	Function	Remarks
KEY_ROW1	I	KEY matrix I/O signal	-
KEY_ROW2	I		-
KEY_ROW3	I		-
KEY_ROW4	I		-
KEY_COL1	O		-
KEY_COL2	O		-
KEY_COL3	O		-

Configure a circuit for the matrix signals terminals for KEY commands as shown in the applied circuit diagram figure 9.

The operation corresponding to the key pressed over the circuit is performed.

Details of each operation are explained in Chapter 21.

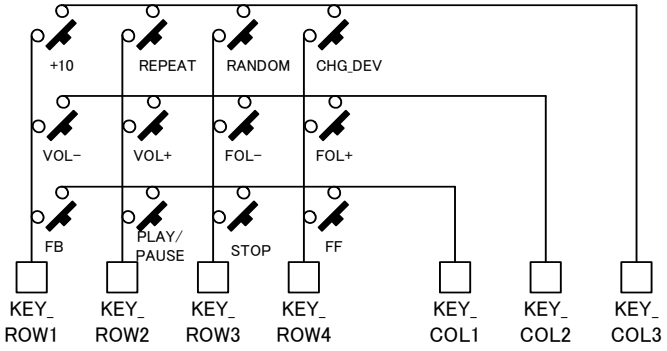

Figure 9 KEY Matrix Applied Circuit Diagram

11. I²C interface format

I²C serial interface

Signal name	I/O	Function	Remarks
SCL	I	I²C interface clock input	-
SDA	I/O	I²C interface data I/O	-
A0	I	Slave address selection terminal	Slave address [0] bit setting terminal
A1	I	Slave address selection terminal	Slave address [1] bit setting terminal

This is an I²C serial interface terminal. By inputting L to SEL_SLAVE terminal, the interface terminal becomes enabled.

The terminal supports slave I²C operation.

11.1 I²C protocol

When I²C bus is in IDLE, SDA and SCL are set to H by the external Pull-up resistance. When starting communications, the master sets SDA to L while SCL is set to H (Start condition). When ending communications, the master sets SDA to H while SCL is set to H (Stop condition). During transfer, SDA is changed only when SCL is set to L. Figure 10 shows Start condition, Stop condition of I²C.

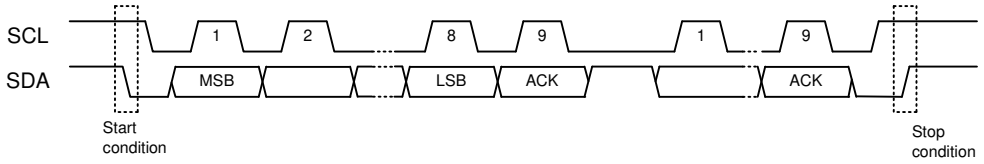

Figure 10 I²C start, stop condition

11.2 Slave address

An I²C bus slave address corresponds to the 7-bit addressing mode. As shown in Table 3., you can select the slave address using input of A0 terminal and A1 terminal. Figure 11 shows the slave address transfer format.

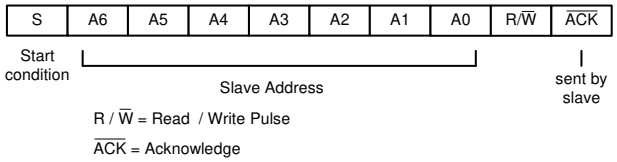

Figure 11 Slave Address Transfer Format

Table 3. Settable Slave Addresses

MSB A6	A5	A4	A3	A2	A1 terminal	LSB A0 terminal
1	0	0	0	0	0	0
1	0	0	0	0	0	1
1	0	0	0	0	1	0
1	0	0	0	0	1	1

11.3 Write protocol from master

To send a master command using an I²C bus, follow the transfer protocol shown in Figure 12. For details on each command, see Chapter of “Command operation”.

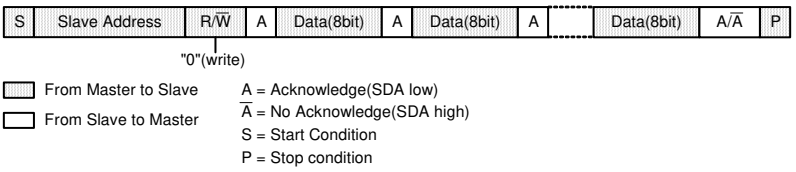

Figure 12 Command send protocol

11.4 Read protocol to master

To send reception data using an I²C bus from the slave to the master, follow the transfer protocol shown in Figure 13. First, transfer the status read command (step1). Then, input SCL clock of required bytes in step 2 to read the status.

When the device is BUSY at reception of device status or memory data, the I²C bus may possibly be occupied by the device during BUSY. This LSI transfers the bus to the master so as not to generate such bus occupation. However, as a BUSY state still exists inside of the system, appropriate data may not be transferred during BUSY. Therefore, the first byte of transfer data (Step2) is used to judge the transfer data is enabled/disabled. When specifying addresses from the master to the slave and the first byte of the transfer data immediately after data transfer is required is 0x00, transfer data from the slave is enabled. If the first byte is 0xFF, it shows the BUSY state. Therefore, the transfer data should be disabled. If this happens, retry command transfer at Step 1 to read out the status.

Figure 14 shows the relationship between the transfer data and BUSY.

* For further information on BUSY, see Chapter 17.

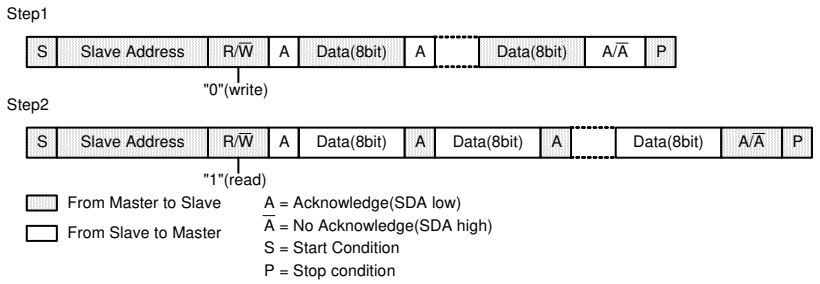

Figure 13 Status Reception Protocol

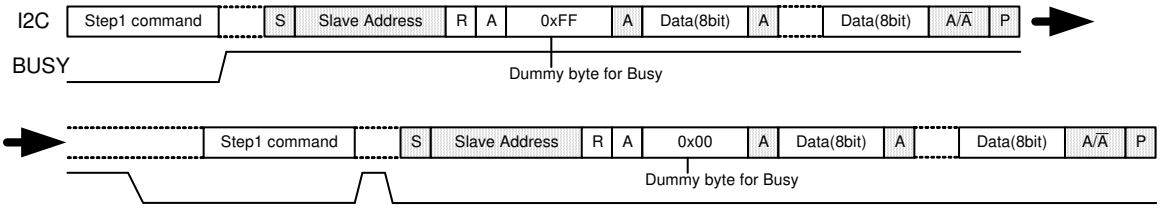

Figure 14 Relationship between Transfer Data and BUSY

11.5 I²C Bus line electrical specification and timing

SDA and SCL bus-line characteristic (Unless specified, Ta=25℃, VDD1=3.3V)

	Parameter	Code	Min.	Max.	Unit
1	SDA, SCL H input voltage	VIH	VDD*0.7	VDD	V
2	SDA, SCL L input voltage	VIL	DVSS	VDD*0.3	V
3	SDA H output voltage	VOH	VDD-0.4	VDD	V
4	SDA L output voltage	VOL	0	0.4	V
5	SCL clock frequency	fSCL	0	400	kHz
6	Bus-free-time between "Stop" condition and "Start" condition	tBUF	1.3	—	us
7	Hold time for "Start" condition After this, the first clock pulse is generated.	tHD;STA	0.6	—	us
8	LOW status hold-time of SCL clock	tLOW	1.3	—	us
9	HIGH status hold-time of SCL clock	tHIGH	0.6	—	us
10	Data-hold-time	tHD;DAT	0*	—	us
11	Date-setup-time	tSU;DAT	100	—	ns
12	Rising time of SDA and SCL signal	tR	20+0.1*Cb	300	ns
13	Fall time of SDA and SCL signal	tF	20+0.1*Cb	300	ns
14	Setup time of "Stop" condition	tSU;STO	0.6	—	us
15	Capacitive load of each bus-line	Cb	—	400	pF

The above-mentioned numerical values are all the values corresponding to $V_{IH\ min}$ and $V_{IL\ max}$ level.

*To exceed an undefined area on falling edged of SCL, transmission device should internally offer the hold-time of 300ns or more for SDA signal ($V_{IH\ min}$ of SCL signal).

Because the "Repeated Start" condition to send "Start" condition without sending "Stop" condition doesn't correspond, after sending "Start" condition, always send "Stop" condition.

Neither terminal SCL nor terminal SDA correspond to 5V tolerant.

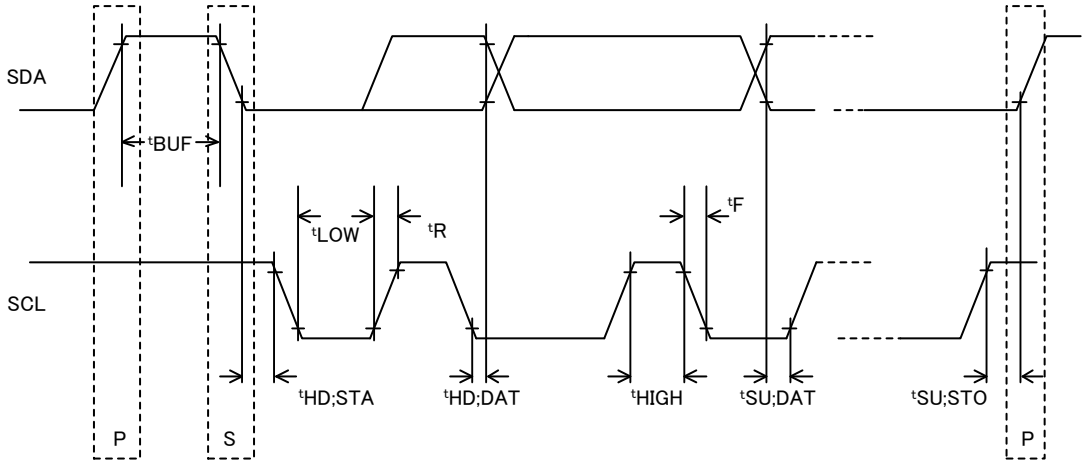

Figure 15 Timing chart

12. I²S format

I²S format

Signal name	I/O	Function	Remarks
LRCK	O	I²S Bit clock output (fs=44.1kHz)	-
BCK	O	I²S Bit clock output	-
DATA	O	I²S data output	-

This is digital audio interface terminal. By inputting L to SEL_DOUT terminal, the interface terminal becomes enabled. When selecting the I²S digital audio output, the output format varies depending on MODE. MODE2 allows you to select 32fs, 48fs or 64fs. *See Chapter 4.

Figures 16, 17 and 18 show the I²S format to be output.

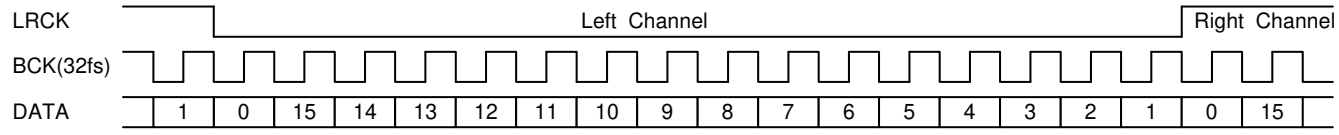

Figure 16 I²S Output Timing (32fs)

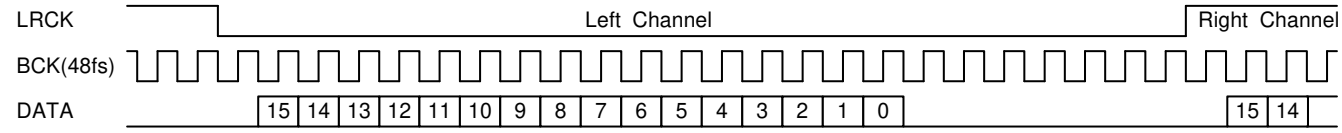

Figure 17 I²S Output Timing (48fs)

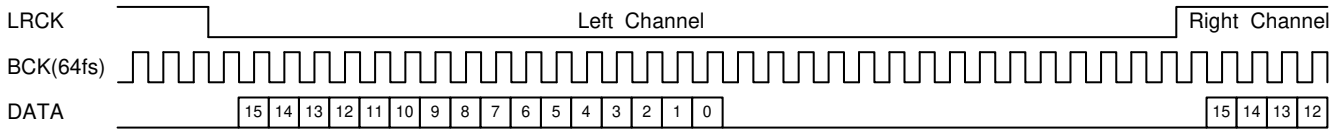

Figure 18 I²S Output Timing (64fs)

12.1 I²S Timing

48fs I²S format (Unless specified, Ta=25℃, VDD1=3.3V, Load : 20pF)

Parameter	Symbol	Min	Typ	Max	unit
BCK Clock Frequency	Tbck	-	472.4	-	ns
BCK Low time	Tbck1	216	236	-	ns
BCK High time	Tbck2	216	236	-	ns
LRCK Clock Frequency	Tlrck	-	44.1	-	kHz
LRCK Output delay	Tlrck1	-20	0	20	ns
DATA Output delay	Tda1	-20	0	20	ns
Output High Voltage	Voh	VDD1-0.4	-	-	V
Output Low Voltage	Vol	-	-	0.4	V

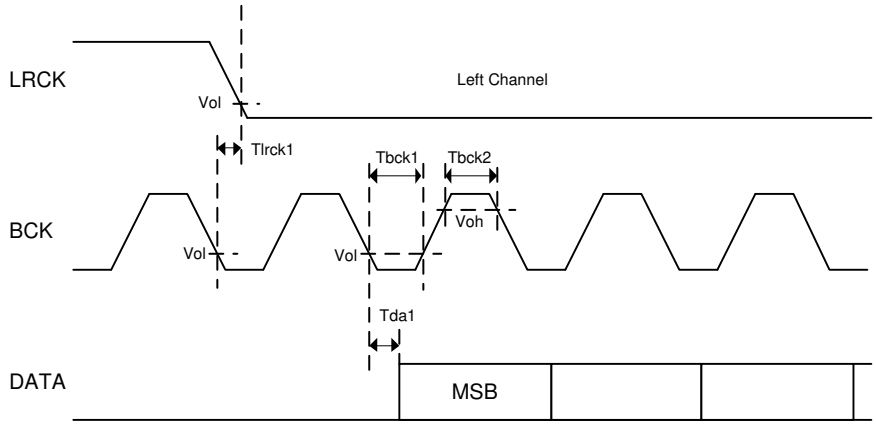

Figure 19 Timing chart

13. SPDIF format

SPDIF format

Signal name	I/O	Function	Remarks
SPDIF	O	SPDIF output	-

SPDIF output becomes enabled by setting SEL_DOUT terminal to L and setting this condition using the I²C command.

Figure20 shows the SPDIF digital audio signal output format.

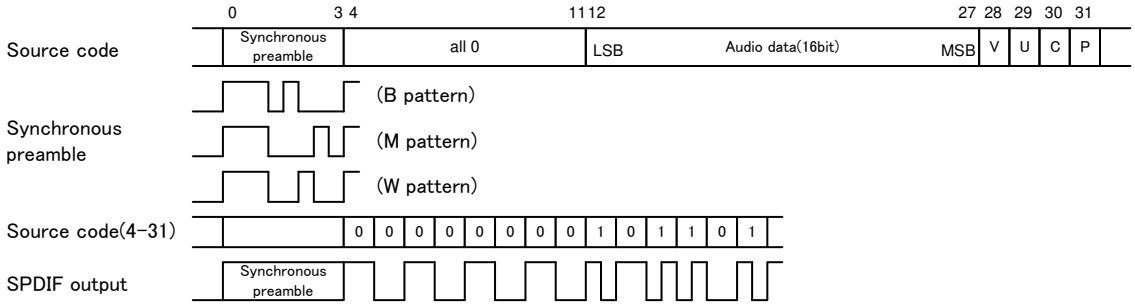

Figure 20 SPDIF Output Format

A sub-frame of SPDIF is composed of synchronous preamble, 16-bit audio data, V bit (validity flag), U bit (user data), C bit (channel status) and P bit (parity bit).

Output rate is fixed to 1X speed.

SPDIF outputs synchronous preamble (source code 0-3) as it is and others (source code 4-31) as bi-phase output. It outputs L while the operation is stopped.

Synchronous preamble and C bit use 32 frames (≈4.4ms) as one cycle. Table 4. and Table 5 show these formats.

V bit is fixed to L. U bit uses 98 frames (≈13.3ms) as one cycle.

Table 4. Synchronous Preamble Pattern

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	B	W	M	W	M	W	M	W	M	W	M	W
1	M	W	M	W	M	W	M	W	M	W	M	W
:	:	:	:	:	:	:	:	:	:	:	:	:
31	M	W	M	W	M	W	M	W	M	W	M	W

Table 5. C Bit Format

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	0		0		0		0		0		0	
1	0		0		1		0		0		0	
2	0		0		0		0		0		0	
3	0		0		1	0	0	1	0		0	
4	0		0		0		0		0		0	
5	0		0		0		0		0		0	
:	:		:		:		:		:		:	
31	0		0		0		0		0		0	

Table 6. U Bit Format

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:	:
97	1	0	0	0	0	0	0	0	0	0	0	0

P bit is set to 1 if the number of “1s” of source codes 4-30 is odd, and set to 0 if the number is even. Therefore, the number of source codes which turn to 1 for one data must be an odd value, SPDIF ends with L output and preamble output always starts in the same direction.

13.1 SPDIF Timing

(Unless specified, Ta=25℃, VDD1=3.3V, Load : 20pF)

Parameter	Symbol	Min	Typ	Max	unit
SPDIF Clock Frequency	Tck	-	2.822	-	MHz
SPDIF Clock High time	Tck1	150	177	-	ns
SPDIF Clock Low time	Tck2	150	177	-	
Output High Voltage	Voh	VDD1-0.4	-	-	V
Output Low Voltage	Vol	-	-	0.4	V

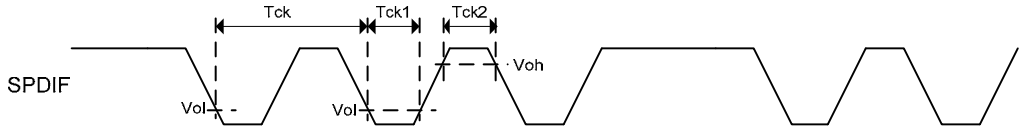

Figure 21 Timing chart

14. USB I/F

USB I/O I/F

Signal name	I/O	Function	Remarks
USB_DP	I/O	USB D+I/O terminal	-
USB_DM	I/O	USB D-I/O terminal	-
REXTI	O	USB bias resistance connection terminal	Connect resistance of 12kΩ ± 1% to GND.

Differential signals of USB_DP and USB_DM enable communications with USB devices.
REXTI terminals become bias resistance connection terminals of the USB-PHY block.

15. SD I/F

SPI interface for SD memory card I/F

Signal name	I/O	Function	Remarks
SD_CS	O	SPI chip select	-
SD_CLK	O	SPI clock	-
SD_DI	O	SPI data input	-
SD_DO	I	SPI data output	-
SD_CON	I	SD card connect detection terminal	H: Not detecting SD card connection. L: Detecting SD card connection.

These I/F enable communication with SD memory cards through SD memory card slots.

Since SD memory card slot requires detecting insertion of SD memory card, use of slot equipped with SD memory card detecting terminal and connection to SD_CON terminal are required.

SD_CON terminal is pulled up within the device and detects SD memory card connection by L input.

15.1 SD I/F Timing

(Unless specified, Ta=25℃, VDD1=3.3V, Load : 20pF,10kΩ)

Parameter	Symbol	Min	Typ	Max	unit
SD_CS Setup time	Tcss	-	0.25	-	us
SD_CS Hold time	Tcsh	-	1.15	-	us
SD_CLK Clock Frequency	Tclk	-	4.23	-	MHz
SD_DI Output delay	Tod	-20	-	20	ns
SD_DO Data in Setup time	Tds	20	-	-	ns
SD_DO Data in Hold time	Tdh	120	-	-	ns
Output High Voltage	Voh	0.625*VDD1	-	-	V
Output Low Voltage	Vol	-	-	0.25*VDD1	V

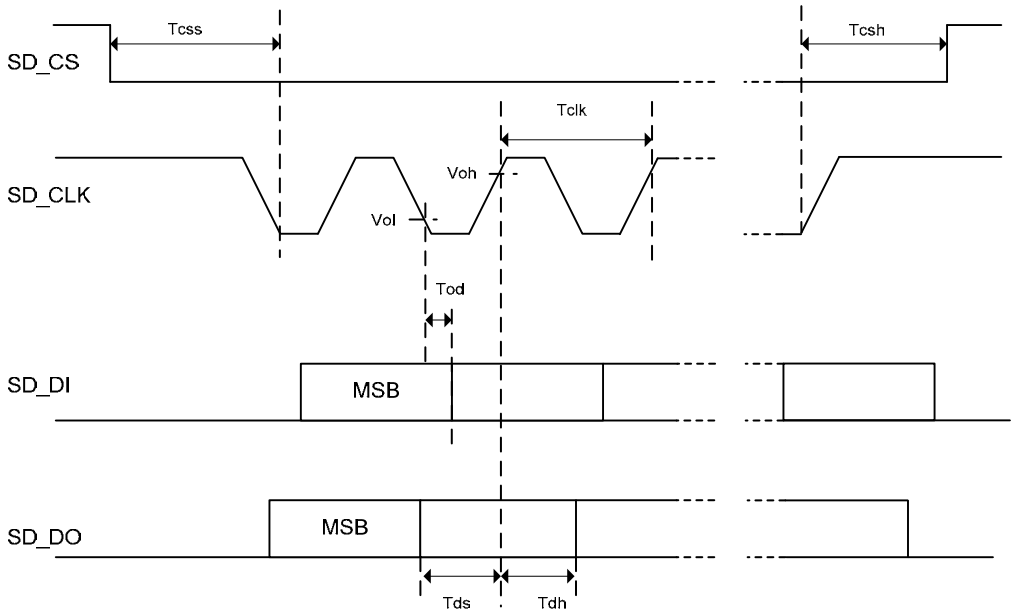

Figure 22 Timing chart of SPI for SD memory card

16. MCHNG

Playing sound tune number detection output

Signal name	I/O	Function	Remarks
MCHNG	O	Music tune number change detection output signal	H: Playing, L: Tune completed/stopped

This signal outputs change of file to be played during playing MP3 file in the memory device.

MCHNG correctly outputs "H" during MP3 decode sequence, outputs "L" during "STOP" status.

Connect it to the interruption port of the microcomputer.

17. BUSY

BUSY state detection output

Signal name	I/O	Function	Remarks
BUSY	O	BUSY state detection output signal	H: Busy, L: Not Busy

This signal outputs to indicate that this LSI is in BUSY.

BUSY signal analyzes commands from the master and outputs H until the operation is executed.

This LSI ignores command input during BUSY. However, only the ABORT and STOP commands can be accepted even during BUSY, which can be executed. *See Chapter 11.

18. IRPTO

CONFIG outputs it for two more device connection state detection.

Signal name	I/O	Function	Remarks
IRPTO	O	USB CONFIG outputs it for two more device connection state detection.	H: Detection , L: Undetection.

When the USB device is chosen, output it to show that the USB device that two USB CONFIGURATION DESCRIPTOR or more has in this LSI is connected. The timing of an output is dependent on the connected USB device.

19. TEST terminal

By the terminal setting of TEST15, TEST16 and TEST17, It is possible to following function.

TEST15	TEST16	TEST17	Function
H	H	H	Full function effective
L	L	L	Only WMA and MP3 can play-back. The AAC file is disregarded. *1
H	L	L	The IRPTO function is invalidated. *2

*1 Except for BU94601KV

*2 Only BU94604BKV

20. File detection

20.1 Function

- This function supports FAT16 and FAT32 file systems. (It does not support NTFS and FAT12.)
- The maximum number of playable files per folder

Table 7. Maximum Number of Playable Files

	Root folder	Sub folder
FAT16	512	65534
FAT32	65535	65534

The number of files described above contains unsupported files and folders. If unsupported files and folders exit within the folder and exceed the maximum number, all the supported files may not be played.

- Files less than 100 can be sorted by UNICODE in the FAT order within the folder. Files over 100 are sorted in the FAT order. Also, the folders can be sorted in the same manner and those over 100 are sorted in the FAT order.
- The searchable folder hierarchy is of 8 layers containing the root folder. Figure 23 shows an example of memory layers.

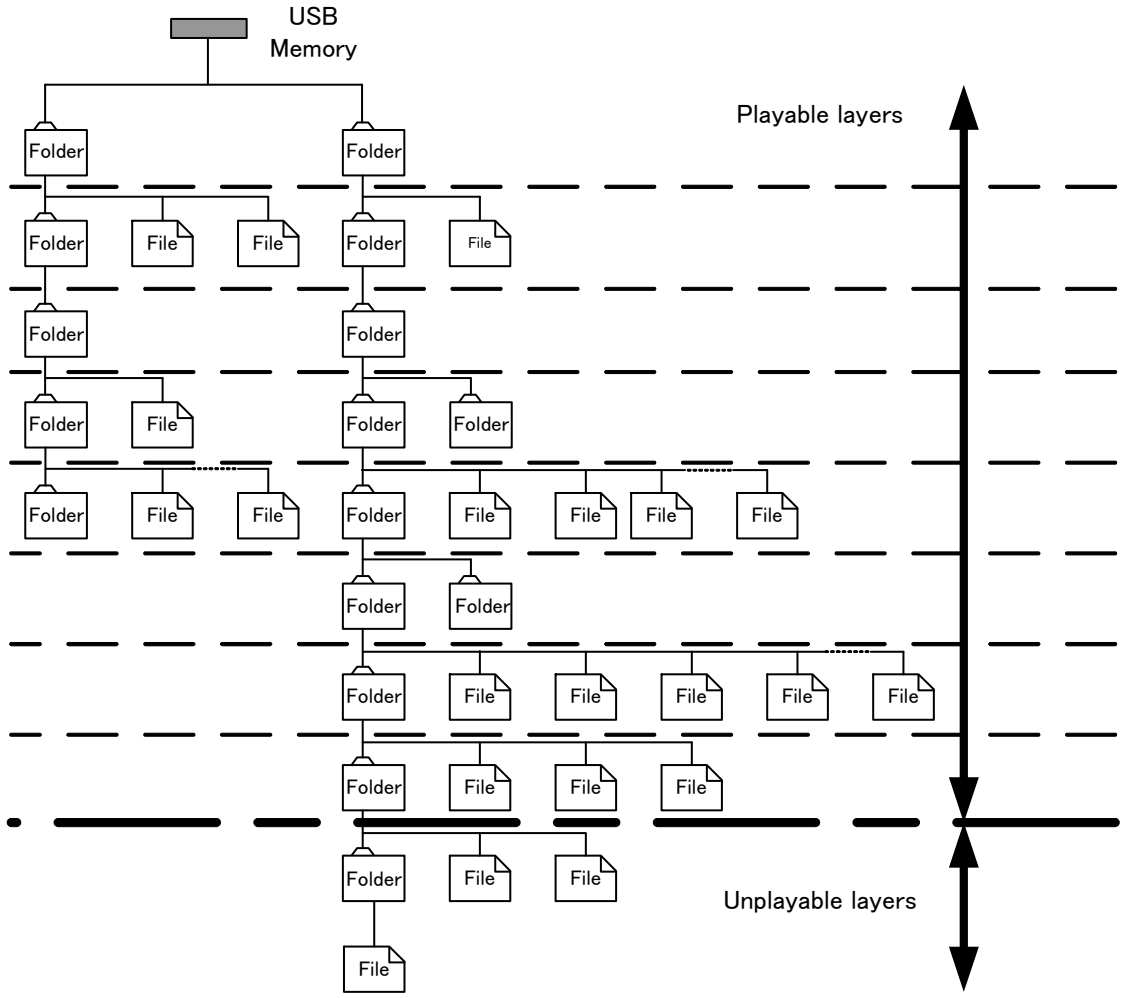

Figure 23 Example of Memory Layers