Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

USB Audio Decoder LSI Series

AAC/WMA/MP3 +SD Memory Card +CD-ROM+MP3 Record

BU94605AKV BU94607AKV BU94702AKV BU94705AKV

●Description

BU94605AKV BU94607AKV BU94702AKV BU94705AKV are MP3 encoder + WAV/AAC/WMA/MP3 decoder IC which contains program download function from external serial Flash ROM and contains USB host, SD card I/F, CD-ROM I/F, audio DAC, system controller, regulator for internal CORE power supply.

●Features

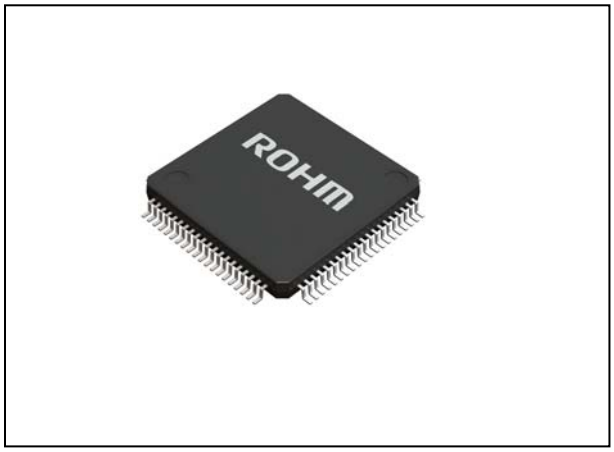
- USB2.0 Full Speed host I/F function contained.
- SD card I/F function contained.
- I^2C format I/F function contained.
- Protocol conversion from I^2C to USB HID or from USB HID to I^2C. *1
- MP3 encode function contained. *2,*3,*10
- MP3 decode function contained. *4
- WMA decode function contained. *5
- AAC decode function contained. *6,*7
- WAV format file playing function contained. *7
- Sample Rate Converter contained. *8
- System Controller contained.
- FAT analysis function contained.
- CD-ROM I/F function and CD-ROM decoder function contained.
- Browsing function of File Names, Folder Names on music playing contained.
- ID3TAG and WMATAG and AACTAG Analysis.
- Fast forward/backward playing function contained.
- Resume function contained.
- File data Reading/Writing function contained.
- Program download function from external serial Flash ROM contained.
- Audio DAC and Sound Effect function contained.
- Digital Audio Out function contained. *9
- Regulator for internal CORE power supply contained.

●Applications

Audio products, etc

●Package

VQFP80 14.00mm x 14.00mm x 1.60mm



VQFP80

*1 BU94705AKV and BU94607AKV only.
*2 BU94705AKV and BU94702AKV only.
*3 Available for MPEG1, Layer3, support up to 2X inputspeed.
*4 Available for MPEG1, 2 and 2.5, Layer 1, 2 and 3.
*5 Available for WMA9 standard and not available for DRM.
*6 Available for MPEG4 AAC-LC and not available for DRM.
*7 Not available for CD-ROM.
*8 Convert to 44.1 kHz.
*9 Available for I^2S, EIAJ, S/PDIF format.
*10 Writing speed to the memory (USB memory, SD memory card) of the encoding data depends on the response speed of the memory greatly. Examine the memory which a connection is presumed fully, and limit the encoding format specifications of the set because real time encoding can't be realized when a writing response speed is slow.

●Line up

Part number	MP3 encoder	iPod	Package		Ordering part number
BU94605AKV	Not Supported	Not supported	VQFP80	Reel of 1000	BU94605AKV-E2
				Tray of 1000	BU94605AKV
BU94607AKV	Not Supported	Supported	VQFP80	Reel of 1000	BU94607AKV-E2
				Tray of 1000	BU94607AKV
BU94702AKV	Supported	Not supported	VQFP80	Reel of 1000	BU94702AKV-E2
				Tray of 1000	BU94702AKV
BU94705AKV	Supported	Supported	VQFP80	Reel of 1000	BU94705AKV-E2
				Tray of 1000	BU94705AKV

○Product structure:Silicon Monolithic integrated circuit ○Radiation resistance design is not arranged

●**Basic circuit application diagram**

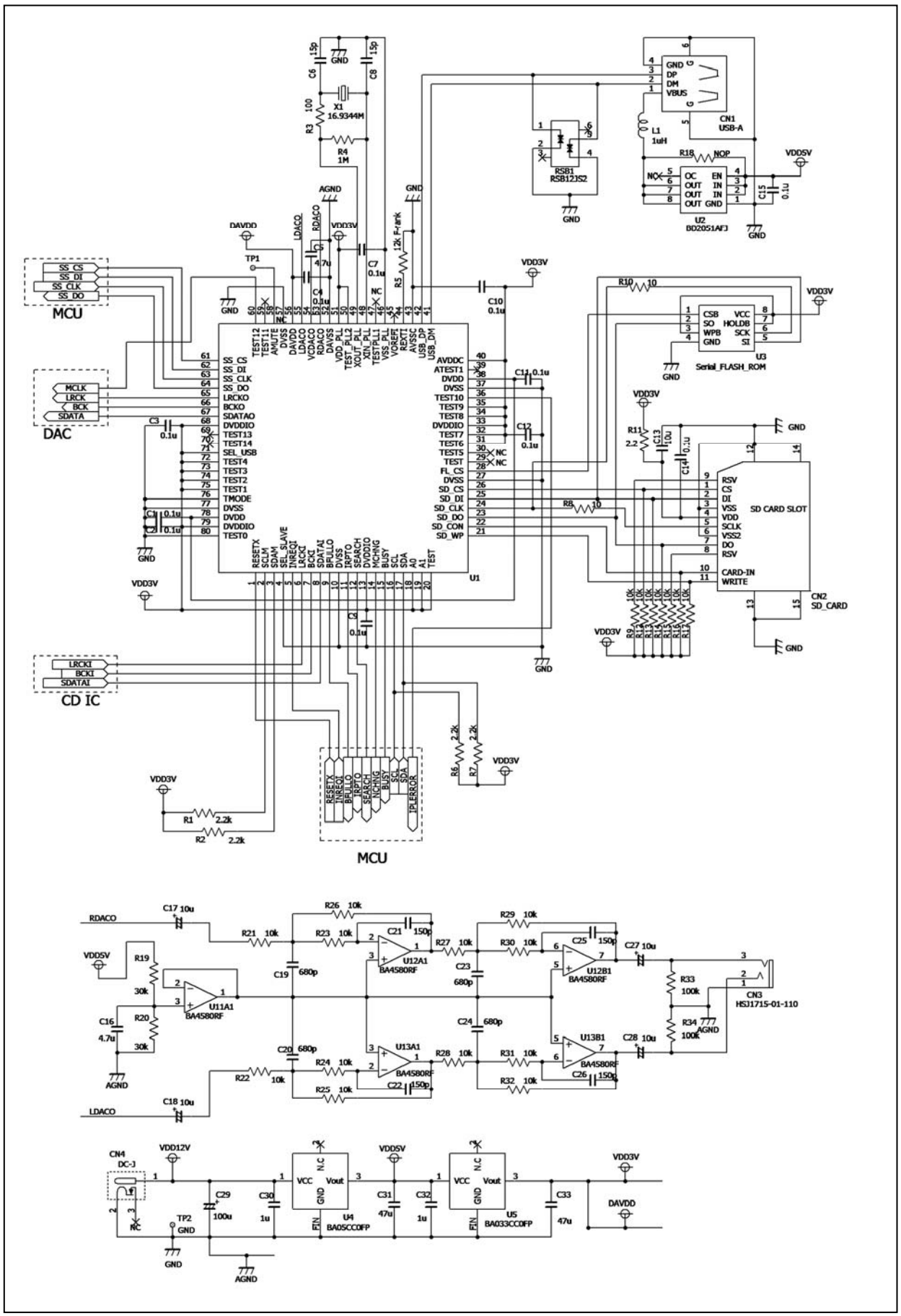


Figure 1. an example of connection circuit application

●Difference of BU94605AKV BU94607AKV BU94702AKV BU94705AKV features

Item	BU94605AKV	BU94607AKV	BU94702AKV	BU94705AKV
Package	VQFP80		VQFP80	
Number of pins	80pin		80pin	
Power supply	3.3V (inner 1.5V regulator)		3.3V (inner 1.5V regulator)	
USB Host I/F	USB Full speed(12Mbps), USB mass storage class		USB Full speed(12Mbps), USB mass storage class	
SD card I/F	SPI mode SD, SDHC, MMC, mini-SDcard		SPI mode SD, SDHC, MC, mini-SDcard	
iPod	Supported	Not supported *1	Supported	Not supported *1
MP3 encode	Not supported		Supported	
I^2C command I/F (Slave)	Supported		Supported	
Change the Setting of timeout and retry mode in USB memory or SD card mount operation	Supported		Supported	
Audio line output	Supported		Supported	
Digital audio output	I^2S, EIAJ, SPDIF		I^2S, EIAJ, SPDIF	
Sample rate convertor	Supported (44.1kHz)		Supported (44.1kHz)	
clock	16.9344MHz (*1)		16.9344MHz (*1)	
Playable MP3 files	*.mp3, *.mp2, *.mp1		*.mp3, *.mp2, *.mp1	
Playable WMA files	*.asf, *.wma		*.asf, *.wma	
Playable AAC files	*.m4a, *.3gp, *.mp4		*.m4a, *.3gp, *.mp4	
Playable WAV files	*.wav		*.wav	
Browsing function	Supported		Supported	
File writing function	Supported		Supported	
File reading function	Supported		Supported	
Play List function	Supported		Supported	

*1 for using of BU94607AKV and BU94705AKV, It is necessary to become a licensee of Apple Inc. regarding "Made for iPod/iPhone/iPad License".

●Block diagram

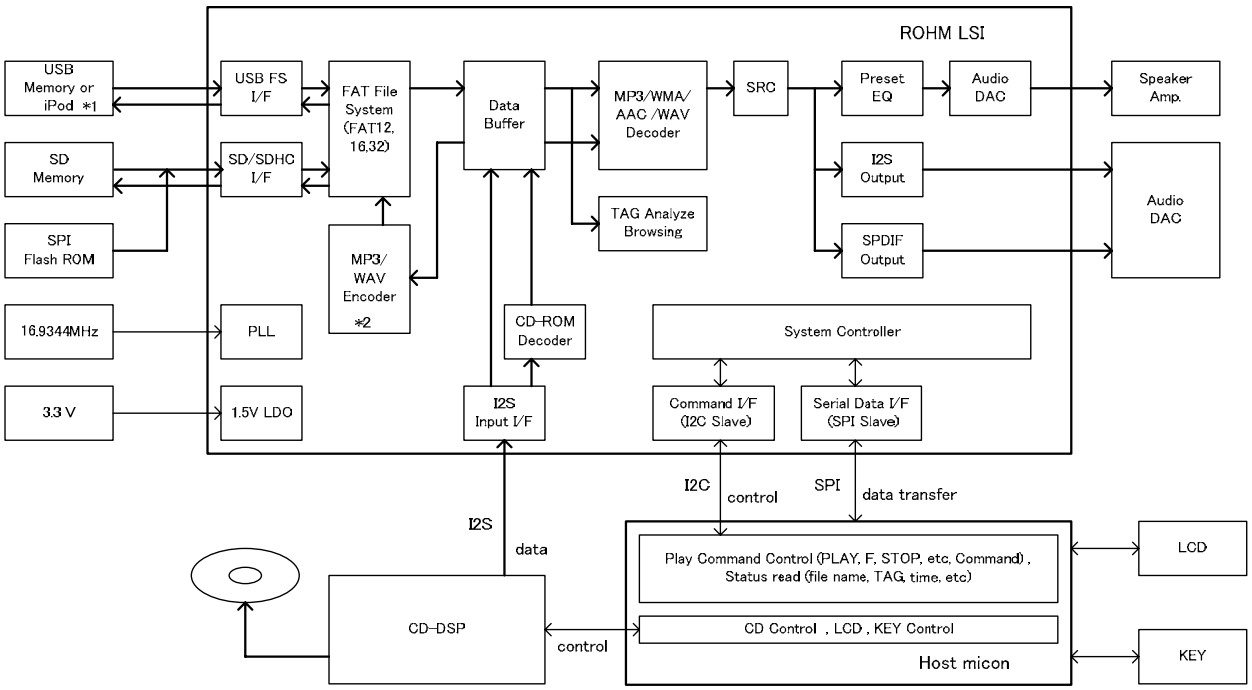


Figure 2. Block diagram

*1 BU94705AKV and BU94607AKV only.
*2 BU94705AKV and BU94702AKV only.

●**Arrangement of Terminals**

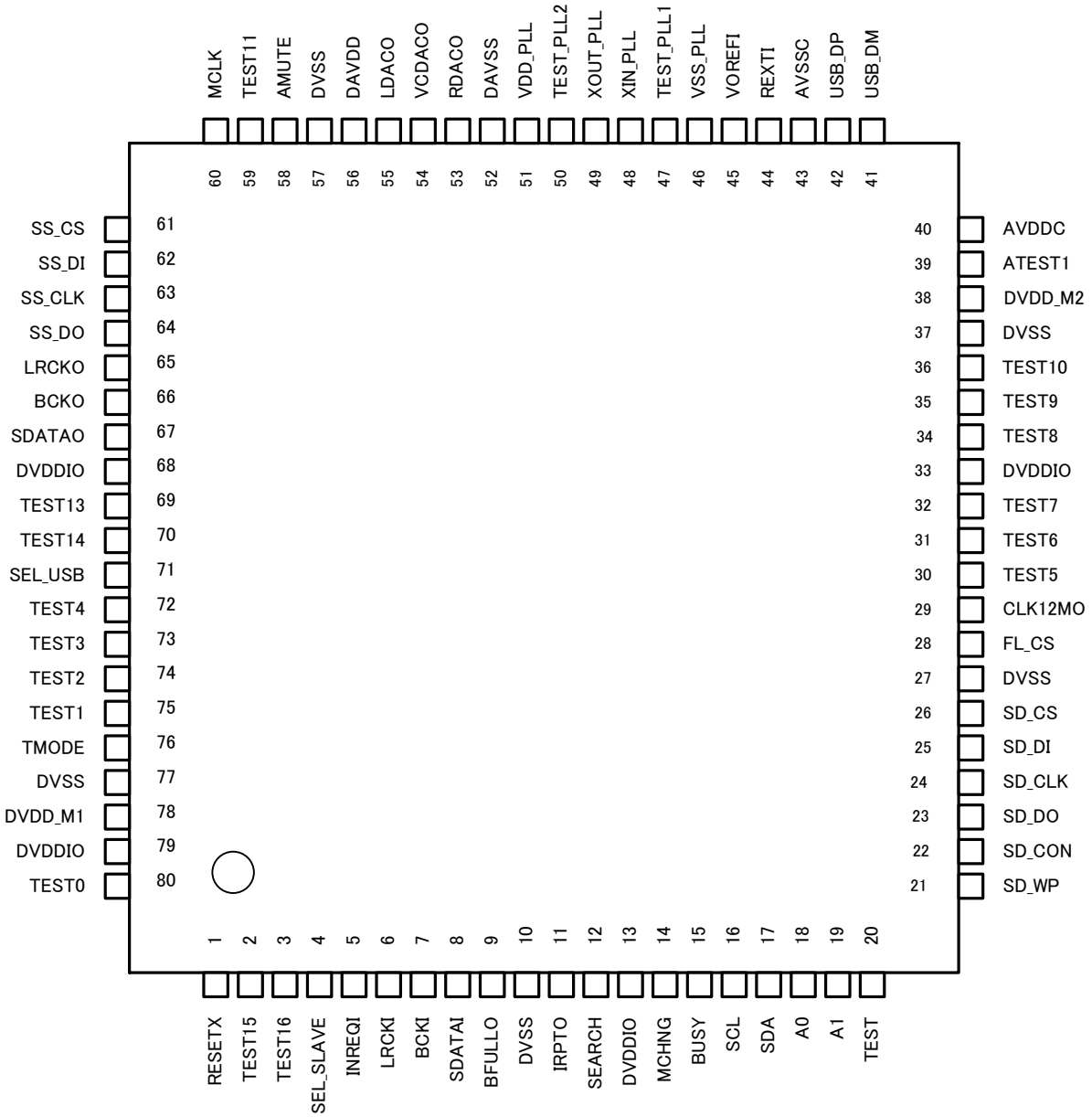


Figure 3. Arrangement of Terminals

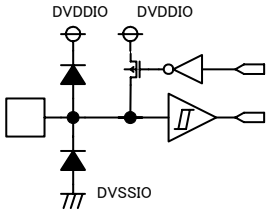
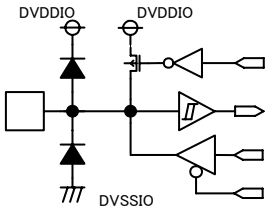
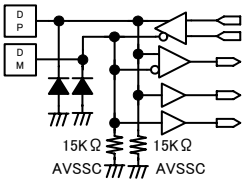
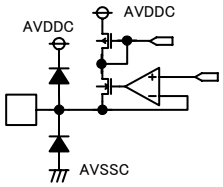
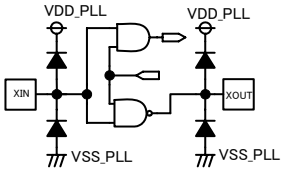
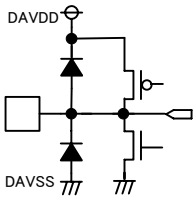
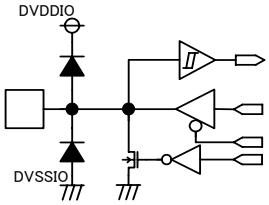
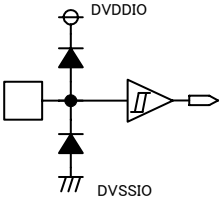
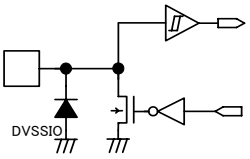
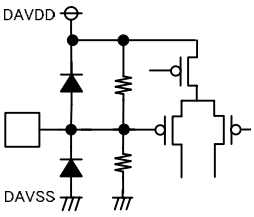
●**Description of Terminals**

No	Pin Name	IO Cir	IO	PU	Function
1	RESETX	A	I	PU*3	H: Release RESET, L: RESET
2	TEST15	I	O	*2	Test mode terminal. Pull it up at VDD1 power.
3	TEST16	I	I/O	*2	Test mode terminal. Pull it up at VDD1 power.
4	SEL_SLAVE	B	I	-	Test mode terminal. Connect it to GND.
5	INREQI	B	I	-	Input data valid terminal *5
6	LRCKI	B	I	-	Digital Audio channel clock input terminal
7	BCKI	B	I	-	Digital Audio bit clock input terminal
8	SDATAI	B	I	-	Digital Audio channel data input terminal
9	BFULLO	B	O	-	Input buffer full flag output terminal *5
10	DVSS	-	-	-	GND terminal
11	IRPTO	B	O	-	Connection interrupt output terminal *5
12	SEARCH	B	O	-	Search flag output terminal *5
13	DVDDIO	-	-	-	IO power (VDD1) terminal
14	MCHNG	B	O	-	File play end flag output terminal *5
15	BUSY	B	O	-	Command analysis BUSY output temrinal *5
16	SCL	I	I	*2	I^2C slave clock input terminal *5
17	SDA	I	I/O	*2	I^2C slave data I/O terminal *5
18	A0	B	I	-	I^2C slave address setting terminal
19	A1	B	I	-	I^2C slave address setting terminal
20	TEST	B	I	-	Test mode terminal. Pull it up at VDD1 power.
21	SD_WP	B	I	PU*3	SD card I/F WP detection terminal
22	SD_CON	B	I	PU*3	SD card I/F connection detection terminal
23	SD_DO	B	I	-	SD card I/F data input terminal
24	SD_CLK	B	O	-	SD card I/F clock output terminal
25	SD_DI	B	O	-	SD card I/F data output terminal
26	SD_CS	B	O	-	SD card I/F chip select output terminal
27	DVSS	-	-	-	GND terminal
28	FL_CS	B	O	-	Serial Flash ROM chip select output terminal
29	CLK12MO	B	O	-	12MHz CLK Output.
30	TEST5	B	O	-	Test mode terminal. Use it as OPEN.
31	TEST6	H	I	-	Test mode terminal. Pull it up at VDD1 power.
32	TEST7	H	I	-	Test mode terminal. Pull it up at VDD1 power.
33	DVDDIO	-	-	-	IO power (VDD1) terminal
34	TEST8	H	I	-	Test mode terminal. Pull it up at VDD1 power.
35	TEST9	H	I	-	Test mode terminal. Pull it up at VDD1 power.
36	TEST10	B	O	-	Test mode terminal. (IPL ERROR status). Use it as OPEN.
37	DVSS	-	-	-	GND terminal.
38	DVDD_M2	-	-	-	CORE power (VDD2) monitor terminal Short-circuit to DVDD_M1. Connect bypass capacitor.
39	ATEST1	-	O	-	USB test terminal (OPEN).
40	AVDDC	-	-	-	USB power (VDD1) terminal.
41	USB_DM	C	I/O	-	USB D-I/O terminal.
42	USB_DP	C	I/O	-	USB D+ I/O terminal.
43	AVSSC	-	-	-	USB GND terminal.
44	REXTI	D	O	-	USB reference voltage output terminal Connect to AVSSC terminal using USB bias resistor (12kΩ). Please arrange the resistance of 12kΩ near PIN. The wiring for the PIN side must not intersect with other signal lines.

45	VOREFI	-	O	-	USB test terminal (OPEN).
46	VSS_PLL	-	-	-	PLL GND terminal.
47	TEST_PLL1	-	I	-	PLL test terminal. (OPEN)
48	XIN_PLL	E	I	-	X'tal (16.9344MHz) connection input terminal. *4
49	XOUT_PLL	E	O	-	X'tal (16.9344MHz) connection output terminal. *4
50	TEST_PLL2	-	I	-	PLL test terminal. Pull it up at VDD1 power.
51	VDD_PLL	-	-	-	PLL power (VDD1) terminal.
52	DAVSS	-	-	-	Audio DAC GND terminal
53	RDACO	F	O	-	Audio DAC Rch line output terminal
54	VCDACO	J	O	-	Audio DAC reference voltage output terminal
55	LDACO	F	O	-	Audio DAC Lch line output terminal
56	DAVDD	-	-	-	Audio DAC power (VDD1) terminal
57	DVSS	-	-	-	GND terminal
58	AMUTE	G	O	-	Audio mute output (H: Mute OFF, L: Mute ON) terminal
59	TEST11	B	O	-	Test mode terminal. Use it as OPEN.
60	TEST12	B	O	-	Master Clock output(16.9344MHz)
61	SS_CS	B	I	-	SIO Slave CS input terminal
62	SS_DI	B	I	-	SIO Slave DATA input terminal
63	SS_CLK	B	I	-	SIO Slave clock input terminal
64	SS_DO	B	O	-	SIO Slave DATA output terminal
65	LRCKO	B	O	-	Digital Audio channel clock output / SPDIF output
66	BCKO	B	O	-	Digital Audio bit clock output
67	SDARAO	B	O	-	Digital Audio data output
68	DVDDIO	-	-	-	I/O power (VDD1) terminal
69	TEST13	B	O	-	Test mode terminal Use it as OPEN.
70	TEST14	B	O	-	Test mode terminal Use it as OPEN.
71	SEL_USB	B	I	PU *1*3	Preference detection device select(H: USB, L: SD)
72	TEST4	H	I	-	Test mode terminal. Pull it up at VDD1 power.
73	TEST3	H	I	-	Test mode terminal (IPL WRITE MODE1). Pull it up at VDD1 power.
74	TEST2	H	I	-	Test mode terminal (IPL WRITE MODE2). Pull it up at VDD1 power.
75	TEST1	H	I	-	Test mode terminal. Pull it up at VDD1 power.
76	TMODE	H	I	-	Test mode terminal. Connect it to GND.
77	DVSS	-	-	-	GND terminal
78	DVDD_M1	-	-	-	CORE power (VDD2) monitor terminal. Connect it to bypass capacitor.
79	DVDDIO	-	-	-	IO power (VDD1) terminal
80	TEST0	-	I	-	Test mode terminal. Connect it to GND.

*1 Pull-Up turns OFF when L is input.
*2 An external pull-up resistor is required because of Open Drain IO.
*3 please input L level directly without resistance when you input L to the terminal with Pull-Up (about 33 kΩ).
*4 Please confirm the optimal oscillation circuit parameters applicable to your systems or products with the oscillator manufacturer in advance.
*5 Please connect with the microcomputer terminal.

●**Terminal equivalent circuit diagram**

A	B	C	D
			
E	**F**	**G**	**H**
			
I	**J**		
			

●Description of each block's movement -part1

1. USB host interface

- Builds in the USB Full speed (12Mbps) HOST control function.
- Supports the USB mass storage class.
- Converts the protocol from I^2C to USB (HID) or vice versa during communications with the master microcomputer. *1
- Builds in isochronous transmission functions up to 192byte/Frame. *1
- Builds in the interrupt IN transfer function. *1
- Doesn't support external HUB.

*1 These functions are available for a device having two or more configurations.
BU94607AKV and BU94705AKV only.

2. SD card interface

- Supports the SPI mode.
- Supports SDHC memory cards.
- Supports MMC, mini-SD and micro-SD cards.
- Does not support CPRM.

3. CD input interface

- Supports digital audio 3-line inputs (I2S, EIAJ format). *2
- Supports CD-ROM 3-line inputs (I2S, EIAJ format).
- Supports the data connection function by comparison with data at the last time. *2
- Encodes the input data in the MP3 or WAV format and writes encoded data to a USB or SD memory. *2
- Builds in the CD-ROM decoder function.

*2 BU94702AKV and BU94705AKV only.
Real time recording can be realized only by the recording memory (USB memory /SD memory card) that a writing response speed *) **) is fast. Even the recording memory that a response speed is early when it is written in in a short time, a response sometimes becomes slow by long writing. Use the recording memory that it was fully verified by the product specifications.

*) It is a response speed toward an order for mass storage writing in the USB "Full Speed" standard connection of the USB memory. It doesn't influence a response speed in "High Speed" or "Ultra High Speed" and an average transfer speed.

**) It is a response speed toward an order for mass storage writing in the SPI mode connection of the SD memory card. It doesn't influence a response speed in the SD mode connection and a Class speed.

4. I^2C command interface (Slave I/F)

- Communicates with the master microcomputer using the I^2C interface format.
- Operates as I^2C slave I/F.
- Supports the standard mode (100kbps) and the fast mode (400kbps).
- Supports 7-bit addresses.
- Can select four types of slave addresses.

5. Serial interface (Slave I/F)

- Supports the SPI mode.
- Operates as SPI slave I/F.
- Supports 8-, 16 and 32 bit/transfer data. An input clock supports to Max. =2MHz.
- Supports to download data such as images within the memory to the microcomputer.

6. Audio output

- Supports audio line outputs from built-in 1bit-DAC.
- Builds in the digital soft mute function. *
- Supports digital audio outputs of the I2S format, the EIAJ format and those and the digital audio interface (SPDIF).
- Builds in sound effects including POPS, JAZZ, and ROCK, CLASSIC, R&B and BassBoost. *

*This is available for audio line outputs only.

7. Sample rate converter

- Converts all support sample rates to 44.1 kHz based on the polyphase calculation.

8. System controller

- Control all operations including interface control to the master microcomputer, USB device access, SD card access, FAT analysis, sort function, decoding, encoding and audio output.

●**Description of each block's movement -part2**

9. FAT analysis

- Supports FAT32, FAT16 and FAT12 file system.
- Supports VFAT (long file name).
- Supports multi-partition up to 1 partition.
- Supports multi-drive up to 1 drive.
- Supports playable folder hierarchies up to 16 hierarchies whose full path including the file name is within 260 characters.
- Supports playable file extension of *.wav for WAV files.
- Supports playable file extensions of *.m4a, *.3gp and *.mp4 for AAC files.
- Supports playable file extensions of *.asf and *.wma for WMA files.
- Supports playable file extensions of *.mp3, *.mp2 and*.mp1 for MP3 files. For *.mp2 and *.mp1, the function allows you to select whether to play. Does not extinguish between upper case letters and lower case letters of file extensions.
- Up to 100 folders and 100 files can be sorted and played in the order of UNICODE when sorting functional effective.
- Can obtain 5 file names ahead from current music file.
- Can obtain a folder name or file name within 128 bytes.
- Supports 512, 1024, 2048 and 4096 bytes per sector.
- Playable file size up to 2G-1 byte. A file over 2Gbyte is recognized as a playable file, too. But, it is for 2Gbyte -1byte that it can play.
- Supports the device size up to FAT specification (2T byte).

10. Control from master microcomputer (little endian order)

- Can control from the master microcomputer using the I^2C interface. (This function is available in MODE2 only.)
- Controllable using commands of play, pause, stop, tune skip, tune forward, folder move, device change, volume setting, repeat change, random play, digital audio output setting, sound effect setting and direct tune selection and etc.
- Can read information on internal status during play or stop, folder number, file number within the folder, play time, total number of folders, total number of files, name of folder being played, name of file being played and TAG (title, artist, album, genre), and etc.

11. MP3 encoder (*3 BU94702AKV and BU94705AKV only.)

- Supports MP3 format encode (MPEG1 Layer3).
- Decoding operation cannot be performed during encoding operation.
- Supports sample rate of 32 k, 44.1 k and 48 kHz.
- Can select encoding bit rate from 32 kbps, 64 kbps, 128 kbps, 192 kbps, 256 kbps and 320 kbps (CBR).
- Supports the writing of the encoded file to USB or SD card.

12. MP3 decoder

- Supports MPEG audio 1, 2 and 2.5.
- Supports Layer1, 2 and 3.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k, 12 k, 24 k and 48 kHz.
- Supports bit rate of 8 to 320 kbps and VBR (Variable Bit Rate). *Excluding the free format
- Supports ID3TAG V1.0, V1. 1, V2.2, V2.3 and V2.4.
  (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)

13. WMA decoder

- Supports Windows Media Audio 9 standard.
- Not supports DRM files.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k and 48 kHz.
- Supports bit rate of 5 to 384 kbps and VBR (Variable Bit Rate).
- Supports WMA-TAG.
  (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)

●Description of each block's movement -part2

14. AAC decoder

- Supports MPEG4 AAC-LC (Audio stream).
- Based on 3GPP TS 26.244 and iTunes.
- Supports File Type of m4a, mp42 and 3gpX. (X stands for any numeric value.)
- Not supports DRM files. Not supports CD-ROM playing.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k, 12 k, 24 k and 48 kHz.
- Supports bit rate of 8 to 320kbps and VBR (Variable Bit Rate).
- Supports AACTAG (iTunes Meta-data and 3GP Meta-data).
  (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)
  *For files other than those encoded by iTunes, sound interruption may occur when skipping or forwarding to the next tune if streams such as gaps and video data are contained in the file.

15. WAV play

- Supports WAV format.
- Supports sample rate of 8 k, 16 k, 32 k, 11.025 k, 22.05 k, 44.1 k, 12 k, 24 k and 48 kHz.
- Supports 16-bit PCM data.
- Not supports CD-ROM playing.
- Supports RIFF TAG.
  (Up to 128 bytes can obtain for album, artist, title and genre, respectively.)

16. Browsing and direct tune selection

- Can analyzes and read other file name in memory while playing the current music.
- Up to 64 bytes can obtain for file name, folder name respectively.
- Supports direct music selection using the analysis data.

17. Repeat and random play

- Supports repeat within the memory, repeat within folder and repeat with single tune.
- Supports random play within the area of ±128 files.
- Can select auto-play of next music or stop playing at the end of current music playing.

18. Play according to play list

- Supports play in the order given in the specified play list within the specified folder.
- Supports extensions of *.m3u and *.pls.
- Supports play lists described in full path of ASCII or SHIFT-JIS.

19. CD-ROM Decoder

- Supports CD-ROM Mode1, Mode2 form1, and Mode2 form2 format.
- Supports CD-ROM ECC and CD-ROM EDC function.
- Supports ISO9660 level 1 and level 2 file systems.
- Supports Remeo and Joliet extension.
- Supports playable folder hierarchies up to 8 hierarchies.
- Supports playable file extension of *. asf, wma for WMA files, mp3, mp2, mp1 for MP3 files.
- Output the interruption signal and status of the required LBN for seeking operation.
- Build in the input data buffer of about 100 kByte. (include file system analysis data)
- Up to 48bytes can obtain for file name, folder name respectively.

20. Read/Write from/to files within memory

- Can read the data from specified file stored in the specified folder within the memory.
- Can write the data to specified file in the specified folder within the memory.

21. IPL (Initial Program Download)

- Communicates with a serial FLASH ROM using a SD interface (SPI master I/F).
- Downloads the program data to the internal Program RAM at power ON.
- Serial FLASH ROM supports to 8 bit-Command, 24 bit-ADDRESS, and clock MIN=15MHz by minimum size 2Mbit.
- In the IPL write mode, writes the specified data in USB or SD memory to a serial FLASH ROM.

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage(Analog, I/O)	VDD1MAX	-0.3 to 4.5	V	DVDDIO, VDD_PLL, DAVDD, AVDDC
Input voltage	VIN	-0.3 to VDD1 + 0.3	V	
Storage temperature range	TSTG	-55 to 125	˚C	
Operating temperature range	TOPR	-40 to 85	˚C	
Power dissipation *1	PD1	900	mW	

*1:In the case of use at Ta=25℃ or more, 9mW should be reduced per 1℃.
Radiation resistance design is not arranged.

●Operating conditions (Ta = 25℃)

Parameter	Symbol	Limits	Unit	Comment
Supply voltage(Analog, I/O)	VDD1	3.0 to 3.6	V	DVDDIO, VDD_PLL, DAVDD, AVDDC

●Electrical characteristics

(Unless specified, Ta=25℃, VDD1=3.3V, DVSS=AVSSC=VSS_PLL=DAVSS=0V, XIN_PLL=16.9344MHz)

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
<Total >						
Circuit current (VDD1 USB1)	IDD1USB1	-	51.0	75.0	mA	*1 When USB memory is played.
Circuit current (VDD1 SD1)	IDD1SD1	-	26.0	45.0	mA	*1 When SD card is played.
<Digital block>						
H-Level input voltage	VIH	VDD1*0.7	—	VDD1	V	*2
L-Level input voltage	VIL	DVSS	—	VDD1*0.3	V	*2
H-Level output voltage1	VOH1	VDD1-0.4	—	VDD1	V	IOH=-1.6mA, *3
L-Level output voltage1	VOL1	0	—	0.4	V	IOL=1.6mA. *3
L-Level output voltage2	VOL2	0	—	0.4	V	IOL=3.6mA, *4
H-Level output voltage3	VOH3	VDD1-0.4	—	VDD1	V	IOH=-0.6mA, *5
L-Level output voltage3	VOL3	0	—	0.4	V	IOL=0.6mA, *5
H-Level output voltage4	VOH4	VDD1-1.0	—	VDD1	V	IOH=-1.6mA, *6
L-Level output voltage4	VOL4	0	—	1.0	V	IOL=1.6mA, *6
<USB-HOST >						
H-Level input voltage	VIHUSB	VDD1*0.6	—	VDD1	V	*7
L-Level input voltage	VILUSB	AVSSC	—	VDD1*0.3	V	*7
Output impedance(H)	ZOH	22.0	45.0	60.0	Ω	*7
Output impedance(L)	ZOL	22.0	45.0	60.0	Ω	*7
H-Level output voltage	VOHUSB	VDD1-0.5	—	VDD1	V	*7
L-Level output voltage	VOLUSB	0	—	0.3	V	*7
Rise/Fall time	Tr/Tf	—	11	—	ns	*7, Output capacity 50pF
Voltage of crossing point	VCRS	—	VDD1/2	—	V	*7, Output capacity 50pF
Range of differential input	VDIFF	0.8	—	2.5	V	*7
Differential input sensitivity	VSENS	0.2	—	—	V	*7
Pull-down resistance	RPD	14.25	20.0	24.8	kΩ	*7
<Audio DAC>						
Distortion rate	THD	—	0.005	0.05	%	1kHz, 0dB, sine, *8
Dynamic range	DR	—	90	—	dB	1kHz, -60dB, sine, *8
S/N ratio	S/N	66	96	—	dB	1kHz, 0dB, A-weighted, *8
Max output level	VSMAX	0.60	0.75	—	Vrms	1kHz, 0dB, sine, *8

*1 3.3V system I/O, Analog Power supply (VDD1), 1kHz, 0dB, sine-wave playing
*2 1, 3, 4-9, 14-23, 29, 31-32, 34-35, 61-63, 71-76 pin
*3 9, 11-12, 14-15, 18-20, 30, 36, 58-60, 61-67, 69-70 pin
*4 2, 3, 17 pin
*5 24-26, 28, 29 pin
*6 49 pin
*7 41, 42 pin
*8 53, 55 pin output no-load

●Application Information

1. Clock and Reset

Clock

Clock name	I/O	Function	Function
XIN_PLL	I	X'tal (16.9344MHz) connection input terminal	
XOUT_PLL	O	X'tal (16.9344MHz) connection terminal	

Reset

Signal name	I/O	Function	Remarks
RESETX	I	System reset input terminal	

Please release the reset signal continue L input for more than 100 us after clock input from the oscillation I/O terminal becomes stable. (See Figure 4)

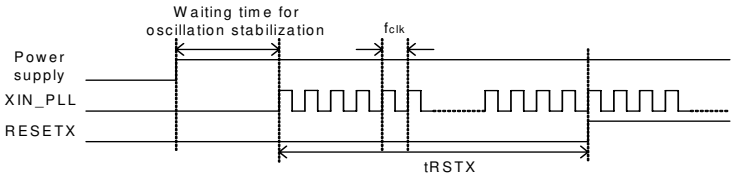


Figure 4. Reset Timing

Table 1. Timing

Item	Symbol	Rating			Unit	Remarks
		min	typ	max		
Clock frequency	f_{CLK}	16.9302	16.9344	16.9386	MHz	
Reset L interval	t_{RSTX}	100	-	-	us	

2. USB I/F

USB I/O interface

Signal name	I/O	Function	Remarks
USB_DP	I/O	USB D+ I/O terminal	
USB_DM	I/O	USB D- I/O terminal	
REXTI	O	USB bias resistor connection terminal	Connect a resistor of 12 kΩ±1% to GND.

This interface communicates with the USB device using USB_DP and USB_DM differential signals.
REXTI terminal is used to connect to the bias resistor in the USB-PHY block.
Builds in the USB Full speed (12Mbps) HOST control function.
Supports the USB mass storage class.
Doesn't support external HUB.

3. SD I/F

SD memory card SPI interface

Signal name	I/O	Function	Remarks
FL_CS	O	Serial flash ROM chip select	
SD_CS	O	SD chip select	
SD_CLK	O	SPI clock	
SD_DI	O	SPI data input	
SD_DO	I	SPI data output	
SD_CON	I	SD card connect detection terminal	H: Do not detect SD card connect, L: Detect SD card connect
SD_WP	I	SD card write-protect detection terminal	H: SD write-protect valid, L: SD write-protect invalid

This interface connects to the SD memory card slot to communicate with the SD memory device.
Supports the SPI mode.
Supports SD, SDHC memory cards and MMC, mini-SD and micro-SD cards.
Does not support CPRM.
Since the SD memory card slot needs to detect the insertion status of the SD memory device and the write-protect status, be sure to use the slot having the SD memory card insertion status detection terminal and the WP terminal and connect it to the terminals. The SD_CON terminal is pulled up within the device and detects “SD card connect” when L is input. The SD_WP terminal is pulled up within the device and detects “SD card no-write-protect” when L is input.
SD I/F is also used as an external serial flash ROM I/F.

3.1 Timing

Table 2. Timing

(Unless specified, Ta=25℃, VDD1=3.3V, Load=20pF, 10kΩ)

Item	Symbol	Rating			Unit	Remarks
		min	typ	max		
SD_CS Setup time	Tcss	-	5	-	us	
SD_CS Hold time	Tcsh	-	15	-	us	
SD_CLK Clock Frequency	Tclk	-	13.5	-	MHz	
SD_DI Output delay	Tod	-20	-	20	ns	
SD_DO Data in Setup time	Tds	18	-	-	ns	
SD_DO Data in Hold time	Tdh	5	-	-	ns	
Output High Voltage	Voh	0.625*VDD1	-	-	V	
Output Low Voltage	Vol	-	-	0.25*VDD1	V	

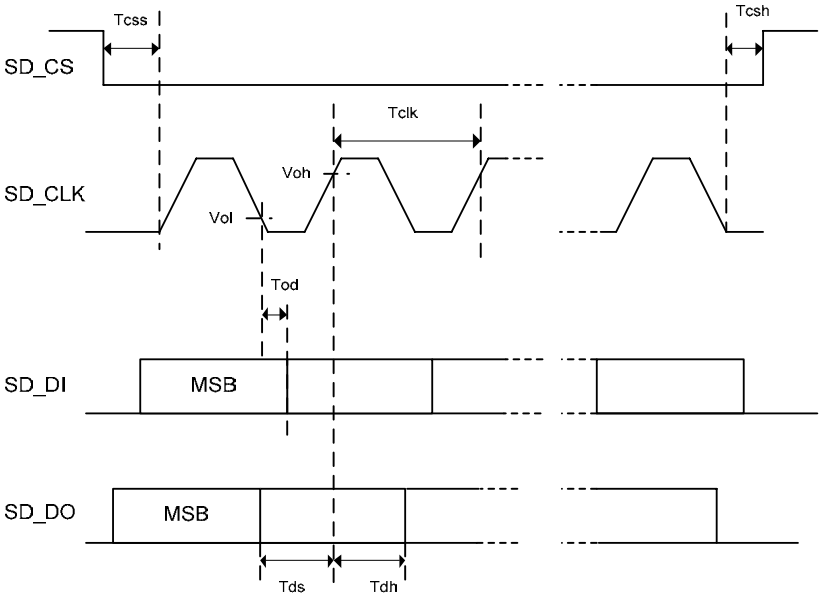


Figure 5. SPI I/F Timing

4. Audio line output

Audio line output

Signal name	I/O	Function	Function
LDACO	O	Lch audio line output	
RDACO	O	Rch audio line output	

Supports Audio line outputs from built-in 1bit-DAC.
Builds in the digital soft mute function.
Builds in sound effects including POPS, JAZZ, ROCK, CLASSIC, R&B and BassBoost.
It turns ON when line output is selected by a command.
The data of the sample rate 48 kHz and 32 kHz is converted into 44.1 kHz and output.

4.1 Volume

Figure 6 shows the relationship between audio outputs and volume steps.
The initial value is step=6=–24.1dB at power ON.

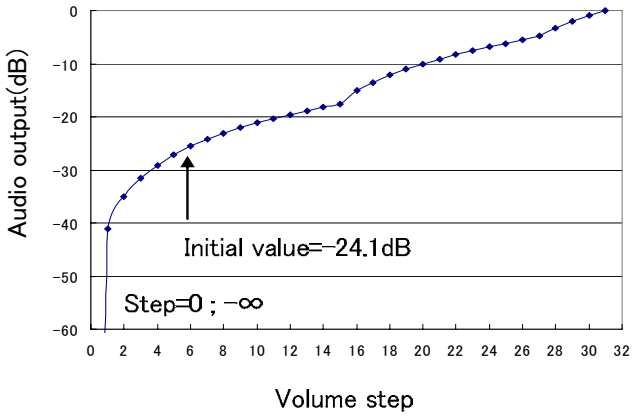


Figure 6. Volume Step Function

4.2 Equalizers

You can select audio line output from 5 types of equalizers and 2 types of bus boosts, using commands. You can use a combination of an equalizer and bus boost 1.
Even when line output is not selected, the equalizer setting is valid. However, for digital output, the equalizer cannot change the sound quality.
Clipping may occur by the combination of volume and equalizer setting.
Figures 7 to 12 show frequency characteristics of each filter.

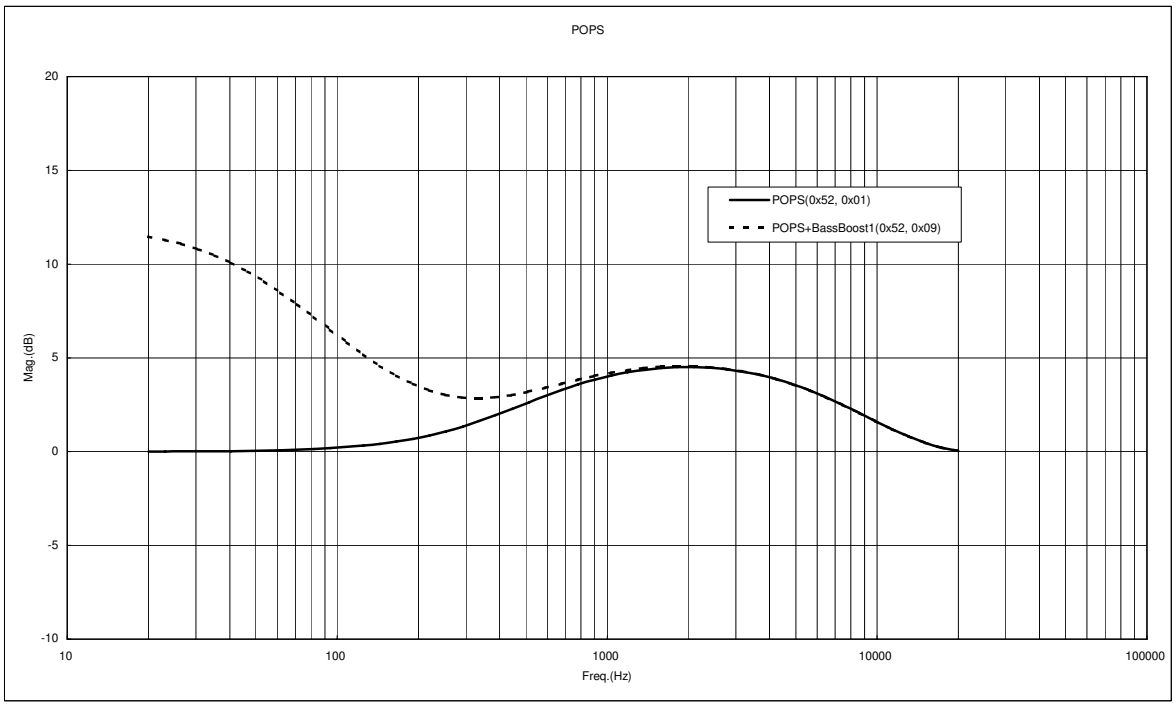


Figure 7. POPS Frequency Characteristics

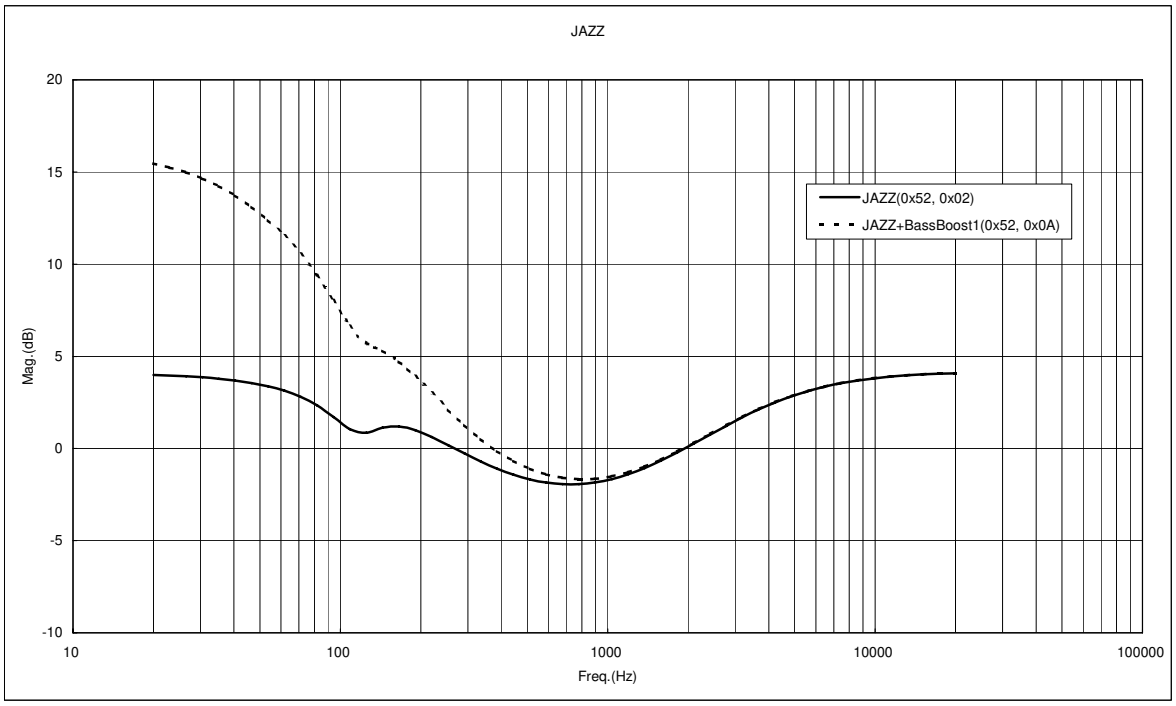


Figure 8. JAZZ Frequency Characteristics

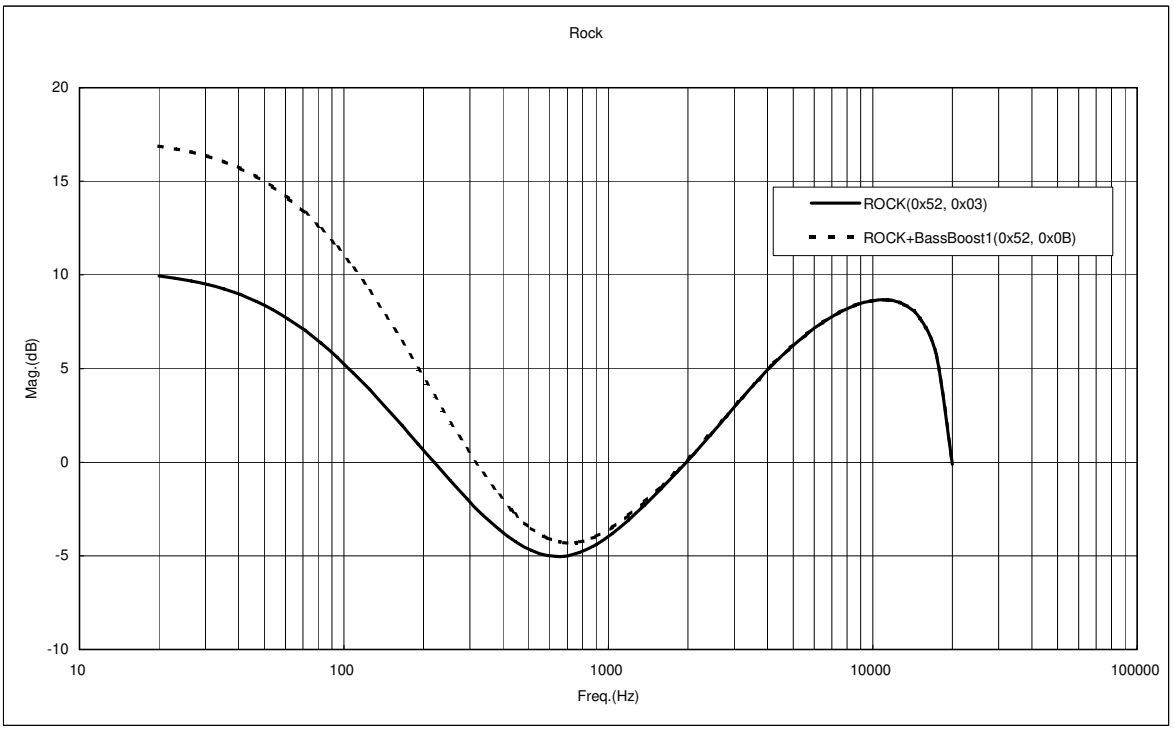


Figure 9. ROCK Frequency Characteristics

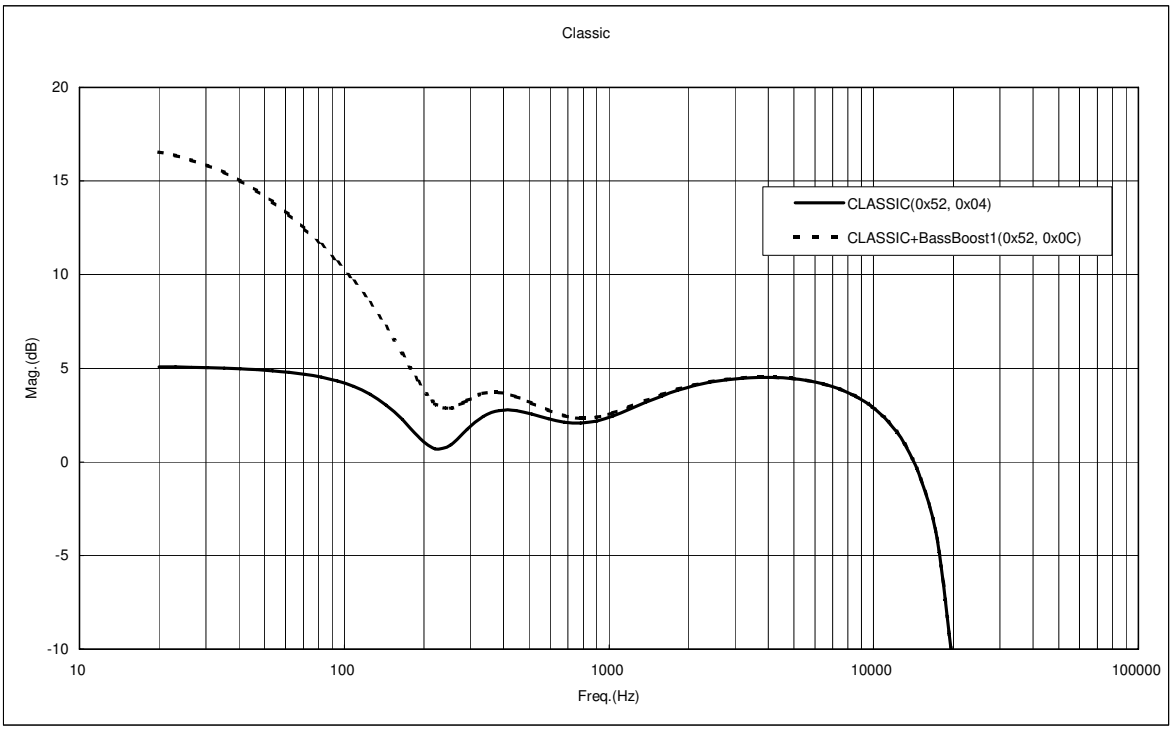


Figure 10. CLASSIC Frequency Characteristics

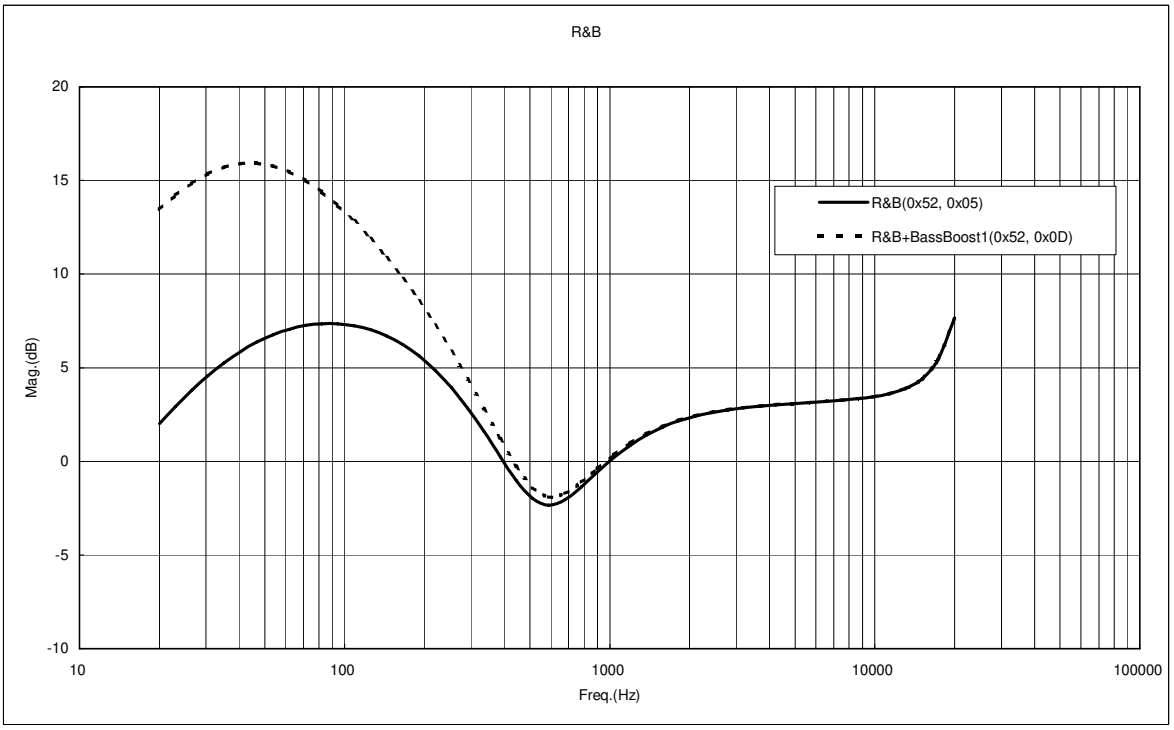


Figure 11. R&B

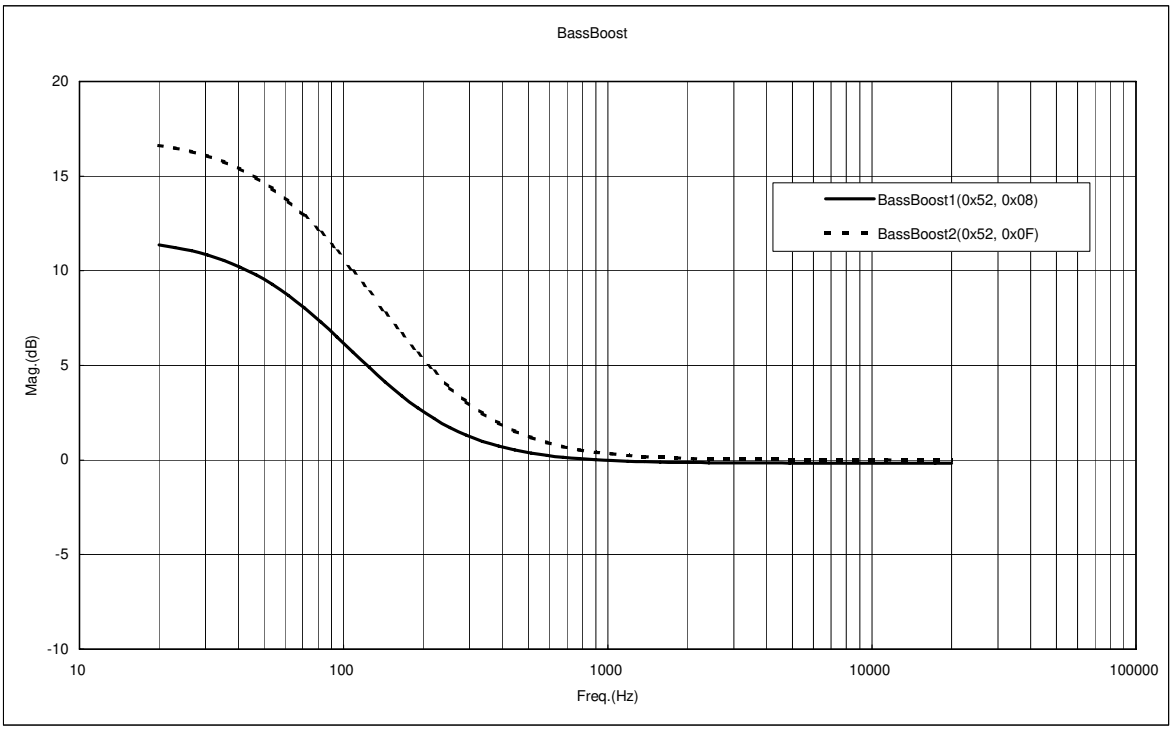


Figure 12. Bass Boost

5. MUTE control output

Audio MUTE

Signal name	I/O	Function	Remarks
AMUTE	O	Audio mute control terminal	H: At audio output , L: At mute

It outputs H at audio output and L at mute.
It is possible to use it as a flag to do the mute with the amplifier etc. of latter part at no sounds such as power supplies ON and FF and FB.
Figure 13 shows the operation waveforms.

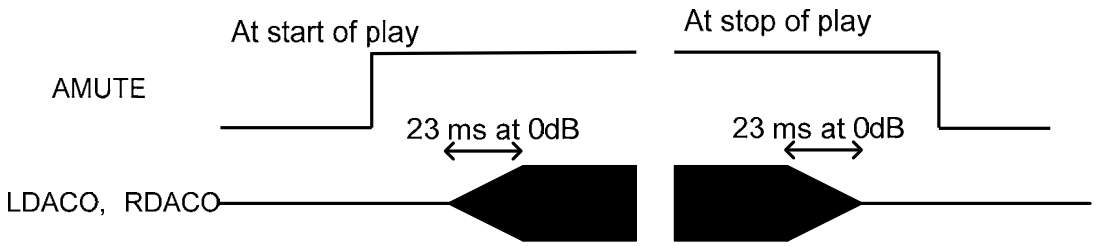


Figure 13. Waveform at Audio Mute

6. Digital Audio output

Three-line serial Digital audio interface

Signal name	I/O	Function	Remarks
LRCKO	O	LR clock output (fs=44.1kHz)	
BCKO	O	Bit clock output	
DATAO	O	Data output	

This is a Digital audio output interface terminal. It becomes enabled by using the appropriate command.
The output format can be selected from the EIAJ format or I^2S format of 32fs, 48fs or 64fs.
The data of the sample rate 48 kHz and 32 kHz is converted into 44.1 kHz and output.

6.1 Output Format

Figures 14, 15, 16, 17, 18 and 19 show the output formats.

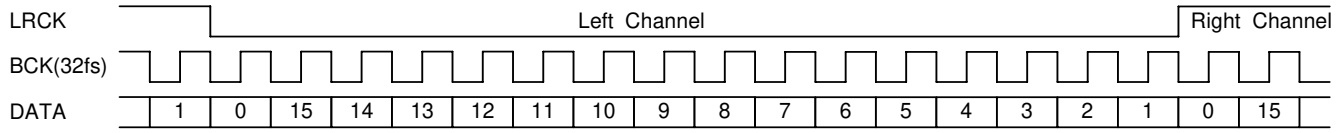


Figure 14. I^2S Output Timing (32fs)

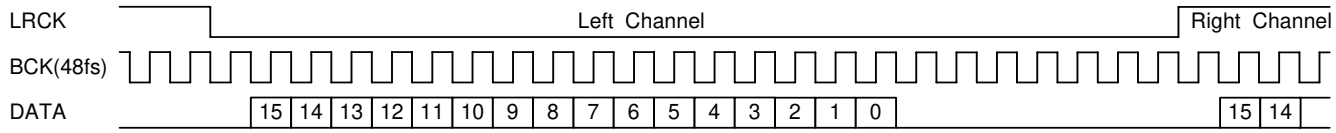


Figure 15. I^2S Output Timing (48fs)

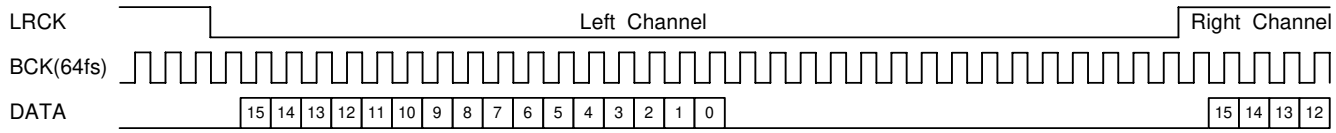


Figure 16. I^2S Output Timing (64fs)

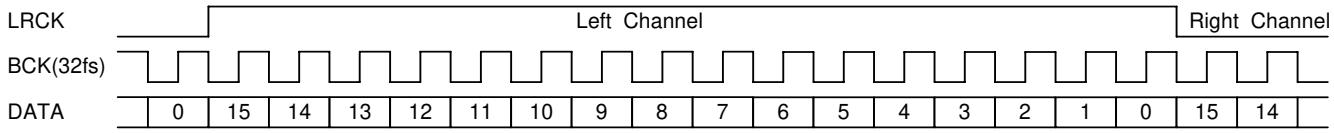


Figure 17. EIAJ Output Timing (32fs)

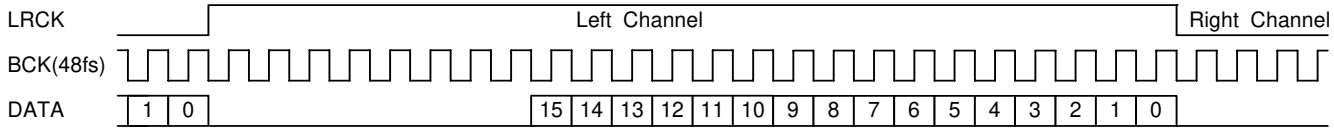


Figure 18. EIAJ Output Timing (48fs)

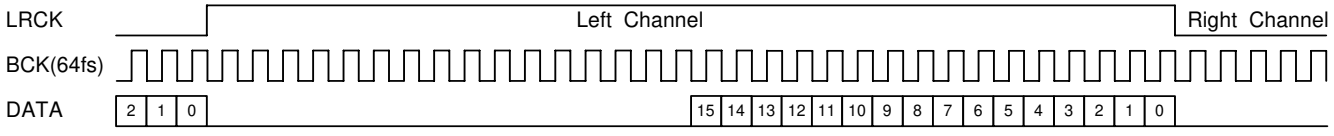


Figure 19. EIAJ Output Timing (64fs)

6.2 Timing

Table 3. Timing

48fs I^2S format (Unless specified, Ta=25℃, VDD1=3.3V, Load=20pF)

Item	Symbol	Rating			Unit	Remarks
		min	typ	max		
BCK Clock Frequency	Tbck	-	472.4	-	ns	
BCK Low time	Tbck1	216	236	-	ns	
BCK High time	Tbck2	216	236	-	ns	
LRCK Clock Frequency	Tlrck	-	44.1	-	kHz	
LRCK Output delay	Tlrck1	-20	0	20	ns	
DATA Output delay	Tda1	-20	0	20	ns	
Output High Voltage	Toh	VDD1-0.4	-	-	V	
Output Low Voltage	Vol	-	-	0.4	V	

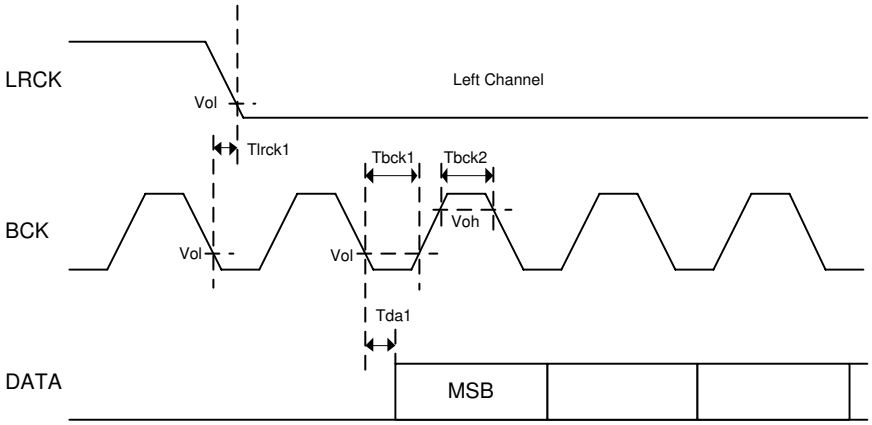


Figure 20. Output Timing

7. SPDIF output

SPDIF interface

Signal Name	I/O	Function	Remarks
SPDIF	O	SPDIF output	

SPDIF output become enabled by setting it using the appropriate command.
The data of the sample rate 48 kHz and 32 kHz is converted into 44.1 kHz and output.

7.1 Format

Figure 21. shows the SPDIF signal output format.

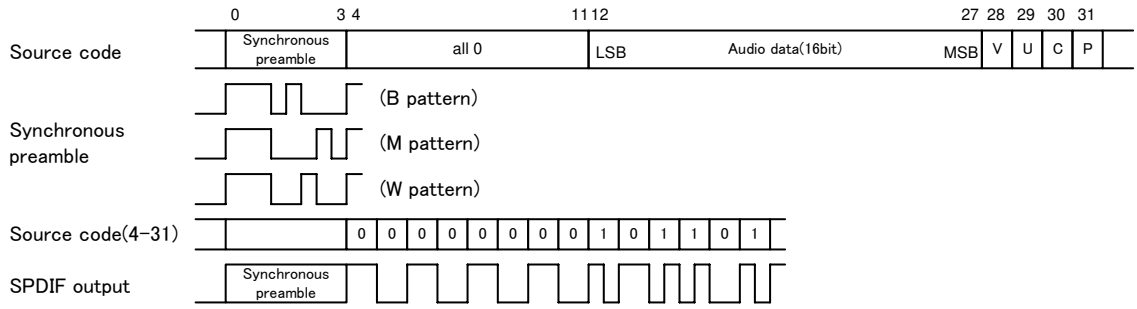


Figure 21. SPDIF Output Format

One sub frame of SPDIF consists of synchronous preambles, 16-bit audio data, V bit (validity flag), U bit (user data), C bit (channel status) and P bit (parity bit).
Output rate is fixed to 1X speed (44.1 kHz).
SPDIF outputs synchronous preambles (source code 0-3) as they are, and other elements (source code 4-31) as the biphase output. While the operation stops, L output is enabled.
Synchronous preambles and C bit use 32 frames (≈4.4 ms) for one cycle. The data formats are shown in Table 4 and Table 5 V bit is fixed to L. U bit uses 98 frames (≈13.3 ms) for one cycle.

Table 4. Synchronous Preamble Pattern

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	B	W	M	W	M	W	M	W	M	W	M	W
1	M	W	M	W	M	W	M	W	M	W	M	W
:	:	:	:	:	:	:	:	:	:	:	:	:
31	M	W	M	W	M	W	M	W	M	W	M	W

Table 5. C Bit Format

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	0		0		Copy		0		0		0	
1	0		0		1		0		0		0	
2	0		0		0		Lbit		0		0	
3	0		0		1	0	0	1	0		0	
4	0		0		0		0		0		0	
5	0		0		0		0		0		0	
:	:		:		:		:		:		:	
31	0		0		0		0		0		0	

Table 6. U Bit Format

	L0	R0	L1	R1	L2	R2	L3	R3	L4	R4	L5	R5
0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0
2	1	0	0	0	0	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:	:	:	:	:
97	1	0	0	0	0	0	0	0	0	0	0	0

P bit is set to 1 if the number of “1” contained in source codes 4-30 is odd, and set to 0 if the number is even. Therefore, the number of source codes to be set to 1 for one data must be even, SPDIF ends with L output, and preamble output always starts in the same direction.

7.2 Timing

,

Table 7. Timing

(Unless specified, Ta=25℃, VDD1=3.3V, Load=20pF)

Item	Symbol	Rating			Unit	Remarks
		min	typ	max		
SPDIF Clock Frequency	Tck	-	2.822	-	MHz	
SPDIF Clock High time	Tck1	157	177	-	ns	
SPDIF Clock Low time	Tck2	157	177	-	ns	
Output High Voltage	Voh	VDD1-0.4	-	-	V	
Output Low Voltage	Vol	-	-	0.4	V	

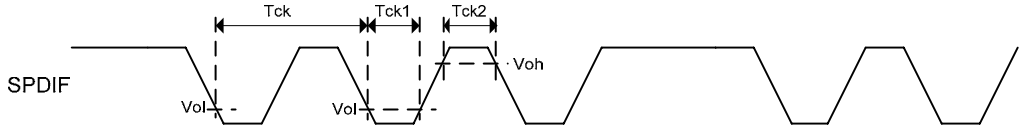


Figure 22. SPDIF Output Timing

8. I²C command interface

Slave I²C serial interface

Signal name	I/O	Function	Remarks
SCL	I	I²C interface clock input	External pull-up resistor is required.
SDA	I/O	I²C interface data I/O	External pull-up resistor is required.
A0	I	Slave address selection terminal	Slave address [0] bit setting terminal
A1	I	Slave address selection terminal	Slave address [1] bit setting terminal

This is an I²C serial interface terminal to communicate with the microcomputer (master).
It supports slave I²C operations.
Supports the standard mode (100kbps) and the fast mode (400kbps).
Supports 7-bit addresses.

8.1 I²C protocol

When the I²C bus is in the IDLE state, SDA and SCL are set to H by the external Pull-up resistor.
To start communications, the master sets SDA to L while SCL set to H (Start condition). To finish communications, the master sets SDA to H while SCL set to H (Stop condition). During transfer, the master changes SDA only while SCL is L.
Figure 23 shows Start condition, Stop condition of I²C.

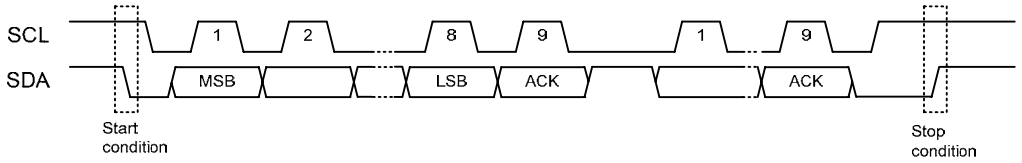


Figure 23. **I²C** Start and Stop Conditions

8.2 Slave address

I²C bus slave addresses support the 7-bit addressing mode. By inputting to terminals A0 and A1, the bus slave address can be selected as shown in Table 8. Figure 24 shows the slave address transfer format.

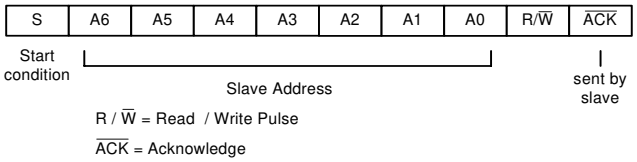


Figure 24. Slave Address Transfer Format

Table 8. Settable Slave Addresses

MSB A6	A5	A4	A3	A2	A1 terminal	LSB A0 terminal
1	0	0	0	0	0	0
1	0	0	0	0	0	1
1	0	0	0	0	1	0
1	0	0	0	0	1	1

8.3 Protocol to write from the master

When sending commands from the master using the I^2C bus, be sure to conform to the transfer protocol shown in Figure 25 after BUSY PIN confirms the state of L, for details on each command, see Chapter 26.

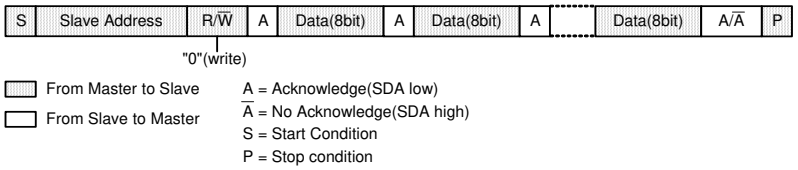


Figure 25. Command Send Protocol

8.4 Protocol to read to the master

When sending the received data from the slave to the master using the I^2C bus, be sure to conform to the transfer protocol shown in Figure 26. First, transfer the status read command (step1). Then, input SCL clock of required bytes in step2 to read the status after BUSY PIN confirms the state of L.

When BUSY PIN is H, correct data is not transmitted.

The first byte of the transferred data (step2) outputs the status shown in Table 9. Data is output from the second byte.

Figure 27 shows the relationship between the transferred data and BUSY.

* For details on BUSY, see Chapter 9.

Table 9. BUSY Byte Structure

bit	STATUS
7	0
6	0
5	0
4	PRECOM
3	IRPTO
2	SEARCH
1	MCHNG
0	BUSY

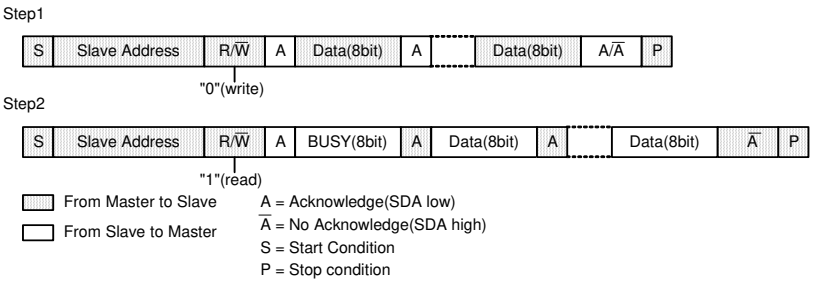


Figure 26. Status Reception Protocol

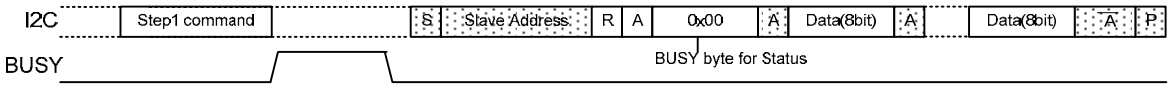


Figure 27. Relationship between Transferred Data and BUSY