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LCD Segment Drivers

# Multi- function LCD Segment Drivers

BU97510CKV-M MAX 216 Segment(54SEGx4COM)

## General Description

The BU97510CKV-M is 1/4 or 1/3-Duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The BU97510CKV-M can drive up to 216 LCD. Segments directly. The BU97510CKV-M can also control up to 6 general-purpose output ports.

## Features

- AEC-Q100 Qualified (Note)
- Either 1/4 or 1/3-Duty can be selected with the Serial Control Data.
  1/4-Duty Drive: Up to 216 Segments
  1/3-Duty Drive: Up to 162 Segments
- Serial Data Control of Frame Frequency for Common and Segment Output Waveforms.
- Serial Data Control of Switching between the Segment Output Port , PWM Output Port and General-purpose Output Port Functions.(Max 6 port)
- Built-in OSC Circuit
- The INHb Pin can force the Display to the off state.
- Integrated Power-on Reset Circuit
- No External Component
- Low Power Consumption Design

(Note) Grade 3

## Applications

- Car Audio, Home Electrical Appliance, Meter Equipment etc.

## Key Specifications

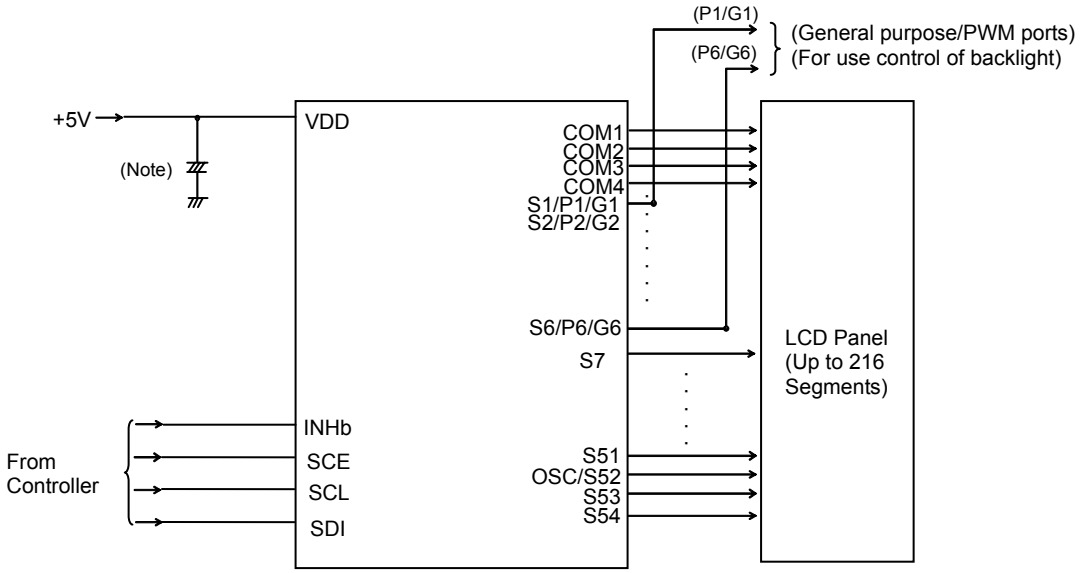
- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 216 Segments
- Display Duty: 1/3, 1/4 Selectable
- Bias: 1/2, 1/3 Selectable
- Interface: 3wire Serial Interface

## Packages

VQFP64 W(Typ.) × D(Typ.) × H(Max.)

**VQFP64**
12.00mm x 12.00mm x 1.60mm

## Typical Application Circuit




(Note) Insert capacitors between VDD and VSS C≥0.1uF

Figure 1. Typical Application Circuit

## Block Diagram

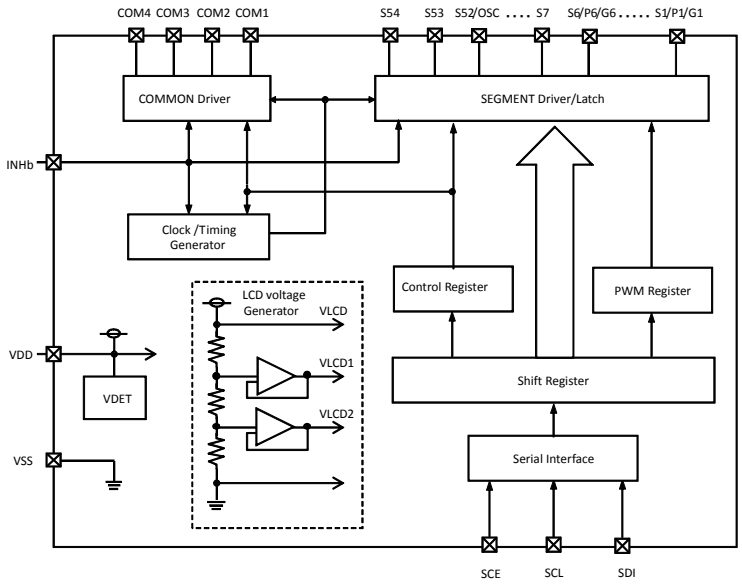



Figure 2. Block Diagram

## Pin Arrangement

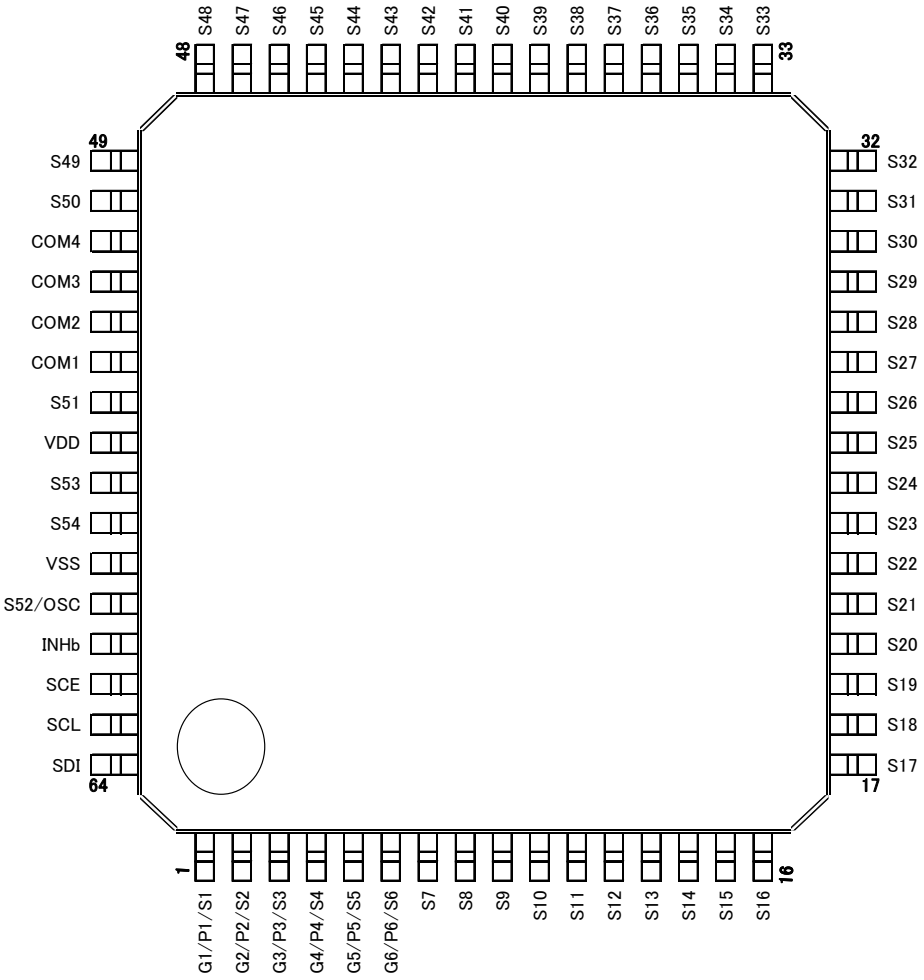



Figure 3. Pin Configuration (TOP VIEW)

### Absolute Maximum Ratings(Ta = 25°C, VSS = 0.0V)

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum Supply Voltage | VDD max | VDD | -0.3 to +6.5 | V |
| Input Voltage | VIN1 | SCE, SCL, SDI, INHb | -0.3 to +6.5 | V |
| Allowable Loss | Pd | | 1.0(Note) | W |
| Operating Temperature | Topr | | -40 to +85 | °C |
| Storage Temperature | Tstg | | -55 to +125 | °C |

(Note) When use more than Ta=25°C, subtract 10mW per degree. (Using ROHM standard board)
(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

**Caution:** Operating the IC over absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

### Recommended Operating Conditions (Ta = -40 to +85°C, VSS = 0.0V)

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Supply Voltage | VDD | VDD | 2.7 | | 6.0 | V |

### Electrical Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

| Parameter | Symbol | Pin | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Hysteresis | VH | SCE, SCL, SDI, INHb, OSC | | - | 0.03VDD | - | V |
| Power-On Detection Voltage | VDET | VDD | | 1.4 | 1.8 | 2.2 | V |
| “H” Level Input Voltage | VIH1 | SCE, SCL, SDI, INHb, OSC | VDD=4.0V to 6.0V | 0.4VDD | - | VDD | V |
| | VIH2 | SCE, SCL, SDI, INHb, OSC | VDD=2.7V to 4.0V | 0.8VDD | - | VDD | V |
| “L” Level Input Voltage | VIL1 | SCE, SCL, SDI, INHb, OSC | | 0 | - | 0.2VDD | V |
| “H” Level Input Current | IIH1 | SCE, SCL, SDI, INHb, OSC | VI = 6.0V | - | - | 5.0 | µA |
| “L” Level Input Current | IIL1 | SCE, SCL, SDI, INHb, OSC | VI = 0V | -5.0 | - | - | µA |
| “H” Level Output Voltage | VOH1 | S1 to S54 | IO = -20µA | VDD-0.9 | - | - | V |
| | VOH2 | COM1 to COM4 | IO = -100µA | VDD-0.9 | - | - | |
| | VOH3 | P1/G1 to P6/G6 | IO = -1mA | VDD-0.9 | - | - | |
| “L” Level Output Voltage | VOL1 | S1 to S54 | IO = 20µA | - | - | 0.9 | V |
| | VOL2 | COM1 to COM4 | IO = 100µA | - | - | 0.9 | |
| | VOL3 | P1/G1 to P6/G6 | IO = 1mA | - | - | 0.9 | |
| Middle Level Output Voltage | VMID1 | S1 to S54 | 1/2-Bias IO = ±20µA | 1/2VDD -0.9 | - | 1/2VDD +0.9 | V |
| | VMID2 | COM1 to COM4 | 1/2-Bias IO = ±100µA | 1/2VDD -0.9 | - | 1/2VDD +0.9 | |
| | VMID3 | S1 to S54 | 1/3-Bias IO = ±20µA | 2/3VDD -0.9 | - | 2/3VDD +0.9 | |
| | VMID4 | S1 to S54 | 1/3-Bias IO = ±20µA | 1/3VDD -0.9 | - | 1/3VDD +0.9 | |
| | VMID5 | COM1 to COM4 | 1/3-Bias IO = ±100µA | 2/3VDD -0.9 | - | 2/3VDD +0.9 | |
| | VMID6 | COM1 to COM4 | 1/3-Bias IO = ±100µA | 1/3VDD -0.9 | - | 1/3VDD +0.9 | |
| Current Drain | IDD1 | VDD | Power-saving mode | - | - | 15 | µA |
| | IDD2 | VDD | VDD = 5.0V Output open 1/2-Bias Frame Frequency = 80Hz | - | 70 | 150 | |
| | IDD3 | VDD | VDD = 5.0V Output open 1/3-Bias Frame Frequency = 80Hz | - | 95 | 200 | |

Oscillation Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

| Parameter | Symbol | Pin | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Oscillator Frequency1 | fosc1 | Internal Oscillator Circuit | VDD = 2.7V to 6.0V | 150 | - | 360 | kHz |
| Oscillator Frequency2 | fosc2 | | VDD = 5.0V | 255 | 300 | 345 | kHz |
| External Clock Frequency(Note3) | fosc3 | OSC | External clock mode (OC=1) | 30 | - | 600 | kHz |

(Note3) Frame frequency is decided external frequency and dividing ratio of FC0-2 setting.

【Reference Data】

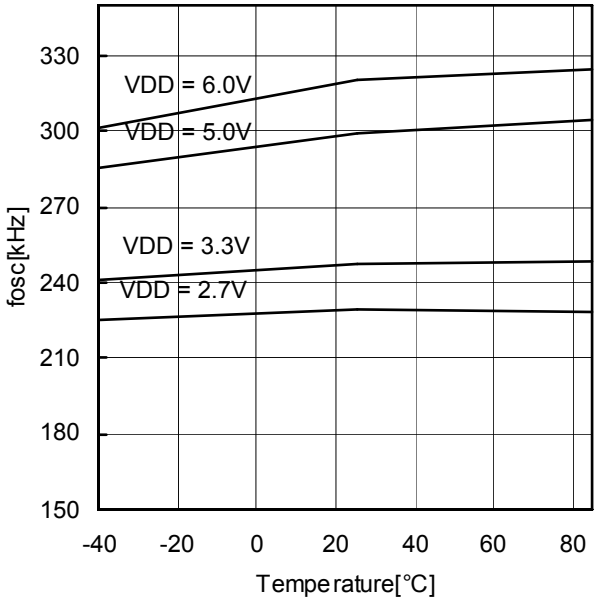
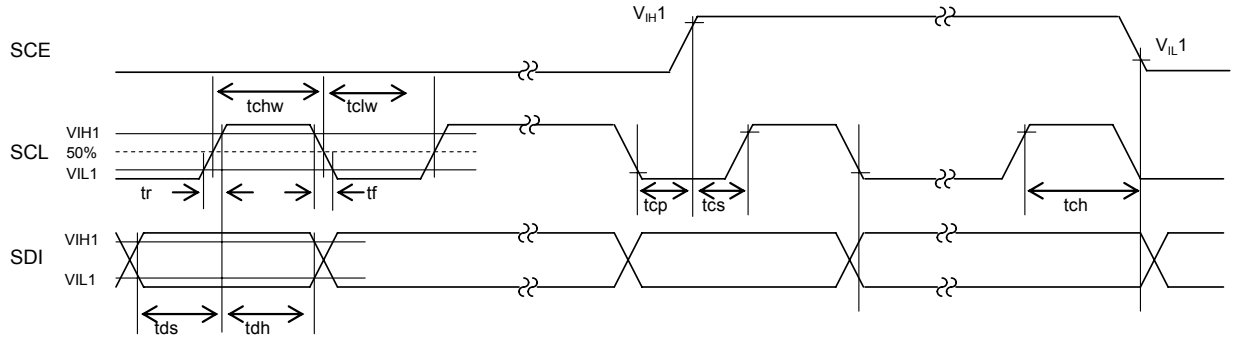



Figure 4. Typical Temperature Characteristics

MPU Interface Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

| Parameter | Symbol | Pin | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| Data Setup Time | tds | SCL, SDI | | 160 | - | - | ns |
| Data Hold Time | tdh | SCL, SDI | | 160 | - | - | ns |
| SCE Wait Time | tcp | SCE, SCL | | 160 | - | - | ns |
| SCE Setup Time | tcs | SCE, SCL | | 160 | - | - | ns |
| SCE Hold Time | tch | SCE, SCL | | 160 | - | - | ns |
| High-Level Clock Pulse Width | tchw | SCL | | 160 | - | - | ns |
| Low-Level Clock Pulse Width | tclw | SCL | | 160 | - | - | ns |
| Rise Time | tr | SCE, SCL, SDI | | - | 160 | - | ns |
| Fall Time | tf | SCE, SCL, SDI | | - | 160 | - | ns |
| INH Switching Time | tc | INHb, SCE | | 10 | - | - | µs |

1. When SCL is stopped at the low level




2. When SCL is stopped at the high level

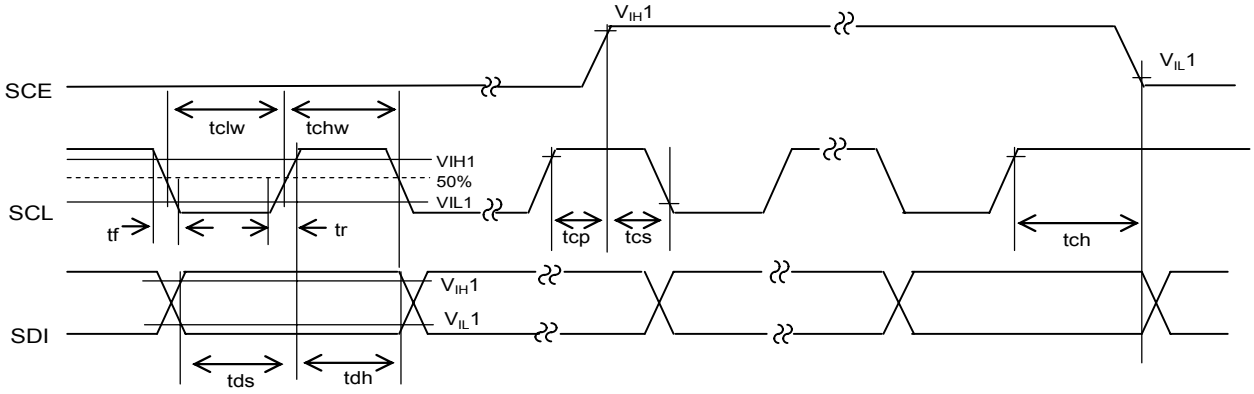



Figure 5.Serial Interface Timing

### Pin Description

| Symbol | Pin No. | Function | Active | I/O | Handling when unused |
|---|---|---|---|---|---|
| S1/P1/G1 to S6/P6/G6<br>S7 to S54 | 1 to 6<br>7 to 50<br>55,57,58 | Segment output.<br>The S1/P1/G1 to S6/P6/G6 pins can be used as general –purpose outputs. | - | O | OPEN |
| COM1 to COM4 | 51 to 54 | Common driver output pins. The frame frequency is fo[Hz]. | - | O | OPEN |
| S52/OSC | 60 | Segment output.<br>The pin S52/OSC can be used external frequency input pin when set up by the control data. | - | I/O | OPEN |
| | | Serial data transfer inputs. Must be connected to the controller. | | | GND |
| SCE<br>SCL<br>SDI | 62<br>63<br>64 | SCE: Chip enable<br>SCL: Synchronization clock<br>SDI: Transfer data | H<br>↑<br>- | I<br>I<br>I | |
| INHb | 61 | Display off control input<br>• INHb = low (VSS) ...Display forced off<br>S1/P1/G1 to S6/P6/G6 = low (VSS)<br>S7 to S54 = low (VSS)<br>COM1 to COM4 = low (VSS)<br>Shuts off current to the LCD drive bias voltage generation divider resistors.<br>Stop the internal oscillation circuit.<br>• INHb = high (VDD)...Display on<br>However, serial data transfer is possible when the display is forced off. | L | I | VDD |
| $V_{DD}$ | 56 | Power supply pin for the logic circuit block.<br>A power voltage of 2.7V to 6.0V must be applied to this pin. | - | - | - |
| $V_{SS}$ | 59 | Power supply pin. Must be connected to ground. | - | - | - |

### IO Equivalence Circuit

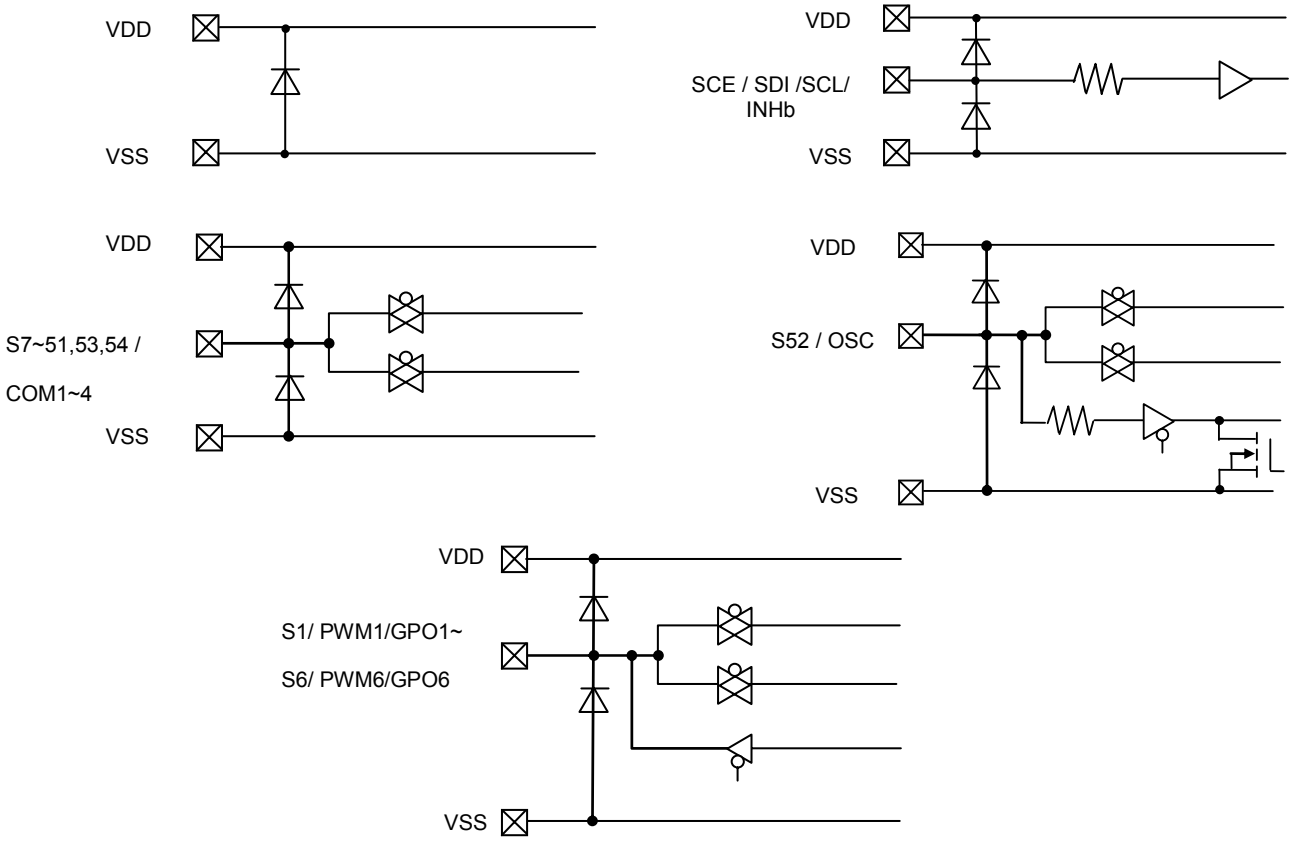



Figure 6. I/O Equivalence Circuit

**Serial Data Transfer Formats**

1. 1/4-Duty

(1) When SCL is stopped at the low level

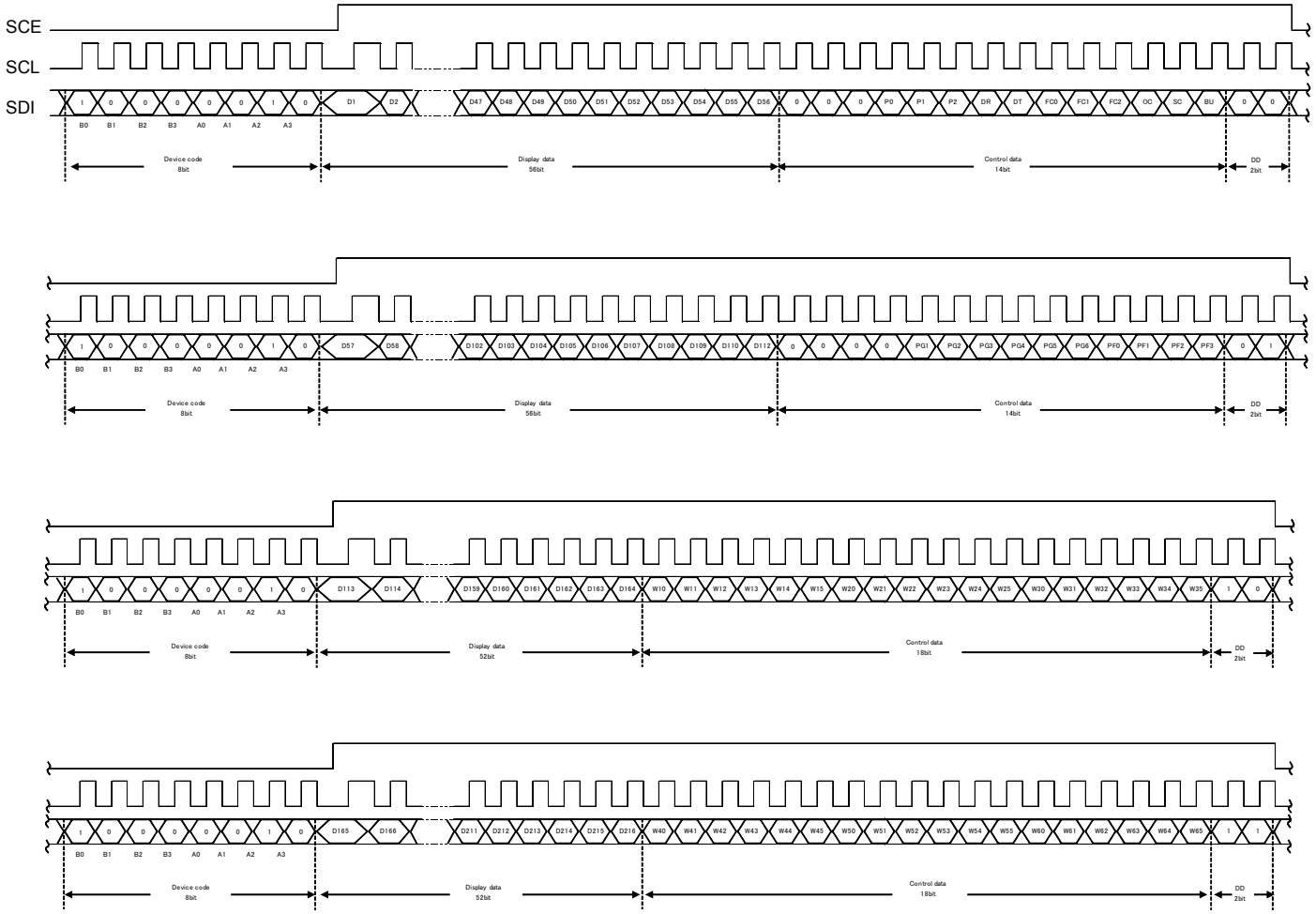



Figure 7. 3-SPI Data Transfer Format

Note : DD is direction data.

(2) When SCL is stopped at the high level

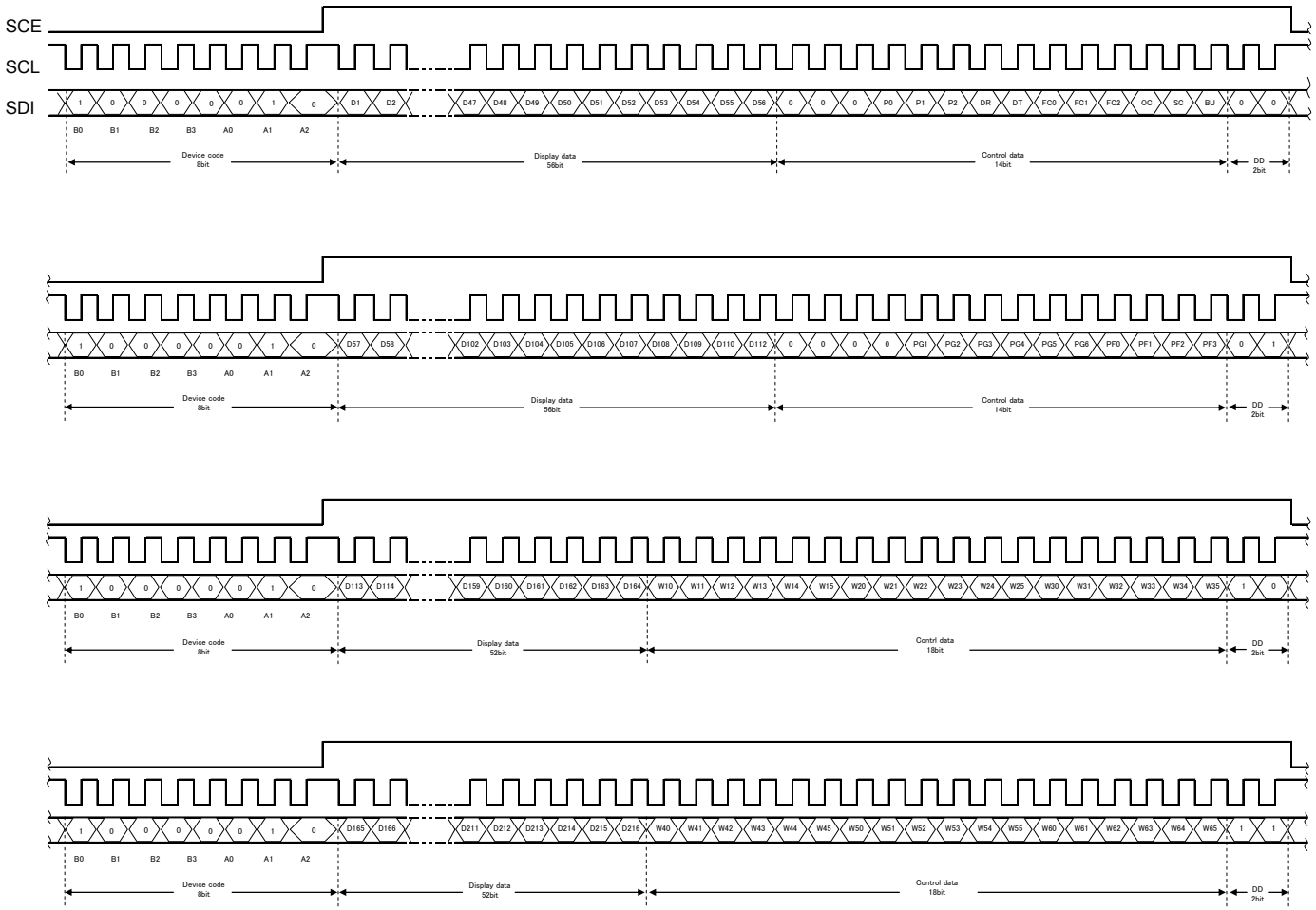



Figure 8. 3-SPI Data Transfer Format

Note : DD is direction data.

・Device code・・・・・・・・・・・・・・・・・・・・・・・”41H”
・D1～D216・・・・・・・・・・・・・・・・・・・・・・・・Display data
・P0～2・・・・・・・・・・・・・・・・・・・・・・・・・・・Segment / PWM / General Purpose output port switching control data
・DR・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・1/3-Bias drive or 1/2-Bias drive switching control data
・DT・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・1/4-Duty drive or 1/3-Duty drive switching control data
・FC0～FC2・・・・・・・・・・・・・・・・・・・・・・・・Frame frequency switching control data
・OC・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・Internal oscillator operating mode/External clock operating mode switching control data
・SC・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・Segment on/off switching control data
・BU・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・Normal mode/power-saving mode switching control data
・PG1～PG6・・・・・・・・・・・・・・・・・・・・・・・・PWM/General Purpose output switching control data
・PF0～PF3・・・・・・・・・・・・・・・・・・・・・・・・PWM output waveform frame frequency switching control data
・W10～W15, W20～W25, W30～W35,W40～W45, W50～W55, W60～W65
・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・PWM output waveform duty switching control data

2. 1/3-Duty
(1) When SCL is stopped at the low level

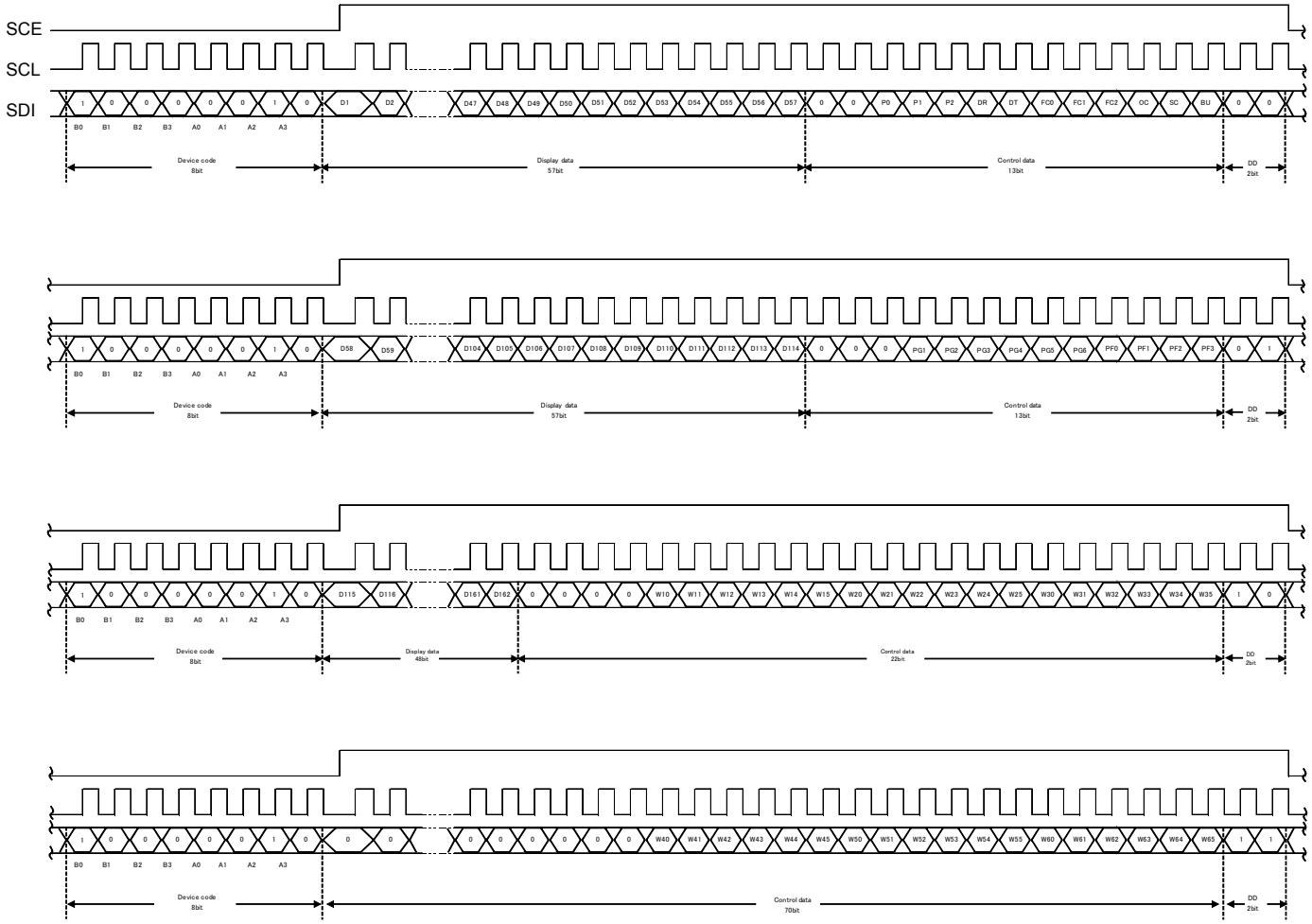



Figure 9. 3-SPI Data Transfer Format

Note : DD is direction data.

(2) When SCL is stopped at the high level

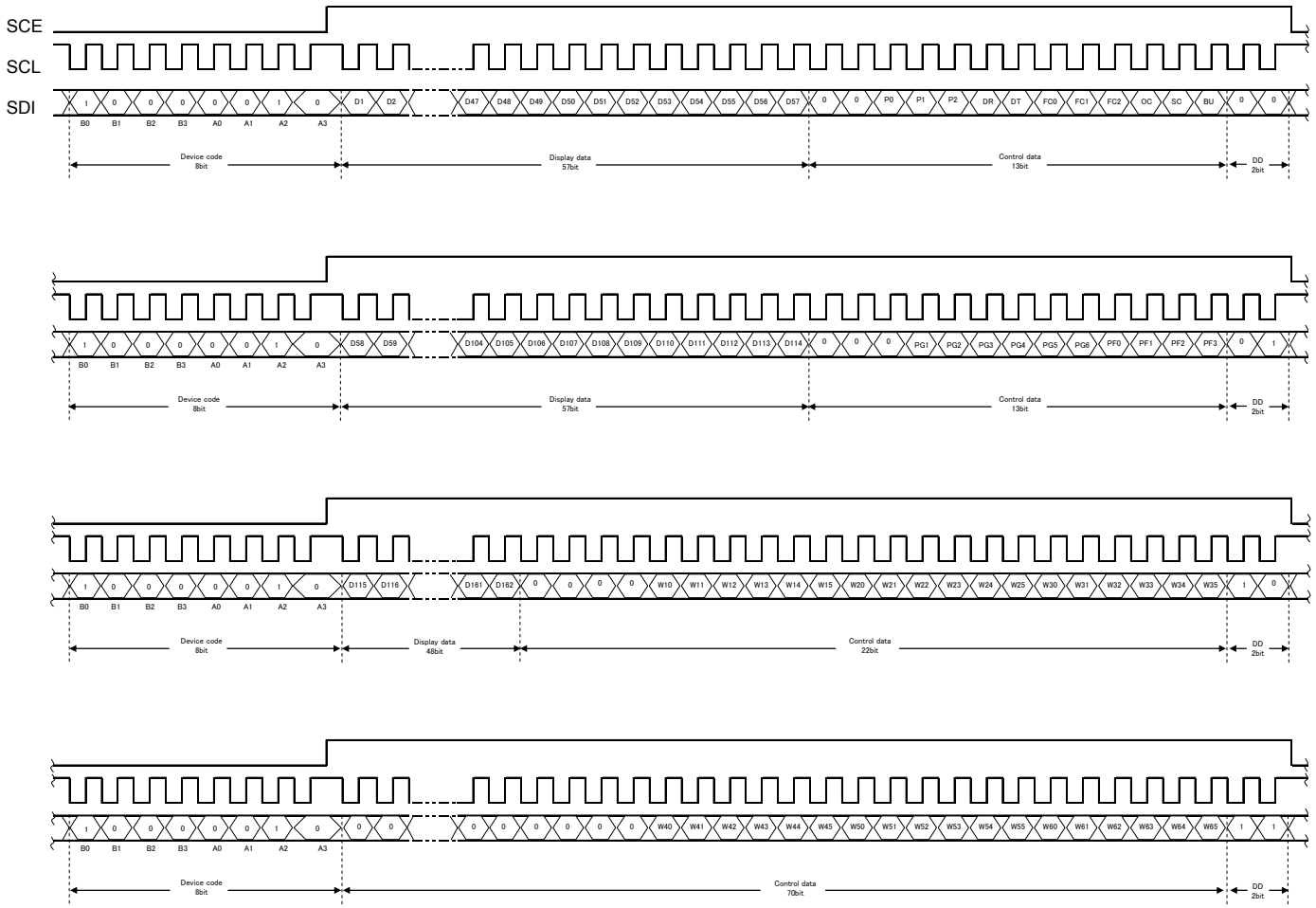



Figure 10. 3-SPI Data Transfer Format

Note : DD is direction data.

- Device code・・・・・・・・・・・・・・・・・・・・・・・”41H”
- D1～D162・・・・・・・・・・・・・・・・・・・・・・・・Display data
- P0～2・・・・・・・・・・・・・・・・・・・・・・・・・・・・Segment / PWM / General Purpose output port switching control data
- DR・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・1/3-Bias drive or 1/2-Bias drive switching control data
- DT・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・1/4-Duty drive or 1/3-Duty drive switching control data
- FC0～FC2・・・・・・・・・・・・・・・・・・・・・・・・Frame frequency switching control data
- OC・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・Internal oscillator operating mode/External clock operating mode switching control data
- SC・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・Segment on/off switching control data
- BU・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・Normal mode/power-saving mode switching control data
- PG1～PG6・・・・・・・・・・・・・・・・・・・・・・・・PWM/General Purpose output switching control data
- PF0～PF3・・・・・・・・・・・・・・・・・・・・・・・・PWM output waveform frame frequency switching control data
- W10～W15, W20～W25, W30～W35,W40～W45, W50～W55, W60～W65
  ・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・・PWM output waveform duty switching control data

### Control Data Functions

1.P0～P2:Segment / PWM / General Purpose output port switching control data

These control bits are used to select the function of the S1/P1 to S6/P6 output pins (Segment Output Pins or PWM Output Pins or General Purpose Output Pins).

Please refer to the table below.

| P0 | P1 | P2 | S1/P1/G1 | S2/P2/G2 | S3/P3/G3 | S4/P4/G4 | S5/P5/G5 | S6/P6/G6 |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | S1 | S2 | S3 | S4 | S5 | S6 |
| 0 | 0 | 1 | P1/G1 | S2 | S3 | S4 | S5 | S6 |
| 0 | 1 | 0 | P1/G1 | P2/G2 | S3 | S4 | S5 | S6 |
| 0 | 1 | 1 | P1/G1 | P2/G2 | P3/G3 | S4 | S5 | S6 |
| 1 | 0 | 0 | P1/G1 | P2/G2 | P3/G3 | P4/G4 | S5 | S6 |
| 1 | 0 | 1 | P1/G1 | P2/G2 | P3/G3 | P4/G4 | P5/G5 | S6 |
| 1 | 1 | 0 | P1/G1 | P2/G2 | P3/G3 | P4/G4 | P5/G5 | P6/G6 |
| 1 | 1 | 1 | S1 | S2 | S3 | S4 | S5 | S6 |

PWM output or General Purpose output is selected by PGx(x=1～6) control data bit.

When the General Purpose Output Port Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

| Output Pins | Corresponding Display Data | |
|---|---|---|
| | 1/4-Duty mode | 1/3-Duty mode |
| S1/P1/G1 | D1 | D1 |
| S2/P2/G2 | D5 | D4 |
| S3/P3/G3 | D9 | D7 |
| S4/P4/G4 | D13 | D10 |
| S5/P5/G5 | D17 | D13 |
| S6/P6/G6 | D21 | D16 |

When the General Purpose Output Port Function is selected, the respective output pin is output a “HIGH” level when it corresponding display data is set to “1”. Likewise, it will output a “LOW” level, if its corresponding display data is set to “0”.

For example, S4/P4/G4 is used as a General Purpose Output Port, if its corresponding display data – D13 is set to “1”, then S4/P4/G4 will output “HIGH” level. Likewise, if D13 is set to “0”, then S4/P4/G4 will output “LOW” level.

2. DR: 1/3-Bias drive or 1/2-Bias drive switching control data

This control data bit selects either 1/3-Bias drive or 1/2-Bias drive.

| DR | Bias drive scheme |
|---|---|
| 0 | 1/3-Bias drive |
| 1 | 1/2-Bias drive |

3. DT: 1/4-Duty drive or 1/3-Duty drive switching control data

This control data bit selects either 1/4-Duty drive or 1/3-Duty drive.

| DT | Duty drive scheme |
|---|---|
| 0 | 1/4-Duty drive |
| 1 | 1/3-Duty drive |

4. FC0, FC1, FC2: Frame frequency switching control data

These control data bits set the frame frequency for common and segment output waveforms.

| FC0 | FC1 | FC2 | Frame Frequency fo(Hz) |
|---|---|---|---|
| 0 | 0 | 0 | fosc/6144 |
| 0 | 0 | 1 | fosc/5376 |
| 0 | 1 | 0 | fosc/4608 |
| 0 | 1 | 1 | fosc/3840 |
| 1 | 0 | 0 | fosc/3072 |
| 1 | 0 | 1 | fosc/2304 |
| 1 | 1 | 0 | fosc/1920 |
| 1 | 1 | 1 | fosc/1536 |

Note: fosc: Internal oscillation frequency (300 [kHz] typ.)

5. OC: Internal oscillator operating mode/External clock operating mode switching control data

| OC | Operating mode | In/Out pin(S52/OSC) status |
|---|---|---|
| 0 | Internal oscillator | S52 (segment output) |
| 1 | External Clock | OSC (clock input) |

6. SC: Segment on/off switching control data
This control data bit controls the on/off state of the segments.

| SC | Display state |
|---|---|
| 0 | On |
| 1 | Off |

Note that when the segments are turned off by setting SC to “1”, the segments are turned off by outputting segment off waveforms from the segment output pins.

7. BU: Normal mode/power-saving mode switching control data
This control data bit selects either normal mode or power-saving mode.

| BU | Mode |
|---|---|
| 0 | Normal Mode |
| 1 | Power-saving Mode |

Power-saving mode status: S1/P1/G1 to S6/P6/G6 = active only General Purpose output
S7 to S54 = low(VSS)
COM1 to COM4 = low(VSS)
Shut off current to the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However , serial data transfer is possible when Power-saving mode.

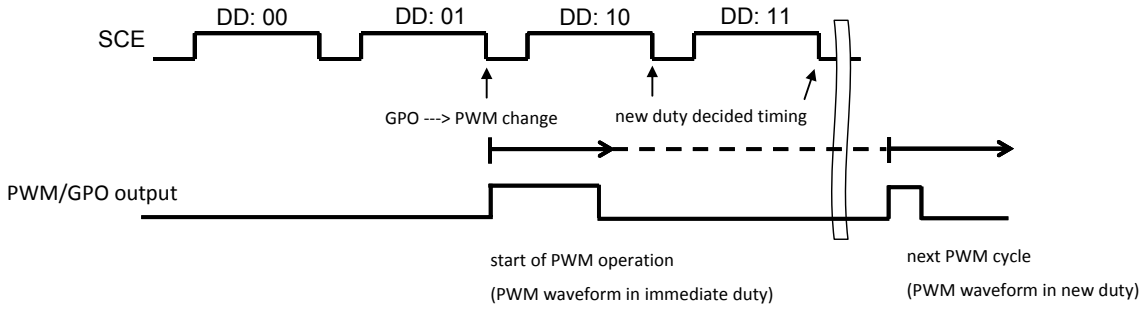
8. PG1, PG2, PG3, PG4, PG5, PG6: PWM/General Purpose output switching control data
This control data bit select either PWM output or General Purpose output of Sx/Px/Gx pins.(x=1～6)

| PGx(x=1～6) | Mode |
|---|---|
| 0 | PWM output |
| 1 | General Purpose output |

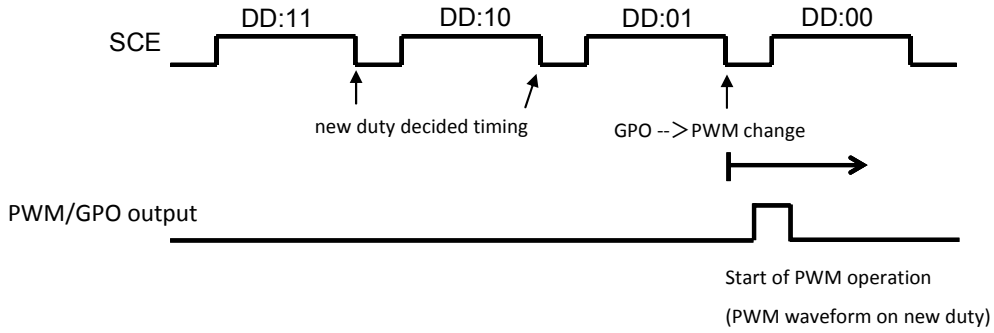
<Note: PWM<->GPO Changing function>

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 01 during GPO ---> PWM change.
- Please take care of reflect timing of new duty setting of DD: 10, DD: 11 is from the next PWM.




In order to avoid this operation, please input commands reversely as below.



9. PF0, PF1, PF2, PF3: PWM output waveform frame frequency switching control data
These control data bits set the frame frequency for PWM output waveforms.

| PF0 | PF1 | PF2 | PF3 | PWM output Frame Frequency fp(Hz) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | fosc/2048 |
| 0 | 0 | 0 | 1 | fosc/1920 |
| 0 | 0 | 1 | 0 | fosc/1792 |
| 0 | 0 | 1 | 1 | fosc/1664 |
| 0 | 1 | 0 | 0 | fosc/1536 |
| 0 | 1 | 0 | 1 | fosc/1408 |
| 0 | 1 | 1 | 0 | fosc/1280 |
| 0 | 1 | 1 | 1 | fosc/1152 |
| 1 | 0 | 0 | 0 | fosc/1024 |
| 1 | 0 | 0 | 1 | fosc/896 |
| 1 | 0 | 1 | 0 | fosc/768 |
| 1 | 0 | 1 | 1 | fosc/640 |
| 1 | 1 | 0 | 0 | fosc/512 |
| 1 | 1 | 0 | 1 | fosc/384 |
| 1 | 1 | 1 | 0 | fosc/256 |
| 1 | 1 | 1 | 1 | fosc/128 |

10.W10～W15, W20～W25, W30～W35, W40～W45, W50～W55, W60～W65: PWM output waveform duty switching control data
These control data bits set the high level pulse width(duty) for PWM output waveforms.

| Wn0 | Wn1 | Wn2 | Wn3 | Wn4 | Wn5 | PWM duty |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | (1/64) x Tp |
| 1 | 0 | 0 | 0 | 0 | 0 | (2/64) x Tp |
| 0 | 1 | 0 | 0 | 0 | 0 | (3/64) x Tp |
| 1 | 1 | 0 | 0 | 0 | 0 | (4/64) x Tp |
| 0 | 0 | 1 | 0 | 0 | 0 | (5/64) x Tp |
| 1 | 0 | 1 | 0 | 0 | 0 | (6/64) x Tp |
| 0 | 1 | 1 | 0 | 0 | 0 | (7/64) x Tp |
| 1 | 1 | 1 | 0 | 0 | 0 | (8/64) x Tp |
| 0 | 0 | 0 | 1 | 0 | 0 | (9/64) x Tp |
| 1 | 0 | 0 | 1 | 0 | 0 | (10/64) x Tp |
| 0 | 1 | 0 | 1 | 0 | 0 | (11/64) x Tp |
| 1 | 1 | 0 | 1 | 0 | 0 | (12/64) x Tp |
| 0 | 0 | 1 | 1 | 0 | 0 | (13/64) x Tp |
| 1 | 0 | 1 | 1 | 0 | 0 | (14/64) x Tp |
| 0 | 1 | 1 | 1 | 0 | 0 | (15/64) x Tp |
| 1 | 1 | 1 | 1 | 0 | 0 | (16/64) x Tp |
| 0 | 0 | 0 | 0 | 1 | 0 | (17/64) x Tp |
| 1 | 0 | 0 | 0 | 1 | 0 | (18/64) x Tp |
| 0 | 1 | 0 | 0 | 1 | 0 | (19/64) x Tp |
| 1 | 1 | 0 | 0 | 1 | 0 | (20/64) x Tp |
| 0 | 0 | 1 | 0 | 1 | 0 | (21/64) x Tp |
| 1 | 0 | 1 | 0 | 1 | 0 | (22/64) x Tp |
| 0 | 1 | 1 | 0 | 1 | 0 | (23/64) x Tp |
| 1 | 1 | 1 | 0 | 1 | 0 | (24/64) x Tp |
| 0 | 0 | 0 | 1 | 1 | 0 | (25/64) x Tp |
| 1 | 0 | 0 | 1 | 1 | 0 | (26/64) x Tp |
| 0 | 1 | 0 | 1 | 1 | 0 | (27/64) x Tp |
| 1 | 1 | 0 | 1 | 1 | 0 | (28/64) x Tp |
| 0 | 0 | 1 | 1 | 1 | 0 | (29/64) x Tp |
| 1 | 0 | 1 | 1 | 1 | 0 | (30/64) x Tp |
| 0 | 1 | 1 | 1 | 1 | 0 | (31/64) x Tp |
| 1 | 1 | 1 | 1 | 1 | 0 | (32/64) x Tp |

| Wn0 | Wn1 | Wn2 | Wn3 | Wn4 | Wn5 | PWM duty |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 1 | (33/64) x Tp |
| 1 | 0 | 0 | 0 | 0 | 1 | (34/64) x Tp |
| 0 | 1 | 0 | 0 | 0 | 1 | (35/64) x Tp |
| 1 | 1 | 0 | 0 | 0 | 1 | (36/64) x Tp |
| 0 | 0 | 1 | 0 | 0 | 1 | (37/64) x Tp |
| 1 | 0 | 1 | 0 | 0 | 1 | (38/64) x Tp |
| 0 | 1 | 1 | 0 | 0 | 1 | (39/64) x Tp |
| 1 | 1 | 1 | 0 | 0 | 1 | (40/64) x Tp |
| 0 | 0 | 0 | 1 | 0 | 1 | (41/64) x Tp |
| 1 | 0 | 0 | 1 | 0 | 1 | (42/64) x Tp |
| 0 | 1 | 0 | 1 | 0 | 1 | (43/64) x Tp |
| 1 | 1 | 0 | 1 | 0 | 1 | (44/64) x Tp |
| 0 | 0 | 1 | 1 | 0 | 1 | (45/64) x Tp |
| 1 | 0 | 1 | 1 | 0 | 1 | (46/64) x Tp |
| 0 | 1 | 1 | 1 | 0 | 1 | (47/64) x Tp |
| 1 | 1 | 1 | 1 | 0 | 1 | (48/64) x Tp |
| 0 | 0 | 0 | 0 | 1 | 1 | (49/64) x Tp |
| 1 | 0 | 0 | 0 | 1 | 1 | (50/64) x Tp |
| 0 | 1 | 0 | 0 | 1 | 1 | (51/64) x Tp |
| 1 | 1 | 0 | 0 | 1 | 1 | (52/64) x Tp |
| 0 | 0 | 1 | 0 | 1 | 1 | (53/64) x Tp |
| 1 | 0 | 1 | 0 | 1 | 1 | (54/64) x Tp |
| 0 | 1 | 1 | 0 | 1 | 1 | (55/64) x Tp |
| 1 | 1 | 1 | 0 | 1 | 1 | (56/64) x Tp |
| 0 | 0 | 0 | 1 | 1 | 1 | (57/64) x Tp |
| 1 | 0 | 0 | 1 | 1 | 1 | (58/64) x Tp |
| 0 | 1 | 0 | 1 | 1 | 1 | (59/64) x Tp |
| 1 | 1 | 0 | 1 | 1 | 1 | (60/64) x Tp |
| 0 | 0 | 1 | 1 | 1 | 1 | (61/64) x Tp |
| 1 | 0 | 1 | 1 | 1 | 1 | (62/64) x Tp |
| 0 | 1 | 1 | 1 | 1 | 1 | (63/64) x Tp |
| 1 | 1 | 1 | 1 | 1 | 1 | (64/64) x Tp |

Note:W10～W15:S1/P1/G1 PWM duty data
W20～W25:S2/P2/G2 PWM duty data
W30～W35:S3/P3/G3 PWM duty data
W40～W45:S4/P4/G4 PWM duty data
W50～W55:S5/P5/G5 PWM duty data
W60～W65:S6/P6/G6 PWM duty data

n = 1～6
Tp = 1/fp

**Display Data and Output Pin Correspondence**

1. 1/4-Duty

| Output pin | COM1 | COM2 | COM3 | COM4 |
|---|---|---|---|---|
| S1/P1/G1 | D1 | D2 | D3 | D4 |
| S2/P2/G2 | D5 | D6 | D7 | D8 |
| S3/P3/G3 | D9 | D10 | D11 | D12 |
| S4/P4/G4 | D13 | D14 | D15 | D16 |
| S5/P5/G5 | D17 | D18 | D19 | D20 |
| S6/P6/G6 | D21 | D22 | D23 | D24 |
| S7 | D25 | D26 | D27 | D28 |
| S8 | D29 | D30 | D31 | D32 |
| S9 | D33 | D34 | D35 | D36 |
| S10 | D37 | D38 | D39 | D40 |
| S11 | D41 | D42 | D43 | D44 |
| S12 | D45 | D46 | D47 | D48 |
| S13 | D49 | D50 | D51 | D52 |
| S14 | D53 | D54 | D55 | D56 |
| S15 | D57 | D58 | D59 | D60 |
| S16 | D61 | D62 | D63 | D64 |
| S17 | D65 | D66 | D67 | D68 |
| S18 | D69 | D70 | D71 | D72 |
| S19 | D73 | D74 | D75 | D76 |
| S20 | D77 | D78 | D79 | D80 |
| S21 | D81 | D82 | D83 | D84 |
| S22 | D85 | D86 | D87 | D88 |
| S23 | D89 | D90 | D91 | D92 |
| S24 | D93 | D94 | D95 | D96 |
| S25 | D97 | D98 | D99 | D100 |
| S26 | D101 | D102 | D103 | D104 |
| S27 | D105 | D106 | D107 | D108 |
| S28 | D109 | D110 | D111 | D112 |
| S29 | D113 | D114 | D115 | D116 |
| S30 | D117 | D118 | D119 | D120 |
| S31 | D121 | D122 | D123 | D124 |
| S32 | D125 | D126 | D127 | D128 |
| S33 | D129 | D130 | D131 | D132 |
| S34 | D133 | D134 | D135 | D136 |
| S35 | D137 | D138 | D139 | D140 |
| S36 | D141 | D142 | D143 | D144 |
| S37 | D145 | D146 | D147 | D148 |
| S38 | D149 | D150 | D151 | D152 |
| S39 | D153 | D154 | D155 | D156 |
| S40 | D157 | D158 | D159 | D160 |
| S41 | D161 | D162 | D163 | D164 |
| S42 | D165 | D166 | D167 | D168 |
| S43 | D169 | D170 | D171 | D172 |
| S44 | D173 | D174 | D175 | D176 |
| S45 | D177 | D178 | D179 | D180 |
| S46 | D181 | D182 | D183 | D184 |
| S47 | D185 | D186 | D187 | D188 |
| S48 | D189 | D190 | D191 | D192 |
| S49 | D193 | D194 | D195 | D196 |
| S50 | D197 | D198 | D199 | D200 |
| S51 | D201 | D202 | D203 | D204 |
| S52 | D205 | D206 | D207 | D208 |
| S53 | D209 | D210 | D211 | D212 |
| S54 | D213 | D214 | D215 | D216 |

Note: The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

To illustrate further, the states of the S21 output pin is given in the table below.

| Display data | | | | State of S21 Output Pin |
|---|---|---|---|---|
| D81 | D82 | D83 | D84 | |
| 0 | 0 | 0 | 0 | LCD Segments corresponding to COM1 to COM4 are OFF. |
| 0 | 0 | 0 | 1 | LCD Segment corresponding to COM4 is ON. |
| 0 | 0 | 1 | 0 | LCD Segment corresponding to COM3 is ON. |
| 0 | 0 | 1 | 1 | LCD Segments corresponding to COM3 and COM4 are ON. |
| 0 | 1 | 0 | 0 | LCD Segment corresponding to COM2 is ON. |
| 0 | 1 | 0 | 1 | LCD Segments corresponding to COM2 and COM4 are ON. |
| 0 | 1 | 1 | 0 | LCD Segments corresponding to COM2 and COM3 are ON. |
| 0 | 1 | 1 | 1 | LCD Segments corresponding to COM2, COM3 and COM4 are ON. |
| 1 | 0 | 0 | 0 | LCD Segment corresponding to COM1 is ON. |
| 1 | 0 | 0 | 1 | LCD Segments corresponding to COM1 and COM4 are ON. |
| 1 | 0 | 1 | 0 | LCD Segments corresponding to COM1 and COM3 are ON. |
| 1 | 0 | 1 | 1 | LCD Segments corresponding to COM1, COM3 and COM4 are ON. |
| 1 | 1 | 0 | 0 | LCD Segments corresponding to COM1 and COM2 are ON. |
| 1 | 1 | 0 | 1 | LCD Segments corresponding to COM1, COM2, and COM4 are ON. |
| 1 | 1 | 1 | 0 | LCD Segments corresponding to COM1, COM2, and COM3 are ON. |
| 1 | 1 | 1 | 1 | LCD Segments corresponding to COM1 to COM 4 are ON. |

2. 1/3-Duty

| Output pin | COM1 | COM2 | COM3 |
|---|---|---|---|
| S1/P1/G1 | D1 | D2 | D3 |
| S2/P2/G2 | D4 | D5 | D6 |
| S3/P3/G3 | D7 | D8 | D9 |
| S4/P4/G4 | D10 | D11 | D12 |
| S5/P5/G5 | D13 | D14 | D15 |
| S6/P6/G6 | D16 | D17 | D18 |
| S7 | D19 | D20 | D21 |
| S8 | D22 | D23 | D24 |
| S9 | D25 | D26 | D27 |
| S10 | D28 | D29 | D30 |
| S11 | D31 | D32 | D33 |
| S12 | D34 | D35 | D36 |
| S13 | D37 | D38 | D39 |
| S14 | D40 | D41 | D42 |
| S15 | D43 | D44 | D45 |
| S16 | D46 | D47 | D48 |
| S17 | D49 | D50 | D51 |
| S18 | D52 | D53 | D54 |
| S19 | D55 | D56 | D57 |
| S20 | D58 | D59 | D60 |
| S21 | D61 | D62 | D63 |
| S22 | D64 | D65 | D66 |
| S23 | D67 | D68 | D69 |
| S24 | D70 | D71 | D72 |
| S25 | D73 | D74 | D75 |
| S26 | D76 | D77 | D78 |
| S27 | D79 | D80 | D81 |
| S28 | D82 | D83 | D84 |
| S29 | D85 | D85 | D87 |
| S30 | D88 | D89 | D90 |
| S31 | D91 | D92 | D93 |
| S32 | D94 | D95 | D96 |
| S33 | D97 | D98 | D99 |
| S34 | D100 | D101 | D102 |
| S35 | D103 | D104 | D105 |
| S36 | D106 | D107 | D108 |
| S37 | D109 | D110 | D111 |
| S38 | D112 | D113 | D114 |
| S39 | D115 | D116 | D117 |
| S40 | D118 | D119 | D120 |
| S41 | D121 | D122 | D123 |
| S42 | D124 | D125 | D126 |
| S43 | D127 | D128 | D129 |
| S44 | D130 | D131 | D132 |
| S45 | D133 | D134 | D135 |
| S46 | D136 | D137 | D138 |
| S47 | D139 | D140 | D141 |
| S48 | D142 | D143 | D144 |
| S49 | D145 | D146 | D147 |
| S50 | D148 | D149 | D150 |
| S51 | D151 | D152 | D153 |
| S52 | D154 | D155 | D156 |
| S53 | D157 | D158 | D159 |
| S54 | D160 | D161 | D162 |

Note: The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S6/P6/G6.

To illustrate further, the states of the S21 output pin is given in the table below.

| Display data | | | State of S21 Output Pin |
|---|---|---|---|
| D61 | D62 | D63 | |
| 0 | 0 | 0 | LCD Segments corresponding to COM1 to COM3 are OFF. |
| 0 | 0 | 1 | LCD Segment corresponding to COM3 is ON. |
| 0 | 1 | 0 | LCD Segment corresponding to COM2 is ON. |
| 0 | 1 | 1 | LCD Segments corresponding to COM2 and COM3 are ON. |
| 1 | 0 | 0 | LCD Segment corresponding to COM1 is ON. |
| 1 | 0 | 1 | LCD Segments corresponding to COM1 and COM3 are ON. |
| 1 | 1 | 0 | LCD Segments corresponding to COM1 and COM2 are ON. |
| 1 | 1 | 1 | LCD Segments corresponding to COM1, COM2 and COM3 are ON. |

### Output Waveforms (1/4-Duty 1/3-Bias Drive Scheme)

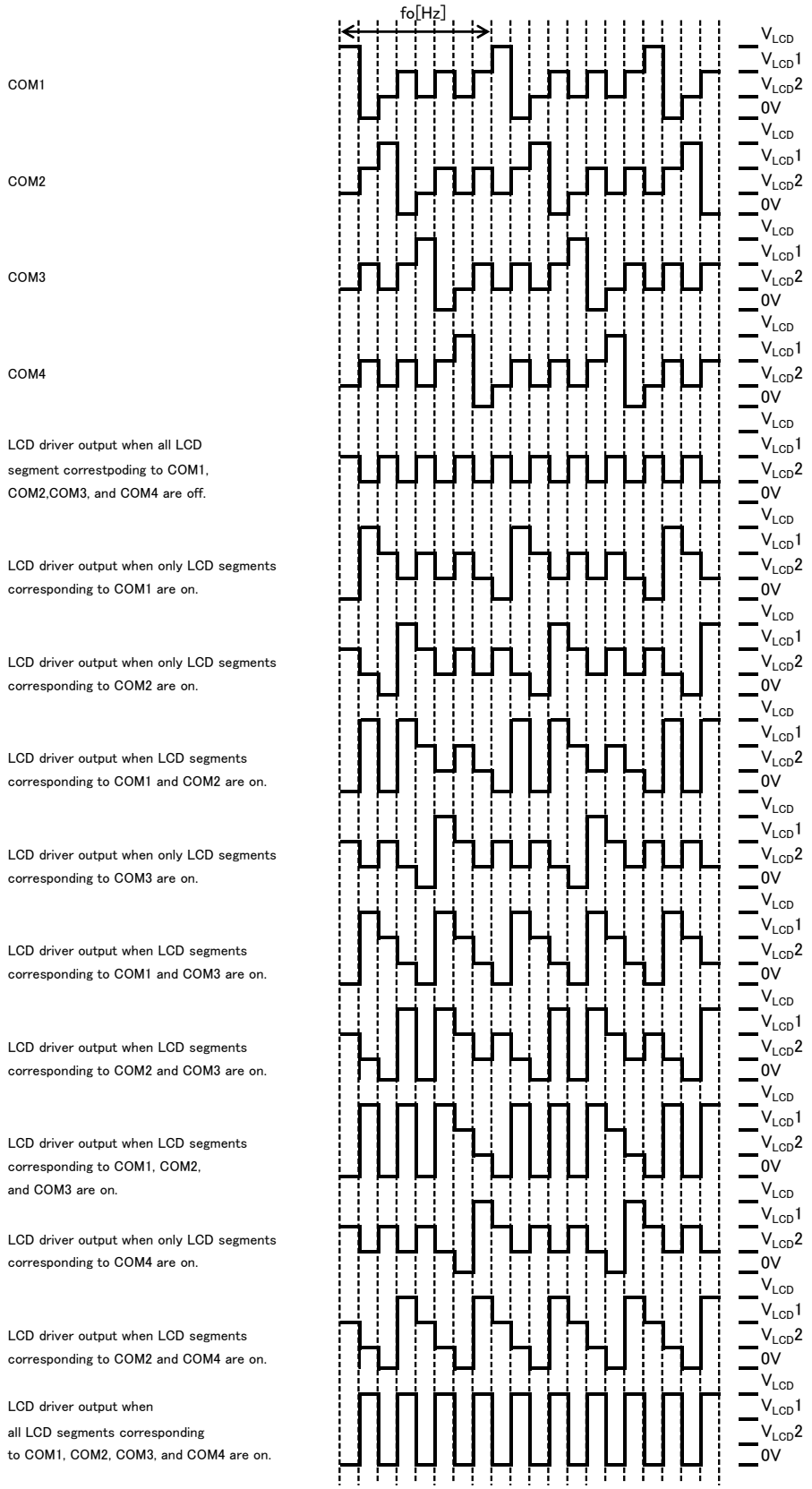



Figure 11. LCD Waveform (1/4-Duty, 1/3-Bias)

### Output Waveforms (1/4-Duty 1/2-Bias Drive Scheme)

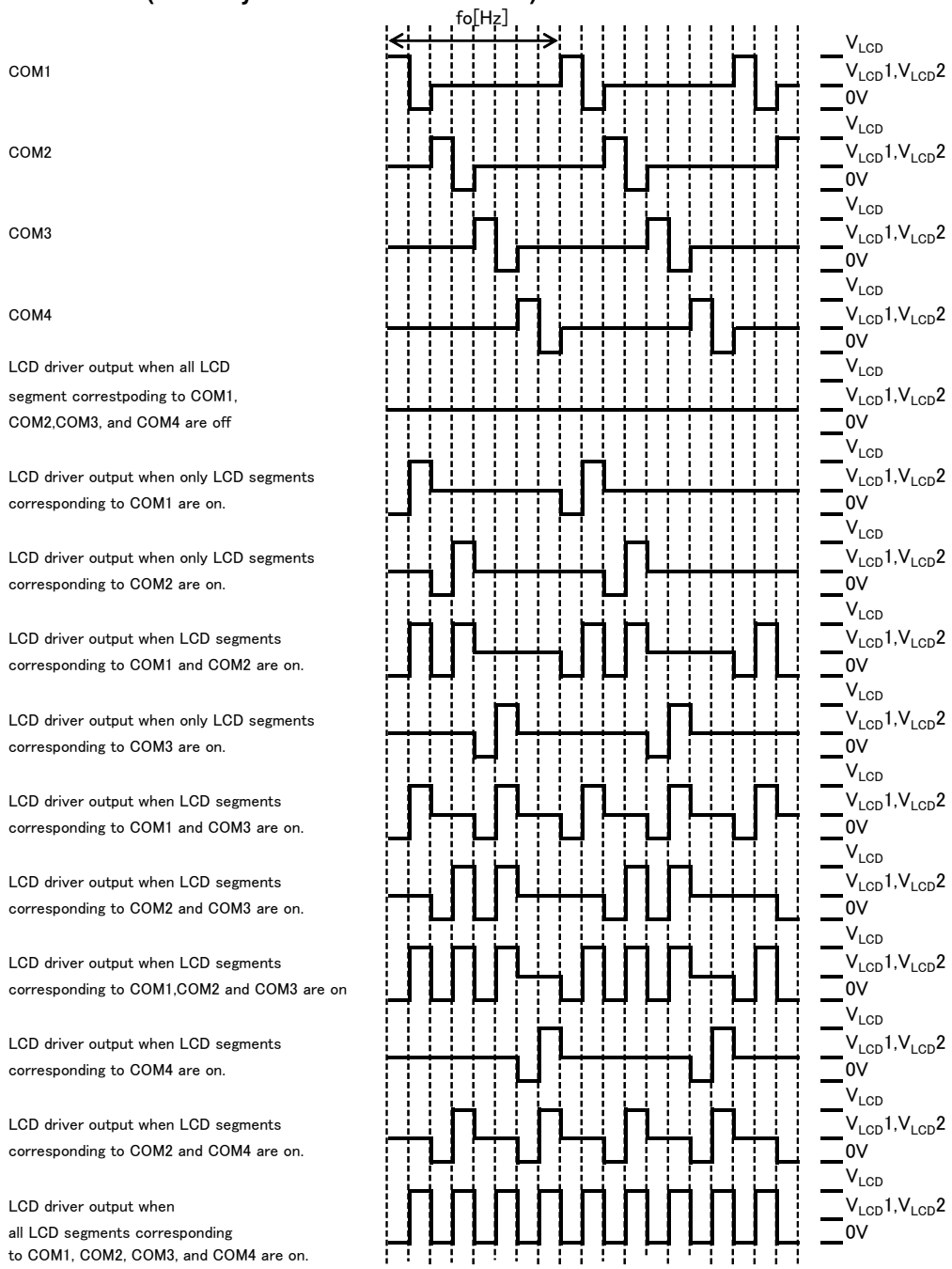



Figure 12. LCD Waveform (1/4-Duty, 1/2-Bias)

### Output Waveforms (1/3-Duty 1/3-Bias Drive Scheme)

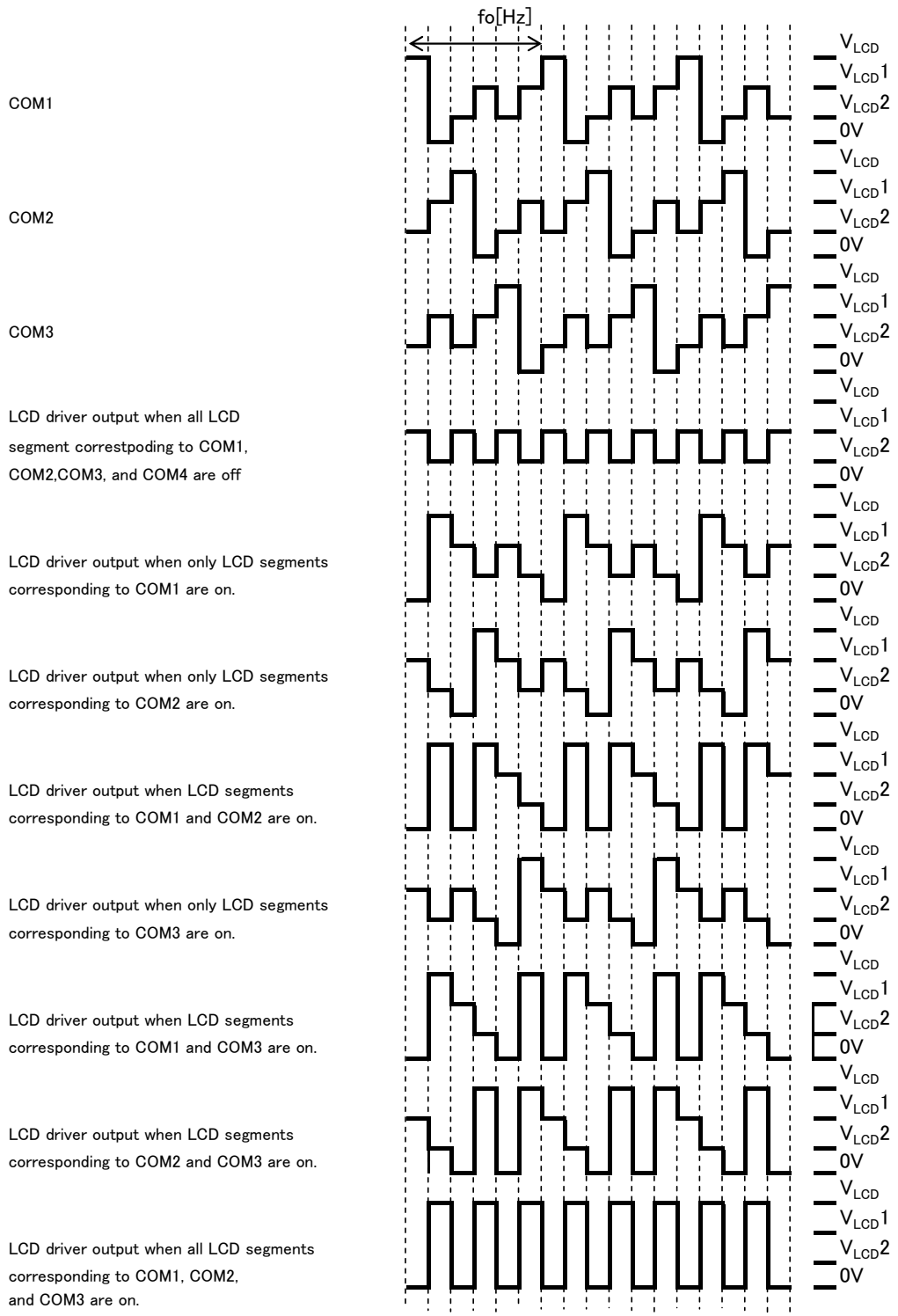



Figure 13. LCD Waveform (1/3-Duty, 1/3-Bias)

※COM4 function is same as COM1 at 1/3-Duty.

### Output Waveforms (1/3-Duty 1/2-Bias Drive Scheme)

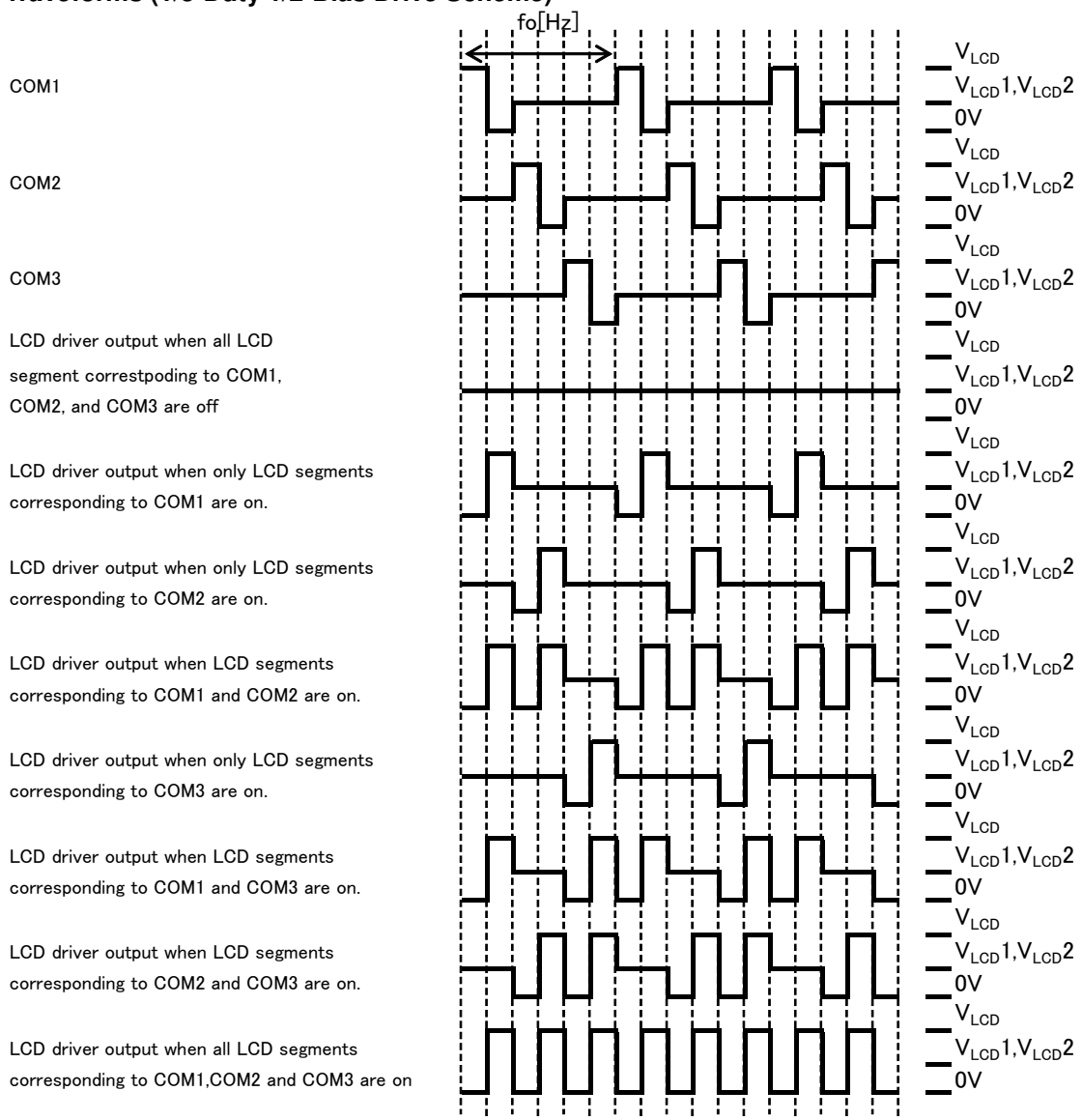



Figure 14. LCD Waveform (1/3-Duty, 1/2-Bias)

※COM4 function is same as COM1 at 1/3-Duty.

**The INHb pin and Display Control**

Since the IC internal data (1/4-Duty: the display data D1 to D216 and the control data, 1/3-Duty: the display data D1 to D162 and the control data) is undefined when power is first applied, applications should set the INH pin low at the same time as power is applied to turn off the display (This sets the S1/P1/G1 to S6/P6/G6, S7 to S54, COM1 to COM4 to the VSS level.) and during this period send serial data from the controller. The controller should then set the INH pin high after the data transfer has completed. This procedure prevents meaningless displays at power on.

1. 1/4-Duty

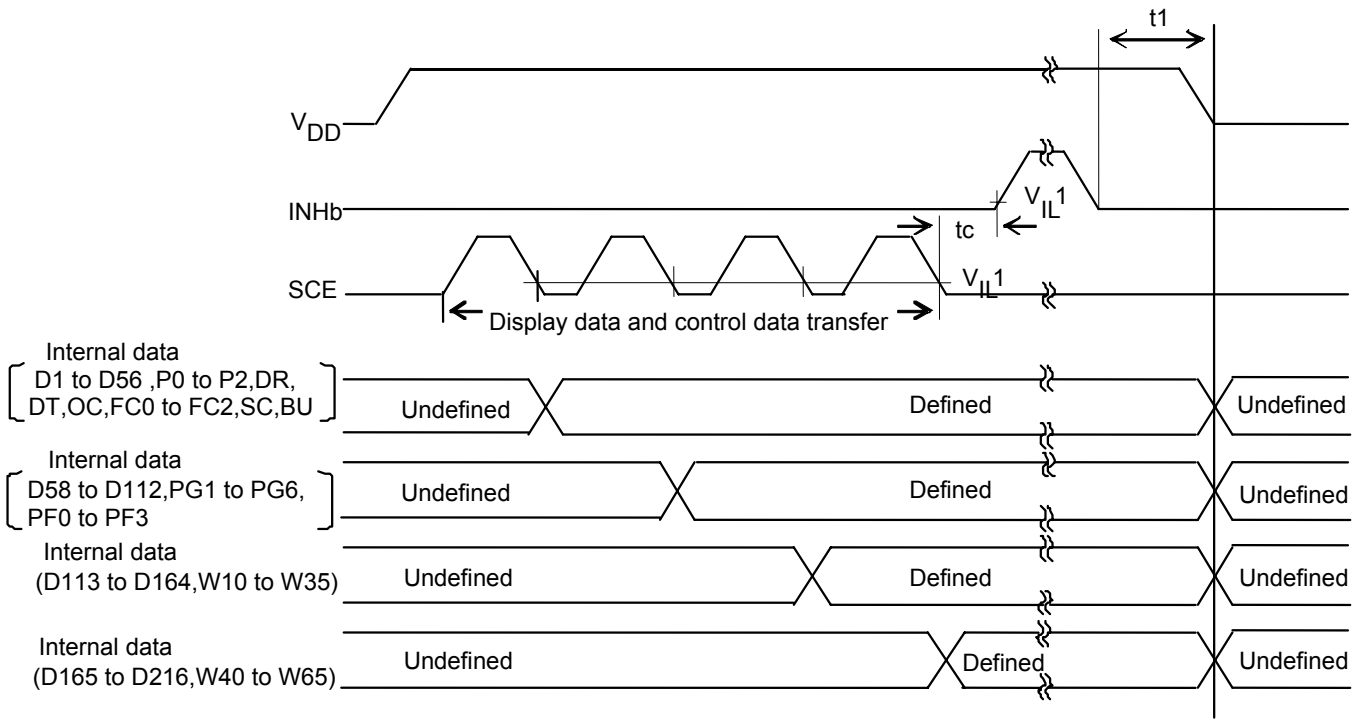



Figure 15. Power ON/OFF and INHb Control Sequence (1/4-Duty)

2. 1/3-Duty

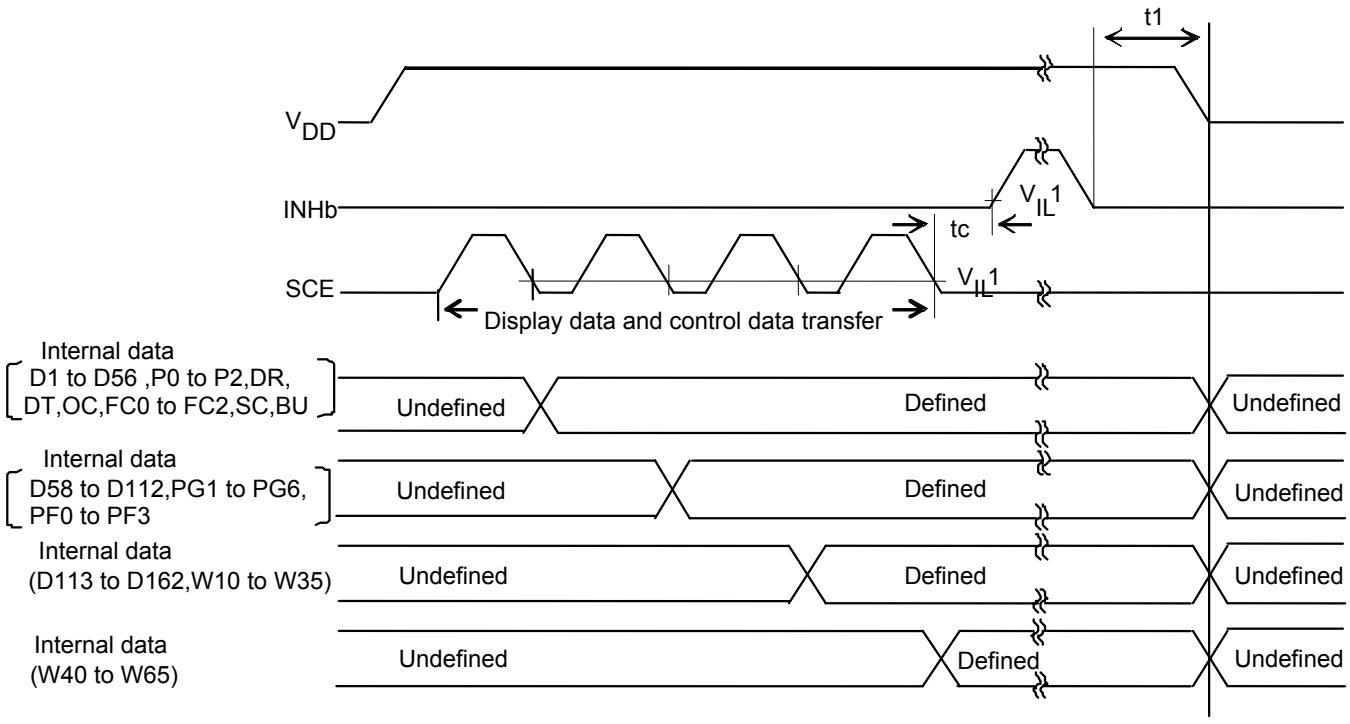



Figure 16. Power ON/OFF and INHb Control Sequence (1/3-Duty)

Note: t1≥0, tc: min 10us

### Oscillation Stabilization Time of the Internal Oscillation Circuit

It must be noted that the oscillation of the internal oscillation circuit is unstable for a maximum of 100μs (oscillation stabilization time) after oscillation has started.

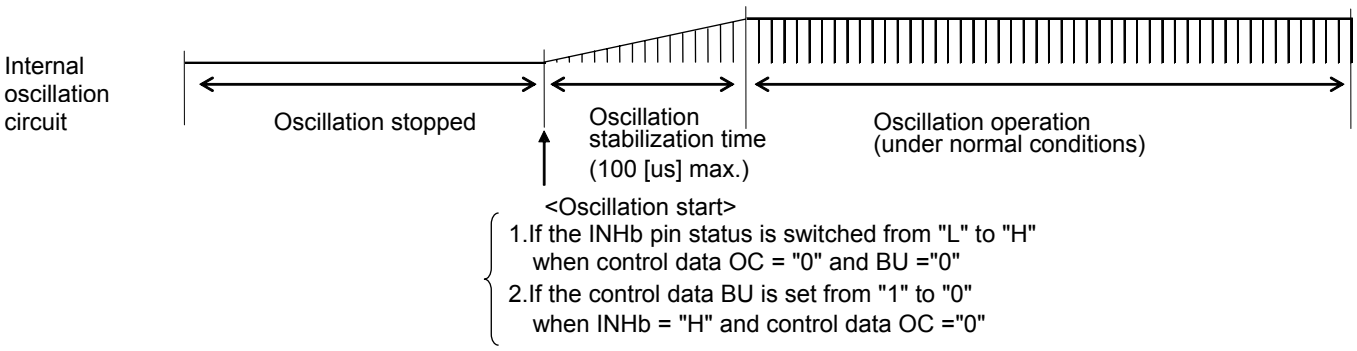



Figure 17. Oscillation Stabilization Time

### Voltage Detection Type Reset Circuit (VDET)

The Voltage Detection Type Reset Circuit generates an output signal and resets the system when power is applied for the first time and when voltage drops (that is, for example, the power supply voltage is less than or equal to the power down detection voltage (VDET = 1.8V typ.). To ensure that this reset function works properly, it is recommended that a capacitor must be connected to the power supply line so that both the power supply voltage (VDD) rise time when power is first applied and the power supply voltage (VDD) fall time when the voltage drops are at least 1ms.

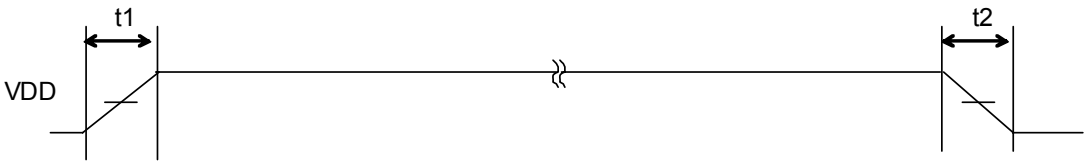



Figure 18. VDET Detection Timing

Power supply voltage VDD rise time: t1 > 1ms
Power supply voltage VDD fall time: t2 > 1ms

### Reset Condition

When BU97510CKV-M is initialized, the internal status after power supply has been reset as the following table.

Table 1. control data reset condition

| Instruction | At Reset Condition |
|---|---|
| S1/P1/G1 to S2/P2/G2 pin | [P0,P1,P2]=[0,0,0]:all segment output |
| LCD bias | DR=0:1/3-Bias |
| LCD duty | DT=0:1/4-Duty |
| DISPLAY frequency | [FC0,FC1,FC2]=[0,0,0]:fosc/6144 |
| Display clock mode | OC=0:Internal oscillator |
| LCD display | SC=1:OFF |
| Power mode | BU=1:Power saving mode |
| PWM/GPO output | PGx=0:PWM output(x=1～6) |
| PWM frequency | [PF0,PF1,PF2,PF3]=[0,0,0,0]: fosc /2048 |
| PWM duty | [Wn0～Wn5]=[0,0,0,0,0,0]<br>:(1/64)xTp(n=1～6,Tp=1/fp) |

## Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## Operational Notes – continued

**11. Unused Input Pins**

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

**12. Regarding the Input Pin of the IC**

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

**13. Ceramic Capacitor**

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

**14. Data transmission**

To refrain from data transmission is strongly recommended while power supply is rising up or falling down to prevent from the occurrence of disturbances on transmission and reception.