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LCD Segment Drivers

Multi-function LCD Segment Drivers

BU97530KVT

MAX 445 Segment(89segx5COM)

General Description

The BU97530KVT is 1/5, 1/4, 1/3 or 1/1 duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The BU97530KVT can drive up to 445 LCD Segments directly. The BU97530KVT can also control up to 9 general-purpose output ports. These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

Features

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- Either 1/5, 1/4, 1/3 or 1/1 duty (static) can be selected with the serial control data.
 - 1/5 duty drive: Up to 445 segments can be driven
 - 1/4 duty drive: Up to 360 segments can be driven
 - 1/3 duty drive: Up to 270 segments can be driven
 - 1/1 duty drive: Up to 90 segments can be driven
- Serial data control of frame frequency for common and segment output waveforms.
- Serial data control of switching between the segment output port, PWM output port and general-purpose output port functions.(Max 9 ports)
- Built-in OSC circuit
- Integrated Power-on Reset circuit
- No external component
- Low power consumption design
- Supports Line and Frame Inversion

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 445 Segments
- Display Duty: 1/1,1/3,1/4,1/5 selectable
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

Packages

TQFP100V

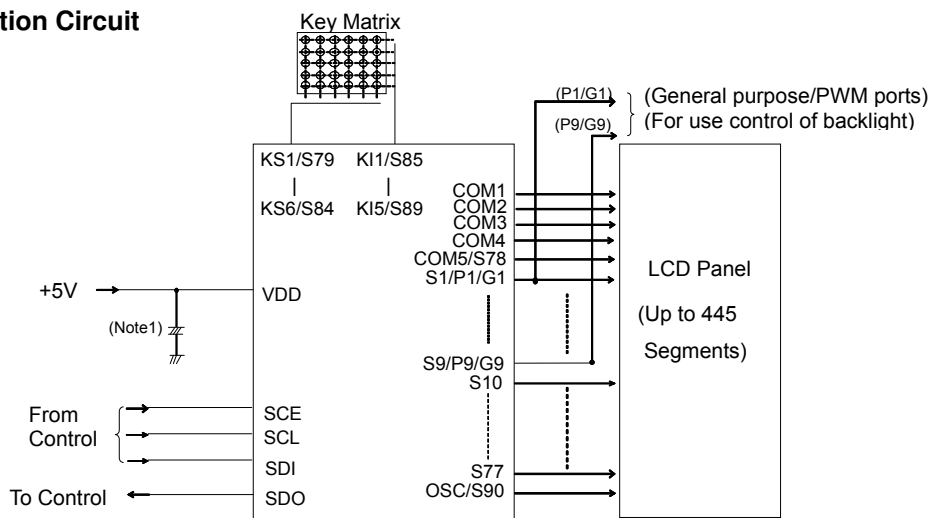
W(Typ.)×D(Typ.)×H(Max.)



Applications

- Car audio, Home electrical appliance, Meter equipment etc.

Typical Application Circuit



(Note1) Insert capacitors between VDD and VSS C≥0.1µF

Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

Block Diagram

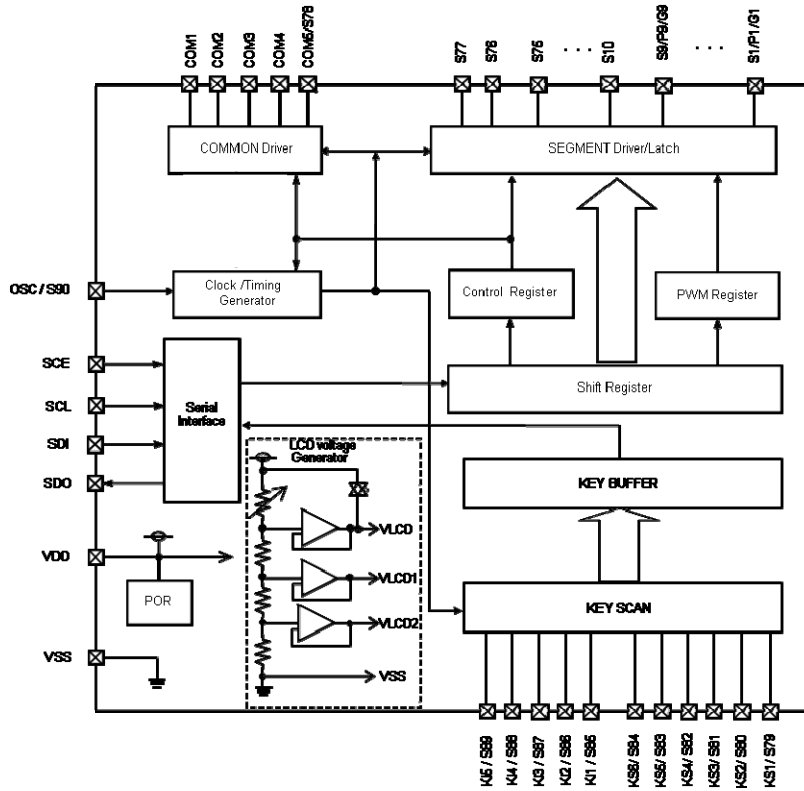


Figure 2. Block Diagram

Pin Arrangement

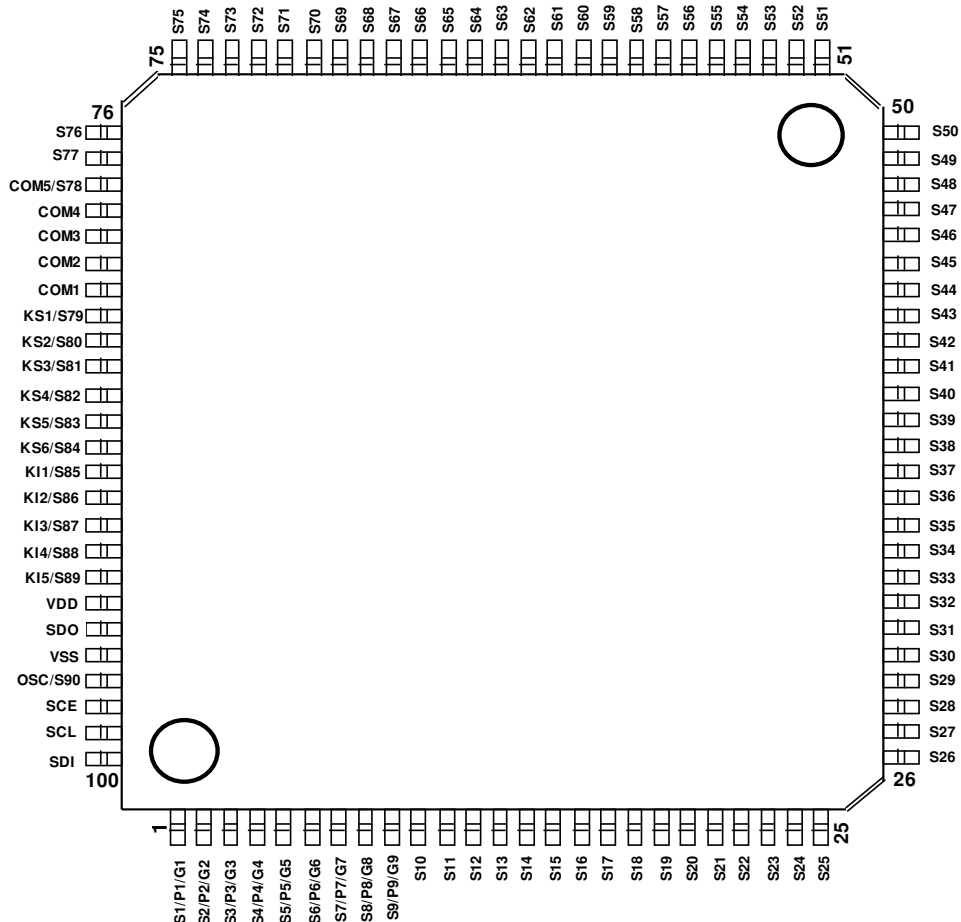


Figure 3. Pin Configuration(TOP VIEW)

Absolute Maximum Ratings(Ta = 25°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VDD max	VDD	-0.3 to +6.5	V
Input voltage	VIN1	SCE, SCL, SDI	-0.3 to +6.5	V
	VIN2	KI1 to KI5	-0.3 to +6.5	V
Allowable loss	Pd		1.49(Note2)	W
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

(Note2) Derate by 1.49mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta = -40 to +85°C, VSS = 0.0V)

Parameter	Symbol	Conditions	Ratings			Unit
			Min	Typ	Max	
Supply Voltage	VDD		2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	VH1	SCE, SCL, SDI		-	0.03VDD	-	V
	VH2	KI1 to KI5		-	0.1VDD	-	V
Power-on Detection Voltage	VDET	VDD		1.4	1.8	2.2	V
"H" Level Input Voltage	VIH1	SCE, SCL, SDI	4.0V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	VIH2	SCE, SCL, SDI	2.7V ≤ VDD < 4.0V	0.8VDD	-	VDD	V
	VIH3	KI1 to KI5		0.7VDD	-	VDD	V
"L" Level Input Voltage	VIL1	SCE, SCL, SDI KI1 to KI5		0	-	0.2VDD	V
Input Floating Voltage	VIF	KI1 to KI5		-	-	0.05VDD	V
Pull-down Resistance	RPD	KI1 to KI5	VDD=5.0V	50	100	250	KΩ
Output Off Leakage Current	IOFFH	SDO	VO=6.0V	-	-	6.0	μA
"H" Level Input Current	IIH1	SCE, SCL, SDI	VI = 5.5V	-	-	5.0	μA
"L" Level Input Current	IIL1	SCE, SCL, SDI	VI = 0V	-5.0	-	-	μA
"H" Level Output Voltage	VOH1	S1 to S90	IO = -20μA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	VOH2	COM1 to COM5	IO = -100μA, VLCD=1.00*VDD	VDD-0.9	-	-	
	VOH3	P1/G1 to P9/G9	IO = -1mA	VDD-0.9	-	-	
	VOH4	KS1 to KS6	IO = -500uA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	VOL1	S1 to S90	IO = 20μA	-	-	0.9	V
	VOL2	COM1 to COM5	IO = 100μA	-	-	0.9	
	VOL3	P1/G1 to P9/G9	IO = 1mA	-	-	0.9	
	VOL4	KS1 to KS6	IO = 25uA	0.2	0.5	1.5	
	VOL5	SDO	IO = 1mA	-	0.1	0.5	
Middle Level Output Voltage	VMID1	S1 to S90	1/2 bias IO = ±20μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	V
	VMID2	COM1 to COM5	1/2 bias IO = ±100μA VLCD=1.00*VDD	1/2VDD -0.9	-	1/2VDD +0.9	
	VMID3	S1 to S90	1/3 bias IO = ±20μA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	VMID4	S1 to S90	1/3 bias IO = ±20μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
	VMID5	COM1 to COM5	1/3 bias IO = ±100μA VLCD=1.00*VDD	2/3VDD -0.9	-	2/3VDD +0.9	
	VMID6	COM1 to COM5	1/3 bias IO = ±100μA VLCD=1.00*VDD	1/3VDD -0.9	-	1/3VDD +0.9	
Current Consumption	IDD1	VDD	Power-saving mode	-	-	15	μA
	IDD2	VDD	VDD = 5.0V Output open, 1/2 bias Frame frequency=80Hz VLCD=1.00*VDD	-	100	200	
	IDD3	VDD	VDD = 5.0V Output open, 1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	130	250	

Oscillation Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency 1	fosc1	-	VDD = 2.7V to 6.0V	300	-	720	kHz
Oscillator Frequency 2	fosc2	-	VDD = 5V	510	600	690	kHz
External Clock Frequency ^(Note3)	fosc3	OSC/S90	External clock mode (OC=1)	30	-	1000	kHz
External Clock Duty	tdty	OSC/S90	External clock mode (OC=1)	30	50	70	%

(Note3) Frame frequency is decided external frequency and dividing ratio of FC0,FC1,FC2 setting.

【Reference Data】

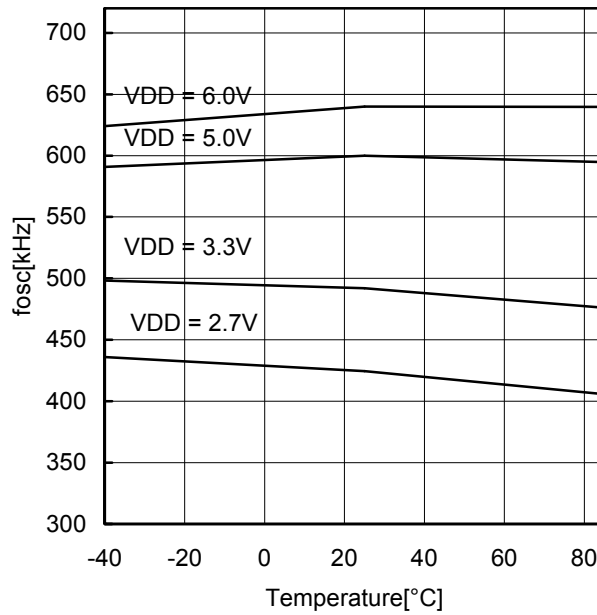


Figure 4. Typical Temperature Characteristics

MPU Interface Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

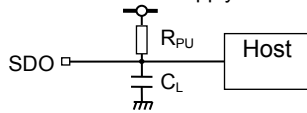
Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	tds	SCL, SDI		120	-	-	ns
Data Hold Time	tdh	SCL, SDI		120	-	-	ns
SCE Wait Time	tcp	SCE, SCL		120	-	-	ns
SCE Setup Time	tcs	SCE, SCL		120	-	-	ns
SCE Hold Time	tch	SCE, SCL		120	-	-	ns
Clock Cycle Time	tccyc	SCL		320	-	-	ns
High-level Clock Pulse Width	tchwh	SCL		120	-	-	ns
Low-level Clock Pulse Width (Write)	tclww	SCL		120	-	-	ns
Low-Level Clock Pulse Width (Read)	tclwr	SCL	RPU=4.7KΩ CL=10pF(Note4)	1.6	-	-	us
Rise Time	tr	SCE, SCL, SDI		-	160	-	ns
Fall Time	tf	SCE, SCL, SDI		-	160	-	ns
SDO Output Delay Time	tdc	SDO	RPU=4.7KΩ CL=10pF(Note4)	-	-	1.5	μs
SDO Rise Time	tdr	SDO	RPU=4.7KΩ CL=10pF(Note4)	-	-	1.5	μs

(Note4) Since SDO is an open-drain output, "tdc" and "tdr" depend on the resistance of the pull-up resistor RPU and the load capacitance CL.

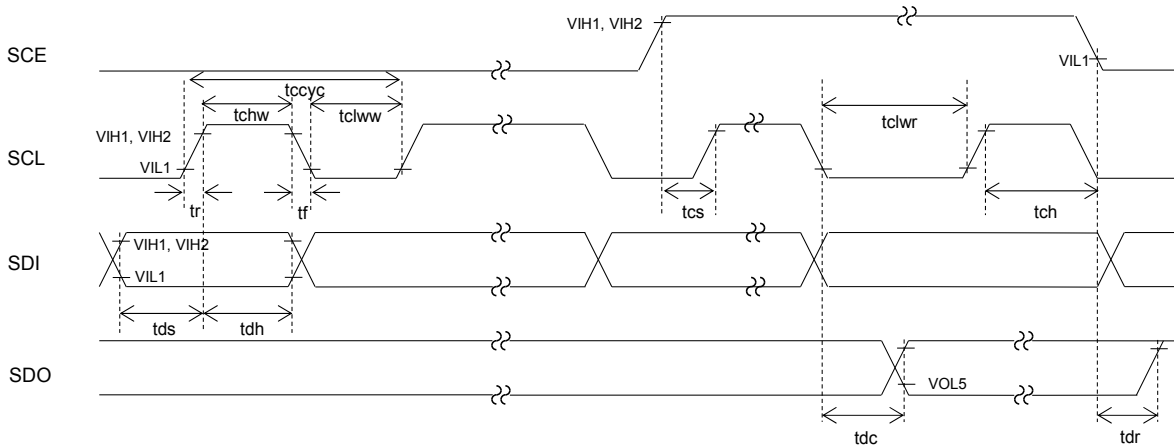
RPU: 1kΩ≤RPU≤10kΩ is recommended.

CL: A parasitic capacitance to VSS in an application circuit. Any component is not necessary to be attached.

Power supply for I/O level



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

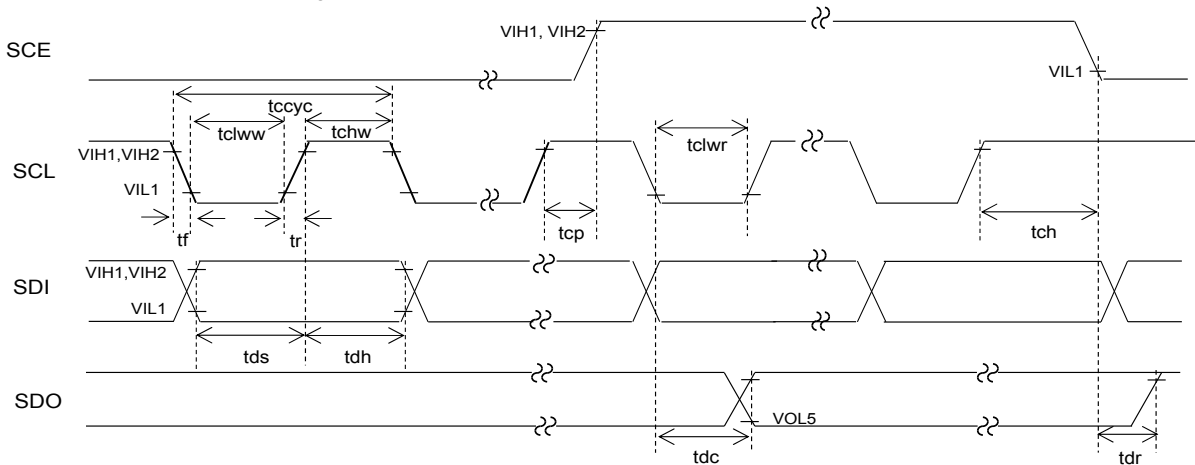


Figure 5. Serial Interface Timing

Pin Description

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S9/P9/G9	1 to 9	Segment output for displaying the display data transferred by serial data input. The S1/P1/G1 to S9/P9/G9 pins can also be used as General –purpose outputs when so set up by the control data.	-	O	OPEN
S10 to S77	10 to 77	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S79 to KS6/S84	83 to 88	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S79 to KS6/S84 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
K11/S85 to K15/S89	89 to 93	Key scan inputs These pins have built-in pull-down resistors. The K11/S85 to K15/S89 pins can be used as segment outputs when so specified by the control data.	-	I/O	OPEN
COM1 to COM4	79 to 82	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
COM5/S78	78	COMMON / SEGMENT output for LCD driving Assigned as COMMON output in 1/5 Duty mode and SEGMENT output in 1/1 Duty, 1/3 Duty and 1/4 Duty modes	-	O	OPEN
OSC/S90	97	Segment output for displaying the display data transferred by serial data input. The pin OSC/S90 can be used as external frequency input pin when set up by the control data.	-	I/O	OPEN
SCE SCL SDI	98 99 100	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable SCL: Synchronization clock SDI: Transfer data	H ↑ -	I I I	GND
SDO	95	Output data	-	O	OPEN
VDD	94	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	96	Power supply pin. Must be connected to ground.	-	-	-

IO Equivalent Circuit

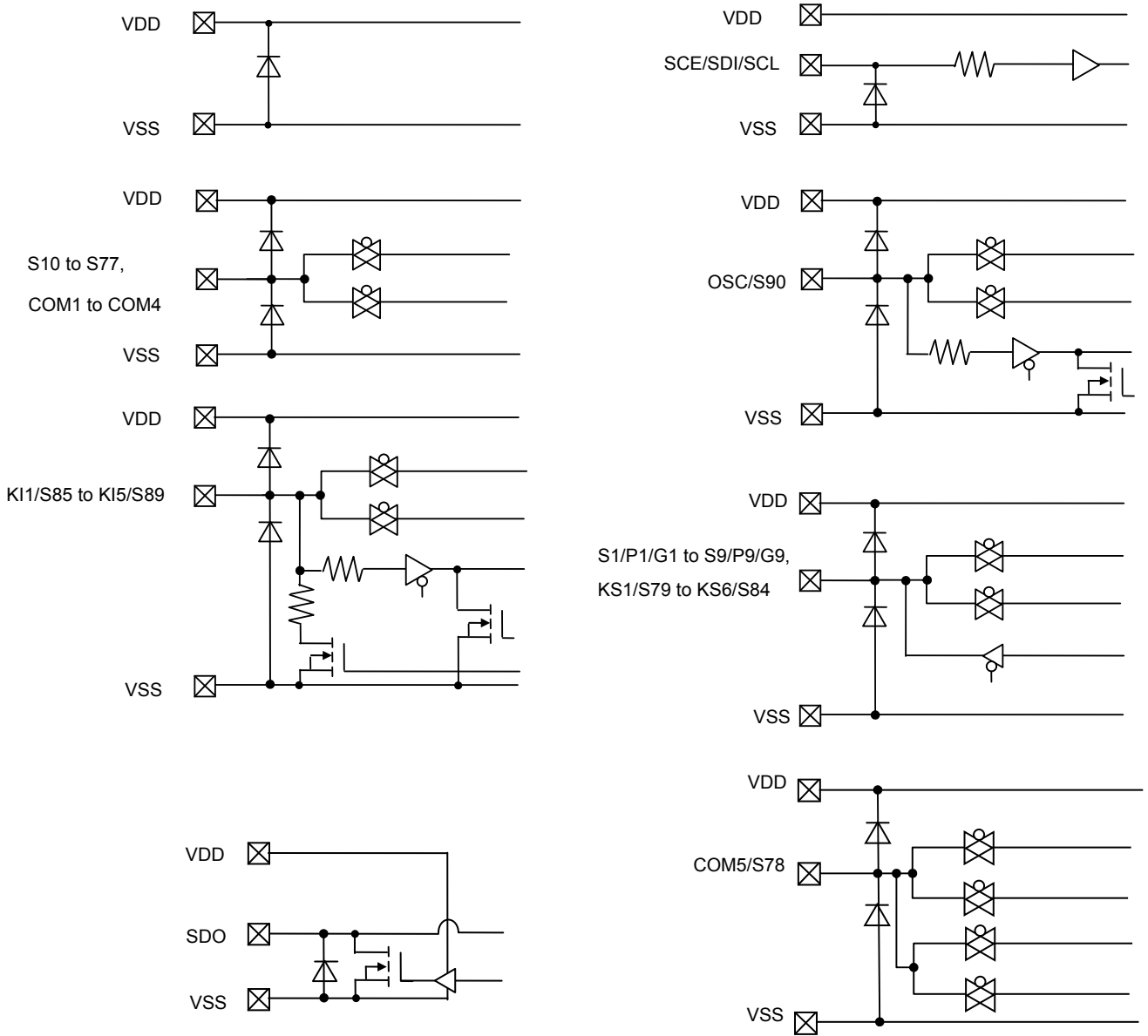


Figure 6. I/O Equivalent Circuit

Serial Data Transfer Formats

1.1/5-Duty

(1)When SCL is stopped at the low level

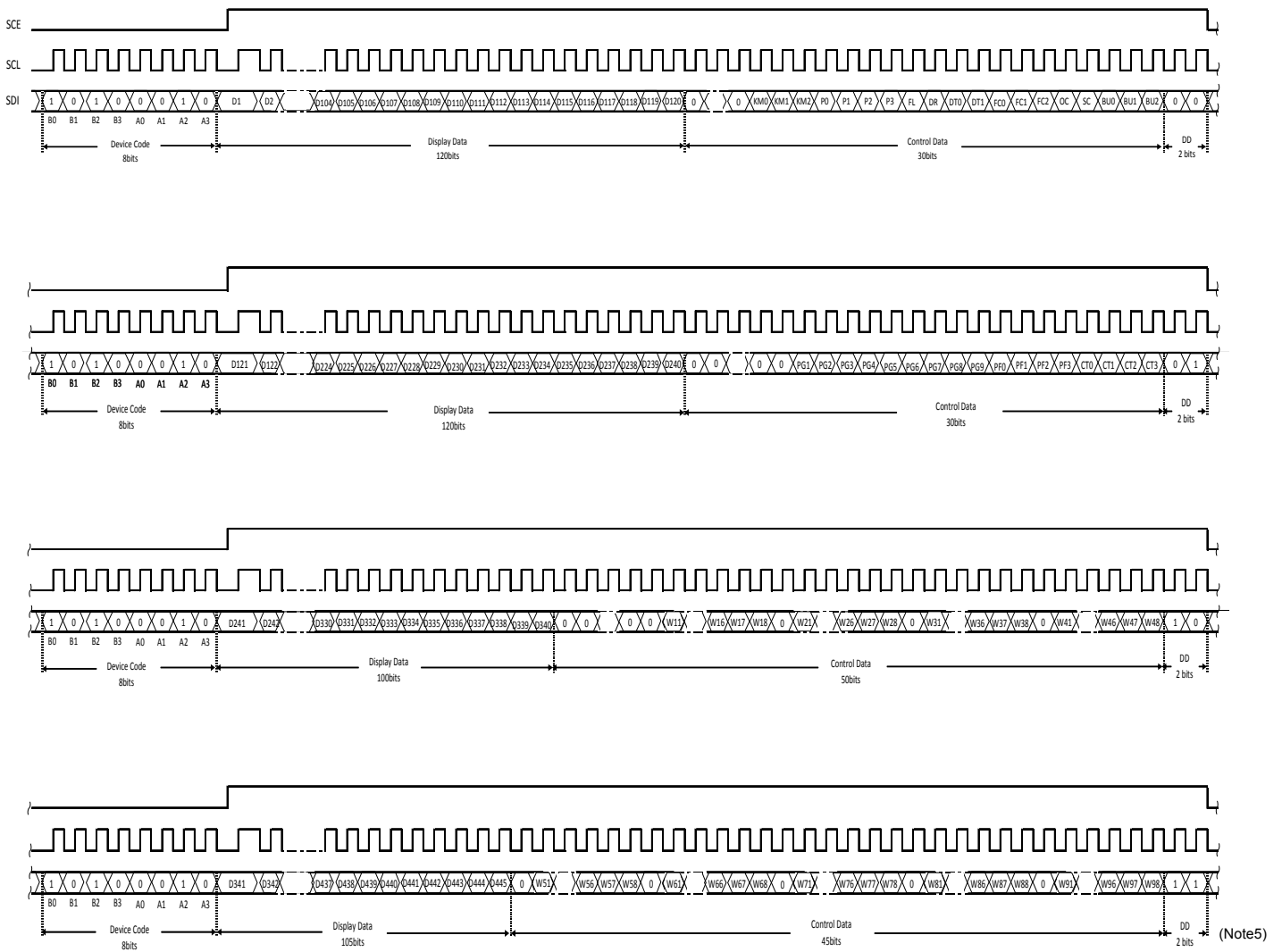


Figure 7. 3-SPI Data Transfer Format

(Note5) DD is direction data.

(2)When SCL is stopped at the high level

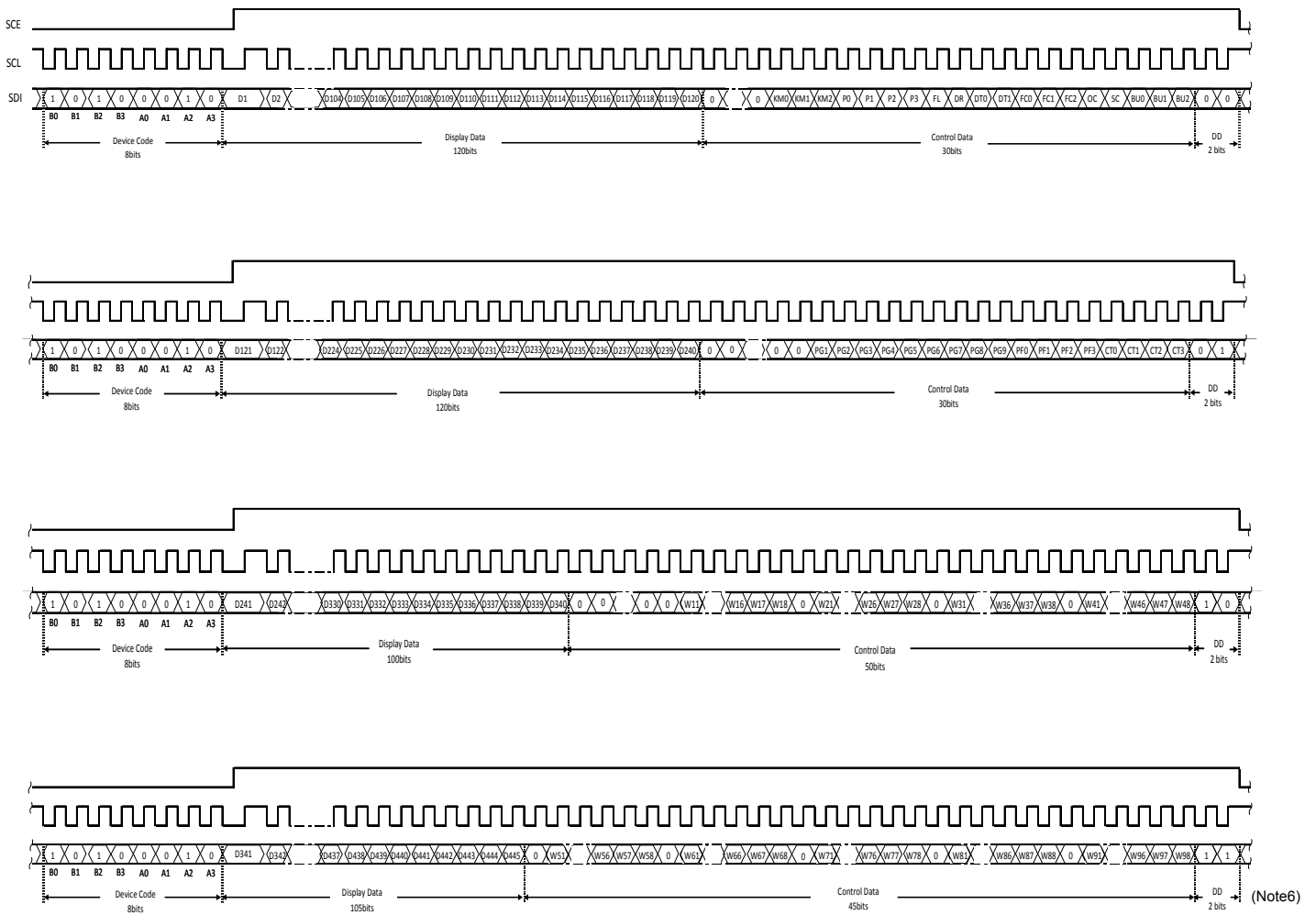


Figure 8. 3-SPI Data Transfer Format

(Note6) DD is direction data.

- Device code....."45H"
- KM0~KM2.....Key Scan output port/Segment output port switching control data
- D1~D445.....Display data
- P0~P3.....Segment / PWM / General Purpose output port switching control data
- FL.....Line Inversion or Frame Inversion switching control data
- DR.....1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1.....1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
- FC0~FC3.....Common/Segment output waveform frame frequency switching control data
- OC.....Internal oscillator operating mode/External clock operating mode switching control data
- SC.....Segment on/off switching control data
- BU0~BU2.....Normal mode/power-saving mode switching control data
- PG1~PG9.....PWM/General Purpose output switching control data
- PF0~PF3.....PWM output waveform frame frequency switching control data
- CT0~CT3.....LCD display contrast switching control data
- W11~W18, W21~W28, W31~W38, W41~W48, W51~W58, W61~W68, W71~W78, W81~W88, W91~W98
.....PWM output duty switching control data

2. 1/4-Duty

(1)When SCL is stopped at the low level

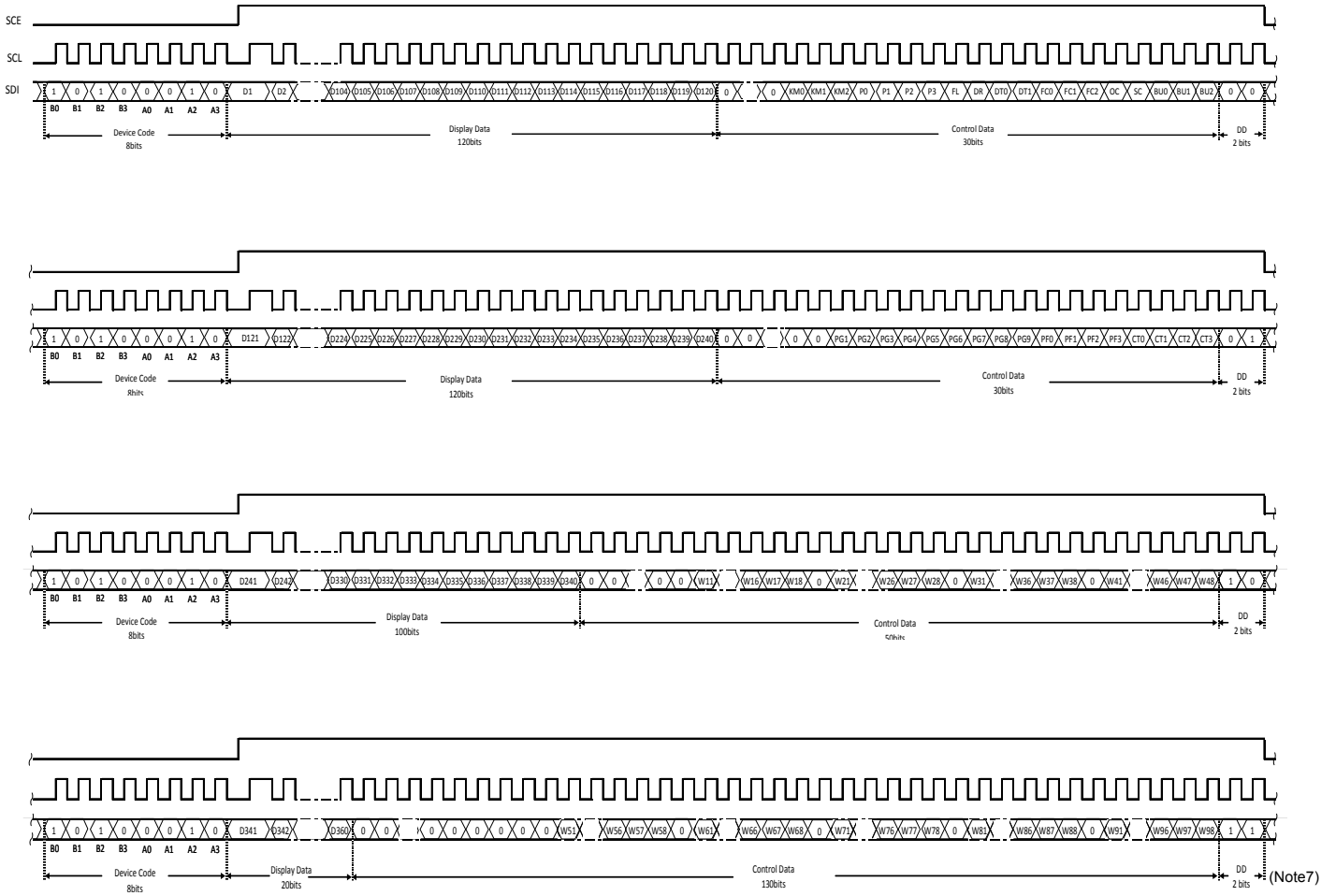


Figure 9. 3-SPI Data Transfer Format

(Note7) DD is direction data.

(2)When SCL is stopped at the high level

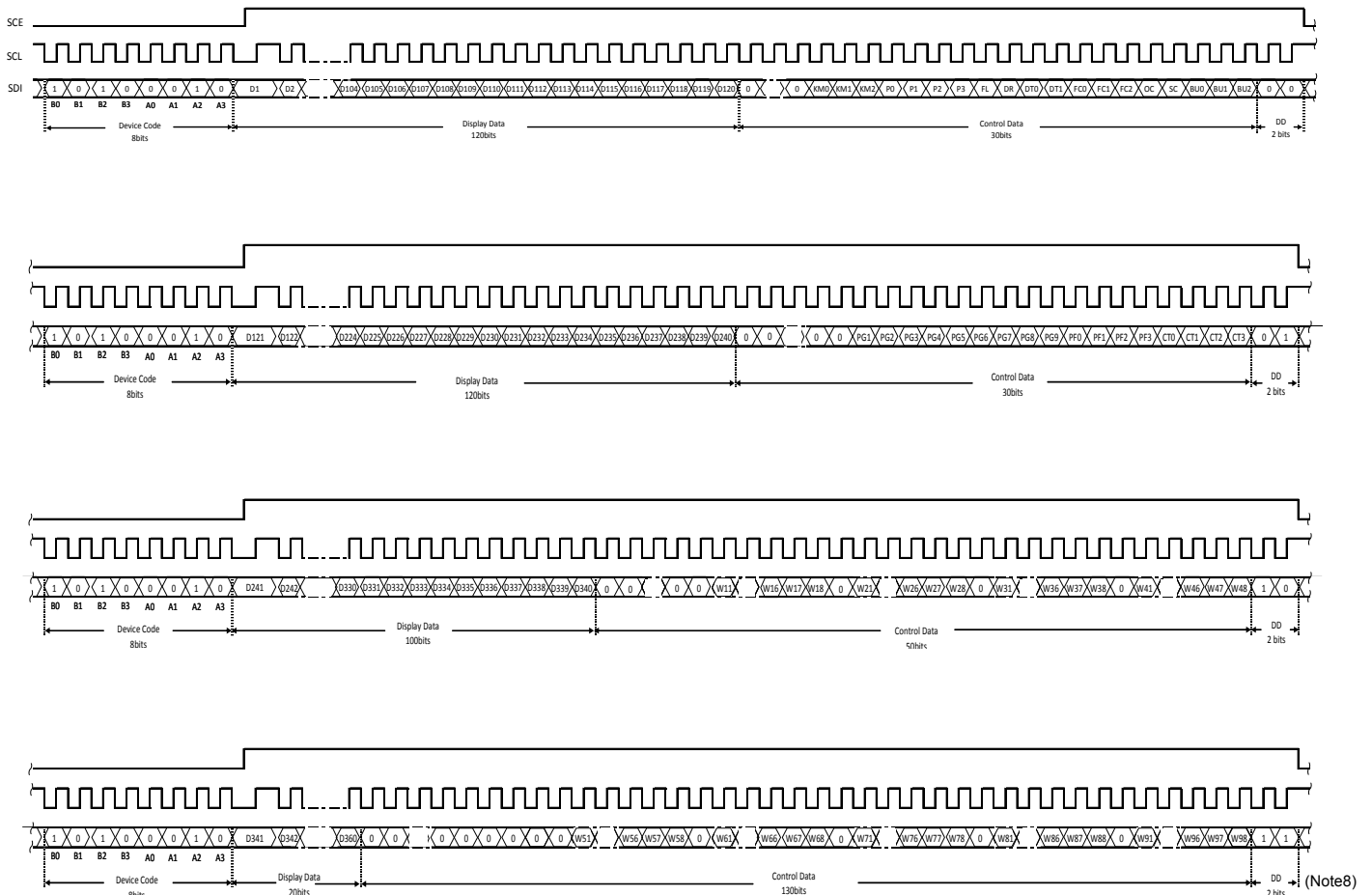


Figure 10. 3-SPI Data Transfer Format

(Note8) DD is direction data.

- Device code....."45H"
- KM0~KM2..... Key Scan output port/Segment output port switching control data
- D1~D445..... Display data
- P0~P3..... Segment / PWM / General Purpose output port switching control data
- FL..... Line Inversion or Frame Inversion switching control data
- DR..... 1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1..... 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
- FC0~FC3..... Common/Segment output waveform frame frequency switching control data
- OC..... Internal oscillator operating mode/External clock operating mode switching control data
- SC..... Segment on/off switching control data
- BU0~BU2..... Normal mode/power-saving mode switching control data
- PG1~PG9..... PWM/General Purpose output switching control data
- PF0~PF3..... PWM output waveform frame frequency switching control data
- CT0~CT3..... LCD display contrast switching control data
- W11~W18, W21~W28, W31~W38, W41~W48, W51~W58, W61~W68, W71~W78, W81~W88, W91~W98
..... PWM output duty switching control data

3. 1/3-Duty

(1) When SCL is stopped at the low level

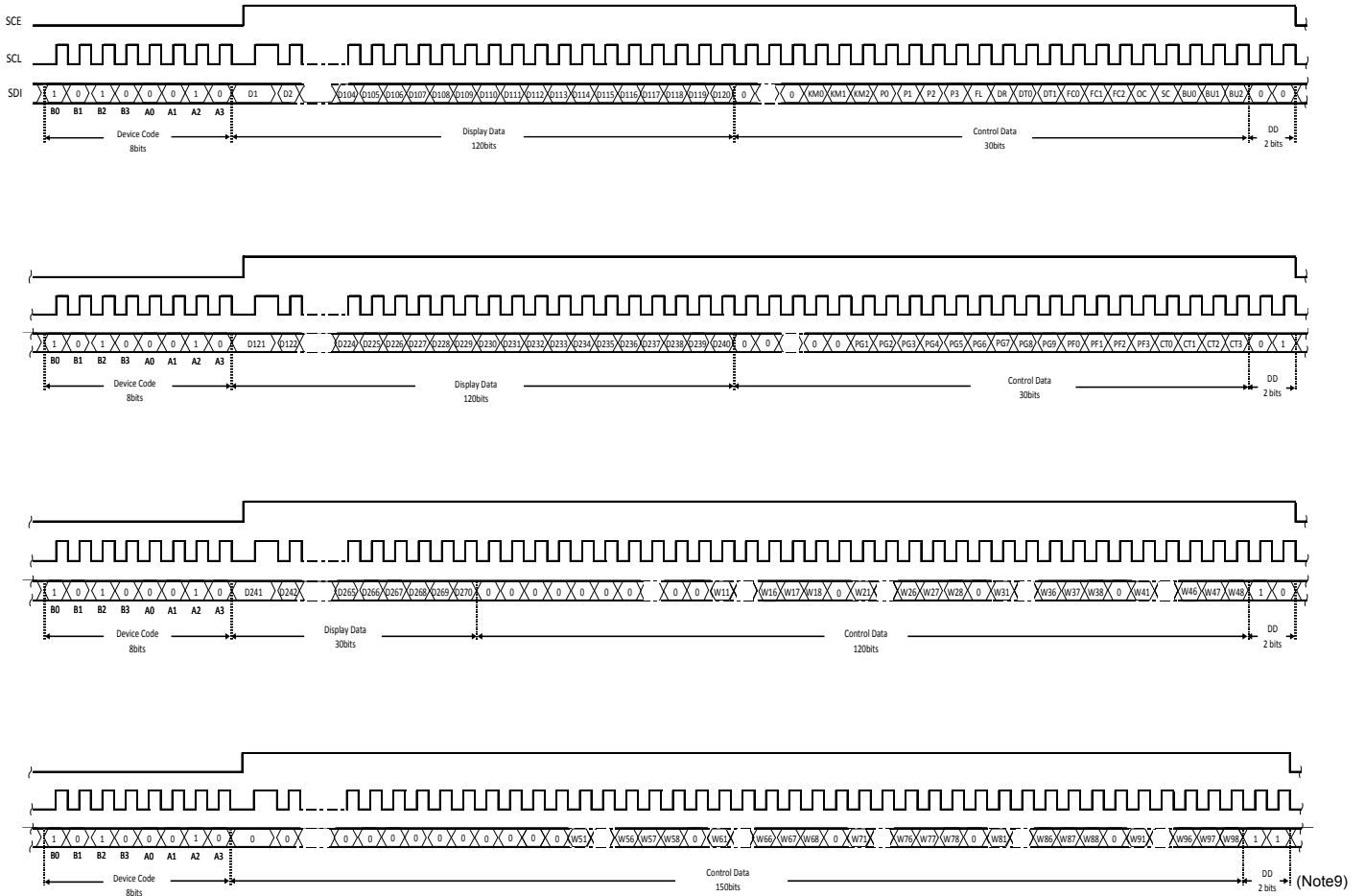


Figure 11. 3-SPI Data Transfer Format

(Note9) DD is direction data.

(2)When SCL is stopped at the high level

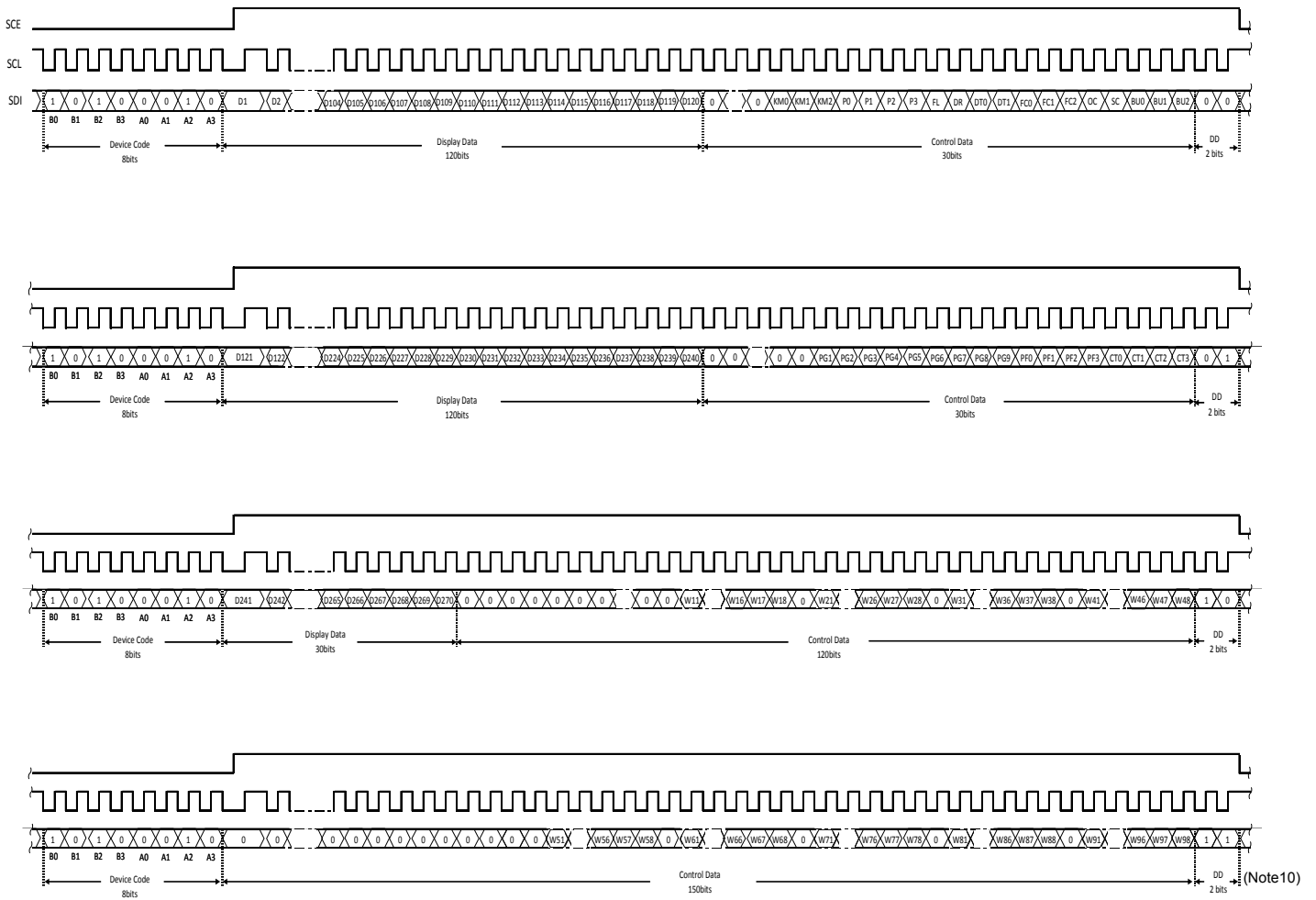


Figure 12. 3-SPI Data Transfer Format

(Note10) DD is direction data.

- Device code....."45H"
- KM0~KM2.....Key Scan output port/Segment output port switching control data
- D1~D445.....Display data
- P0~P3.....Segment / PWM / General Purpose output port switching control data
- FL.....Line Inversion or Frame Inversion switching control data
- DR.....1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1.....1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
- FC0~FC3.....Common/Segment output waveform frame frequency switching control data
- OC.....Internal oscillator operating mode/External clock operating mode switching control data
- SC.....Segment on/off switching control data
- BU0~BU2.....Normal mode/power-saving mode switching control data
- PG1~PG9.....PWM/General Purpose output switching control data
- PF0~PF3.....PWM output waveform frame frequency switching control data
- CT0~CT3.....LCD display contrast switching control data
- W11~W18, W21~W28, W31~W38, W41~W48, W51~W58, W61~W68, W71~W78, W81~W88, W91~W98
.....PWM output duty switching control data

4. 1/1-Duty(Static)

(1)When SCL is stopped at the low level

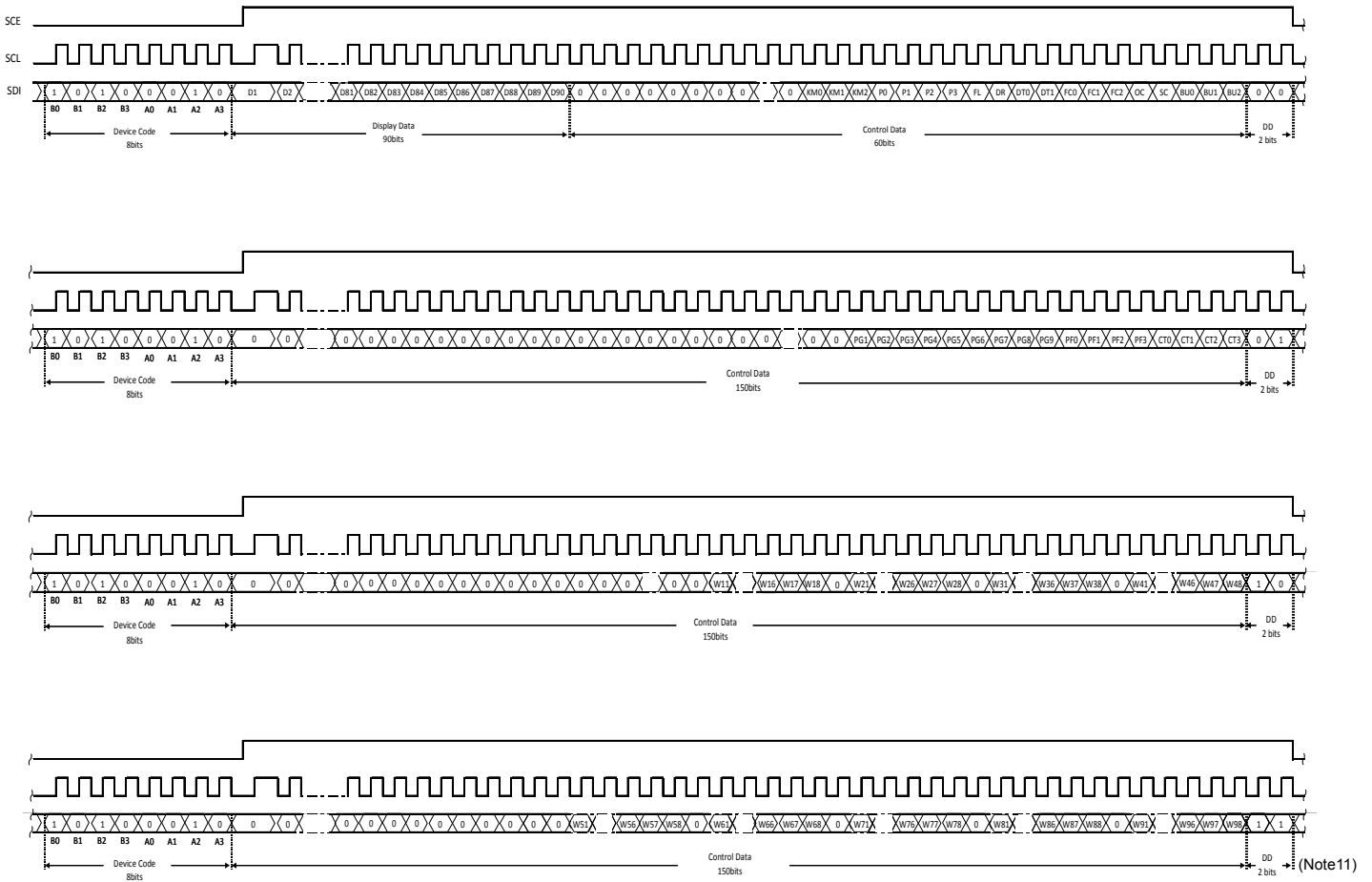


Figure 13. 3-SPI Data Transfer Format

(Note11) DD is direction data.

(2)When SCL is stopped at the high level

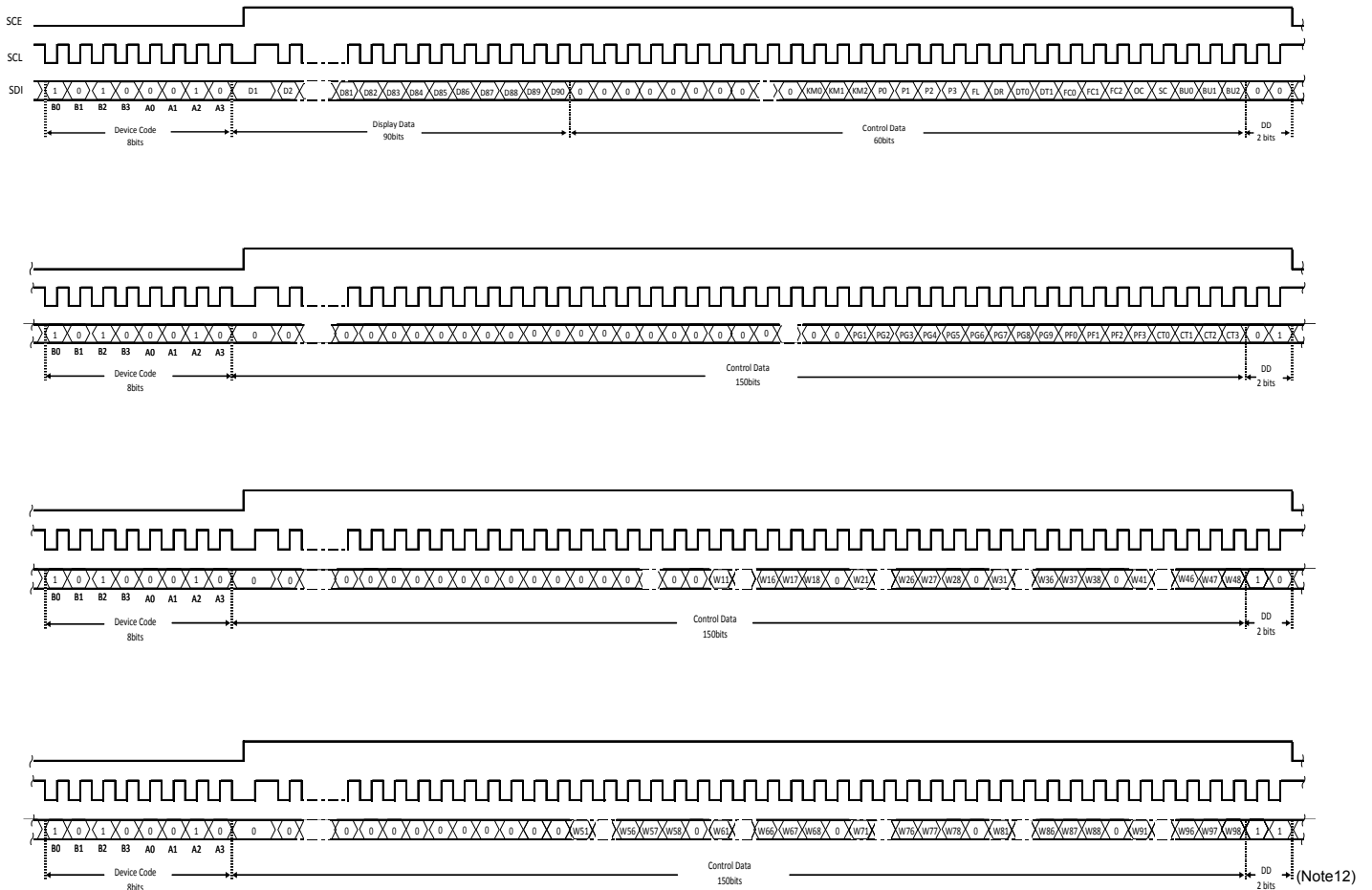


Figure 14. 3-SPI Data Transfer Format

(Note12) DD is direction data.

- Device code....."45H"
- KM0~KM2.....Key Scan output port/Segment output port switching control data
- D1~D445.....Display data
- P0~P3.....Segment / PWM / General Purpose output port switching control data
- FL.....Line Inversion or Frame Inversion switching control data
- DR.....1/3 bias drive or 1/2 bias drive switching control data
- DT0~DT1.....1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data
- FC0~FC3.....Common/Segment output waveform frame frequency switching control data
- OC.....Internal oscillator operating mode/External clock operating mode switching control data
- SC.....Segment on/off switching control data
- BU0~BU2.....Normal mode/power-saving mode switching control data
- PG1~PG9.....PWM/General Purpose output switching control data
- PF0~PF3.....PWM output waveform frame frequency switching control data
- CT0~CT3.....LCD display contrast switching control data
- W11~W18, W21~W28, W31~W38, W41~W48, W51~W58, W61~W68, W71~W78, W81~W88, W91~W98
.....PWM output duty switching control data

Control Data Functions

1. KM0, KM1 and KM2: Key Scan output port/Segment output port switching control data

These control data bits switch the functions of the KS1/S79 to KS6/S84 output pins between key scan output and segment output.

KM0	KM1	KM2	Output Pin State						Maximum Number of Input keys
			KS1/S79	KS2/S80	KS3/S81	KS4/S82	KS5/S83	KS6/S84	
0	0	0	KS1	KS2	KS3	KS4	KS5	KS6	30
0	0	1	S79	KS2	KS3	KS4	KS5	KS6	25
0	1	0	S79	S80	KS3	KS4	KS5	KS6	20
0	1	1	S79	S80	S81	KS4	KS5	KS6	15
1	0	0	S79	S80	S81	S82	KS5	KS6	10
1	0	1	S79	S80	S81	S82	S83	KS6	5
1	1	0	S79	S80	S81	S82	S83	S84	0
1	1	1	S79	S80	S81	S82	S83	S84	0

2. P0, P1, P2 and P3: Segment / PWM / General Purpose output port switching control data

These control bits are used to select the function of the S1/P1/G1 to S9/P9/G9 output pins (Segment Output Pins or PWM Output Pins or General Purpose Output Pins).

P0	P1	P2	P3	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	S7/P7/G7	S8/P8/G8	S9/P9/G9
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
0	0	0	1	P1/G1	S2	S3	S4	S5	S6	S7	S8	S9
0	0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	S7	S8	S9
0	0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	S7	S8	S9
0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	S7	S8	S9
0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	S7	S8	S9
0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S7	S8	S9
0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S8	S9
1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	S9
1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	P9/S9
1	0	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	0	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	0	1	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9

PWM output or General Purpose output is selected by PGx(x=1~9) control data bit.

When the General Purpose Output Port Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data			
	1/5 Duty mode	1/4 Duty mode	1/3 Duty mode	1/1 Duty (static) mode
S1/P1/G1	D1	D1	D1	D1
S2/P2/G2	D6	D5	D4	D2
S3/P3/G3	D11	D9	D7	D3
S4/P4/G4	D16	D13	D10	D4
S5/P5/G5	D21	D17	D13	D4
S6/P6/G6	D26	D21	D16	D5
S7/P7/G7	D31	D25	D19	D7
S8/P8/G8	D36	D29	D22	D8
S9/P9/G9	D41	D33	D25	D9

When the General Purpose Output Port Function is selected, the respective output pin outputs a "HIGH" level when its corresponding display data is set to "1". Likewise, it will output a "LOW" level, if its corresponding display data is set to "0". For example, at 1/4 Duty mode, S4/P4/G4 is used as a General Purpose Output Port, if its corresponding display data D13 is set to "1", then S4/P4/G4 will output "HIGH" level. Likewise, if D13 is set to "0", then S4/P4/G4 will output "LOW" level.

3. FL: Line Inversion or Frame Inversion switching control data

This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion mode
0	Line Inversion
1	Frame Inversion

4. DR: 1/3 bias drive or 1/2 bias drive switching control data

This control data bit selects either 1/3 bias drive or 1/2 bias drive.

DR	Bias drive scheme
0	1/3 bias drive
1	1/2 bias drive

5. DT: 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty(static) drive switching control data

These control data bits select either 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty (static) drive

DT0	DT1	Duty drive scheme
0	0	1/1 duty (static) drive
0	1	1/3 duty drive
1	0	1/4 duty drive
1	1	1/5 duty drive

6. FC0, FC1, FC2 and FC3: Common/Segment output waveform frame frequency switching control data

These control data bits set the frame frequency for common and segment output waveforms.

FC0	FC1	FC2	FC3	Frame Frequency fo(Hz)
0	0	0	0	fosc ^(Note13) / 12288
0	0	0	1	fosc / 10752
0	0	1	0	fosc / 9216
0	0	1	1	fosc / 7680
0	1	0	0	fosc / 6144
0	1	0	1	fosc / 4608
0	1	1	0	fosc / 3840
0	1	1	1	fosc / 3072
1	0	0	0	fosc / 2880
1	0	0	1	fosc / 2688
1	0	1	0	fosc / 2496
1	0	1	1	fosc / 2304
1	1	0	0	fosc / 2112
1	1	0	1	fosc / 1920
1	1	1	0	fosc / 1728
1	1	1	1	fosc / 1536

(Note13) fosc: Internal oscillation frequency (600 [kHz] typ.)

7. OC: Internal oscillator operating mode/External clock operating mode switching control data

OC	Operating mode	In/Out pin(OSC/S90) status
0	Internal oscillator	S90 (segment output)
1	External Clock	OSC (clock input)

8. SC: Segment on/off switching control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to "1", the segments are turned off by outputting segment off waveforms from the segment output pins.

9. BU0, BU1 and BU2: Normal mode/power-saving mode switching control data

These control data bits select either normal mode or power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment outputs Common outputs	Output Pin States During Key Scan Standby						
						KS1	KS2	KS3	KS4	KS5	KS6	
0	0	0	Normal	Operating	Operating	H	H	H	H	H	H	
0	0	1				L	L	L	L	L	L	H
0	1	0	Power-saving	Stopped	Low(VSS)	L	L	L	L	H	H	
0	1	1				L	L	L	H	H	H	H
1	0	0				L	L	H	H	H	H	H
1	0	1				L	H	H	H	H	H	H
1	1	0				H	H	H	H	H	H	H
1	1	1				H	H	H	H	H	H	H

Power-saving mode status: S1/P1/G1 to S9/P9/G9 = active only General Purpose output

S10 to OSC/S90 = low (VSS)

COM1 to COM5 = low (VSS)

Stop the LCD drive bias voltage generation circuit

Stop the Internal oscillation circuit

However, serial data transfer is possible when at Power-saving mode.

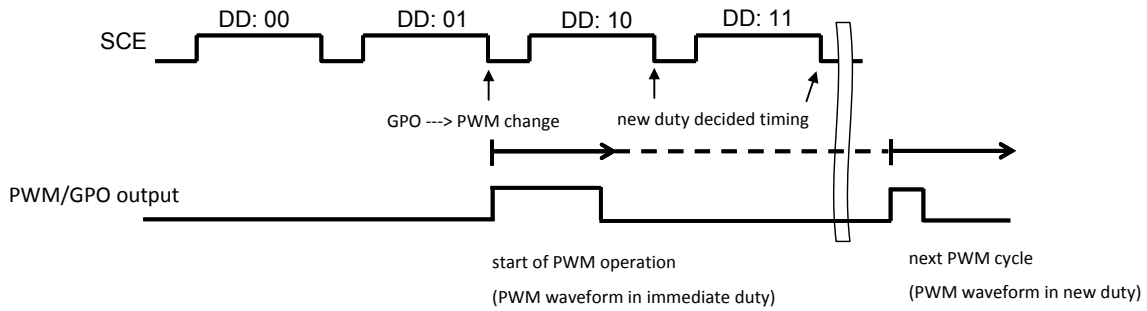
10. PG1, PG2, PG3, PG4, PG5, PG6, PG7, PG8 and PG9: PWM/General Purpose output switching control data
 This control data bit select either PWM output or General Purpose output of Sx/Px/Gx pins. (x=1~9)

PGx(x=1~9)	Mode
0	PWM output
1	General Purpose output

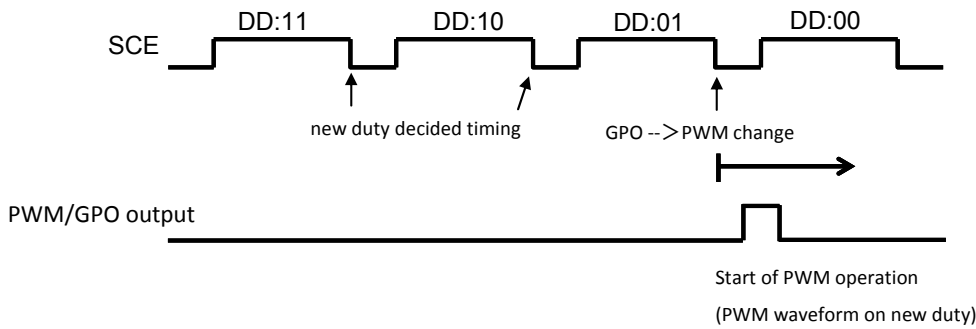
<PWM<->GPO Changing function>

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 01 during GPO -> PWM change.
- Please take care of reflect timing of new duty setting of DD: 10 and DD: 11 is from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



11. PF0, PF1, PF2, and PF3: PWM output waveform frame frequency switching control data
 These control data bits set the frame frequency for PWM output waveforms.

PF0	PF1	PF2	PF3	PWM output Frame Frequency fp(Hz)
0	0	0	0	fosc / 4096
0	0	0	1	fosc / 3840
0	0	1	0	fosc / 3584
0	0	1	1	fosc / 3328
0	1	0	0	fosc / 3072
0	1	0	1	fosc / 2816
0	1	1	0	fosc / 2560
0	1	1	1	fosc / 2304
1	0	0	0	fosc / 2048
1	0	0	1	fosc / 1792
1	0	1	0	fosc / 1536
1	0	1	1	fosc / 1280
1	1	0	0	fosc / 1024
1	1	0	1	fosc / 768
1	1	1	0	fosc / 512
1	1	1	1	fosc / 256

12. CT0, CT1, CT2 and CT3: LCD display contrast switching control data

These control data bits set display contrast

CT0	CT1	CT2	CT3	LCD Drive bias voltage for VLCD Level
0	0	0	0	1.000*VDD
0	0	0	1	0.975*VDD
0	0	1	0	0.950*VDD
0	0	1	1	0.925*VDD
0	1	0	0	0.900*VDD
0	1	0	1	0.875*VDD
0	1	1	0	0.850*VDD
0	1	1	1	0.825*VDD
1	0	0	0	0.800*VDD
1	0	0	1	0.775*VDD
1	0	1	0	0.750*VDD
1	0	1	1	0.725*VDD
1	1	0	0	0.700*VDD
1	1	0	1	0.675*VDD
1	1	1	0	0.650*VDD
1	1	1	1	0.625*VDD

13. W11~W18(Notes14), W21~W28, W31~W38, W41~W48, W51~W58, W61~W68, W71~W78, W81~W88 and W90~W97:
 PWM output waveform duty setting control data.

These control data bits set the high level pulse width (duty) for PWM output waveforms.

$$N = 1 \sim 9, T_p = 1/f_p$$

Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	Wn8	PWM duty
0	0	0	0	0	0	0	0	(0/256) x Tp
0	0	0	0	0	0	0	1	(1/256) x Tp
0	0	0	0	0	0	1	0	(2/256) x Tp
0	0	0	0	0	0	1	1	(3/256) x Tp
0	0	0	0	0	1	0	0	(4/256) x Tp
0	0	0	0	0	1	0	1	(5/256) x Tp
0	0	0	0	0	1	1	0	(6/256) x Tp
0	0	0	0	0	1	1	1	(7/256) x Tp
0	0	0	0	1	0	0	0	(8/256) x Tp
0	0	0	0	1	0	0	1	(9/256) x Tp
0	0	0	0	1	0	1	0	(10/256) x Tp
0	0	0	0	1	0	1	1	(11/256) x Tp
0	0	0	0	1	1	0	0	(12/256) x Tp
0	0	0	0	1	1	0	1	(13/256) x Tp
0	0	0	0	1	1	1	0	(14/256) x Tp
0	0	0	0	1	1	1	1	(15/256) x Tp
0	0	0	1	0	0	0	0	(16/256) x Tp
0	0	0	1	0	0	0	1	(17/256) x Tp
0	0	0	1	0	0	1	0	(18/256) x Tp
0	0	0	1	0	0	1	1	(19/256) x Tp
0	0	0	1	0	1	0	0	(20/256) x Tp
...
1	1	1	0	1	0	1	1	(235/256) x Tp
1	1	1	0	1	1	0	0	(236/256) x Tp
1	1	1	0	1	1	0	1	(237/256) x Tp
1	1	1	0	1	1	1	0	(238/256) x Tp
1	1	1	0	1	1	1	1	(239/256) x Tp
1	1	1	1	0	0	0	0	(240/256) x Tp
1	1	1	1	0	0	0	1	(241/256) x Tp
1	1	1	1	0	0	1	0	(242/256) x Tp
1	1	1	1	0	0	1	1	(243/256) x Tp
1	1	1	1	0	1	0	0	(244/256) x Tp
1	1	1	1	0	1	0	1	(245/256) x Tp
1	1	1	1	0	1	1	0	(246/256) x Tp
1	1	1	1	0	1	1	1	(247/256) x Tp
1	1	1	1	1	0	0	0	(248/256) x Tp
1	1	1	1	1	0	0	1	(249/256) x Tp
1	1	1	1	1	0	1	0	(250/256) x Tp
1	1	1	1	1	0	1	1	(251/256) x Tp
1	1	1	1	1	1	0	0	(252/256) x Tp
1	1	1	1	1	1	0	1	(253/256) x Tp
1	1	1	1	1	1	1	0	(254/256) x Tp
1	1	1	1	1	1	1	1	(255/256) x Tp

(Note14) W11~W18:S1/P1/G1 pwm duty data
 W21~W28:S2/P2/G2 pwm duty data
 W31~W38:S3/P3/G3 pwm duty data
 W41~W48:S4/P4/G4 pwm duty data
 W51~W58:S5/P5/G5 pwm duty data
 W61~W68:S6/P6/G6 pwm duty data
 W71~W78:S7/P7/G7 pwm duty data
 W81~W88:S8/P8/G8 pwm duty data
 W91~W98:S9/P9/G9 pwm duty data

Display Data and Output Pin Correspondence

1. 1/5 duty

Output pin ^(Note15)	COM1	COM2	COM3	COM4	COM5
S1/P1/G1	D1	D2	D3	D4	D5
S2/P2/G2	D6	D7	D8	D9	D10
S3/P3/G3	D11	D12	D13	D14	D15
S4/P4/G4	D16	D17	D18	D19	D20
S5/P5/G5	D21	D22	D23	D24	D25
S6/P6/G6	D26	D27	D28	D29	D30
S7/P7/G7	D31	D32	D33	D34	D35
S8/P8/G8	D36	D37	D38	D39	D40
S9/P9/G9	D41	D42	D43	D44	D45
S10	D46	D47	D48	D49	D50
S11	D51	D52	D53	D54	D55
S12	D56	D57	D58	D59	D60
S13	D61	D62	D63	D64	D65
S14	D66	D67	D68	D69	D70
S15	D71	D72	D73	D74	D75
S16	D76	D77	D78	D79	D80
S17	D81	D82	D83	D84	D85
S18	D86	D87	D88	D89	D90
S19	D91	D92	D93	D94	D95
S20	D96	D97	D98	D99	D100
S21	D101	D102	D103	D104	D105
S22	D106	D107	D108	D109	D110
S23	D111	D112	D113	D114	D115
S24	D116	D117	D118	D119	D120
S25	D121	D122	D123	D124	D125
S26	D126	D127	D128	D129	D130
S27	D131	D132	D133	D134	D135
S28	D136	D137	D138	D139	D140
S29	D141	D142	D143	D144	D145
S30	D146	D147	D148	D149	D150
S31	D151	D152	D153	D154	D155
S32	D156	D157	D158	D159	D160
S33	D161	D162	D163	D164	D165
S34	D166	D167	D168	D169	D170
S35	D171	D172	D173	D174	D175
S36	D176	D177	D178	D179	D180
S37	D181	D182	D183	D184	D185
S38	D186	D187	D188	D189	D190
S39	D191	D192	D193	D194	D195
S40	D196	D197	D198	D199	D200
S41	D201	D202	D203	D204	D205
S42	D206	D207	D208	D209	D210
S43	D211	D212	D213	D214	D215
S44	D216	D217	D218	D219	D220
S45	D221	D222	D223	D224	D225
S46	D226	D227	D228	D229	D230
S47	D231	D232	D233	D234	D235
S48	D236	D237	D238	D239	D240
S49	D241	D242	D243	D244	D245
S50	D246	D247	D248	D249	D250
S51	D251	D252	D253	D254	D255
S52	D256	D257	D258	D259	D260
S53	D261	D262	D263	D264	D265
S54	D266	D267	D268	D269	D270
S55	D271	D272	D273	D274	D275
S56	D276	D277	D278	D279	D280
S57	D281	D282	D283	D284	D285
S58	D286	D287	D288	D289	D290
S59	D291	D292	D293	D294	D295
S60	D296	D297	D298	D299	D300
S61	D301	D302	D303	D304	D305
S62	D306	D307	D308	D309	D310
S63	D311	D312	D313	D314	D315

Output pin ^(Note15)	COM1	COM2	COM3	COM4	COM5
S64	D316	D317	D318	D319	D320
S65	D321	D322	D323	D324	D325
S66	D326	D327	D328	D329	D330
S67	D331	D332	D333	D334	D335
S68	D336	D337	D338	D339	D340
S69	D341	D342	D343	D344	D345
S70	D346	D347	D348	D349	D350
S71	D351	D352	D353	D354	D355
S72	D356	D357	D358	D359	D360
S73	D361	D362	D363	D364	D365
S74	D366	D367	D368	D369	D370
S75	D371	D372	D373	D374	D375
S76	D376	D377	D378	D379	D380
S77	D381	D382	D383	D384	D385
KS1/S79	D386	D387	D388	D389	D390
KS2/S80	D391	D392	D393	D394	D395
KS3/S81	D396	D397	D398	D399	D400
KS4/S82	D401	D402	D403	D404	D405
KS5/S83	D406	D407	D408	D409	D410
KS6/S84	D411	D412	D413	D414	D415
KI1/S85	D416	D417	D418	D419	D420
KI2/S86	D421	D422	D423	D424	D425
KI3/S87	D426	D427	D428	D429	D430
KI4/S88	D431	D432	D433	D434	D435
KI5/S89	D436	D437	D438	D439	D440
OSC/S90	D441	D442	D443	D444	D445

(Note15) The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89, OSC/S90. Also, COM5/S78 pin is used as Common output.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data					State of S21 Output Pin
D101	D102	D103	D104	D105	
0	0	0	0	0	LCD Segments corresponding to COM1 to COM5 are OFF.
0	0	0	0	1	LCD Segment corresponding to COM5 is ON.
0	0	0	1	0	LCD Segment corresponding to COM4 is ON.
0	0	0	1	1	LCD Segments corresponding to COM4 and COM5 are ON.
0	0	1	0	0	LCD Segment corresponding to COM3 is ON.
0	0	1	0	1	LCD Segments corresponding to COM3 and COM5 are ON.
0	0	1	1	0	LCD Segments corresponding to COM3 and COM4 are ON.
0	0	1	1	1	LCD Segments corresponding to COM3, COM4 and COM5 are ON.
0	1	0	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	0	1	LCD Segments corresponding to COM2 and COM5 are ON.
0	1	0	1	0	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	0	1	1	LCD Segments corresponding to COM2, COM4 and COM5 are ON.
0	1	1	0	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	0	1	LCD Segments corresponding to COM2, COM3, and COM5 are ON.
0	1	1	1	0	LCD Segments corresponding to COM2, COM3, and COM4 are ON.
0	1	1	1	1	LCD Segments corresponding to COM2, COM3, COM4 and COM5 are ON.
1	0	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	0	1	LCD Segments corresponding to COM1 and COM5 are ON.
1	0	0	1	0	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	0	1	1	LCD Segments corresponding to COM1, COM4 and COM5 are ON.
1	0	1	0	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	0	1	LCD Segments corresponding to COM1, COM3 and COM5 are ON.
1	0	1	1	0	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	0	1	1	1	LCD Segments corresponding to COM1, COM3, COM4 and COM5 are ON.
1	1	0	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	0	1	LCD Segments corresponding to COM1, COM2 and COM5 are ON.
1	1	0	1	0	LCD Segments corresponding to COM1, COM2 and COM4 are ON.
1	1	0	1	1	LCD Segments corresponding to COM1, COM2, COM4 and COM5 are ON.
1	1	1	0	0	LCD Segments corresponding to COM1, COM2 and COM3 are ON.
1	1	1	0	1	LCD Segments corresponding to COM1, COM2, COM3 and COM5 are ON.
1	1	1	1	0	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.
1	1	1	1	1	LCD Segments corresponding to COM1, COM2, COM3, COM4 and COM5 are ON.

2.1/4 duty

Output pin ^(Note16)	COM1	COM2	COM3	COM4
S1/P1/G1	D1	D2	D3	D4
S2/P2/G2	D5	D6	D7	D8
S3/P3/G3	D9	D10	D11	D12
S4/P4/G4	D13	D14	D15	D16
S5/P5/G5	D17	D18	D19	D20
S6/P6/G6	D21	D22	D23	D24
S7/P7/G7	D25	D26	D27	D28
S8/P8/G8	D29	D30	D31	D32
S9/P9/G9	D33	D34	D35	D36
S10	D37	D38	D39	D40
S11	D41	D42	D43	D44
S12	D45	D46	D47	D48
S13	D49	D50	D51	D52
S14	D53	D54	D55	D56
S15	D57	D58	D59	D60
S16	D61	D62	D63	D64
S17	D65	D66	D67	D68
S18	D69	D70	D71	D72
S19	D73	D74	D75	D76
S20	D77	D78	D79	D80
S21	D81	D82	D83	D84
S22	D85	D86	D87	D88
S23	D89	D90	D91	D92
S24	D93	D94	D95	D96
S25	D97	D98	D99	D100
S26	D101	D102	D103	D104
S27	D105	D106	D107	D108
S28	D109	D110	D111	D112
S29	D113	D114	D115	D116
S30	D117	D118	D119	D120
S31	D121	D122	D123	D124
S32	D125	D126	D127	D128
S33	D129	D130	D131	D132
S34	D133	D134	D135	D136
S35	D137	D138	D139	D140
S36	D141	D142	D143	D144
S37	D145	D146	D147	D148
S38	D149	D150	D151	D152
S39	D153	D154	D155	D156
S40	D157	D158	D159	D160
S41	D161	D162	D163	D164
S42	D165	D166	D167	D168
S43	D169	D170	D171	D172
S44	D173	D174	D175	D176
S45	D177	D178	D179	D180
S46	D181	D182	D183	D184
S47	D185	D186	D187	D188
S48	D189	D190	D191	D192
S49	D193	D194	D195	D196
S50	D197	D198	D199	D200
S51	D201	D202	D203	D204
S52	D205	D206	D207	D208
S53	D209	D210	D211	D212
S54	D213	D214	D215	D216
S55	D217	D218	D219	D220
S56	D221	D222	D223	D224
S57	D225	D226	D227	D228
S58	D229	D230	D231	D232
S59	D233	D234	D235	D236
S60	D237	D238	D239	D240
S61	D241	D242	D243	D244
S62	D245	D246	D247	D248
S63	D249	D250	D251	D252

Output pin ^(Note16)	COM1	COM2	COM3	COM4
S64	D253	D254	D255	D256
S65	D257	D258	D259	D260
S66	D261	D262	D263	D264
S67	D265	D266	D267	D268
S68	D269	D270	D271	D272
S69	D273	D274	D275	D276
S70	D277	D278	D279	D280
S71	D281	D282	D283	D284
S72	D285	D286	D287	D288
S73	D289	D290	D291	D292
S74	D293	D294	D295	D296
S75	D297	D298	D299	D300
S76	D301	D302	D303	D304
S77	D305	D306	D307	D308
COM5/S78	D309	D310	D311	D312
KS1/S79	D313	D314	D315	D316
KS2/S80	D317	D318	D319	D320
KS3/S81	D321	D322	D323	D324
KS4/S82	D325	D326	D327	D328
KS5/S83	D329	D330	D331	D332
KS6/S84	D333	D334	D335	D336
KI1/S85	D337	D338	D339	D340
KI2/S86	D341	D342	D343	D344
KI3/S87	D345	D346	D347	D348
KI4/S88	D349	D350	D351	D352
KI5/S89	D353	D354	D355	D356
OSC/S90	D357	D358	D359	D360

(Note16) The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, COM5/S78, KS1/S79 to KS6/S84, KI1/S85 to KI5/S89, OSC/S90.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data				State of S21 Output Pin
D81	D82	D83	D84	
0	0	0	0	LCD Segments corresponding to COM1 to COM4 are OFF.
0	0	0	1	LCD Segment corresponding to COM4 is ON.
0	0	1	0	LCD Segment corresponding to COM3 is ON.
0	0	1	1	LCD Segments corresponding to COM3 and COM4 are ON.
0	1	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	1	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	1	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	1	LCD Segments corresponding to COM2, COM3 and COM4 are ON.
1	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	1	LCD Segments corresponding to COM1 and COM4 are ON.
1	0	1	0	LCD Segments corresponding to COM1 and COM3 are ON.
1	0	1	1	LCD Segments corresponding to COM1, COM3 and COM4 are ON.
1	1	0	0	LCD Segments corresponding to COM1 and COM2 are ON.
1	1	0	1	LCD Segments corresponding to COM1, COM2, and COM4 are ON.
1	1	1	0	LCD Segments corresponding to COM1, COM2, and COM3 are ON.
1	1	1	1	LCD Segments corresponding to COM1, COM2, COM3 and COM4 are ON.

3. 1/3 duty

Output pin ^(Note17)	COM1	COM2	COM3
S1/P1/G1	D1	D2	D3
S2/P2/G2	D4	D5	D6
S3/P3/G3	D7	D8	D9
S4/P4/G4	D10	D11	D12
S5/P5/G5	D13	D14	D15
S6/P6/G6	D16	D17	D18
S7/P7/G7	D19	D20	D21
S8/P8/G8	D22	D23	D24
S9/P9/G9	D25	D26	D27
S10	D28	D29	D30
S11	D31	D32	D33
S12	D34	D35	D36
S13	D37	D38	D39
S14	D40	D41	D42
S15	D43	D44	D45
S16	D46	D47	D48
S17	D49	D50	D51
S18	D52	D53	D54
S19	D55	D56	D57
S20	D58	D59	D60
S21	D61	D62	D63
S22	D64	D65	D66
S23	D67	D68	D69
S24	D70	D71	D72
S25	D73	D74	D75
S26	D76	D77	D78
S27	D79	D80	D81
S28	D82	D83	D84
S29	D85	D85	D87
S30	D88	D89	D90
S31	D91	D92	D93
S32	D94	D95	D96
S33	D97	D98	D99
S34	D100	D101	D102
S35	D103	D104	D105
S36	D106	D107	D108
S37	D109	D110	D111
S38	D112	D113	D114
S39	D115	D116	D117
S40	D118	D119	D120
S41	D121	D122	D123
S42	D124	D125	D126
S43	D127	D128	D129
S44	D130	D131	D132
S45	D133	D134	D135
S46	D136	D137	D138
S47	D139	D140	D141
S48	D142	D143	D144
S49	D145	D146	D147
S50	D148	D149	D150
S51	D151	D152	D153
S52	D154	D155	D156
S53	D157	D158	D159
S54	D160	D161	D162
S55	D163	D164	D165
S56	D166	D167	D168
S57	D169	D170	D171
S58	D172	D173	D174
S59	D175	D176	D177
S60	D178	D179	D180
S61	D181	D182	D183
S62	D184	D185	D186
S63	D187	D188	D189