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## LCD Segment Drivers

# Multi-function Segment Drivers

BU97540KV-M

MAX335 Segment(67segx5COM)

**General Description**

The BU97540KV-M is 1/5, 1/4, 1/3, or 1/1 duty general-purpose LCD driver that can be used for frequency display in electronic tuners under the control of a microcontroller. The BU97540KV-M can drive up to 335 LCD Segments directly. The BU97540KV-M can also control up to 9 general-purpose output ports.

These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring

**Features**

- AEC-Q100 Qualified (Note1)
- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- Supports 1 chip(Master) mode and 2 chip(Master + Slave) mode
- Either 1/5, 1/4, 1/3 or 1/1 duty (static) can be selected with the serial control data.
  - 1 chip mode(only Master):
    - 1/5 duty drive: Up to 335 segments can be driven
    - 1/4 duty drive: Up to 272 segments can be driven
    - 1/3 duty drive: Up to 204 segments can be driven
    - 1/1 duty drive: Up to 68 segments can be driven
  - 2 chip mode(Master + Slave):
    - 1/5 duty drive: Up to 680 segments can be driven
    - 1/4 duty drive: Up to 548 segments can be driven
    - 1/3 duty drive: Up to 411 segments can be driven
    - 1/1 duty drive: Up to 137 segments can be driven
- Serial data control of frame frequency for common and segment output waveforms.
- Serial data control of switching between the segment output port , PWM output port and general-purpose output port functions.(Max 9 ports)
- Built-in OSC circuit
- Integrated Power-on Reset circuit
- No external component
- Low power consumption design
- Supports Line and Frame Inversion

(Note1) Grade 3

**Applications**

- Car audio, Home electrical appliance, Meter equipment etc.

**Key Specifications**

- |                                |                               |
|--------------------------------|-------------------------------|
| ■ Supply Voltage Range:        | +2.7V to +6.0V                |
| ■ Operating Temperature Range: | -40°C to +85°C                |
| ■ Max Segments:                | 335 Segments                  |
| ■ Display Duty:                | 1/1, 1/3, 1/4, 1/5 Selectable |
| ■ Bias:                        | 1/1, 1/2, 1/3, 1/4 Selectable |
| ■ Interface:                   | 3Wire Serial Interface        |

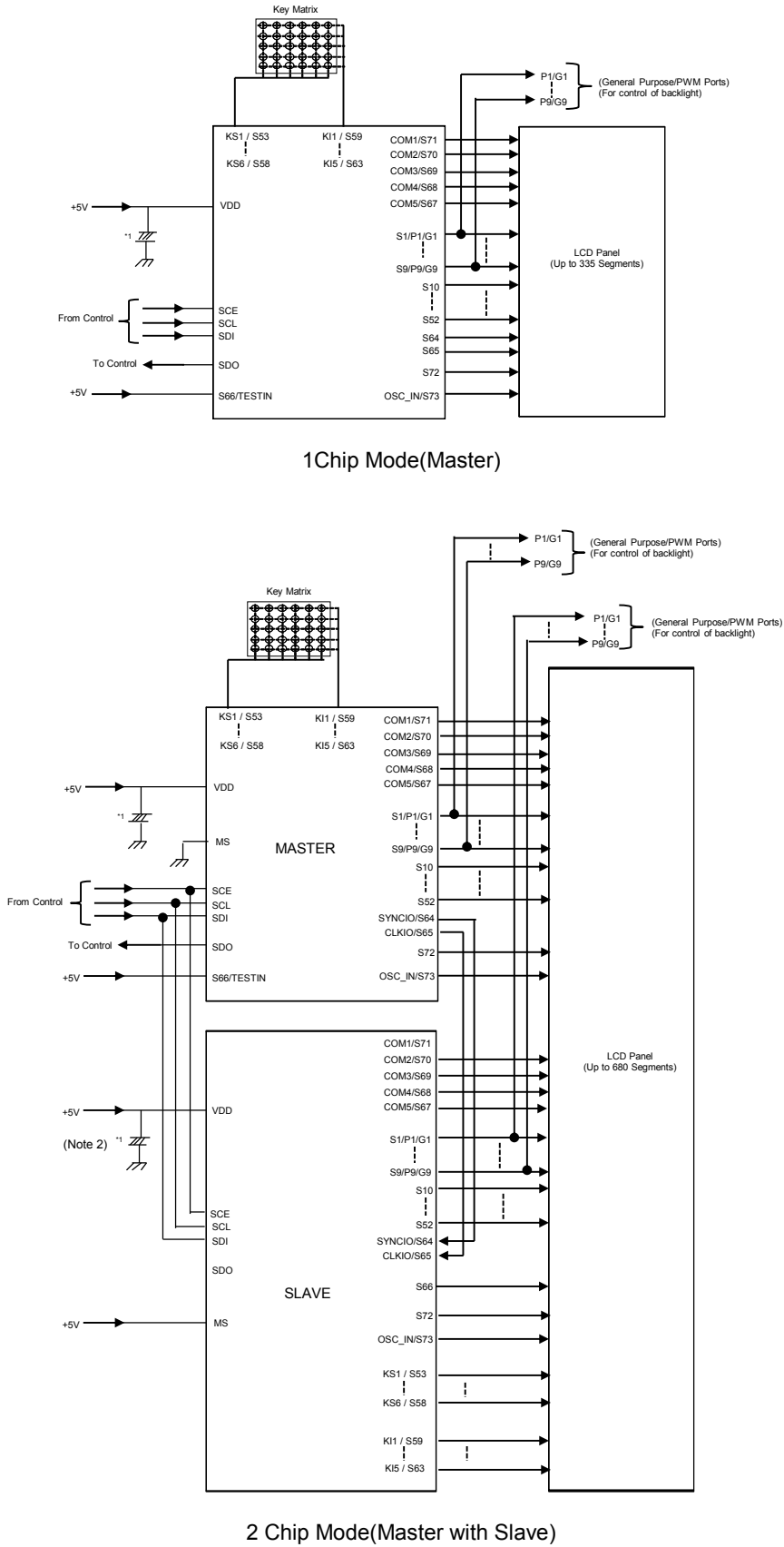
**Packages**

VQFP80

W(Typ) × D(Typ) × H(Max)



Typical Application Circuit



(Note2) Insert capacitors between VDD and VSS C≥0.1uF

Figure 1. Typical Application Circuit

Block Diagram

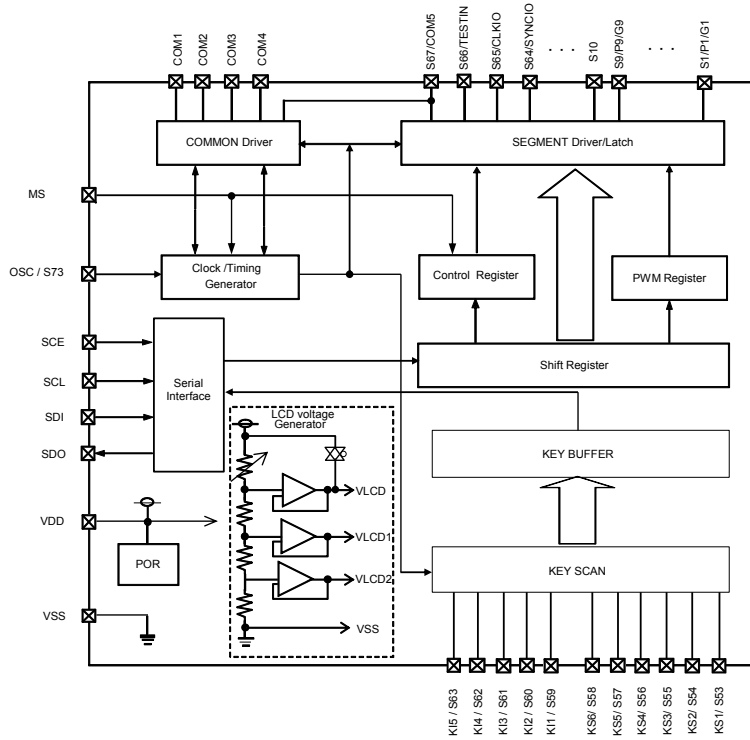


Figure 2. Block Diagram

Pin Arrangement

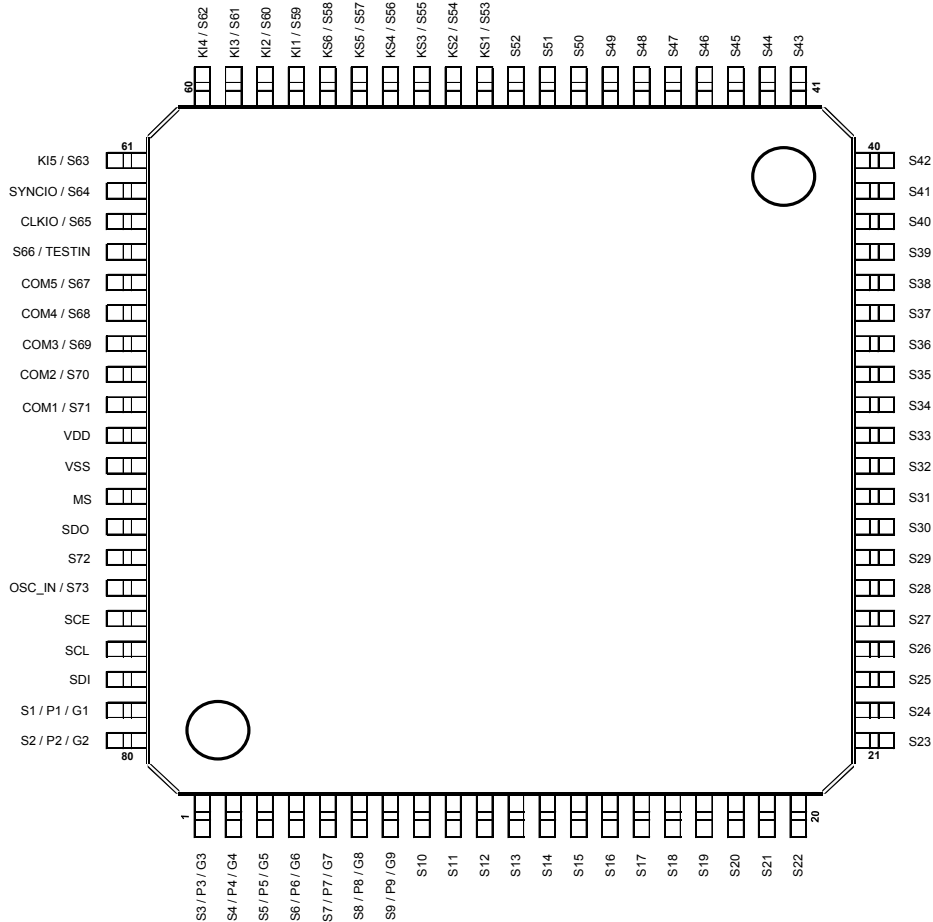


Figure 3. Pin Configuration (TOP VIEW)

**Absolute Maximum Ratings (Ta = 25°C, VSS = 0V)**

Parameter	Symbol	Conditions	Rating	Unit
Maximum Supply Voltage	VDD max	VDD	-0.3 to +7.0	V
Input Voltage	VIN1	SCE, SCL, SDI	-0.3 to +7.0	V
	VIN2	KI1 to KI5	-0.3 to +7.0	V
Allowable Loss	Pd		1.2 <sup>(Note3)</sup>	W
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-55 to +125	°C

(Note3) When use more than Ta=25°C, subtract 12mW per degree. (Using ROHM standard board)

(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

**Recommend Operating Conditions (Ta = -40°C to +85°C, VSS = 0V)**

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Supply Voltage	VDD		2.7	5.0	6.0	V

**Electrical Characteristics for the Allowable Operating Ranges**

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	VH1	SCE, SCL, SDI		-	0.03 VDD	-	V
	VH2	KI1 to KI5		-	0.1 VDD	-	V
Power-on Detection Voltage	VDET	V <sub>DD</sub>		1.3	1.8	2.2	V
"H" Level Input Voltage	VIH1	SCE,SCL,SDI, SYNCIO,CLKIO	4.5V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	VIH2	SCE, SCL, SDI, SYNCIO,CLKIO	2.7V ≤ VDD < 4.5V	0.8VDD	-	VDD	
	VIH3	KI1 to KI5		0.7VDD	-	VDD	
"L" Level Input Voltage	VIL1	SCE, SCL, SDI KI1 to KI5 SYNCIO,CLKIO		0	-	0.2VDD	V
Input Floating Voltage	VIF	KI1 to KI5		-	-	0.05VDD	V
Pull-down Resistance	RPD	KI1 to KI5	VDD=5.0V	50	100	250	KΩ
Output Off Leakage Current	IOFFH	SDO	V <sub>O</sub> =6.0V	-	-	6.0	μA
"H" Level Input Current	IIH1	SCE, SCL, SDI SYNCIO,CLKIO	V <sub>I</sub> = 5.5V	-	-	5.0	μA
"L" Level Input Current	IIL1	SCE, SCL, SDI SYNCIO,CLKIO	V <sub>I</sub> = 0V	-5.0	-	-	μA
"H" Level Output Voltage	VOH1	S1 to S73	I <sub>O</sub> = -20μA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	VOH2	COM1 to COM5	I <sub>O</sub> = -100μA, VDD=1.00*VDD	VDD-0.9	-	-	
	VOH3	P1/G1 to P9/G9	I <sub>O</sub> = -1mA	VDD-0.9	-	-	
	VOH4	KS1 to KS6	I <sub>O</sub> = -500μA	VDD-1.0	VDD-0.5	VDD-0.2	
	VOH5	SYNCIO,CLKIO	I <sub>O</sub> = -1mA	VDD-0.9	-	-	
"L" Level Output Voltage	VOL1	S1 to S70	I <sub>O</sub> = 20μA	-	-	0.9	V
	VOL2	COM1 to COM5	I <sub>O</sub> = 100μA	-	-	0.9	
	VOL3	P1/G1 to P9/G9	I <sub>O</sub> = 1mA	-	-	0.9	
	VOL4	KS1 to KS6	I <sub>O</sub> = 25μA	0.2	0.5	1.5	
	VOL5	SDO	I <sub>O</sub> = 1mA	-	0.1	0.5	
	VOL6	SYNCIO,CLKIO	I <sub>O</sub> = 1mA	-	-	0.9	
Middle Level Output Voltage	VMID1	S1 to S73	1/2 bias I <sub>O</sub> = ±20μA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	V
	VMID2	COM1 to COM5	1/2 bias I <sub>O</sub> = ±100μA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	
	VMID3	S1 to S73	1/3 bias I <sub>O</sub> = ±20μA VLCD=1.00*VDD	2/3 VDD -0.9	-	2/3 VDD +0.9	
	VMID4	S1 to S73	1/3 bias I <sub>O</sub> = ±20μA VLCD=1.00*VDD	1/3 VDD -0.9	-	1/3 VDD +0.9	
	VMID5	COM1 to COM5	1/3 bias I <sub>O</sub> = ±100μA VLCD=1.00*VDD	2/3 VDD -0.9	-	2/3 VDD +0.9	
	VMID6	COM1 to COM5	1/3 bias I <sub>O</sub> = ±100μA VLCD=1.00*VDD	1/3 VDD -0.9	-	1/3 VDD +0.9	

Electrical Characteristics – continued

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Current Consumption	IDD1	VDD	Power-saving mode	-	-	15	μA
	IDD2	VDD	1chip mode VDD = 5.0V Output open, 1/2 bias Frame frequency=80Hz VLCD=1.00*VDD	-	105	220	μA
	IDD3	VDD	1chip mode VDD = 5.0V Output open, 1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	130	270	μA
	IDD4	VDD	2chip mode : Master VDD = 5.0V Output open, 1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	195	370	μA
	IDD5	VDD	2chip mode : Slave VDD = 5.0V Output open, 1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	105	220	μA

Oscillation Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Oscillator Frequency 1	fosc1	-	VDD = 2.7V to 6.0V	300	-	720	kHz
Oscillator Frequency 2	fosc2	-	VDD = 5.0V	540	600	660	kHz
Oscillator Frequency 3	fosc3	-	VDD = 6.0V	562	625	688	kHz
External Clock Frequency <sup>(Note4)</sup>	fosc4	OSC_IN/S73	External clock mode (OC=1)	30	-	1000	kHz
External Clock Duty	tdty	OSC_IN/S73	External clock mode (OC=1)	30	50	70	%

(Note4) Frame frequency is decided external frequency and dividing ratio of FC0 to FC3 setting.

【Reference Data】

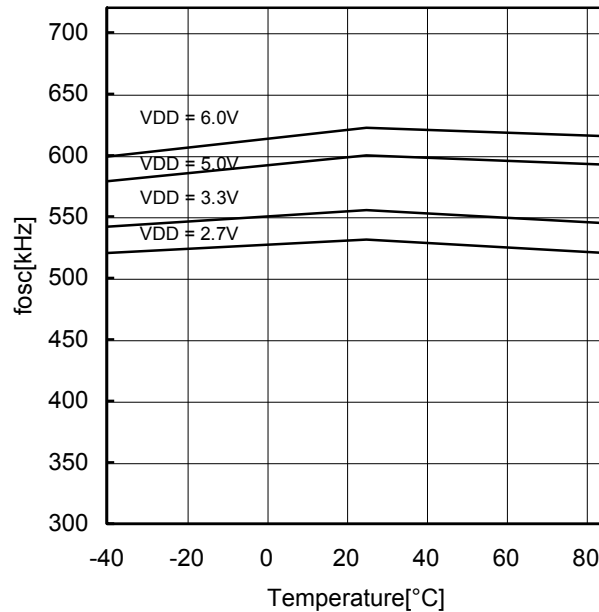
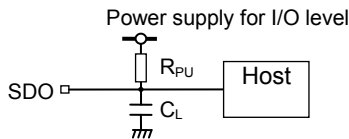


Figure 4. Typical Temperature Characteristics

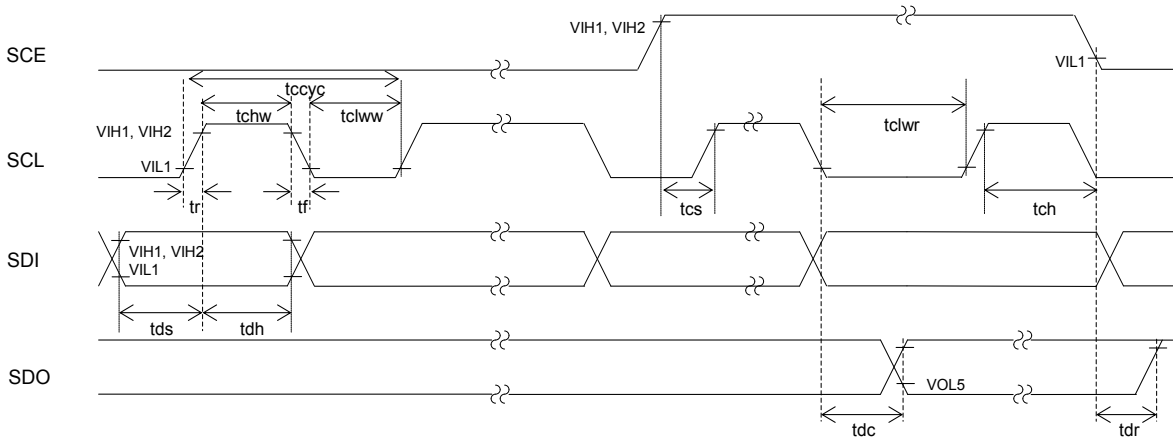
MPU Interface Characteristics (Ta=-40 to +85°C, VDD = 2.7V to 6.0V, VSS=0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	tds	SCL, SDI		120	-	-	ns
Data Hold Time	tdh	SCL, SDI		120	-	-	ns
SCE Wait Time	tcp	SCE, SCL		120	-	-	ns
SCE Setup Time	tcs	SCE, SCL		120	-	-	ns
SCE Hold Time	tch	SCE, SCL		120	-	-	ns
Clock Cycle Time	tccyc	SCL		320	-	-	ns
High-level Clock Pulse Width	tchw	SCL		120	-	-	ns
Low-level Clock Pulse Width (Write)	tclww	SCL		120	-	-	ns
Low-level Clock Pulse Width (Read)	tclwr	SCL	RPU=4.7kΩ CL=10pf <sup>(Note5)</sup>	1.6	-	-	us
Rise Time	tr	SCE, SCL, SDI		-	160	-	ns
Fall Time	tf	SCE, SCL, SDI		-	160	-	ns
SDO Output Delay Time	tdc	SDO	RPU=4.7kΩ CL=10pf <sup>(Note5)</sup>	-	-	1.5	μs
SDO Rise Time	Tdr	SDO	RPU=4.7kΩ CL=10pf <sup>(Note5)</sup>	-	-	1.5	μs

(Note5) Since SDO is an open-drain output, "tdc" and "tdr" depend on the resistance of the pull-up resistor RPU and the load capacitance SCL.  
 RPU: 1kΩ≤RPU≤10kΩ is recommended.  
 CL: A parasitic capacitance to VSS in an application circuit. Any component is not necessary to be attached.



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

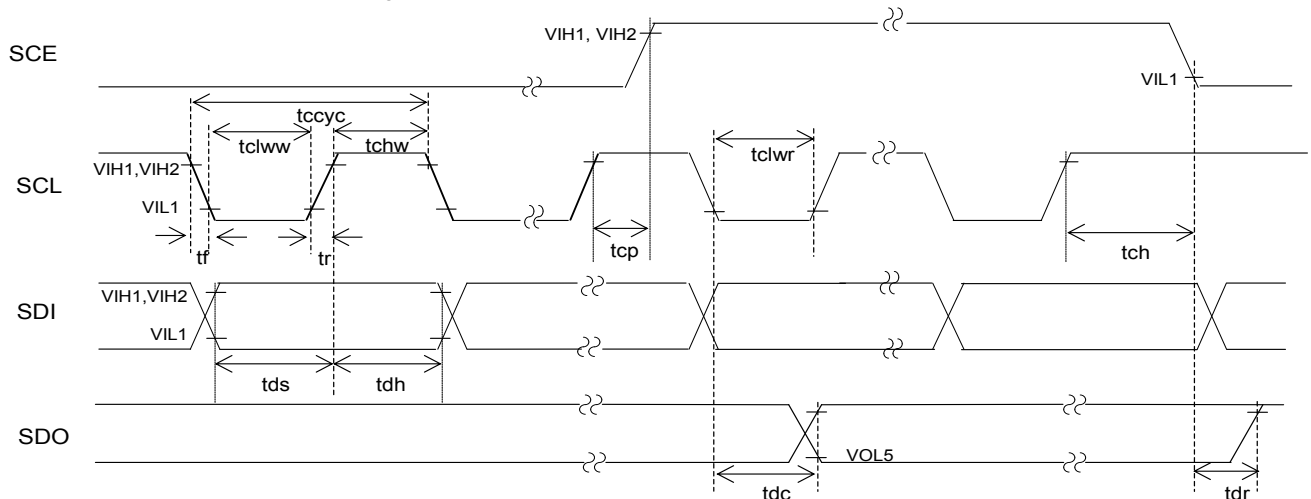




Figure 5. Serial Interface Timing

## Pin Description

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S9/P9/G9	79,80, 1 to 7	Segment output for displaying the display data transferred by serial data input. The S1/P1/G1 to S6/P6/G6 pins can also be used as General –purpose outputs when so set up by the control data.	-	O	OPEN
S10 to S52, S72	8 to 50, 74	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S53 to KS6/S58	51 to 56	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S53 to KS6/S58 pins can be used as segment outputs when so specified by the control data.	-	O	OPEN
KI1/S59 to KI5/S63	57 to 61	Key scan inputs These pins have built-in pull-down resistors. The KI1/S59 to KI5/S63 pins can be used as segment outputs when so specified by the control data.	-	I/O	OPEN
SYNCIO/S64	62	Segment Output for Master without Slave application. SYNC output signal for Master with Slave application and SYNC input signal for Slave application.	- - H	O O I	OPEN - -
CLKIO/S65	63	Segment Output for Master without Slave application. CLK output signal for Master with Slave application and CLK input signal for Slave application.	- - 	O O I	OPEN - -
S66/TESTIN	64	TESTIN Input for Master Application. Segment Output for Slave Application.	- -	I O	VDD OPEN
COM5/S67	65	COMMON / SEGMENT output for LCD driving Assigned as COMMON output in 1/5 Duty mode and SEGMENT output in 1/1 Duty, 1/3 Duty and 1/4 Duty modes	-	O	OPEN
COM1 to COM4	69 to 66	Common driver output pins. The frame frequency is fo[Hz].	-	O	-
MS	72	Master / Slave Control Switch L : Master, H : Slave	-	I	-
OSC_IN/S73	75	Segment output for displaying the display data transferred by serial data input. The pin OSC_IN/S73 can be used as external frequency input pin when set up by the control data.	-	I/O	OPEN
SCE	76	Serial data transfer inputs. Must be connected to the controller. SCE: Chip enable	H 	I	-
SCL	77	SCL: Synchronization clock	-	I	-
SDI	78	SDI: Transfer data	-	I	-
SDO	73	Output data	-	O	OPEN
VDD	70	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	71	Power supply pin. Must be connected to ground.	-	-	-



IO Equivalence Circuit

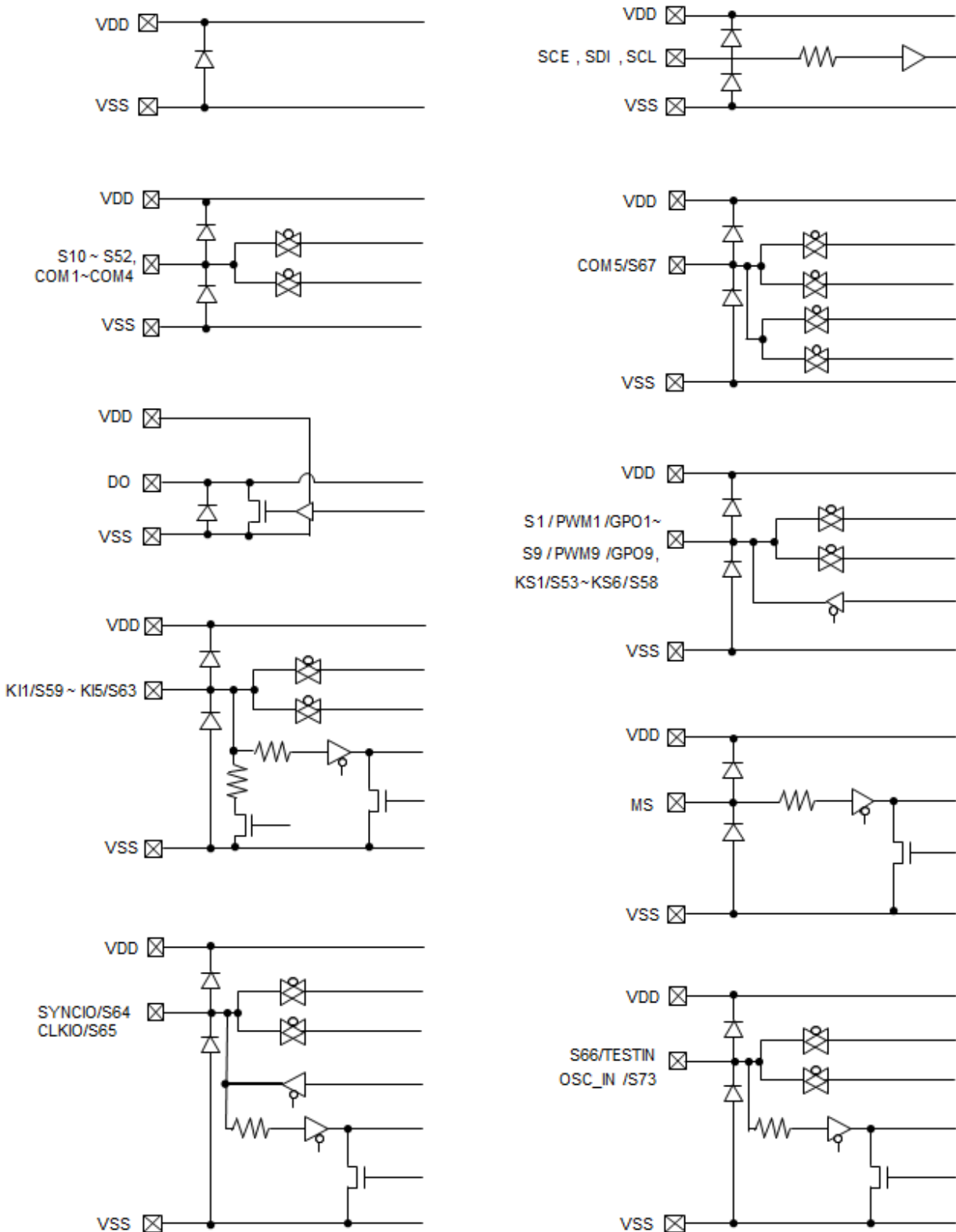


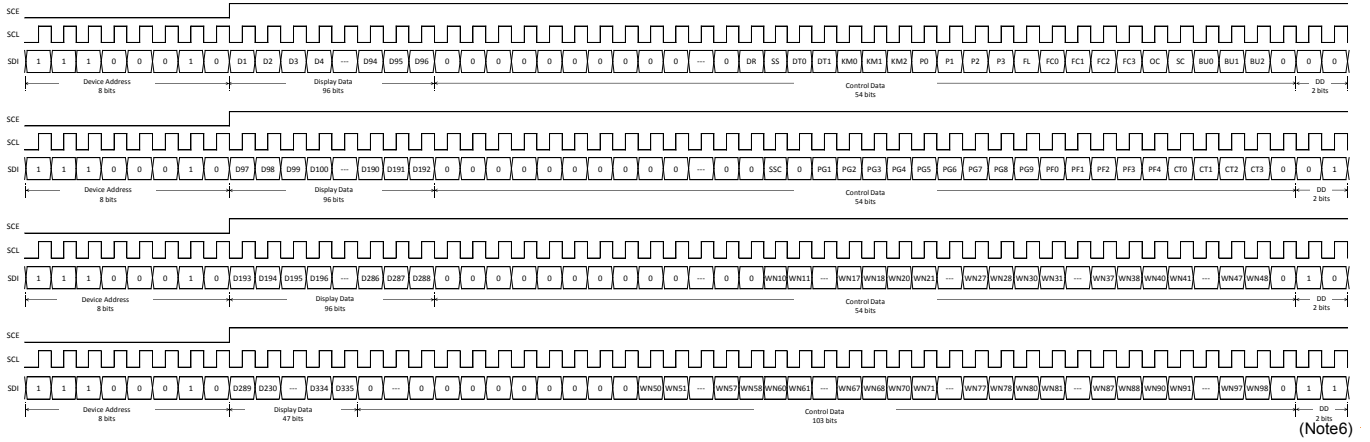
Figure 6. I/O Equivalent Circuit

Serial Data Transfer Formats

1. 1/5 Duty

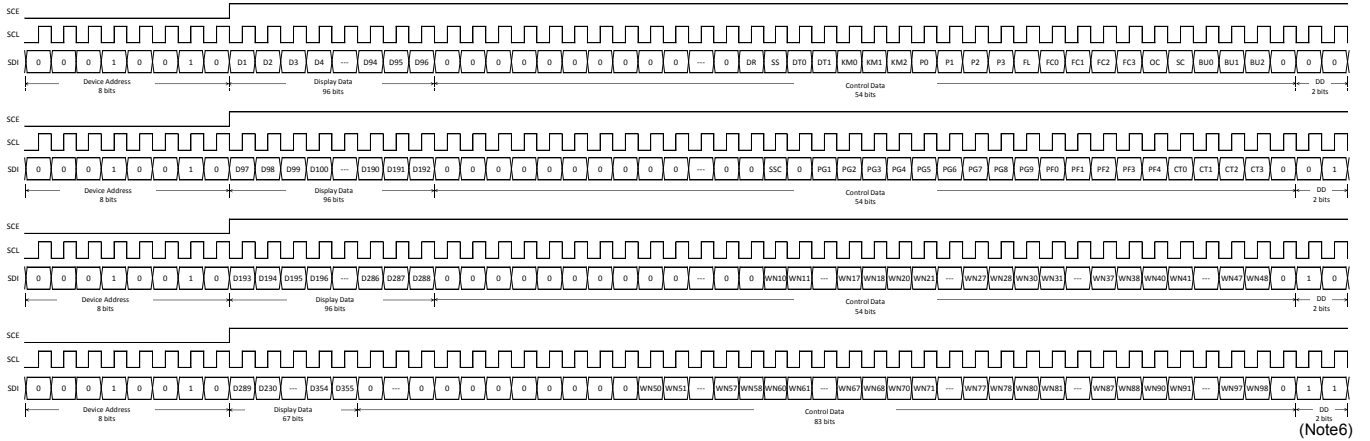
(1) When SCL is stopped at the low level

(a) Master



(Note6)

(b) Slave



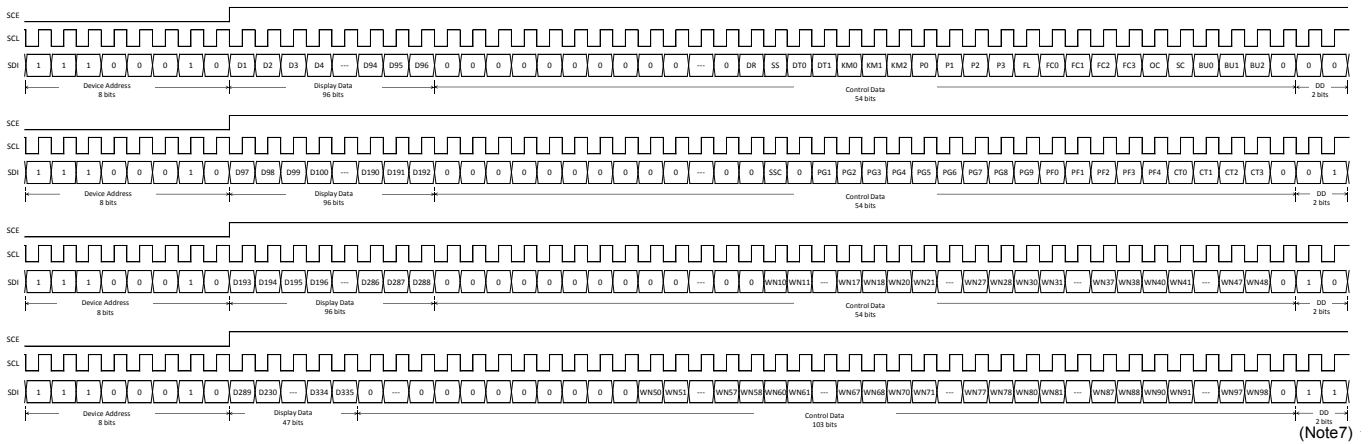
(Note6)

Figure 7. 3-SPI Data Transfer Format

(Note6) DD is direction data.

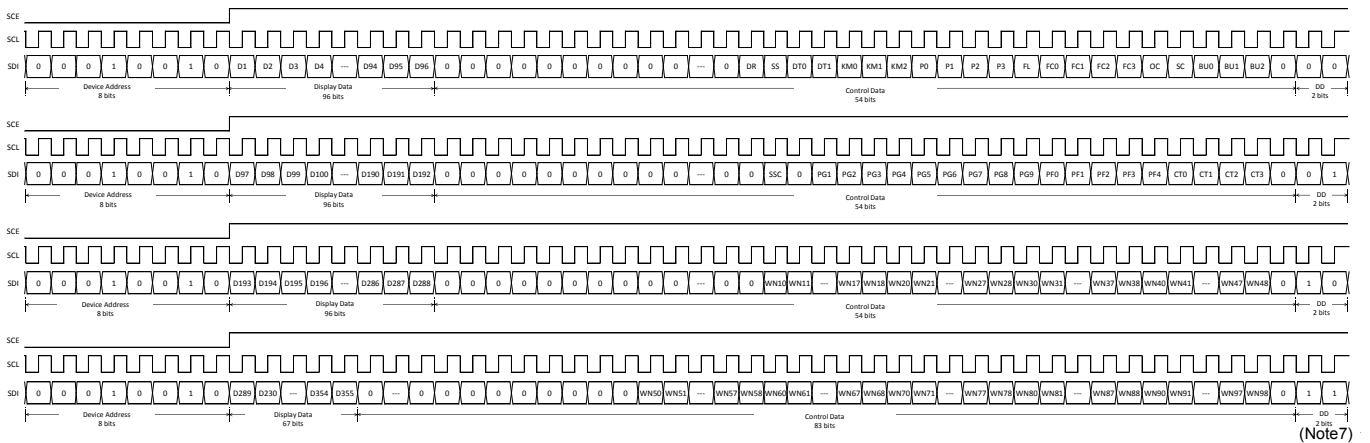
(2) When SCL is stopped at the high level

(a) Master



(Note7)

(b) Slave



(Note7)

Figure 8. 3-SPI Data Transfer Format

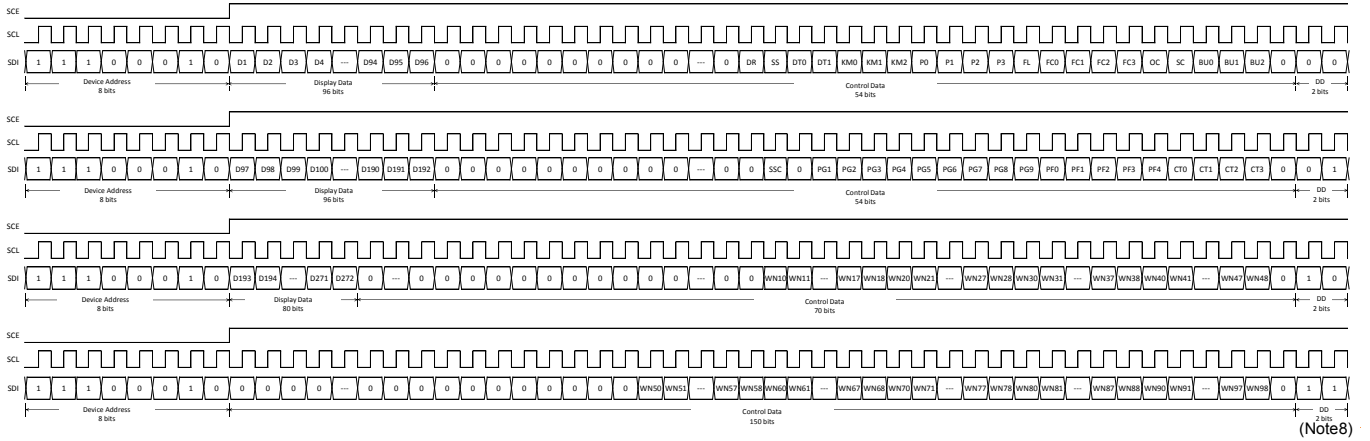
(Note7) DD is direction data.

- Device code....."47H" for Master , "48H" for Slave
- KM0 to KM2.....Key Scan output port/Segment output port switching control data
- D1 to D335.....Display data for Master
- D1 to D355.....Display data for Slave
- SS.....Master Clock and Sync output port/Segment output port switching control data
- SSC.....SEG/COM output port switching control data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- FL.....Line Inversion or Frame Inversion switching control data
- DR.....1/3 bias driver or 1/2 bias driver switching control data
- DT0 to DT1.....1/5-duty drive, 1/4-duty drive, 1/3-duty drive or 1/1-duty(static) drive switching control data
- FC0 to FC3.....Common/segment output waveform frame frequency setting control data
- OC.....Internal oscillator operating mode/External clock operating mode switching control data
- SC.....Segment on/off control data
- BU0 to BU2.....Normal mode/power-saving mode control data
- PG1 to PG9.....PWM/General Purpose output select data
- PF0 to PF4.....PWM output waveform frame frequency setting control data.
- CT0 to CT3.....LCD bias voltage VLCD setting control data.
- W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98  
.....PWM output duty setting control data

2. 1/4 Duty

(1) When SCL is stopped at the low level

(a) Master



(b) Slave

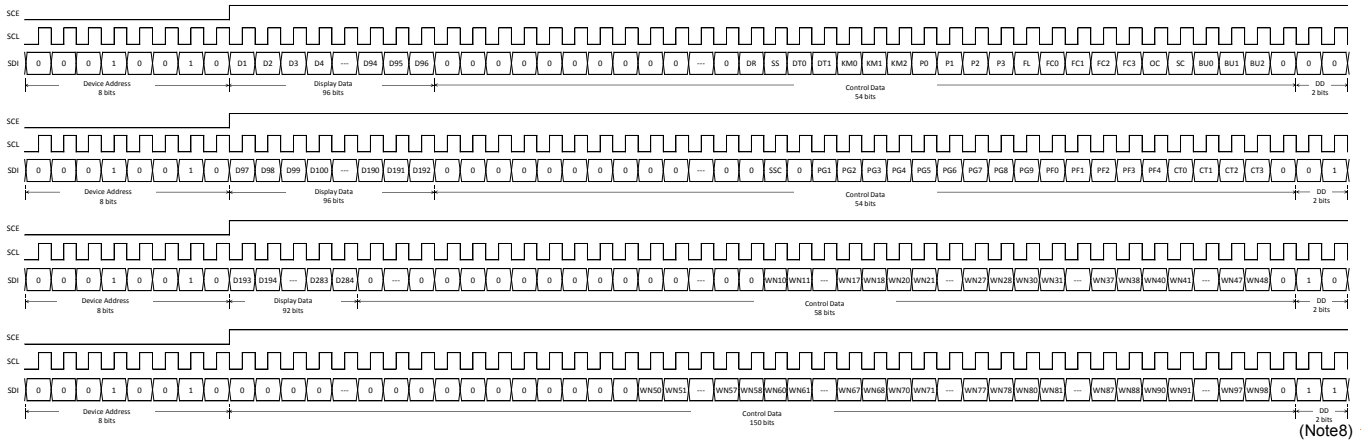
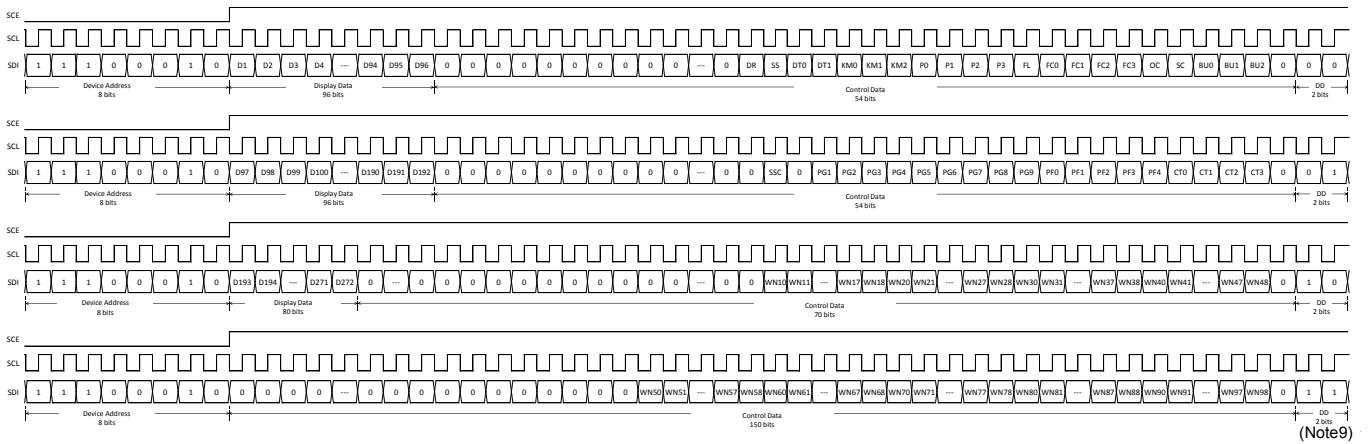


Figure 9. 3-SPI Data Transfer Format

(Note8) DD is direction data.

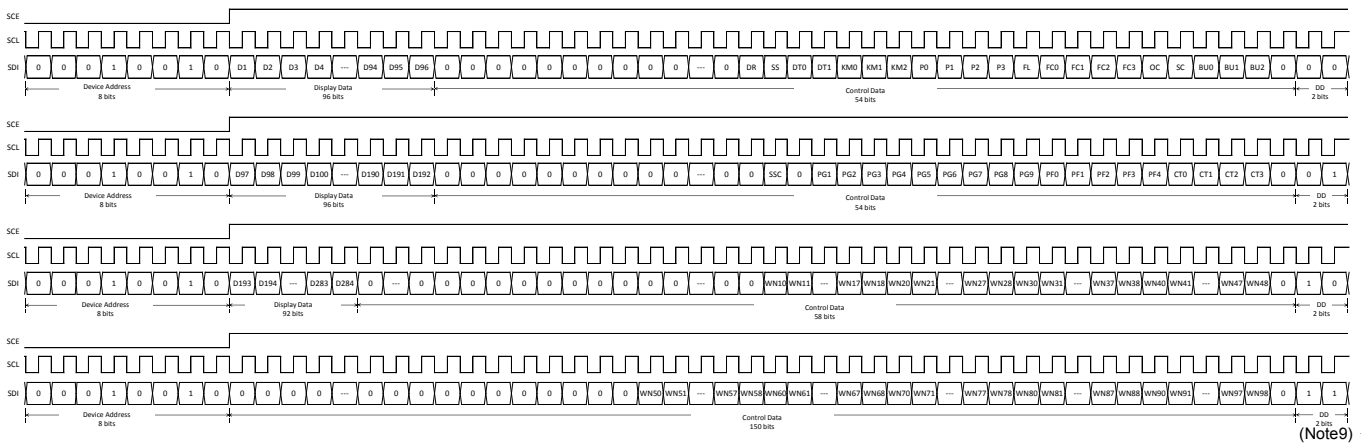
(2) When SCL is stopped at the high level

(a) Master



(Note9)

(b) Slave



(Note9)

Figure 10. 3-SPI Data Transfer Format

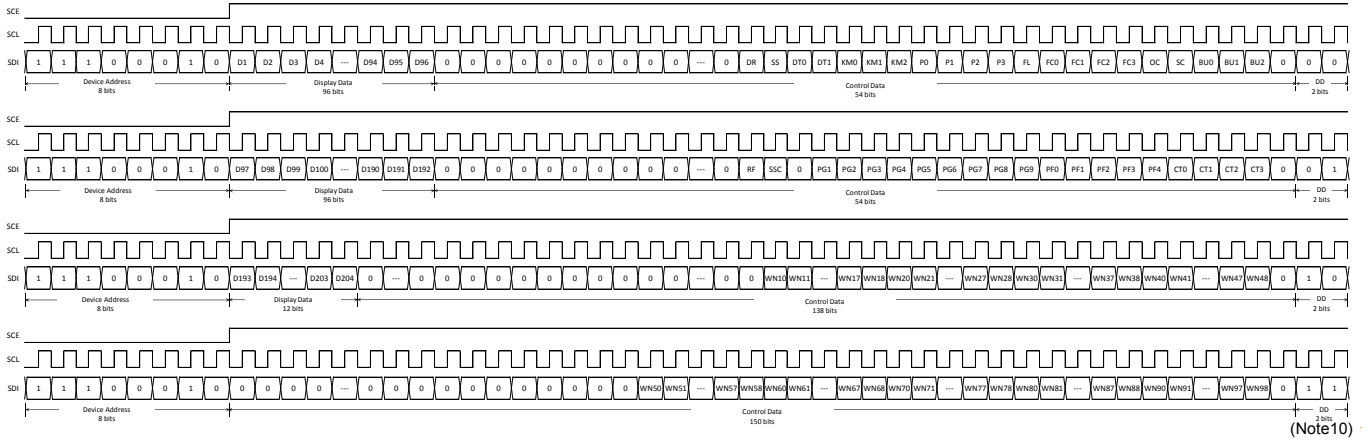
(Note9) DD is direction data.

- Device code.....”47H” for Master , “48H” for Slave
- KM0 to KM2.....Key Scan output port/Segment output port switching control data
- D1 to D272.....Display data for Master
- D1 to D284.....Display data for Slave
- SS.....Master Clock and Sync output port/Segment output port switching control data
- SSC.....SEG/COM output port switching control data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- FL.....Line Inversion or Frame Inversion switching control data
- DR.....1/3 bias driver or 1/2 bias driver switching control data
- DT0 to DT1.....1/5-duty drive, 1/4-duty drive, 1/3-duty drive or 1/1-duty(static) drive switching control data
- FC0 to FC3.....Common/segment output waveform frame frequency setting control data
- OC.....Internal oscillator operating mode/External clock operating mode switching control data
- SC.....Segment on/off control data
- BU0 to BU2.....Normal mode/power-saving mode control data
- PG1 to PG9.....PWM/General Purpose output select data
- PF0 to PF4.....PWM output waveform frame frequency setting control data.
- CT0 to CT3.....LCD bias voltage VLCD setting control data.
- W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98  
.....PWM output duty setting control data

3. 1/3 Duty

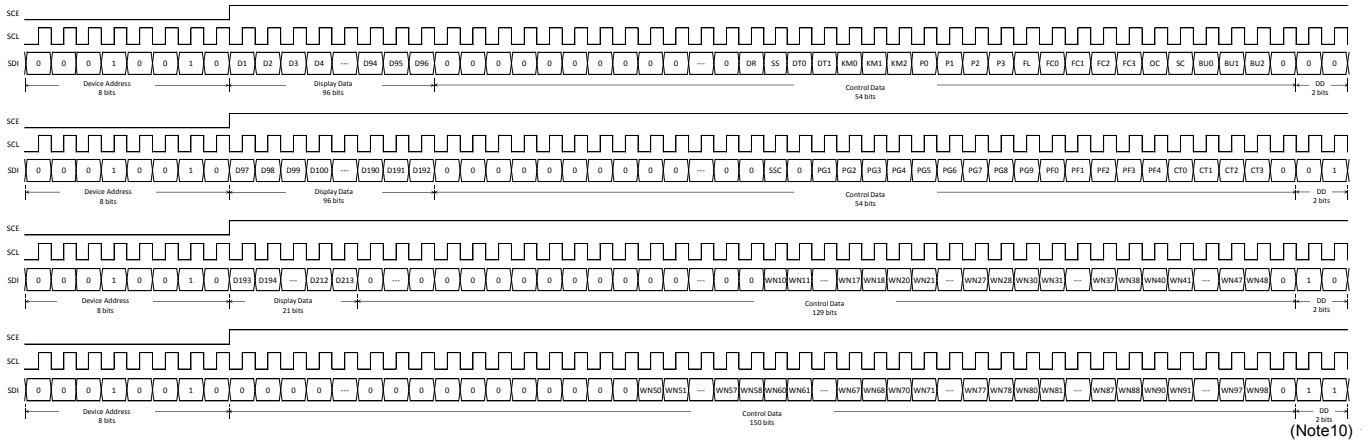
(1) When SCL is stopped at the low level

(a) Master



(Note10)

(b) Slave



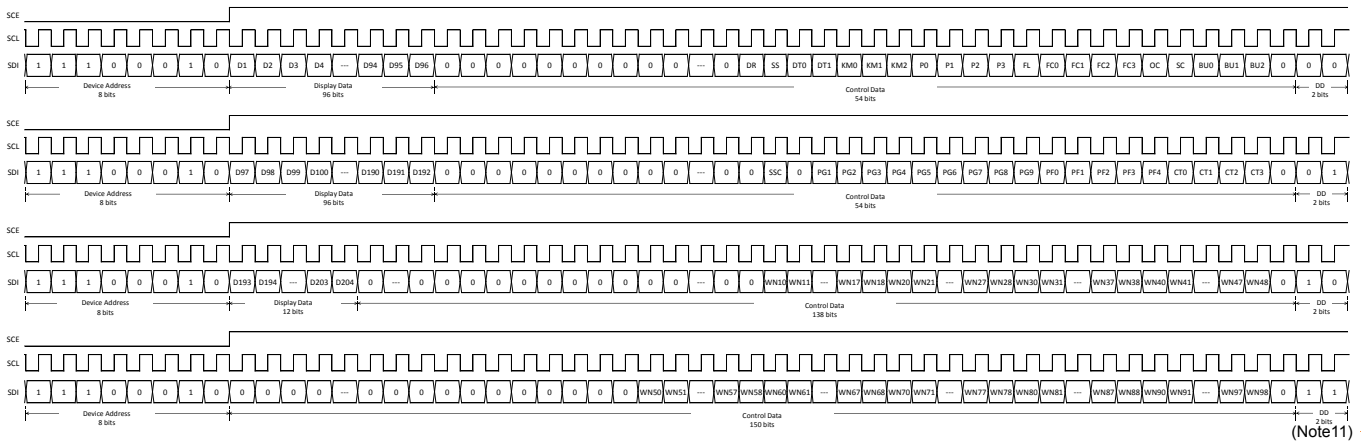
(Note10)

Figure 11. 3-SPI Data Transfer Format

(Note10) DD is direction data.

(2) When SCL is stopped at the high level

(a) Master



(b) Slave

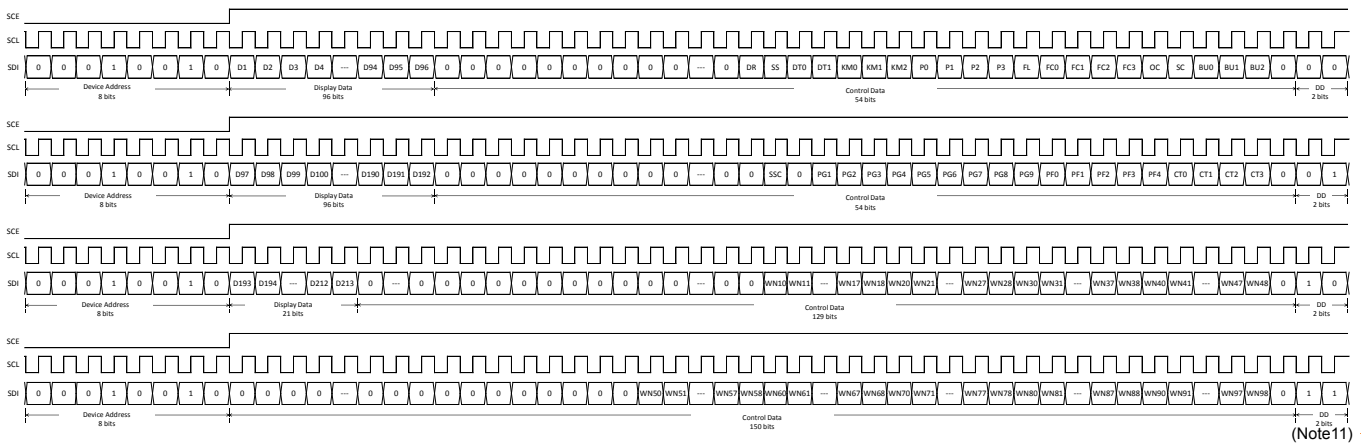


Figure 12. 3-SPI Data Transfer Format

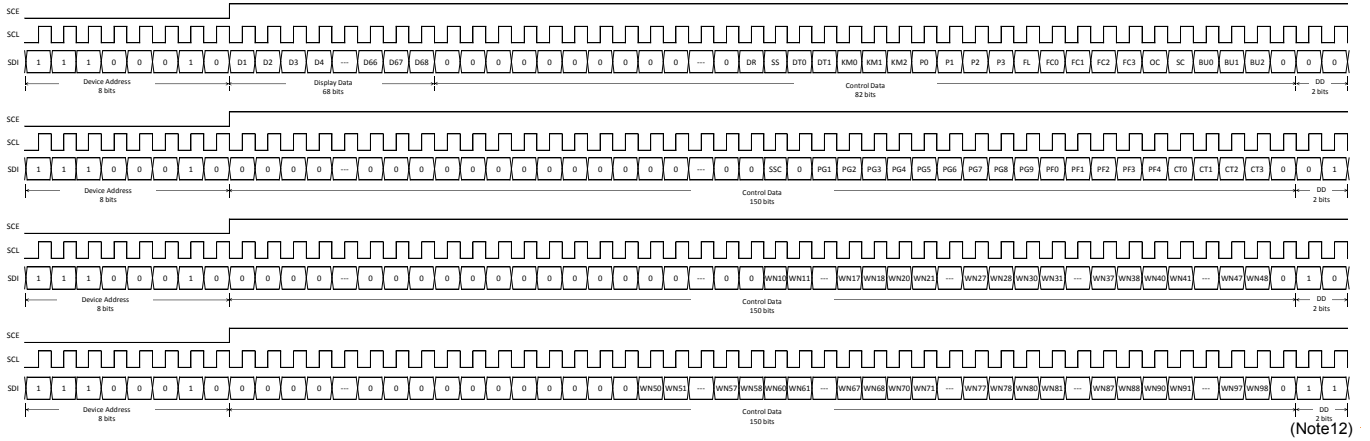
(Note11) DD is direction data.

- Device code....."47H" for Master , "48H" for Slave
- KM0 to KM2.....Key Scan output port/Segment output port switching control data
- D1 to D204.....Display data for Master
- D1 to D213.....Display data for Slave
- SS.....Master Clock and Sync output port/Segment output port switching control data
- SSC.....SEG/COM output port switching control data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- FL.....Line Inversion or Frame Inversion switching control data
- DR.....1/3 bias driver or 1/2 bias driver switching control data
- DT0 to DT1.....1/5-duty drive, 1/4-duty drive, 1/3-duty drive or 1/1-duty(static) drive switching control data
- FC0 to FC3.....Common/segment output waveform frame frequency setting control data
- OC.....Internal oscillator operating mode/External clock operating mode switching control data
- SC.....Segment on/off control data
- BU0 to BU2.....Normal mode/power-saving mode control data
- PG1 to PG9..... PWM/General Purpose output select data
- PF0 to PF4.....PWM output waveform frame frequency setting control data.
- CT0 to CT3.....LCD bias voltage VLCD setting control data.
- W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98  
.....PWM output duty setting control data

4. 1/1 Duty (Static)

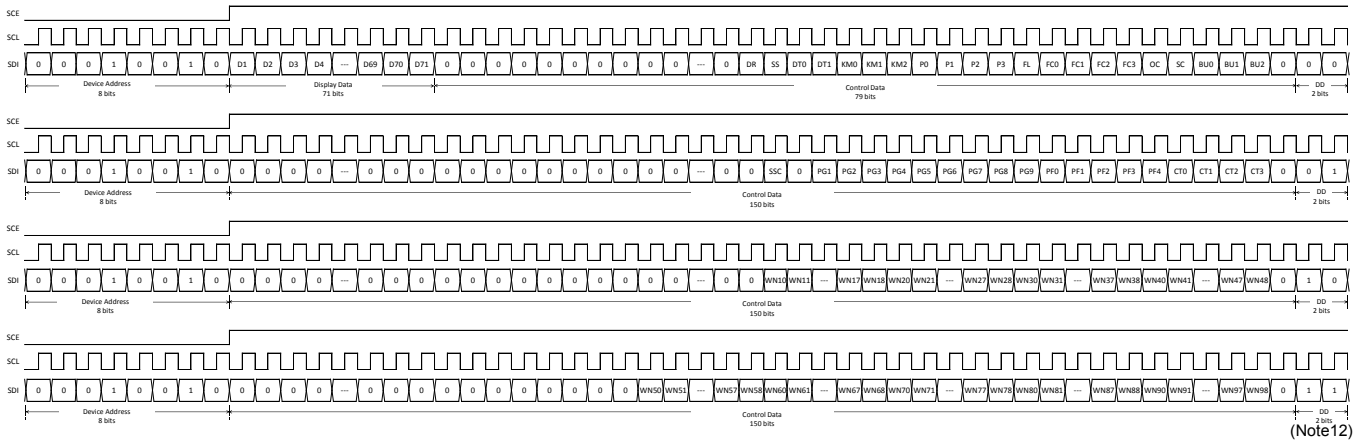
(1) When SCL is stopped at the low level

(a) Master



(Note12)

(b) Slave



(Note12)

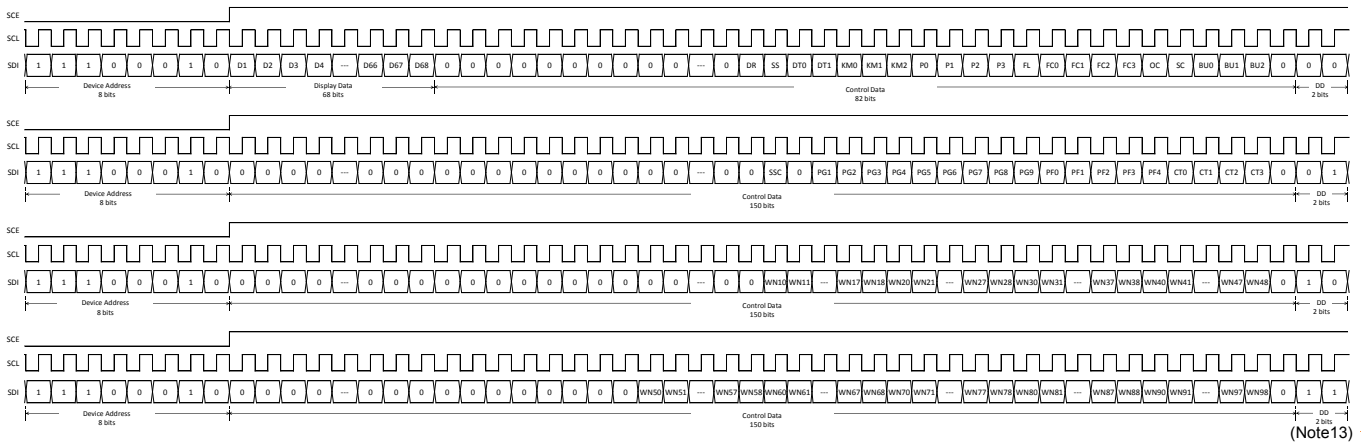
Figure 13. 3-SPI Data Transfer Format

(Note12) DD is direction data.



(2) When SCL is stopped at the high level

(a) Master



(b) Slave

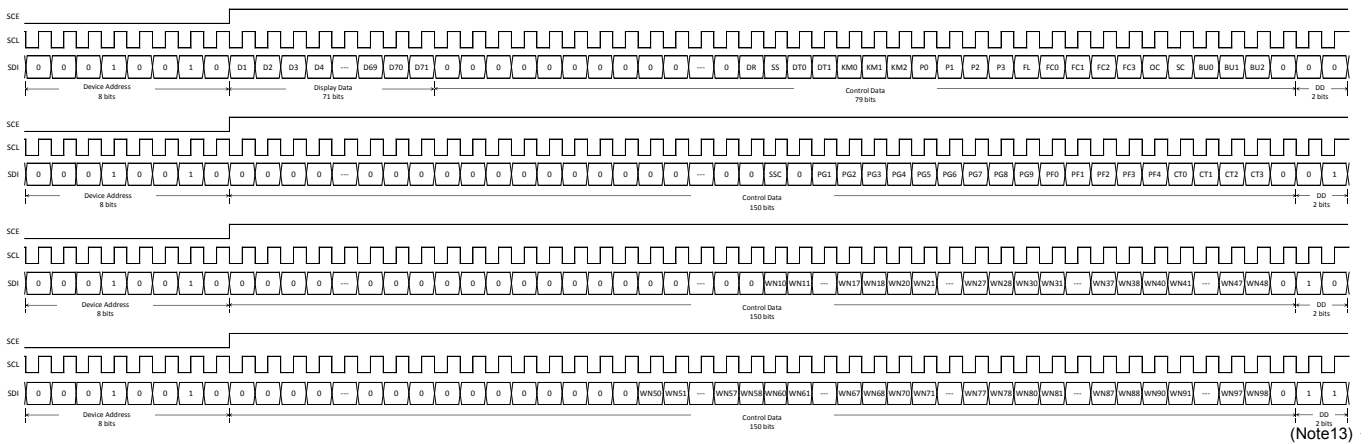


Figure 14. 3-SPI Data Transfer Format

(Note13) DD is direction data.

- Device code.....”47H” for Master , “48H” for Slave
- KM0 to KM2.....Key Scan output port/Segment output port switching control data
- D1 to D68.....Display data for Master
- D1 to D71.....Display data for Slave
- SS.....Master Clock and Sync output port/Segment output port switching control data
- SSC.....SEG/COM output port switching control data
- P0 to P3.....Segment output port/general-purpose output port switching control data
- FL.....Line Inversion or Frame Inversion switching control data
- DR.....1/3 bias driver or 1/2 bias driver switching control data
- DT0 to DT1.....1/5-duty drive, 1/4-duty drive, 1/3-duty drive or 1/1-duty(static) drive switching control data
- FC0 to FC3.....Common/segment output waveform frame frequency setting control data
- OC.....Internal oscillator operating mode/External clock operating mode switching control data
- SC.....Segment on/off control data
- BU0 to BU2.....Normal mode/power-saving mode control data
- PG1 to PG9.....PWM/General Purpose output select data
- PF0 to PF4.....PWM output waveform frame frequency setting control data.
- CT0 to CT3.....LCD bias voltage VLCD setting control data.
- W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98  
.....PWM output duty setting control data

## Control Data Functions

### 1. KM0, KM1 and KM2 : Key Scan output port/Segment output port switching control data

These control data bits switch the functions of the KS1/S53 to KS6/S58 output pins between key scan output and segment output.

KM0	KM1	KM2	Output Pin State						Maximum Number of Input keys
			KS1/S53	KS2/S54	KS3/S55	KS4/S56	KS5/S57	KS6/S58	
0	0	0	KS1	KS2	KS3	KS4	KS5	KS6	30
0	0	1	S53	KS2	KS3	KS4	KS5	KS6	25
0	1	0	S53	S54	KS3	KS4	KS5	KS6	20
0	1	1	S53	S54	S55	KS4	KS5	KS6	15
1	0	0	S53	S54	S55	S56	KS5	KS6	10
1	0	1	S53	S54	S55	S56	S57	KS6	5
1	1	0	S53	S54	S55	S56	S57	S58	0
1	1	1	S53	S54	S55	S56	S57	S58	0

In Slave Mode, it is automatically set to all segment output and cannot be controlled by Serial Interface.

### 2. P0, P1, P2, and P3: Segment / PWM / General Purpose output port switching control data

These control bits are used to select the function of the S1/P1/G1 to S9/P9/G9 output pins (Segment Output Pins or PWM Output Pins or General Purpose Output Pins).

P0	P1	P2	P3	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	S7/P7/G7	S8/P8/G8	S9/P9/G9
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
0	0	0	1	P1/G1	S2	S3	S4	S5	S6	S7	S8	S9
0	0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	S7	S8	S9
0	0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	S7	S8	S9
0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	S7	S8	S9
0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	S7	S8	S9
0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S7	S8	S9
0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S8	S9
1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	S9
1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	P9/S9
1	0	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	0	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	0	1	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9
1	1	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9

PWM output or General Purpose output is selected by PGx(x=1 to 9) control data bit.

When the General Purpose Output Port Function is selected, the correspondence between the output pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data			
	1/5 Duty mode	1/4 Duty mode	1/3 Duty mode	1/1 Duty (static) mode
S1/P1/G1	D1	D1	D1	D1
S2/P2/G2	D6	D5	D4	D2
S3/P3/G3	D11	D9	D7	D3
S4/P4/G4	D16	D13	D10	D4
S5/P5/G5	D21	D17	D13	D4
S6/P6/G6	D26	D21	D16	D5
S7/P7/G7	D31	D25	D19	D7
S8/P8/G8	D36	D29	D22	D8
S9/P9/G9	D41	D33	D25	D9

When the General Purpose Output Port Function is selected, the respective output pin outputs a "HIGH" level when its corresponding display data is set to "1". Likewise, it will output a "LOW" level, if its corresponding display data is set to "0". For example, at 1/4 Duty mode, S4/P4/G4 is used as a General Purpose Output Port, if its corresponding display data D13 is set to "1", then S4/P4/G4 will output "HIGH" level. Likewise, if D13 is set to "0", then S4/P4/G4 will output "LOW" level.

### 3. FL: Line Inversion or Frame Inversion switching control data

This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion mode
0	Line Inversion
1	Frame Inversion

## 4. DR: 1/3 bias drive, 1/2 bias drive or 1/1 bias drive switching control data

This control data bit selects either 1/3 bias drive or 1/2 bias drive.

DR	Bias drive scheme
0	1/3 Bias
1	1/2 Bias

## 5. SS: Master Clock and Sync output port/Segment output port switching control data

This control data bit switches the functions of the CLKIO/S64 and SYNCIO/S65 output pins between master/slave output and segment output.

SS	Output Pin State	
	CLKIO/S64	SYNCIO/S65
0	S64	S65
1	CLKIO	SYNCIO

In Slave Mode, it is automatically set to all segment output and cannot be controlled by Serial Interface.

## 6. DT: 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty switching control data

These control data bits select either 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or 1/1 duty (static)

DT0	DT1	Duty drive scheme
0	0	1/1 duty (static) drive
0	0	1/3 duty drive
0	1	1/4 duty drive
1	1	1/5 duty drive

## 7. FC0, FC1, FC2 and FC3: Common/segment output waveform frame frequency setting control data

These control data bits set the frame frequency for common and segment output waveforms.

FC0	FC1	FC2	FC3	Frame Frequency fo(Hz)
0	0	0	0	$f_{osc}^{(Note14)} / 12288$
0	0	0	1	$f_{osc} / 10752$
0	0	1	0	$f_{osc} / 9216$
0	0	1	1	$f_{osc} / 7680$
0	1	0	0	$f_{osc} / 6144$
0	1	0	1	$f_{osc} / 4608$
0	1	1	0	$f_{osc} / 3840$
0	1	1	1	$f_{osc} / 3072$
1	0	0	0	$f_{osc} / 2880$
1	0	0	1	$f_{osc} / 2688$
1	0	1	0	$f_{osc} / 2496$
1	0	1	1	$f_{osc} / 2304$
1	1	0	0	$f_{osc} / 2112$
1	1	0	1	$f_{osc} / 1920$
1	1	1	0	$f_{osc} / 1728$
1	1	1	1	$f_{osc} / 1536$

(Note14)fosc: Internal Oscillation Frequency (600 [kHz] Typ)

## 8. OC: Internal oscillator operating mode/External clock operating mode switching control data

OC	Operating mode	In/Out pin(OSC_IN/S73) status
0	Internal oscillator	S73 (segment output)
1	External Clock	OSC_IN (clock input)

## 9. SC: Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	ON
1	OFF

Note that when the segments are turned off by setting SC to "1", the segments are turned off by outputting segment off waveforms from the segment output pins.

10. BU0, BU1 and BU2 : Normal mode/power-saving mode control data  
 These control data bits select either normal mode or power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment outputs Common outputs	Output Pin States During Key Scan Standby					
						KS1	KS2	KS3	KS4	KS5	KS6
0	0	0	Normal	Operating	Operating	H	H	H	H	H	H
0	0	1	Power-saving	Stopped	Low(VSS)	L	L	L	L	L	H
0	1	0				L	L	L	L	H	H
0	1	1				L	L	L	H	H	H
1	0	0				L	L	H	H	H	H
1	0	1				L	H	H	H	H	H
1	1	0				H	H	H	H	H	H
1	1	1				H	H	H	H	H	H

Power-saving mode status: S1/P1/G1 to S9/P9/G9 = active only General Purpose output  
 S10 to OSC\_IN/S73 = low (VSS)  
 COM1 to COM5 = low (VSS)  
 Shut off current to the LCD drive bias voltage generation circuit  
 Stop the Internal oscillation circuit  
 However, serial data transfer is possible when at Power-saving mode.

11. SSC: SEG/COM output port switching control data  
 This control data bit selects SEG or COM output for Slave.

SSC	Output Pin State				
	COM5/S67	COM4/S68	COM3/S69	COM2/S70	COM1/S71
0	S67	S68	S69	S70	S71
1	COM5	COM4	COM3	COM2	COM1

This option is not available in Master mode.

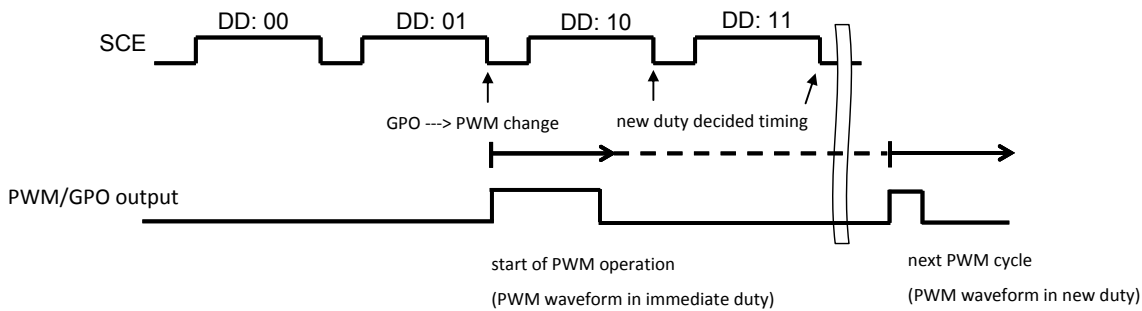
12. PG1, PG2, PG3, PG4, PG5, PG6, PG7, PG8 and PG9: PWM/General Purpose output control data  
 This control data bit select either PWM output or General Purpose output of Sx/Px/Gx pins. (x=1 to 9)

PGx(x=1 to 9)	Mode
0	PWM Output
1	General Purpose Output

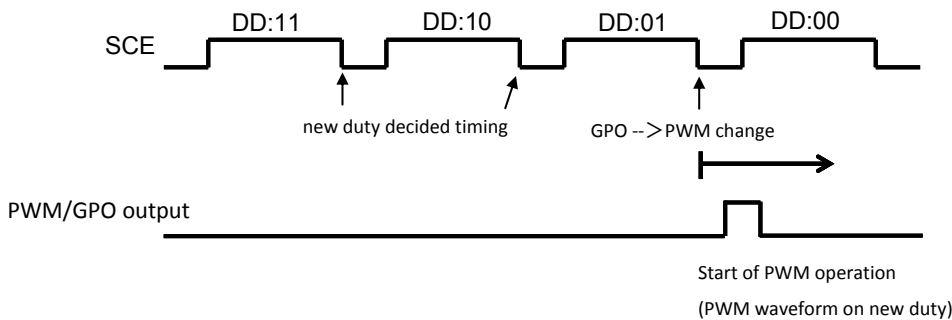
<PWM<->GPO Changing function>

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 01 during GPO → PWM change.
- Please take care of reflect timing of new duty setting of DD: 10 and DD: 11 are from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



## 13. PF0, PF1, PF2, PF3 and PF4: PWM output waveform frame frequency setting control data

These control data bits set the frame frequency for pwm output waveforms.

PF0	PF1	PF2	PF3	PF4	PWM output Frame Frequency fp(Hz)
0	0	0	0	0	fosc / 4096
0	0	0	0	1	fosc / 3840
0	0	0	1	0	fosc / 3584
0	0	0	1	1	fosc / 3328
0	0	1	0	0	fosc / 3072
0	0	1	0	1	fosc / 2816
0	0	1	1	0	fosc / 2560
0	0	1	1	1	fosc / 2304
0	1	0	0	0	fosc / 2048
0	1	0	0	1	fosc / 1792
0	1	0	1	0	fosc / 1536
0	1	0	1	1	fosc / 1280
0	1	1	0	0	fosc / 1024
0	1	1	0	1	fosc / 768
0	1	1	1	0	fosc / 512
0	1	1	1	1	fosc / 256
1	0	0	0	0	fosc / 128
. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	fosc / 128

## 14. CT0, CT1, CT2 and CT3: Display Contrast setting control data

These control data bits set display contrast

CT0	CT1	CT2	CT3	LCD Drive bias voltage for VLCD Level
0	0	0	0	1.000*VDD
0	0	0	1	0.975*VDD
0	0	1	0	0.950*VDD
0	0	1	1	0.925*VDD
0	1	0	0	0.900*VDD
0	1	0	1	0.875*VDD
0	1	1	0	0.850*VDD
0	1	1	1	0.825*VDD
1	0	0	0	0.800*VDD
1	0	0	1	0.775*VDD
1	0	1	0	0.750*VDD
1	0	1	1	0.725*VDD
1	1	0	0	0.700*VDD
1	1	0	1	0.675*VDD
1	1	1	0	0.650*VDD
1	1	1	1	0.625*VDD

15. W10 to W18<sup>(Note15)</sup>, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88 and W90 to W98: PWM output waveform duty setting control data. These control data bits set the high level pulse width (duty) for pwm output waveforms.

Table below shows PWM high level pulse width when PF0 to PF3 command setting is [PF0,PF1,PF2,PF3]=[0,x,x,x]  
 $n = 1 \text{ to } 9, T_p = 1/f_p$

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	Wn8	PWM duty
0	0	0	0	0	0	0	0	0	(0/256) x Tp
0	0	0	0	0	0	0	0	1	(1/256) x Tp
0	0	0	0	0	0	0	1	0	(2/256) x Tp
0	0	0	0	0	0	0	1	1	(3/256) x Tp
0	0	0	0	0	0	1	0	0	(4/256) x Tp
0	0	0	0	0	0	1	0	1	(5/256) x Tp
0	0	0	0	0	0	1	1	0	(6/256) x Tp
0	0	0	0	0	0	1	1	1	(7/256) x Tp
0	0	0	0	0	1	0	0	0	(8/256) x Tp
0	0	0	0	0	1	0	0	1	(9/256) x Tp
0	0	0	0	0	1	0	1	0	(10/256) x Tp
0	0	0	0	0	1	0	1	1	(11/256) x Tp
0	0	0	0	0	1	1	0	0	(12/256) x Tp
0	0	0	0	0	1	1	0	1	(13/256) x Tp
0	0	0	0	0	1	1	1	0	(14/256) x Tp
0	0	0	0	0	1	1	1	1	(15/256) x Tp
0	0	0	0	1	0	0	0	0	(16/256) x Tp
0	0	0	0	1	0	0	0	1	(17/256) x Tp
0	0	0	0	1	0	0	1	0	(18/256) x Tp
0	0	0	0	1	0	0	1	1	(19/256) x Tp
0	0	0	0	1	0	1	0	0	(20/256) x Tp
...	...	...	...	...	...	...	...	...	...
0	1	1	1	0	1	0	1	1	(235/256) x Tp
0	1	1	1	0	1	1	0	0	(236/256) x Tp
0	1	1	1	0	1	1	0	1	(237/256) x Tp
0	1	1	1	0	1	1	1	0	(238/256) x Tp
0	1	1	1	0	1	1	1	1	(239/256) x Tp
0	1	1	1	1	0	0	0	0	(240/256) x Tp
0	1	1	1	1	0	0	0	1	(241/256) x Tp
0	1	1	1	1	0	0	1	0	(242/256) x Tp
0	1	1	1	1	0	0	1	1	(243/256) x Tp
0	1	1	1	1	0	1	0	0	(244/256) x Tp
0	1	1	1	1	0	1	0	1	(245/256) x Tp
0	1	1	1	1	0	1	1	0	(246/256) x Tp
0	1	1	1	1	0	1	1	1	(247/256) x Tp
0	1	1	1	1	1	0	0	0	(248/256) x Tp
0	1	1	1	1	1	0	0	1	(249/256) x Tp
0	1	1	1	1	1	0	1	0	(250/256) x Tp
0	1	1	1	1	1	0	1	1	(251/256) x Tp
0	1	1	1	1	1	1	0	0	(252/256) x Tp
0	1	1	1	1	1	1	0	1	(253/256) x Tp
0	1	1	1	1	1	1	1	0	(254/256) x Tp
0	1	1	1	1	1	1	1	1	(255/256) x Tp
1	0	0	0	0	0	0	0	0	(256/256) x Tp
1	0	0	0	0	0	0	0	1	(256/256) x Tp
1	0	0	0	0	0	0	1	0	(256/256) x Tp
1	0	0	0	0	0	0	1	1	(256/256) x Tp
...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	0	0	(256/256) x Tp
1	1	1	1	1	1	1	0	1	(256/256) x Tp
1	1	1	1	1	1	1	1	0	(256/256) x Tp
1	1	1	1	1	1	1	1	1	(256/256) x Tp

(Note15) W10 to W18:S1/P1/G1 pwm duty data  
 W20 to W28:S2/P2/G2 pwm duty data  
 W30 to W38:S3/P3/G3 pwm duty data  
 W40 to W48:S4/P4/G4 pwm duty data  
 W50 to W58:S5/P5/G5 pwm duty data  
 W60 to W68:S6/P6/G6 pwm duty data  
 W70 to W78:S7/P7/G7 pwm duty data  
 W80 to W88:S8/P8/G8 pwm duty data  
 W90 to W98:S9/P9/G9 pwm duty data

Table below shows PWM high level pulse width when PF0 to PF3 command setting is [PF0,PF1,PF2,PF3]=[1,x,x,x]  
 $n = 1 \text{ to } 9, T_p = 1/f_p$

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Wn6	Wn7	Wn8	PWM duty
0	0	0	0	0	0	0	0	0	(0/128) x Tp
0	0	0	0	0	0	0	0	1	(1/128) x Tp
0	0	0	0	0	0	0	1	0	(2/128) x Tp
0	0	0	0	0	0	0	1	1	(3/128) x Tp
0	0	0	0	0	0	1	0	0	(4/128) x Tp
0	0	0	0	0	0	1	0	1	(5/128) x Tp
0	0	0	0	0	0	1	1	0	(6/128) x Tp
0	0	0	0	0	0	1	1	1	(7/128) x Tp
0	0	0	0	0	1	0	0	0	(8/128) x Tp
0	0	0	0	0	1	0	0	1	(9/128) x Tp
0	0	0	0	0	1	0	1	0	(10/128) x Tp
0	0	0	0	0	1	0	1	1	(11/128) x Tp
0	0	0	0	0	1	1	0	0	(12/128) x Tp
0	0	0	0	0	1	1	0	1	(13/128) x Tp
0	0	0	0	0	1	1	1	0	(14/128) x Tp
0	0	0	0	0	1	1	1	1	(15/128) x Tp
0	0	0	0	1	0	0	0	0	(16/128) x Tp
0	0	0	0	1	0	0	0	1	(17/128) x Tp
0	0	0	0	1	0	0	1	0	(18/128) x Tp
0	0	0	0	1	0	0	1	1	(19/128) x Tp
0	0	0	0	1	0	1	0	0	(20/128) x Tp
...	...	...	...	...	...	...	...	...	...
0	0	1	1	0	1	0	1	1	(107/128) x Tp
0	0	1	1	0	1	1	0	0	(108/128) x Tp
0	0	1	1	0	1	1	0	1	(109/128) x Tp
0	0	1	1	0	1	1	1	0	(110/128) x Tp
0	0	1	1	0	1	1	1	1	(111/128) x Tp
0	0	1	1	1	0	0	0	0	(112/128) x Tp
0	0	1	1	1	0	0	0	1	(113/128) x Tp
0	0	1	1	1	0	0	1	0	(114/128) x Tp
0	0	1	1	1	0	0	1	1	(115/128) x Tp
0	0	1	1	1	0	1	0	0	(116/128) x Tp
0	0	1	1	1	0	1	0	1	(117/128) x Tp
0	0	1	1	1	0	1	1	0	(118/128) x Tp
0	0	1	1	1	0	1	1	1	(119/128) x Tp
0	0	1	1	1	1	0	0	0	(120/128) x Tp
0	0	1	1	1	1	0	0	1	(121/128) x Tp
0	0	1	1	1	1	0	1	0	(122/128) x Tp
0	0	1	1	1	1	0	1	1	(123/128) x Tp
0	0	1	1	1	1	1	0	0	(124/128) x Tp
0	0	1	1	1	1	1	0	1	(125/128) x Tp
0	0	1	1	1	1	1	1	0	(126/128) x Tp
0	0	1	1	1	1	1	1	1	(127/128) x Tp
0	1	0	0	0	0	0	0	0	(128/128) x Tp
0	1	0	0	0	0	0	0	1	(128/128) x Tp
0	1	0	0	0	0	0	1	0	(128/128) x Tp
0	1	0	0	0	0	0	1	1	(128/128) x Tp
...	...	...	...	...	...	...	...	...	...
1	1	1	1	1	1	1	0	0	(128/128) x Tp
1	1	1	1	1	1	1	0	1	(128/128) x Tp
1	1	1	1	1	1	1	1	0	(128/128) x Tp
1	1	1	1	1	1	1	1	1	(128/128) x Tp

(Note15) W10 to W18:S1/P1/G1 pwm duty data  
 W20 to W28:S2/P2/G2 pwm duty data  
 W30 to W38:S3/P3/G3 pwm duty data  
 W40 to W48:S4/P4/G4 pwm duty data  
 W50 to W58:S5/P5/G5 pwm duty data  
 W60 to W68:S6/P6/G6 pwm duty data  
 W70 to W78:S7/P7/G7 pwm duty data  
 W80 to W88:S8/P8/G8 pwm duty data  
 W90 to W98:S9/P9/G9 pwm duty data

## Display Data and Output Pin Correspondence

## 1.1/5 duty Master

Output Pin <sup>(Note16)</sup>	COM1	COM2	COM3	COM4	COM5
S1/P1/G1	D1	D2	D3	D4	D5
S2/P2/G2	D6	D7	D8	D9	D10
S3/P3/G3	D11	D12	D13	D14	D15
S4/P4/G4	D16	D17	D18	D19	D20
S5/P5/G5	D21	D22	D23	D24	D25
S6/P6/G6	D26	D27	D28	D29	D30
S7/P7/G7	D31	D32	D33	D34	D35
S8/P8/G8	D36	D37	D38	D39	D40
S9/P9/G9	D41	D42	D43	D44	D45
S10	D46	D47	D48	D49	D50
S11	D51	D52	D53	D54	D55
S12	D56	D57	D58	D59	D60
S13	D61	D62	D63	D64	D65
S14	D66	D67	D68	D69	D70
S15	D71	D72	D73	D74	D75
S16	D76	D77	D78	D79	D80
S17	D81	D82	D83	D84	D85
S18	D86	D87	D88	D89	D90
S19	D91	D92	D93	D94	D95
S20	D96	D97	D98	D99	D100
S21	D101	D102	D103	D104	D105
S22	D106	D107	D108	D109	D110
S23	D111	D112	D113	D114	D115
S24	D116	D117	D118	D119	D120
S25	D121	D122	D123	D124	D125
S26	D126	D127	D128	D129	D130
S27	D131	D132	D133	D134	D135
S28	D136	D137	D138	D139	D140
S29	D141	D142	D143	D144	D145
S30	D146	D147	D148	D149	D150
S31	D151	D152	D153	D154	D155
S32	D156	D157	D158	D159	D160
S33	D161	D162	D163	D164	D165
S34	D166	D167	D168	D169	D170
S35	D171	D172	D173	D174	D175
S36	D176	D177	D178	D179	D180
S37	D181	D182	D183	D184	D185
S38	D186	D187	D188	D189	D190
S39	D191	D192	D193	D194	D195
S40	D196	D197	D198	D199	D200
S41	D201	D202	D203	D204	D205
S42	D206	D207	D208	D209	D210
S43	D211	D212	D213	D214	D215
S44	D216	D217	D218	D219	D220
S45	D221	D222	D223	D224	D225
S46	D226	D227	D228	D229	D230
S47	D231	D232	D233	D234	D235
S48	D236	D237	D238	D239	D240
S49	D241	D242	D243	D244	D245
S50	D246	D247	D248	D249	D250
S51	D251	D252	D253	D254	D255
S52	D256	D257	D258	D259	D260
KS1/S53	D261	D262	D263	D264	D265
KS2/S54	D266	D267	D268	D269	D270
KS3/S55	D271	D272	D273	D274	D275
KS4/S56	D276	D277	D278	D279	D280
KS5/S57	D281	D282	D283	D284	D285
KS6/S58	D286	D287	D288	D289	D290
KI1/S59	D291	D292	D293	D294	D295
KI2/S60	D296	D297	D298	D299	D300
KI3/S61	D301	D302	D303	D304	D305
KI4/S62	D306	D307	D308	D309	D310
KI5/S63	D311	D312	D313	D314	D315



Output Pin <sup>(Note16)</sup>	COM1	COM2	COM3	COM4	COM5
CLKIO/S64	D316	D317	D318	D319	D320
SYNCIO/S65	D321	D322	D323	D324	D325
S66/TESTIN					
COM5/S67					
COM4/S68					
COM3/S69					
COM2/S70					
COM1/S71					
S72	D326	D327	D328	D329	D330
OSC_IN/S73	D331	D332	D333	D334	D335

(Note 16) The Segment Output Port function is assumed to be selected for the output pins – S1/P1/G1 to S9/P9/G9, KS1/S53 to KS6/S58, K11/S59 to K15/S63, OSC\_IN/S73. Also, COM5/S67 pin is used as Common output.  
 During 1 chip mode, S66/TESTIN functions as TESTIN input.  
 During 2 chip mode(Master with Slave), CLKIO/S64 and SYNCIO/S65 function as CLK and SYNC outputs.

To illustrate further, the states of the S21 output pin is given in the table below.

Display data					State of S21 Output Pin
D101	D102	D103	D104	D105	
0	0	0	0	0	LCD Segments corresponding to COM1 to COM5 are OFF.
0	0	0	0	1	LCD Segment corresponding to COM5 is ON.
0	0	0	1	0	LCD Segment corresponding to COM4 is ON.
0	0	0	1	1	LCD Segments corresponding to COM4 and COM5 are ON.
0	0	1	0	0	LCD Segment corresponding to COM3 is ON.
0	0	1	0	1	LCD Segments corresponding to COM3 and COM5 are ON.
0	0	1	1	0	LCD Segments corresponding to COM3 and COM4 are ON.
0	0	1	1	1	LCD Segments corresponding to COM3, COM4 and COM5 are ON.
0	1	0	0	0	LCD Segment corresponding to COM2 is ON.
0	1	0	0	1	LCD Segments corresponding to COM2 and COM5 are ON.
0	1	0	1	0	LCD Segments corresponding to COM2 and COM4 are ON.
0	1	0	1	1	LCD Segments corresponding to COM2, COM4 and COM5 are ON.
0	1	1	0	0	LCD Segments corresponding to COM2 and COM3 are ON.
0	1	1	0	1	LCD Segments corresponding to COM2, COM3, and COM5 are ON.
0	1	1	1	0	LCD Segments corresponding to COM2, COM3, and COM4 are ON.
0	1	1	1	1	LCD Segments corresponding to COM2, COM3, COM4 and COM5 are ON.
1	0	0	0	0	LCD Segment corresponding to COM1 is ON.
1	0	0	0	1	LCD Segment corresponding to COM1 and COM5 are ON.
1	0	0	1	0	LCD Segment corresponding to COM1 and COM4 are ON.
1	0	0	1	1	LCD Segment corresponding to COM1, COM4 and COM5 are ON.
1	0	1	0	0	LCD Segment corresponding to COM1 and COM3 are ON.
1	0	1	0	1	LCD Segment corresponding to COM1, COM3 and COM5 are ON.
1	0	1	1	0	LCD Segment corresponding to COM1, COM3 and COM4 are ON.
1	0	1	1	1	LCD Segment corresponding to COM1, COM3, COM4 and COM5 are ON.
1	1	0	0	0	LCD Segment corresponding to COM1 and COM2 are ON.
1	1	0	0	1	LCD Segment corresponding to COM1, COM2 and COM5 are ON.
1	1	0	1	0	LCD Segment corresponding to COM1, COM2 and COM4 are ON.
1	1	0	1	1	LCD Segment corresponding to COM1, COM2, COM4 and COM5 are ON.
1	1	1	0	0	LCD Segment corresponding to COM1, COM2 and COM3 are ON.
1	1	1	0	1	LCD Segment corresponding to COM1, COM2, COM3 and COM5 are ON.
1	1	1	1	0	LCD Segment corresponding to COM1, COM2, COM3 and COM4 are ON.
1	1	1	1	1	LCD Segment corresponding to COM1, COM2, COM3, COM4 and COM5 are ON.

## 2.1/5 duty Slave

Output Pin <sup>(Note17)</sup>	COM1	COM2	COM3	COM4	COM5
S1/P1/G1	D1	D2	D3	D4	D5
S2/P2/G2	D6	D7	D8	D9	D10
S3/P3/G3	D11	D12	D13	D14	D15
S4/P4/G4	D16	D17	D18	D19	D20
S5/P5/G5	D21	D22	D23	D24	D25
S6/P6/G6	D26	D27	D28	D29	D30
S7/P7/G7	D31	D32	D33	D34	D35
S8/P8/G8	D36	D37	D38	D39	D40
S9/P9/G9	D41	D42	D43	D44	D45
S10	D46	D47	D48	D49	D50
S11	D51	D52	D53	D54	D55
S12	D56	D57	D58	D59	D60
S13	D61	D62	D63	D64	D65
S14	D66	D67	D68	D69	D70
S15	D71	D72	D73	D74	D75
S16	D76	D77	D78	D79	D80
S17	D81	D82	D83	D84	D85
S18	D86	D87	D88	D89	D90
S19	D91	D92	D93	D94	D95
S20	D96	D97	D98	D99	D100
S21	D101	D102	D103	D104	D105
S22	D106	D107	D108	D109	D110
S23	D111	D112	D113	D114	D115
S24	D116	D117	D118	D119	D120
S25	D121	D122	D123	D124	D125
S26	D126	D127	D128	D129	D130
S27	D131	D132	D133	D134	D135
S28	D136	D137	D138	D139	D140
S29	D141	D142	D143	D144	D145
S30	D146	D147	D148	D149	D150
S31	D151	D152	D153	D154	D155
S32	D156	D157	D158	D159	D160
S33	D161	D162	D163	D164	D165
S34	D166	D167	D168	D169	D170
S35	D171	D172	D173	D174	D175
S36	D176	D177	D178	D179	D180
S37	D181	D182	D183	D184	D185
S38	D186	D187	D188	D189	D190
S39	D191	D192	D193	D194	D195
S40	D196	D197	D198	D199	D200
S41	D201	D202	D203	D204	D205
S42	D206	D207	D208	D209	D210
S43	D211	D212	D213	D214	D215
S44	D216	D217	D218	D219	D220
S45	D221	D222	D223	D224	D225
S46	D226	D227	D228	D229	D230
S47	D231	D232	D233	D234	D235
S48	D236	D237	D238	D239	D240
S49	D241	D242	D243	D244	D245
S50	D246	D247	D248	D249	D250
S51	D251	D252	D253	D254	D255
S52	D256	D257	D258	D259	D260
S53	D261	D262	D263	D264	D265
S54	D266	D267	D268	D269	D270
S55	D271	D272	D273	D274	D275
S56	D276	D277	D278	D279	D280
S57	D281	D282	D283	D284	D285
S58	D286	D287	D288	D289	D290
S59	D291	D292	D293	D294	D295
S60	D296	D297	D298	D299	D300
S61	D301	D302	D303	D304	D305
S62	D306	D307	D308	D309	D310
S63	D311	D312	D313	D314	D315