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LCD Segment Drivers

Multi-function LCD Segment Drivers

BU97550KV-M **MAX 528 Segment(66SEG x 8COM)**

General Description

The BU97550KV-M is 1/8, 1/7, 1/5, 1/4, 1/3, or Static general-purpose LCD driver.
The BU97550KV-M can drive up to 528 LCD Segments directly. The BU97550KV-M can also control up to 9 General-Purpose/PWM output ports.
These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring

Key Specifications

- Supply Voltage Range: +2.7V to +6.0V
- Operating Temperature Range: -40°C to +85°C
- Max Segments: 528 Segments
- Display Duty Static, 1/3, 1/4, 1/5, 1/7, 1/8 Selectable
- Bias: 1/2, 1/3, 1/4 Selectable
- Interface: 3wire Serial Interface

Features

- AEC-Q100 Qualified (Note)
- Key Input Function for Up to 30 Keys (A key scan is performed only when a key is pressed.)
- Either 1/8, 1/7, 1/5, 1/4, 1/3 or Static
  Can be Selected with The Serial Control Data.
  1/8 duty drive: Up to 528 Segments can be driven
  1/7 duty drive: Up to 469 Segments can be driven
  1/5 duty drive: Up to 345 Segments can be driven
  1/4 duty drive: Up to 280 Segments can be driven
  1/3 duty drive: Up to 210 Segments can be driven
  Static drive: Up to 70 Segments can be driven
- Serial Data Control of Frame Frequency for Common and Segment output Waveforms.
- Serial Data Control of Switching Between The Segment output Port, PWM output Port and General-Purpose output Port Functions.(Max 9 ports)
- Built-in Oscillation circuit
- Integrated Voltage Detected Type Power on Reset(VDET) circuit
- No External Component
- Low Power Consumption Design
- Supports Line and Frame Inversion

(Note) Grade 3

Applications

- Car Audio, Home Electrical Appliance, Meter Equipment etc.

Package

W (Typ) x D (Typ) x H (Max)

VQFP80
14.00mm x 14.00mm x 1.60mm

Typical Application Circuit

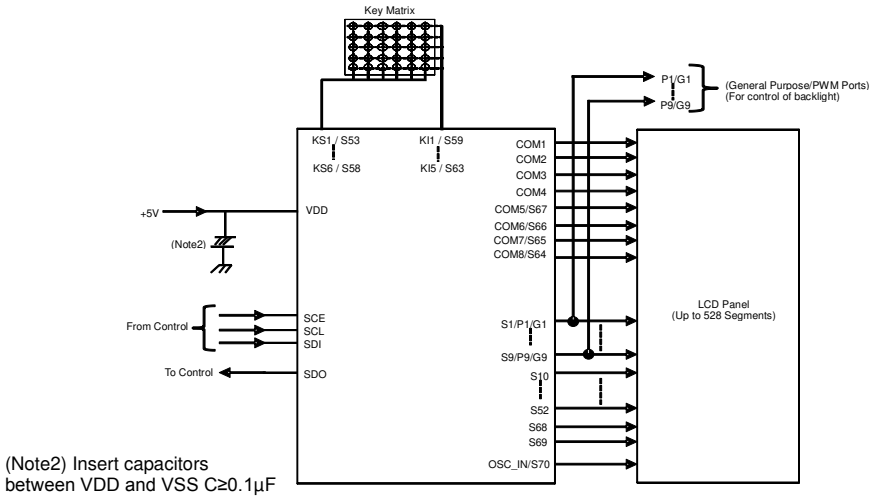


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

Block Diagram

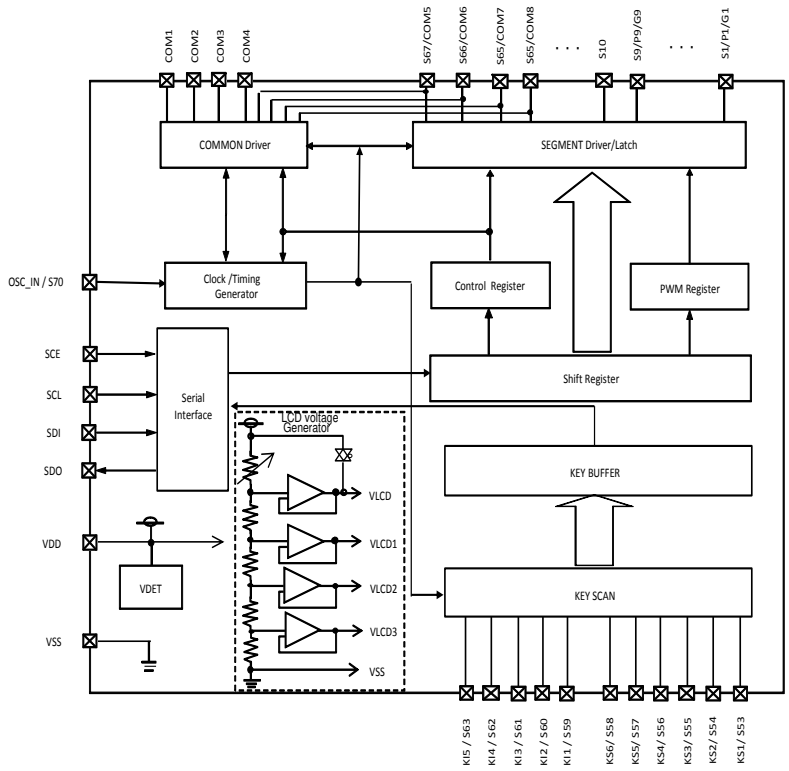


Figure 2. Block Diagram

Pin Arrangement

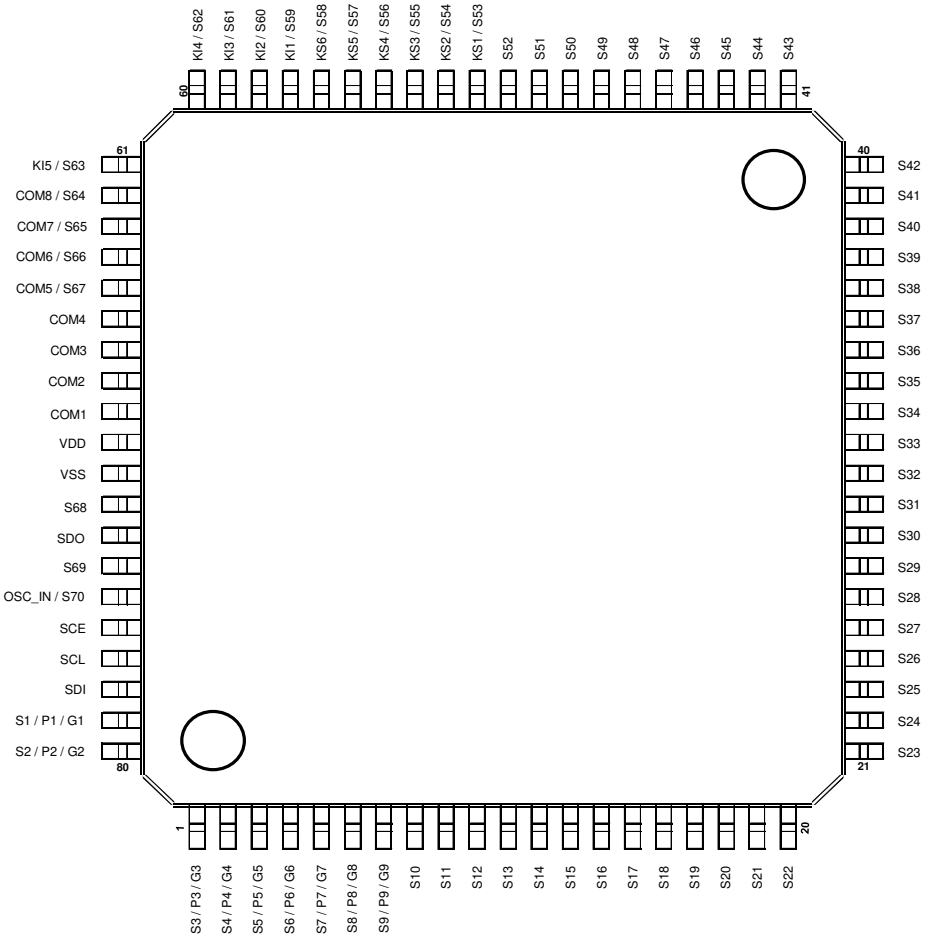


Figure 3. Pin Configuration (TOP VIEW)

Absolute Maximum Ratings (VSS = 0V)

Parameter	Symbol	Pin	Rating	Unit
Maximum Supply Voltage	VDD	VDD	-0.3 to +7.0	V
Input Voltage	V_{IN1}	SCE, SCL, SDI	-0.3 to +7.0	V
	V_{IN2}	KI1 to KI5	-0.3 to +7.0	V
Allowable Loss	Pd		1.2 (Note3)	W
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-55 to +125	°C

(Note3) When use more than Ta=25°C, subtract 12mW per degree. (Using ROHM standard board)
(Board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommend Operating Conditions (Ta = -40°C to +85°C, VSS = 0V)

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
Supply Voltage	VDD		2.7	5.0	6.0	V

Electrical Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Hysteresis	V_{H1}	SCE, SCL, SDI		-	0.03 VDD	-	V
	V_{H2}	KI1 to KI5		-	0.1 VDD	-	
Power-on Detection Voltage	V_{DET}	VDD		1.3	1.8	2.2	V
"H" Level Input Voltage	V_{IH1}	SCE, SCL, SDI	4.5V ≤ VDD ≤ 6.0V	0.4VDD	-	VDD	V
	V_{IH2}	SCE, SCL, SDI	2.7V ≤ VDD < 4.5V	0.8VDD	-	VDD	
	V_{IH3}	KI1 to KI5		0.7VDD	-	VDD	
"L" Level Input Voltage	V_{IL1}	SCE, SCL, SDI KI1 to KI5		0	-	0.2VDD	V
Input Floating Voltage	V_{IF}	KI1 to KI5		-	-	0.05VDD	V
Pull-down Resistance	R_{PD}	KI1 to KI5	VDD=5.0V	50	100	250	kΩ
Output Off Leakage Current	I_{OFFH}	SDO	V_O=6.0V	-	-	6.0	µA
"H" Level Input Current	I_{IH1}	SCE, SCL, SDI	V_I = 5.5V	-	-	5.0	µA
"L" Level Input Current	I_{IL1}	SCE, SCL, SDI	V_I = 0V	-5.0	-	-	µA
"H" Level Output Voltage	V_{OH1}	S1 to S70	I_O = -20µA, VLCD=1.00*VDD	VDD-0.9	-	-	V
	V_{OH2}	COM1 to COM8	I_O = -100µA, VDD=1.00*VDD	VDD-0.9	-	-	
	V_{OH3}	P1/G1 to P9/G9	I_O = -1mA	VDD-0.9	-	-	
	V_{OH4}	KS1 to KS6	I_O = -500µA	VDD-1.0	VDD-0.5	VDD-0.2	
"L" Level Output Voltage	V_{OL1}	S1 to S70	I_O = 20µA	-	-	0.9	V
	V_{OL2}	COM1 to COM8	I_O = 100µA	-	-	0.9	
	V_{OL3}	P1/G1 to P9/G9	I_O = 1mA	-	-	0.9	
	V_{OL4}	KS1 to KS6	I_O = 25µA	0.2	0.5	1.5	
	V_{OL5}	SDO	I_O = 1mA	-	0.1	0.5	
Middle Level Output Voltage	V_{MID1}	S1 to S70	1/2 bias I_O = ±20µA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	V
	V_{MID2}	COM1 to COM8	1/2 bias I_O = ±100µA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	
	V_{MID3}	S1 to S70	1/3 bias I_O = ±20µA VLCD=1.00*VDD	2/3 VDD -0.9	-	2/3 VDD +0.9	
	V_{MID4}	S1 to S70	1/3 bias I_O = ±20µA VLCD=1.00*VDD	1/3 VDD -0.9	-	1/3 VDD +0.9	
	V_{MID5}	COM1 to COM8	1/3 bias I_O = ±100µA VLCD=1.00*VDD	2/3 VDD -0.9	-	2/3 VDD +0.9	
	V_{MID6}	COM1 to COM8	1/3 bias I_O = ±100µA VLCD=1.00*VDD	1/3 VDD -0.9	-	1/3 VDD +0.9	
	V_{MID7}	S1 to S70	1/4 bias I_O = ±20µA VLCD=1.00*VDD	1/2 VDD -0.9	-	1/2 VDD +0.9	
	V_{MID8}	COM1 to COM8	1/4 bias I_O = ±100µA VLCD=1.00*VDD	3/4 VDD -0.9	-	3/4 VDD +0.9	
	V_{MID9}	COM1 to COM8	1/4 bias I_O = ±100µA VLCD=1.00*VDD	1/4 VDD -0.9	-	1/4 VDD +0.9	

Electrical Characteristics – continued

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Current Consumption	I_{DD1}	VDD	Power-saving mode	-	-	15	µA
	I_{DD2}	VDD	VDD = 5.0V Output open, 1/2 bias Frame frequency=80Hz VLCD=1.00*VDD	-	105	220	
	I_{DD3}	VDD	VDD = 5.0V Output open,1/3 bias Frame frequency=80Hz VLCD=1.00*VDD	-	130	270	
	I_{DD4}	VDD	VDD = 5.0V Output open,1/4 bias Frame frequency=80Hz VLCD=1.00*VDD	-	160	330	

Oscillation Characteristics (Ta = -40 to +85°C, VDD = 2.7V to 6.0V, VSS = 0.0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
scillator Frequency 1	f_{OSC1}	-	VDD = 2.7V to 6.0V	300	-	720	kHz
Oscillator Frequency 2	f_{OSC2}	-	VDD = 5.0V	540	600	660	kHz
Oscillator Frequency 3	f_{OSC3}	-	VDD = 6.0V	562	625	688	kHz
External Clock Frequency(Note4)	f_{OSC4}	OSC_IN/S70	External clock mode (OC=1)	30	-	1000	kHz
External Clock Rise Time	tr			-	160	-	ns
External Clock Fall Time	tf			-	160	-	ns
External Clock Duty	t_{DTY}			30	50	70	%

(Note4) Frame frequency is decided external frequency and dividing ratio of FC0 to FC3 setting.

[Reference Data]

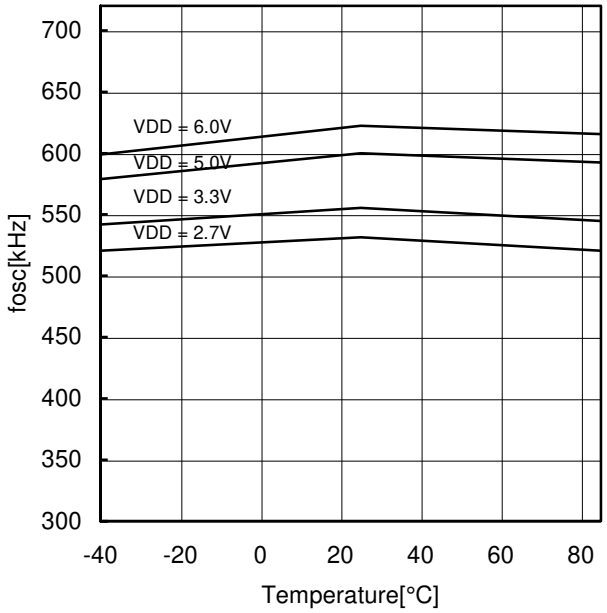
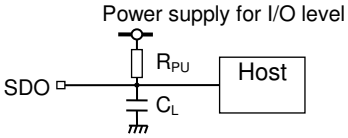


Figure 4. Frame Frequency Typical Temperature Characteristics

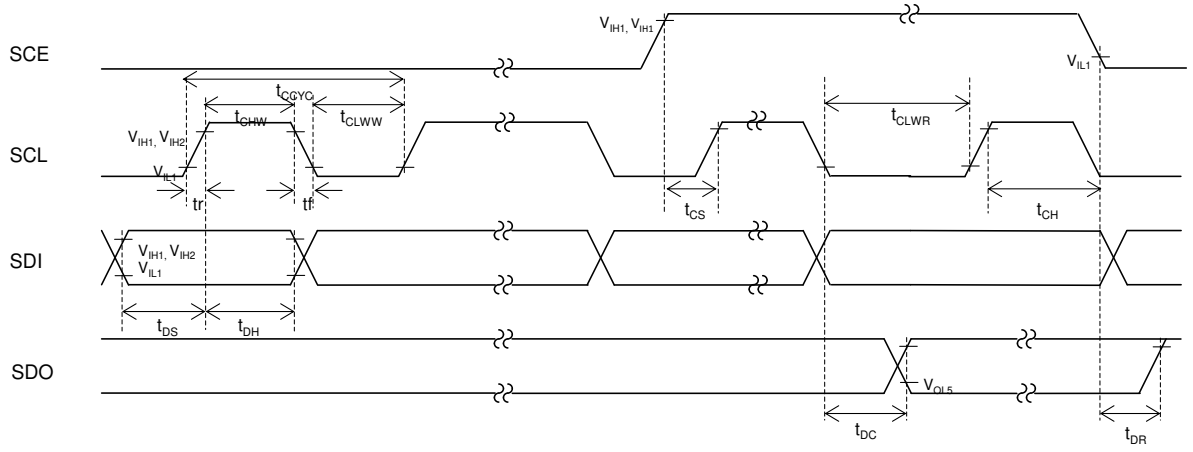
MPU Interface Characteristics (Ta=-40 to +85°C, VDD = 2.7V to 6.0V, VSS=0V)

Parameter	Symbol	Pin	Conditions	Limit			Unit
				Min	Typ	Max	
Data Setup Time	t_{DS}	SCL, SDI		120	-	-	ns
Data Hold Time	t_{DH}	SCL, SDI		120	-	-	ns
SCE Wait Time	t_{CP}	SCE, SCL		120	-	-	ns
SCE Setup Time	t_{CS}	SCE, SCL		120	-	-	ns
SCE Hold Time	t_{CH}	SCE, SCL		120	-	-	ns
Clock Cycle Time	t_{CCYC}	SCL		320	-	-	ns
High-level Clock Pulse Width	t_{CHW}	SCL		120	-	-	ns
Low-level Clock Pulse Width (Write)	t_{CLWW}	SCL		120	-	-	ns
Low-level Clock Pulse Width (Read)	t_{CLWR}	SCL	R_{PU}=4.7kΩ C_L=10pF(Note5)	1.6	-	-	µs
Rise Time	tr	SCE, SCL, SDI		-	160	-	ns
Fall Time	tf	SCE, SCL, SDI		-	160	-	ns
SDO Output Delay Time	t_{DC}	SDO	R_{PU}=4.7kΩ C_L=10pF(Note5)	-	-	1.5	µs
SDO Rise Time	t_{DR}	SDO	R_{PU}=4.7kΩ C_L=10pF(Note5)	-	-	1.5	µs

(Note5) Since SDO is an open-drain output, "t_{DC}" and "t_{DR}" depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.
R_{PU}: 1kΩ≤RPU≤10kΩ is recommended.
C_L: A parasitic capacitance in an application circuit. Any component is not necessary to be attached.



1. When SCL is stopped at the low level



2. When SCL is stopped at the high level

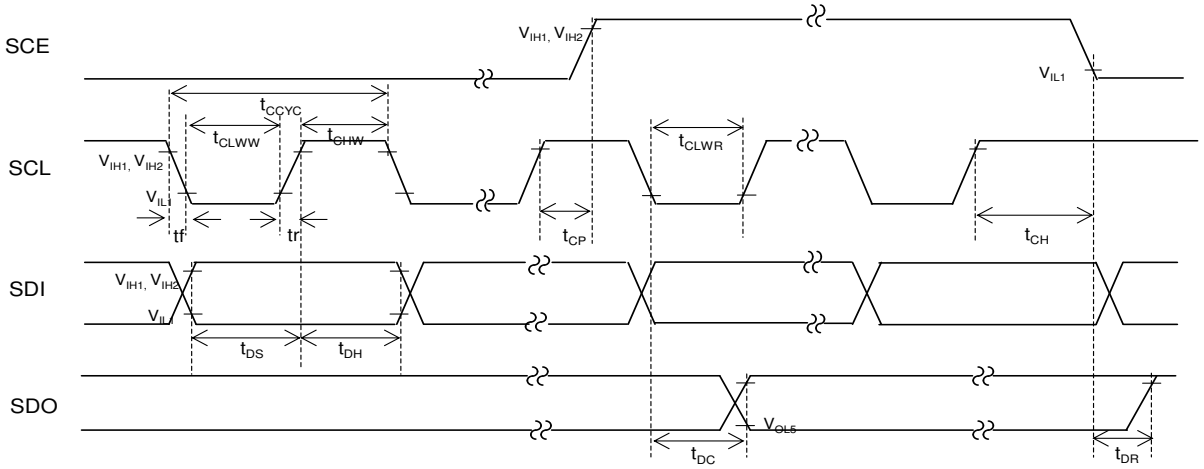


Figure 5. Serial Interface Timing

Pin Description

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1/G1 to S9/P9/G9	79,80, 1 to 7	Segment output for displaying the display data transferred by serial data input. The S1/P1/G1 to S9/P9/G9 pins can also be used as General-Purpose or PWM output when so set up by the control data.	-	O	OPEN
S10 to S52 S68, S69	8 to 50 72, 74	Segment output for displaying the display data transferred by serial data input.	-	O	OPEN
KS1/S53 to KS6/S58	51 to 56	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S53 to KS6/S58 pins can be used as Segment outputs when so specified by the control data.	-	O	OPEN
KI1/S59 to KI5/S63	57 to 61	Key scan inputs These pins have built-in pull-down resistors. The KI1/S59 to KI5/S63 pins can be used as Segment outputs when so specified by the control data.	-	I/O	OPEN
COM1 to COM4	66 to 69	Common driver output pins. The frame frequency is fo[Hz].	-	O	OPEN
COM5/S67 COM6/S66 COM7/S65 COM8/S64	65 64 63 62	Common / Segment output for LCD driving Assigned as Common output in 1/8, 1/7 and 1/5 Duty modes and Segment output in Static, 1/3 and 1/4 Duty modes.	-	O	OPEN
OSC_IN/S70	75	Segment output for displaying the display data transferred by serial data input. The OSC_IN/S70 pin can be used as external frequency input pin when set up by the control data.	-	I/O	OPEN
		Serial data transfer inputs. Must be connected to the controller.			
SCE	76	SCE: Chip enable	H	I	-
SCL	77	SCL: Synchronization clock	↑	I	-
SDI	78	SDI: Transfer data	-	I	-
SDO	73	Output data	-	O	OPEN
VDD	70	Power supply pin of the IC A power voltage of 2.7V to 6.0V must be applied to this pin.	-	-	-
VSS	71	Power supply pin. Must be connected to ground.	-	-	-

IO Equivalent Circuit

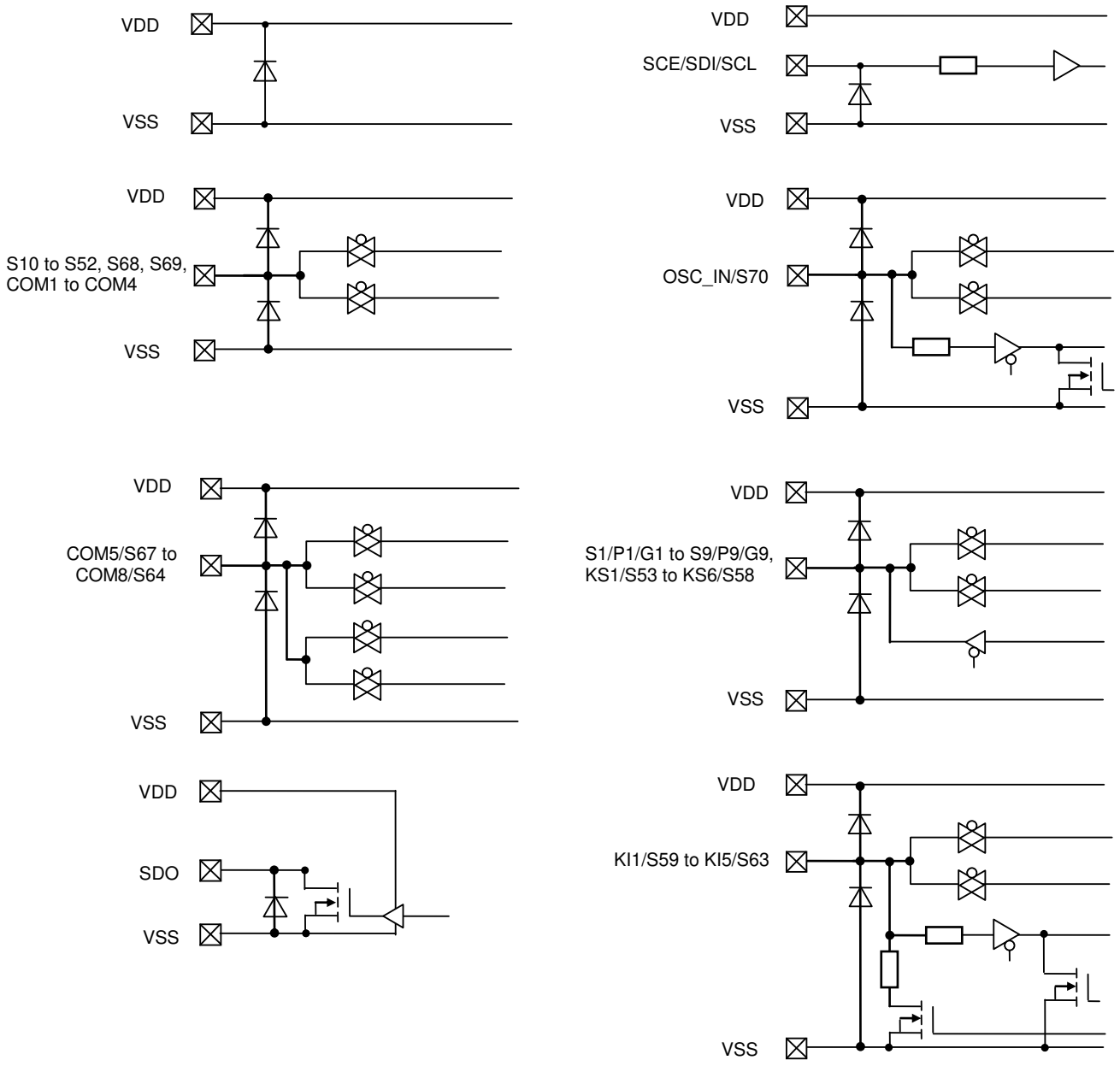
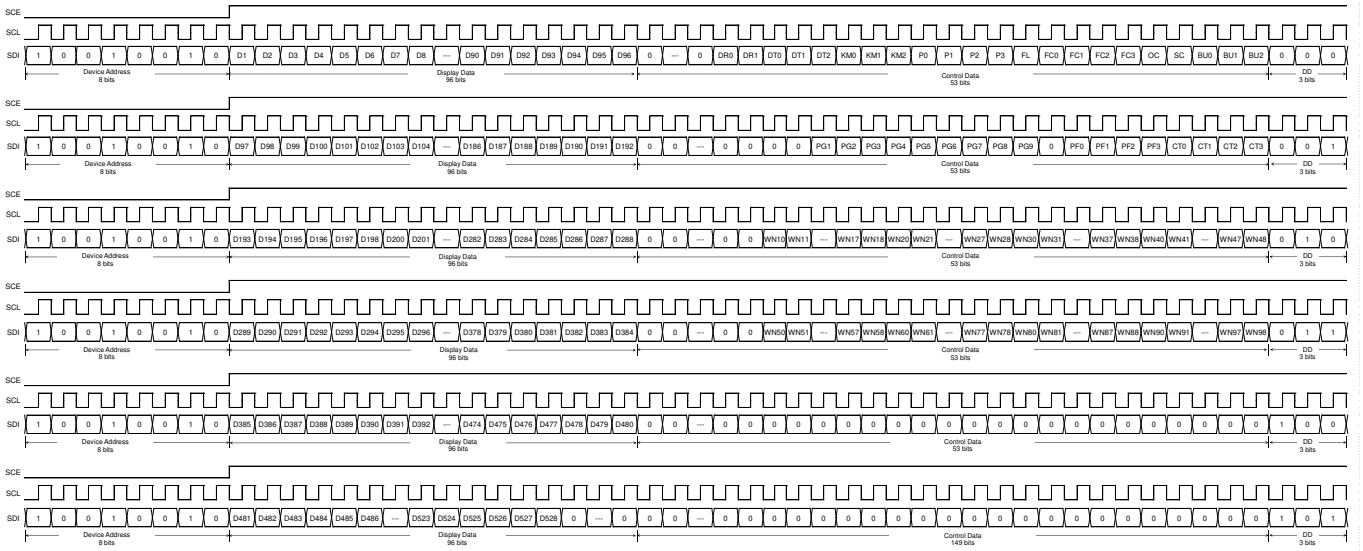


Figure 6. I/O Equivalent Circuit

Serial Data Transfer Formats

1. 1/8 Duty

(1) When SCL is stopped at the low level



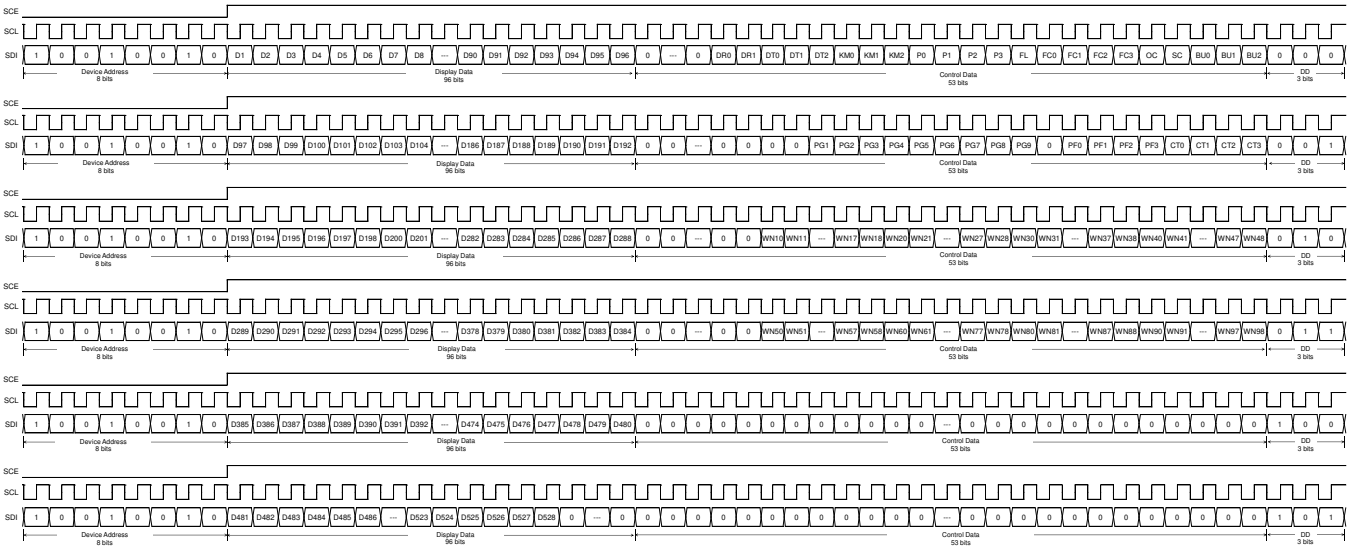
(Note6)

Figure 7. 3-SPI Data Transfer Format

(Note6) DD is direction data.

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note7)

Figure 8. 3-SPI Data Transfer Format

(Note7) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D528……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38,W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

Serial Data Transfer Formats – continued

2. 1/7 Duty

(1) When SCL is stopped at the low level

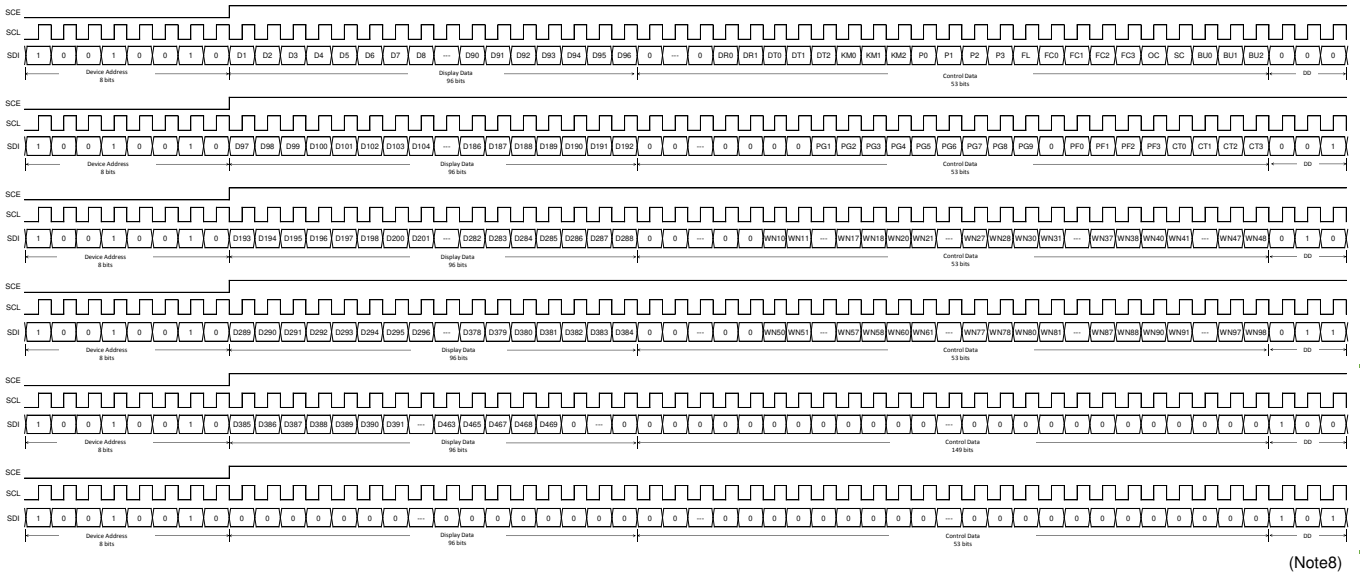
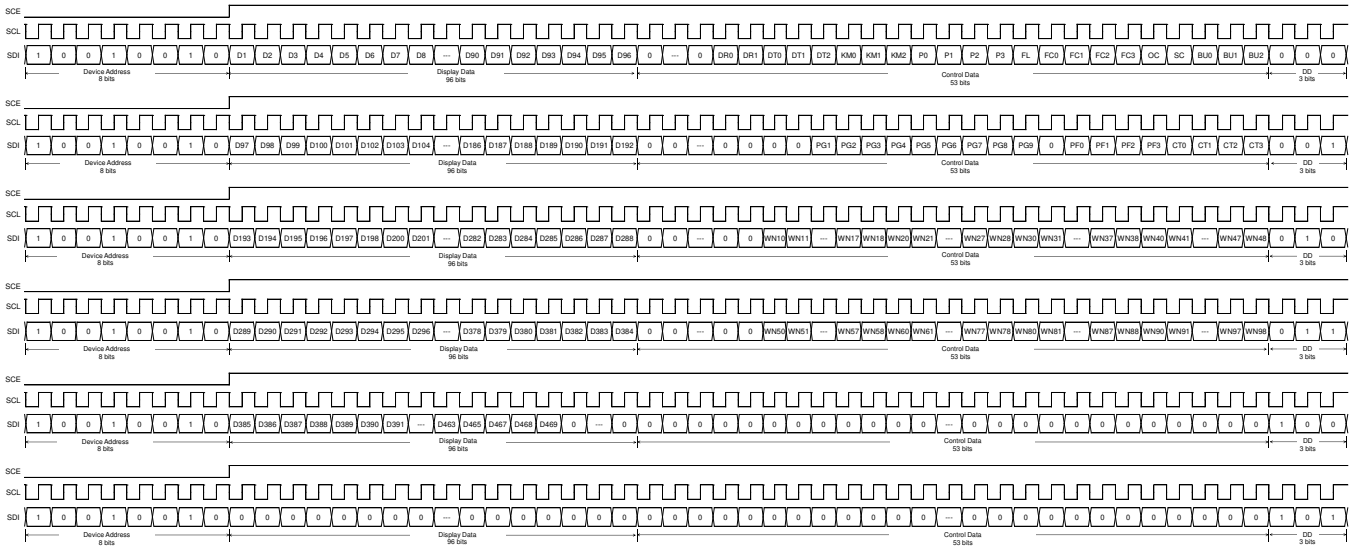


Figure 9. 3-SPI Data Transfer Format

(Note8) DD is direction data.

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note9)

Figure 10. 3-SPI Data Transfer Format

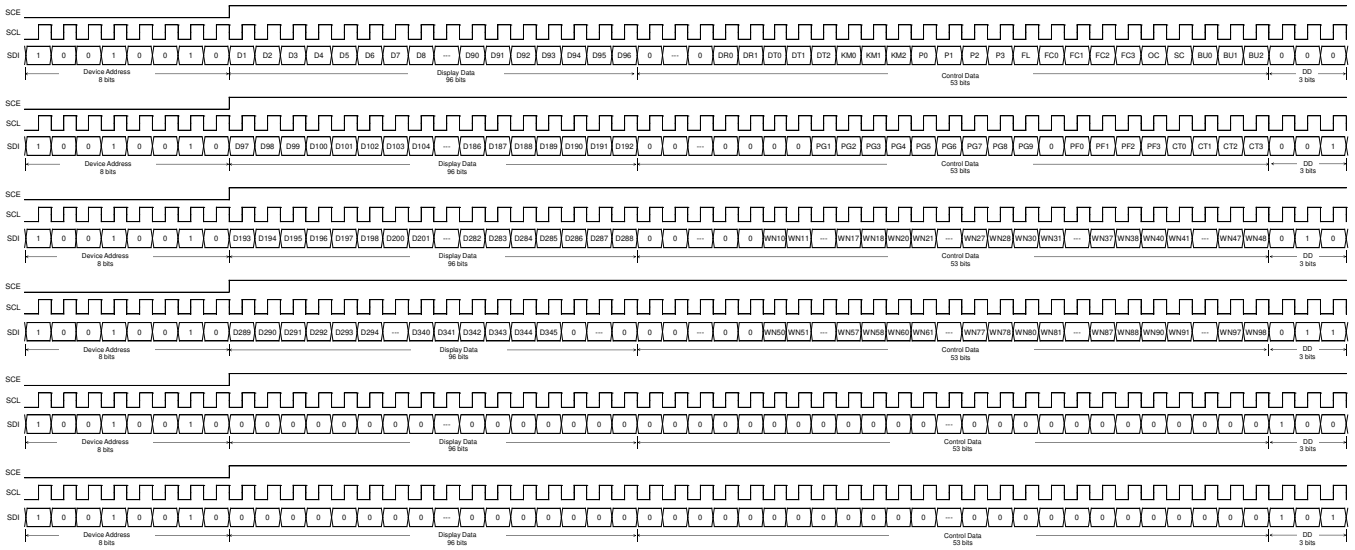
(Note9) DD is direction data.

Device code ·····”49H”
KM0 to KM2 ·····Key Scan output port/Segment output port switching control data
D1 to D469·····Display data
P0 to P3 ·····Segment/PWM/General-Purpose output port switching control data
FL ·····Line Inversion or Frame Inversion switching control data
DR0 to DR1·····1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ·····1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ·····Common/Segment output waveform frame frequency setting control data
OC ·····Internal oscillator operating mode/External clock operating mode switching control data
SC·····Segment on/off control data
BU0 to BU2·····Normal mode/Power-saving mode control data
PG1 to PG9·····PWM/General-Purpose output port select data
PF0 to PF3·····PWM output waveform frame frequency setting control data.
CT0 to CT3 ·····LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38,W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ·····PWM output duty setting control data

Serial Data Transfer Formats – continued

3. 1/5 Duty

(1) When SCL is stopped at the low level



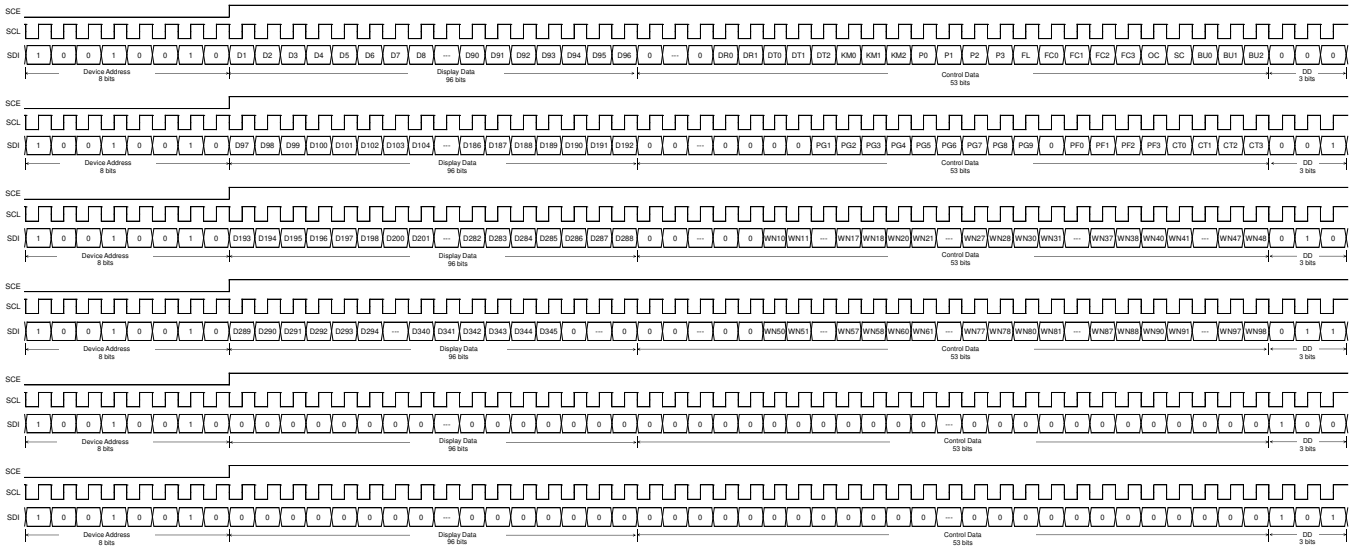
(Note10)

Figure 11. 3-SPI Data Transfer Format

(Note10) DD is direction data.

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note11)

Figure 12. 3-SPI Data Transfer Format

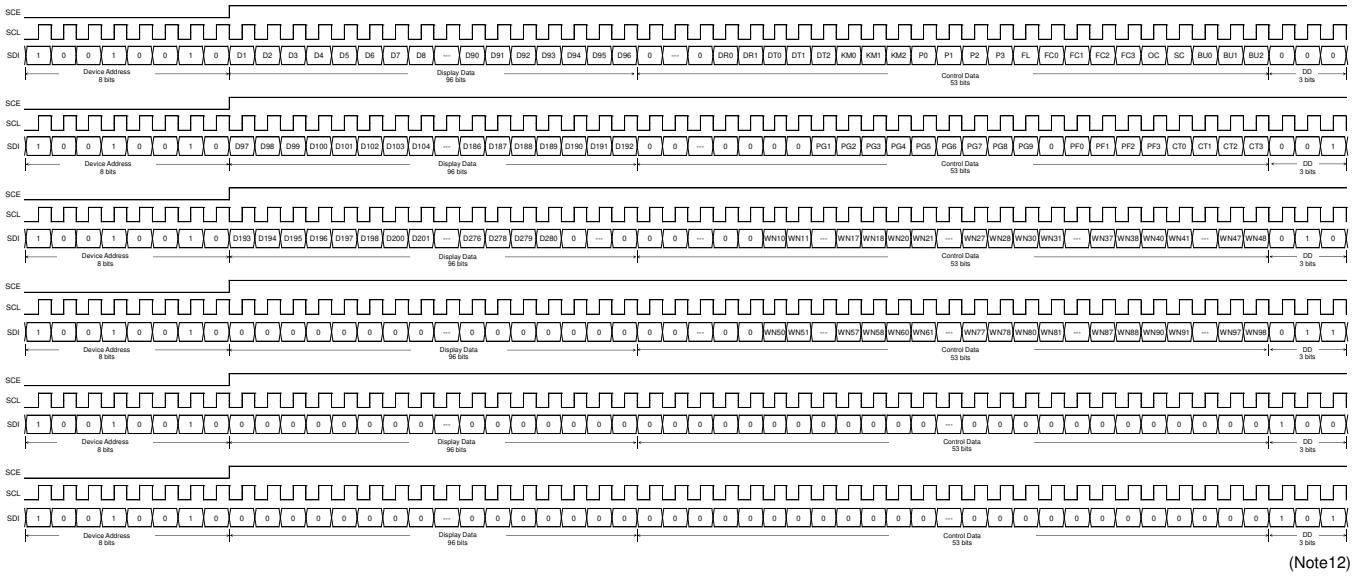
(Note11) DD is direction data.

Device code ·····”49H”
KM0 to KM2 ·····Key Scan output port/Segment output port switching control data
D1 to D345·····Display data
P0 to P3 ·····Segment/PWM/General-Purpose output port switching control data
FL ·····Line Inversion or Frame Inversion switching control data
DR0 to DR1·····1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ·····1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ·····Common/Segment output waveform frame frequency setting control data
OC ·····Internal oscillator operating mode/External clock operating mode switching control data
SC·····Segment on/off control data
BU0 to BU2·····Normal mode/Power-saving mode control data
PG1 to PG9·····PWM/General-Purpose output port select data
PF0 to PF3·····PWM output waveform frame frequency setting control data.
CT0 to CT3 ·····LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ·····PWM output duty setting control data

Serial Data Transfer Formats – continued

4. 1/4 Duty

(1) When SCL is stopped at the low level



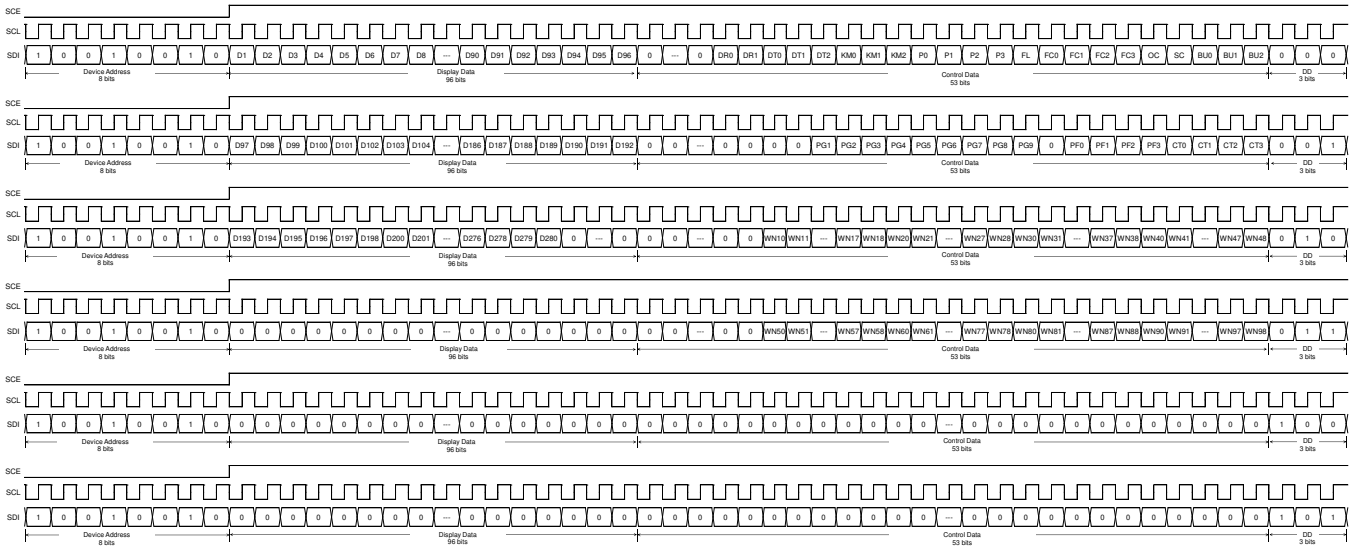
(Note12)

Figure 13. 3-SPI Data Transfer Format

(Note12) DD is direction data.

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note13)

Figure 14. 3-SPI Data Transfer Format

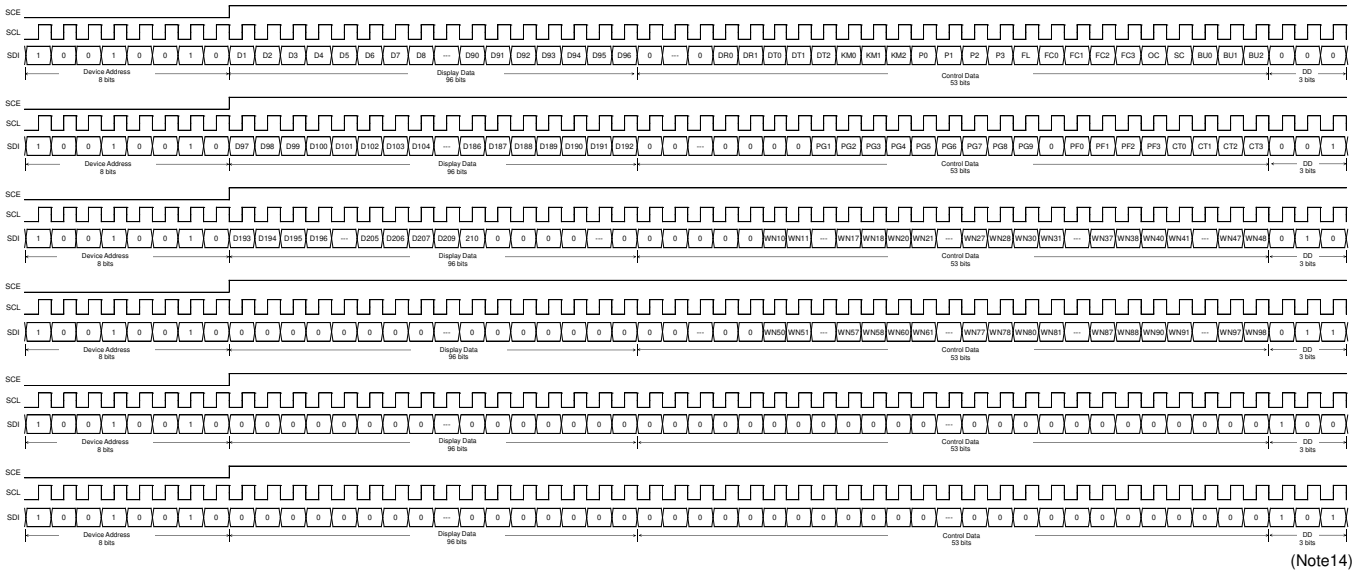
(Note13) DD is direction data.

Device code ·····”49H”
KM0 to KM2 ·····Key Scan output port/Segment output port switching control data
D1 to D280·····Display data
P0 to P3 ·····Segment/PWM/General-Purpose output port switching control data
FL ·····Line Inversion or Frame Inversion switching control data
DR0 to DR1·····1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ·····1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ·····Common/Segment output waveform frame frequency setting control data
OC ·····Internal oscillator operating mode/External clock operating mode switching control data
SC·····Segment on/off control data
BU0 to BU2·····Normal mode/Power-saving mode control data
PG1 to PG9·····PWM/General-Purpose output port select data
PF0 to PF3·····PWM output waveform frame frequency setting control data.
CT0 to CT3 ·····LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ·····PWM output duty setting control data

Serial Data Transfer Formats – continued

5. 1/3 Duty

(1) When SCL is stopped at the low level



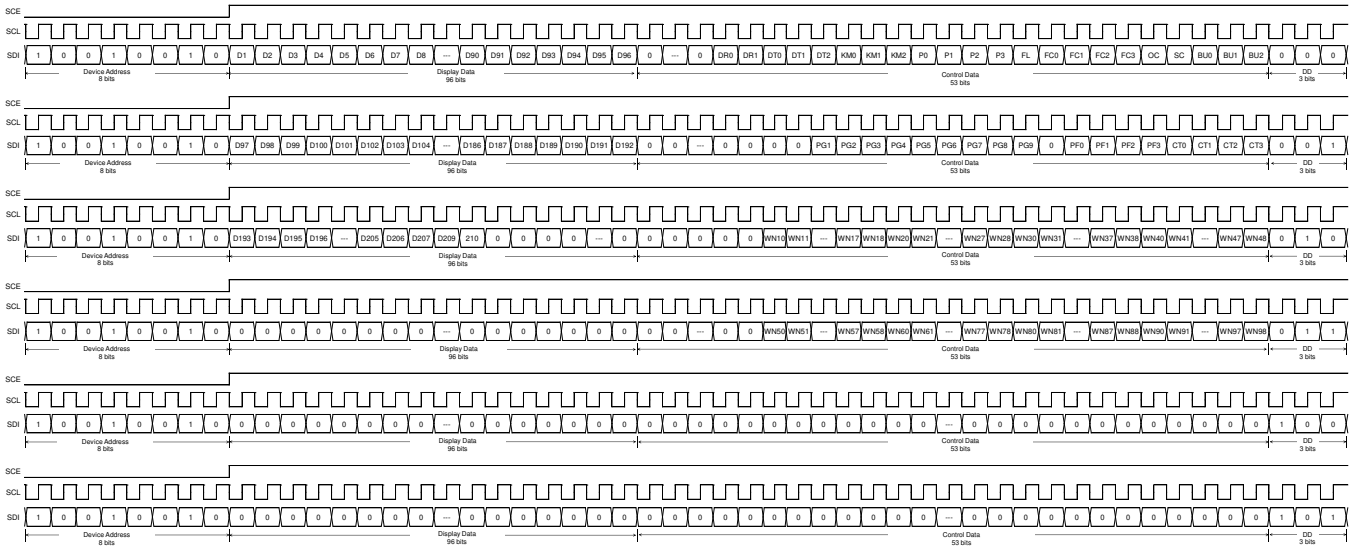
(Note14)

Figure 15. 3-SPI Data Transfer Format

(Note14) DD is direction data.

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note15)

Figure 16. 3-SPI Data Transfer Format

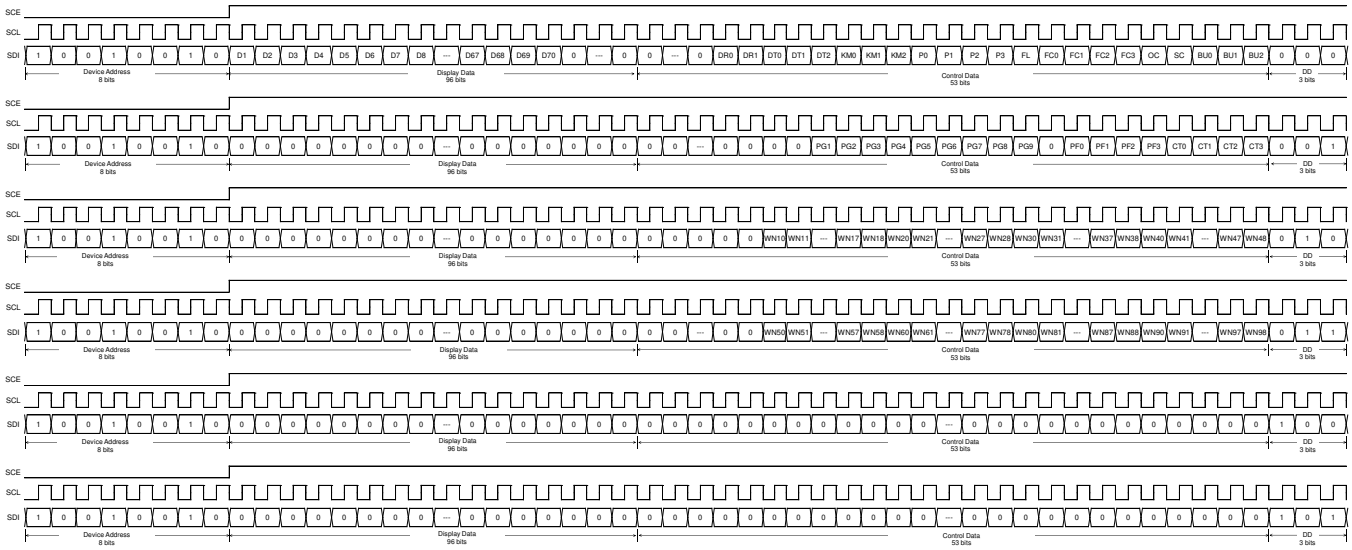
(Note15) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D210……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

Serial Data Transfer Formats – continued

6. Static

(1) When SCL is stopped at the low level



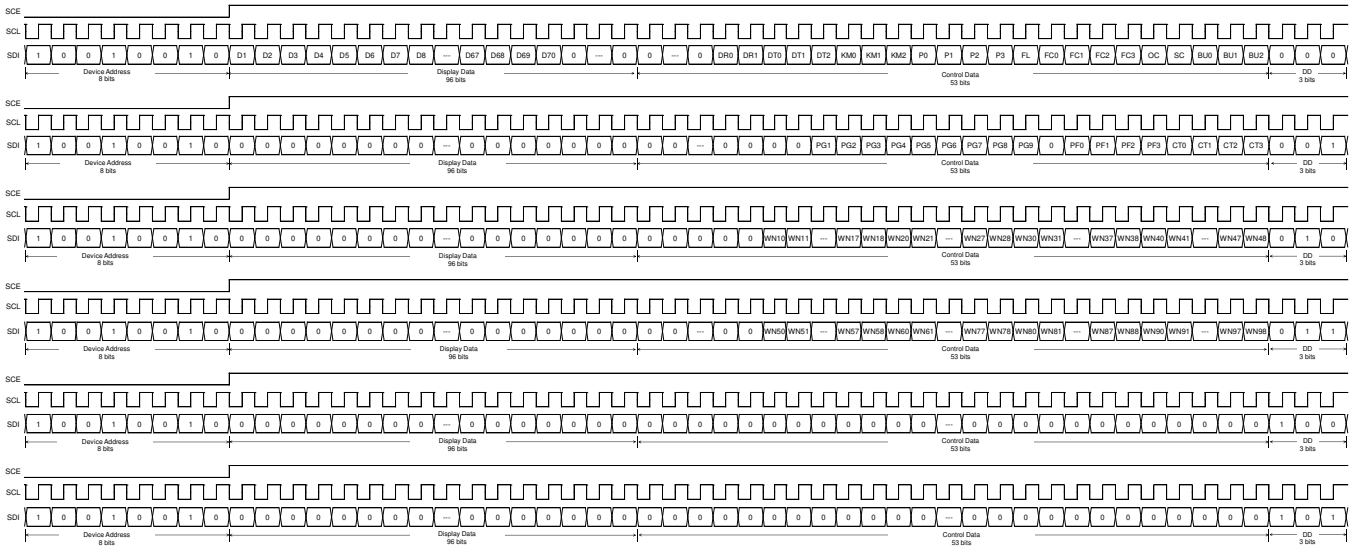
(Note16)

Figure 17. 3-SPI Data Transfer Format

(Note16) DD is direction data.

Serial Data Transfer Formats – continued

(2) When SCL is stopped at the high level



(Note17)

Figure 18. 3-SPI Data Transfer Format

(Note17) DD is direction data.

Device code ……”49H”
KM0 to KM2 ……Key Scan output port/Segment output port switching control data
D1 to D70 ……Display data
P0 to P3 ……Segment/PWM/General-Purpose output port switching control data
FL ……Line Inversion or Frame Inversion switching control data
DR0 to DR1……1/4 bias driver, 1/3 bias driver or 1/2 bias driver switching control data
DT0 to DT2 ……1/8-duty drive, 1/7-duty drive, 1/5-duty drive, 1/4-duty drive, 1/3-duty drive or Static drive switching control data
FC0 to FC3 ……Common/Segment output waveform frame frequency setting control data
OC ……Internal oscillator operating mode/External clock operating mode switching control data
SC……Segment on/off control data
BU0 to BU2……Normal mode/Power-saving mode control data
PG1 to PG9……PWM/General-Purpose output port select data
PF0 to PF3……PWM output waveform frame frequency setting control data.
CT0 to CT3 ……LCD bias voltage VLCD setting control data.
W10 to W18, W20 to W28, W30 to W38, W40 to W48, W50 to W58, W60 to W68, W70 to W78, W80 to W88, W90 to W98 ……PWM output duty setting control data

Control Data Functions

1. KM0, KM1 and KM2: Key Scan output port/Segment output port switching control data

These control data bits switch the functions of the KS1/S53 to KS6/S58 output pins between key scan output and Segment output.

KM0	KM1	KM2	Output Pin State						Maximum Number of Input keys	Reset condition
			KS1/S53	KS2/S54	KS3/S55	KS4/S56	KS5/S57	KS6/S58		
0	0	0	KS1	KS2	KS3	KS4	KS5	KS6	30	-
0	0	1	S53	KS2	KS3	KS4	KS5	KS6	25	-
0	1	0	S53	S54	KS3	KS4	KS5	KS6	20	-
0	1	1	S53	S54	S55	KS4	KS5	KS6	15	-
1	0	0	S53	S54	S55	S56	KS5	KS6	10	-
1	0	1	S53	S54	S55	S56	S57	KS6	5	-
1	1	0	S53	S54	S55	S56	S57	S58	0	-
1	1	1	S53	S54	S55	S56	S57	S58	0	○

2. P0, P1, P2 and P3: Segment/PWM/General-Purpose output port switching control data

These control bits are used to select the function of the S1/P1/G1 to S9/P9/G9 output Pins (Segment output Pins or PWM output Pins or General-Purpose output Pins).

P0	P1	P2	P3	S1/P1/G1	S2/P2/G2	S3/P3/G3	S4/P4/G4	S5/P5/G5	S6/P6/G6	S7/P7/G7	S8/P8/G8	S9/P9/G9	Reset condition
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
0	0	0	1	P1/G1	S2	S3	S4	S5	S6	S7	S8	S9	-
0	0	1	0	P1/G1	P2/G2	S3	S4	S5	S6	S7	S8	S9	-
0	0	1	1	P1/G1	P2/G2	P3/G3	S4	S5	S6	S7	S8	S9	-
0	1	0	0	P1/G1	P2/G2	P3/G3	P4/G4	S5	S6	S7	S8	S9	-
0	1	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	S6	S7	S8	S9	-
0	1	1	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	S7	S8	S9	-
0	1	1	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	S8	S9	-
1	0	0	0	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	S9	-
1	0	0	1	P1/G1	P2/G2	P3/G3	P4/G4	P5/G5	P6/G6	P7/G7	P8/G8	P9/G9	-
1	0	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	0	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	0	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	1	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	-
1	1	1	1	S1	S2	S3	S4	S5	S6	S7	S8	S9	○

PWM output or General-Purpose output is selected by PGx(x=1 to 9) control data bit.

When the General-Purpose output Port Function is selected, the correspondence between the output Pins and the respective display data is given in the table below.

Output Pins	Corresponding Display Data					
	1/8 Duty mode	1/7 Duty mode	1/5 Duty mode	1/4 Duty mode	1/3 Duty mode	Static
S1/P1/G1	D1	D1	D1	D1	D1	D1
S2/P2/G2	D9	D8	D6	D5	D4	D2
S3/P3/G3	D17	D15	D11	D9	D7	D3
S4/P4/G4	D25	D22	D16	D13	D10	D4
S5/P5/G5	D33	D29	D21	D17	D13	D5
S6/P6/G6	D41	D36	D26	D21	D16	D6
S7/P7/G7	D49	D43	D31	D25	D19	D7
S8/P8/G8	D57	D50	D36	D29	D22	D8
S9/P9/G9	D65	D57	D41	D33	D25	D9

When the General-Purpose output Port Function is selected, the respective output pin outputs a “H” level when its corresponding display data is set to “1”. Likewise, it will output a “L” level, if its corresponding display data is set to “0”. For example, at 1/4 Duty mode, S4/P4/G4 is used as a General-Purpose output Port, if its corresponding display data D13 is set to “1”, then S4/P4/G4 will output “H” level. Likewise, if D13 is set to “0”, then S4/P4/G4 will output “L” level.

3. FL: Line Inversion or Frame Inversion switching control data

This control data bit selects either line inversion mode or frame inversion mode.

FL	Inversion mode	Reset condition
0	Line Inversion	○
1	Frame Inversion	-

Control Data Functions – continued

4. DR: 1/4 bias drive, 1/3 bias drive, 1/2 bias drive or 1/1 bias drive switching control data
This control data bit selects either 1/4 bias drive, 1/3 bias drive, 1/2 bias drive or 1/1 bias drive.

DR0	DR1	Bias drive scheme	Reset condition
0	0	1/3 Bias	○
0	1	1/1 Bias	-
1	0	1/4 Bias	-
1	1	1/2 Bias	-

5. DT: 1/8 duty drive, 1/7 duty drive, 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or Static switching control data
These control data bits select either 1/8 duty drive, 1/7 duty drive, 1/5 duty drive, 1/4 duty drive, 1/3 duty drive or Static

DT0	DT1	DT2	Duty drive scheme	Reset condition
0	0	0	Static drive	-
0	0	1	1/3 duty drive	-
0	1	0	1/4 duty drive	○
0	1	1	1/5 duty drive	-
1	0	0	1/7 duty drive	-
1	0	1	1/8 duty drive	-
1	1	0	1/4 duty drive	-
1	1	1	1/4 duty drive	-

6. FC0, FC1, FC2 and FC3: Common/Segment output waveform frame frequency setting control data
These control data bits set the frame frequency for Common and Segment output waveforms.

FC0	FC1	FC2	FC3	Frame Frequency fo(Hz)	Reset condition
0	0	0	0	fosc(Note18) / 12288	○
0	0	0	1	fosc / 10752	-
0	0	1	0	fosc / 9216	-
0	0	1	1	fosc / 7680	-
0	1	0	0	fosc / 6144	-
0	1	0	1	fosc / 4608	-
0	1	1	0	fosc / 3840	-
0	1	1	1	fosc / 3072	-
1	0	0	0	fosc / 2880	-
1	0	0	1	fosc / 2688	-
1	0	1	0	fosc / 2496	-
1	0	1	1	fosc / 2304	-
1	1	0	0	fosc / 2112	-
1	1	0	1	fosc / 1920	-
1	1	1	0	fosc / 1728	-
1	1	1	1	fosc / 1536	-

(Note18)fosc: Internal Oscillation Frequency (600 [kHz] Typ)

Control Data Functions – continued

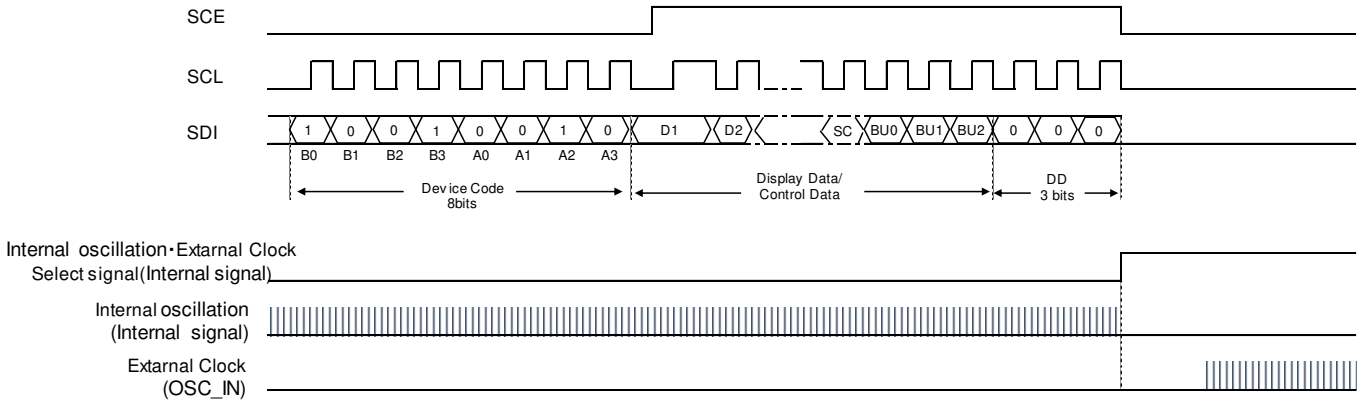
7. OC: Internal oscillator operating mode/External clock operating mode switching control data

This control data bit selects oscillation mode.

OC	Operating mode	In/Out pin(OSC/S70) status	Reset condition
0	Internal oscillator	S70 (Segment output)	○
1	External Clock	OSC_IN (clock input)	-

<External Clock input timing function>

Internal oscillation / external clock select signal behavior is below.
Input external clock after serial data sending.



8. SC: Segment on/off control data

This control data bit controls the on/off state of the Segments.

SC	Display state	Reset condition
0	ON	-
1	OFF	○

Note that when the Segments are turned off by setting SC to “1”, the Segments are turned off by outputting Segment off waveforms from the Segment output pins.

Control Data Functions – continued

9. BU0, BU1 and BU2: Normal mode/Power-saving mode control data

These control data bits select either normal mode or Power-saving mode.

BU0	BU1	BU2	Mode	OSC Oscillator	Segment outputs	Output Pin States During Key Scan Standby						Reset condition
					Common outputs	KS1	KS2	KS3	KS4	KS5	KS6	
0	0	0	Normal	Operating	Operating	H	H	H	H	H	H	-
0	0	1	Power-saving	Stopped	Low(VSS)	L	L	L	L	L	H	-
0	1	0				L	L	L	L	H	H	-
0	1	1				L	L	L	H	H	H	-
1	0	0				L	L	H	H	H	H	-
1	0	1				L	H	H	H	H	H	-
1	1	0				H	H	H	H	H	H	-
1	1	1				H	H	H	H	H	H	○

Power-saving mode status: S1/P1/G1 to S9/P9/G9 = active only General-Purpose output
S10 to OSC_IN/S70 = low (VSS)
COM1 to COM8 = low (VSS)
Shut off current to the LCD drive bias voltage generation circuit
Stop the Internal oscillation circuit
However, serial data transfer is possible when at Power-saving mode.

10. PG1, PG2, PG3, PG4, PG5, PG6, PG7, PG8 and PG9: PWM/ General-Purpose output port control data

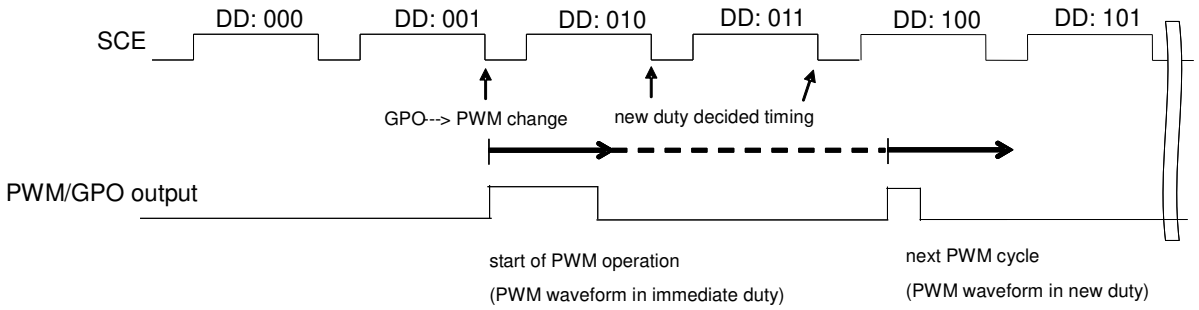
This control data bit select either PWM output or General-Purpose output of Sx/Px/Gx pins. (x=1 to 9)

PGx(x=1 to 9)	Mode	Reset condition
0	PWM output	○
1	General-Purpose output	-

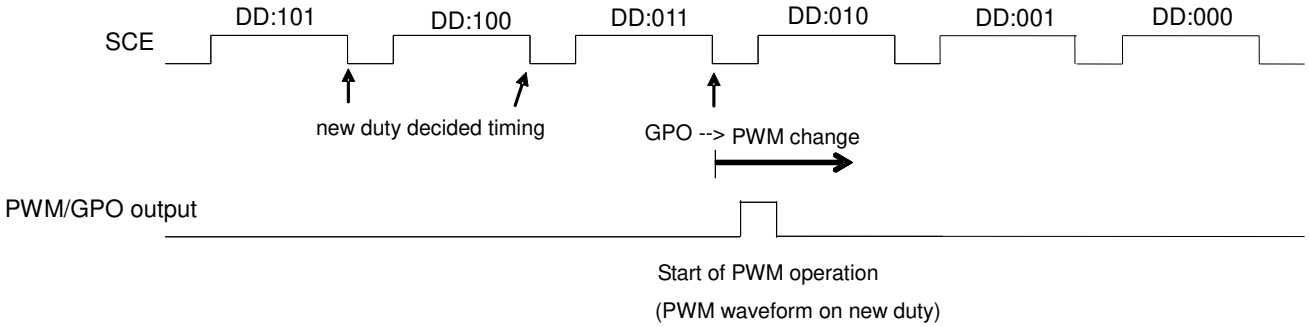
[PWM<->GPO Changing function]

Normal behavior of changing GPO to PWM is below.

- PWM operation is started by command import timing of DD: 001 during GPO → PWM change.
- Please take care of reflect timing of new duty setting of DD: 010 and DD: 011 is from the next PWM.



In order to avoid this operation, please input commands in reverse as below.



Control Data Functions – continued

11. PF0, PF1, PF2, and PF3: PWM output waveform frame frequency setting control data

These control data bits set the frame frequency for PWM output waveforms.

PF0	PF1	PF2	PF3	PWM output Frame Frequency fp(Hz)	Reset condition
0	0	0	0	fosc / 4096	○
0	0	0	1	fosc / 3840	-
0	0	1	0	fosc / 3584	-
0	0	1	1	fosc / 3328	-
0	1	0	0	fosc / 3072	-
0	1	0	1	fosc / 2816	-
0	1	1	0	fosc / 2560	-
0	1	1	1	fosc / 2304	-
1	0	0	0	fosc / 2048	-
1	0	0	1	fosc / 1792	-
1	0	1	0	fosc / 1536	-
1	0	1	1	fosc / 1280	-
1	1	0	0	fosc / 1024	-
1	1	0	1	fosc / 768	-
1	1	1	0	fosc / 512	-
1	1	1	1	fosc / 256	-

Control Data Functions – continued

12. CT0, CT1, CT2 and CT3: Display Contrast setting control data

These control data bits set display contrast

CT0	CT1	CT2	CT3	LCD Drive bias voltage for VLCD Level	Reset condition
0	0	0	0	1.000*VDD	○
0	0	0	1	0.975*VDD	-
0	0	1	0	0.950*VDD	-
0	0	1	1	0.925*VDD	-
0	1	0	0	0.900*VDD	-
0	1	0	1	0.875*VDD	-
0	1	1	0	0.850*VDD	-
0	1	1	1	0.825*VDD	-
1	0	0	0	0.800*VDD	-
1	0	0	1	0.775*VDD	-
1	0	1	0	0.750*VDD	-
1	0	1	1	0.725*VDD	-
1	1	0	0	0.700*VDD	-
1	1	0	1	0.675*VDD	-
1	1	1	0	0.650*VDD	-
1	1	1	1	0.625*VDD	-

Avoid setting VLCD voltage under 2.5V.
And ensure “VDD – VLCD > 0.6V” condition is satisfied.
Unstable IC output voltage may result if the above conditions are not satisfied.

The relationship of LCD display contrast setting and VLCD voltage

CT Setting	formula	VDD= 6.000	VDD= 5.500	VDD= 5.000	VDD= 4.500	VDD= 4.000	VDD= 3.000	[V]
0	VDD	VLCD= 6.000	VLCD= 5.500	VLCD= 5.000	VLCD= 4.500	VLCD= 4.000	VLCD= 3.000	[V]
1	0.975*VDD	VLCD= 5.850	VLCD= 5.363	VLCD= 4.875	VLCD= 4.388	VLCD= 3.900	VLCD= 2.925	[V]
2	0.950*VDD	VLCD= 5.700	VLCD= 5.225	VLCD= 4.750	VLCD= 4.275	VLCD= 3.800	VLCD= 2.850	[V]
3	0.925*VDD	VLCD= 5.550	VLCD= 5.088	VLCD= 4.625	VLCD= 4.163	VLCD= 3.700	VLCD= 2.775	[V]
4	0.900*VDD	VLCD= 5.400	VLCD= 4.950	VLCD= 4.500	VLCD= 4.050	VLCD= 3.600	VLCD= 2.700	[V]
5	0.875*VDD	VLCD= 5.250	VLCD= 4.813	VLCD= 4.375	VLCD= 3.938	VLCD= 3.500	VLCD= 2.625	[V]
6	0.850*VDD	VLCD= 5.100	VLCD= 4.675	VLCD= 4.250	VLCD= 3.825	VLCD= 3.400	VLCD= 2.550	[V]
7	0.825*VDD	VLCD= 4.950	VLCD= 4.538	VLCD= 4.125	VLCD= 3.713	VLCD= 3.300	VLCD= 2.475	[V]
8	0.800*VDD	VLCD= 4.800	VLCD= 4.400	VLCD= 4.000	VLCD= 3.600	VLCD= 3.200	VLCD= 2.400	[V]
9	0.775*VDD	VLCD= 4.650	VLCD= 4.263	VLCD= 3.875	VLCD= 3.488	VLCD= 3.100	VLCD= 2.325	[V]
10	0.750*VDD	VLCD= 4.500	VLCD= 4.125	VLCD= 3.750	VLCD= 3.375	VLCD= 3.000	VLCD= 2.250	[V]
11	0.725*VDD	VLCD= 4.350	VLCD= 3.988	VLCD= 3.625	VLCD= 3.263	VLCD= 2.900	VLCD= 2.175	[V]
12	0.700*VDD	VLCD= 4.200	VLCD= 3.850	VLCD= 3.500	VLCD= 3.150	VLCD= 2.800	VLCD= 2.100	[V]
13	0.675*VDD	VLCD= 4.050	VLCD= 3.713	VLCD= 3.375	VLCD= 3.038	VLCD= 2.700	VLCD= 2.025	[V]
14	0.650*VDD	VLCD= 3.900	VLCD= 3.575	VLCD= 3.250	VLCD= 2.925	VLCD= 2.600	VLCD= 1.950	[V]
15	0.625*VDD	VLCD= 3.750	VLCD= 3.438	VLCD= 3.125	VLCD= 2.813	VLCD= 2.500	VLCD= 1.875	[V]

Disabled