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# Standard LCD Segment Drivers



**BU9795Axxx Series      MAX 140 segments (SEG35×COM4)**

● **Features**

- Integrated RAM for display data (DDRAM) :  
35 × 4bit (Max 140 Segment)
- LCD drive output :  
4 Common output, Max 35Segment output
- Integrated Buffer AMP for LCD driving
- Integrated Oscillator circuit
- No external components
- Low power consumption design

● **Applications**

- Telephone
- FAX
- Portable equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home electrical appliance
- Meter equipment
- etc.

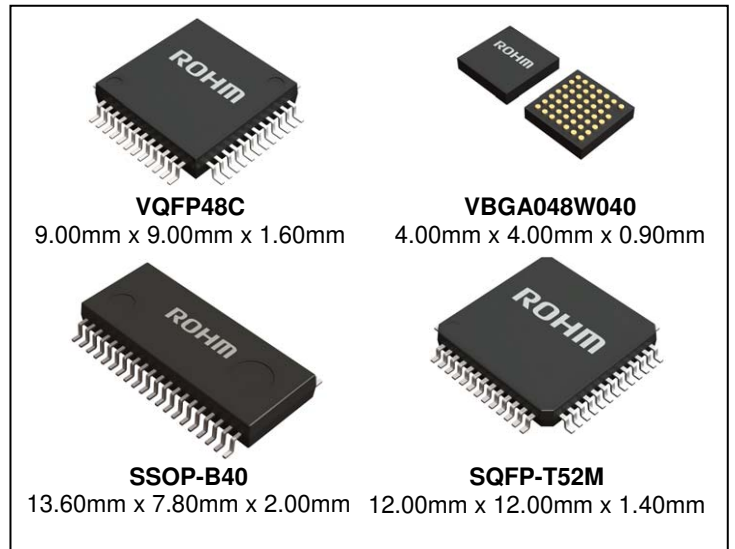
● **Key Specifications**

- Supply Voltage Range: +2.5V to +5.5V
- Operating Temperature Range: -40°C to +85°C
- Max Segments:
 

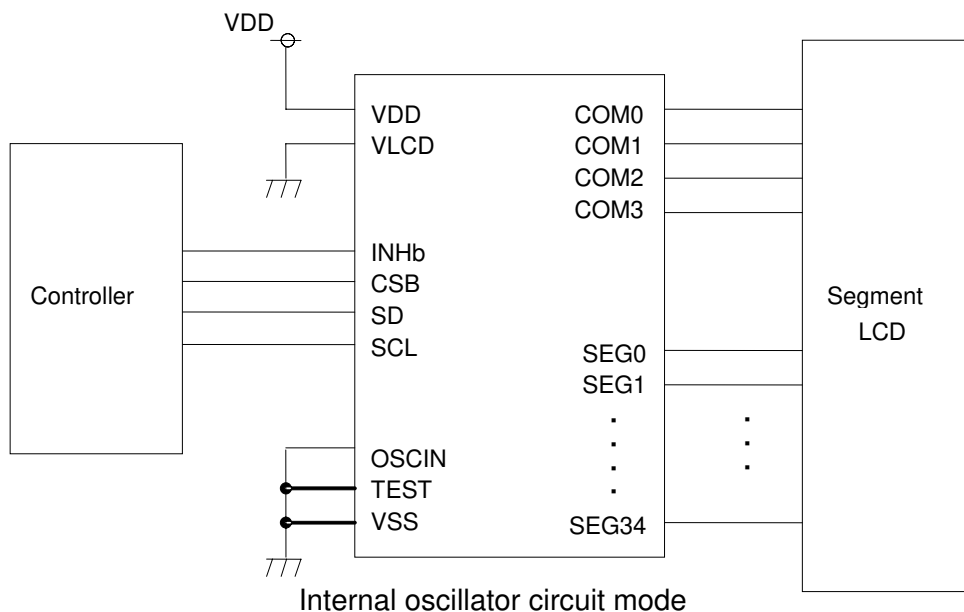
BU9795AKV	140 Segments
BU9795AFV	108 Segments
BU9795AGUW	124 Segments
BU9795AKS2	140 Segments
- Display Duty: 1/4
- Bias: 1/2, 1/3 selectable
- Interface: 3wire serial interface

● **Packages**

W (Typ.) x D (Typ.) x H (Max.)



● **Typical Application Circuit**



**Figure 1. Typical application circuit**

○Product structure : Silicon monolithic integrated circuit    ○This product is not designed for protection against radioactive rays.

●Block Diagrams / Pin Configurations / Pin Descriptions

BU9795AKV

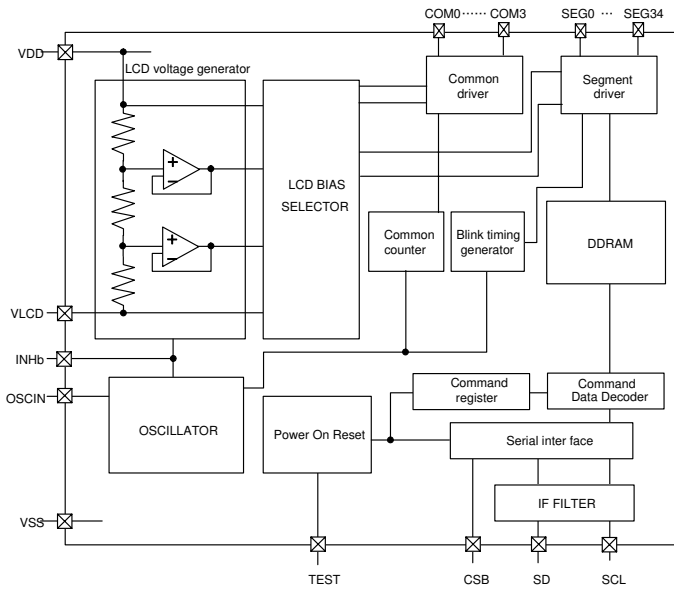


Figure 2. Block Diagram

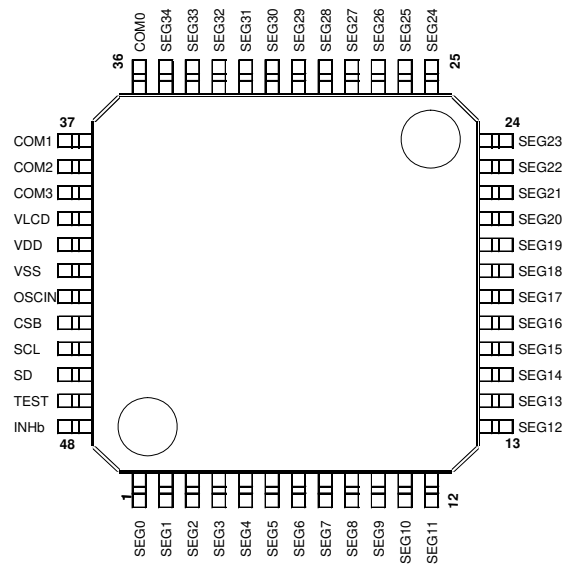


Figure 3. Pin Configuration (TOP VIEW)

Table 1 Pin Description

Pin name	Pin No.	I/O	Function
INHb	48	I	Input terminal for turn off display H : turn on display L : turn off display
TEST	47	I	Test input (ROHM use only) Must be connected to VSS
OSCIN	43	I	External clock input External clock and Internal clock can be selected by command. Must be connected to VSS when using internal oscillation circuit.
SD	46	I	Serial data input
SCL	45	I	Serial data transfer clock
CSB	44	I	Chip select : "L" active
VSS	42		GND
VDD	41		Power supply
VLCD	40		Power supply for LCD driving
SEG0 to 34	1 to 35	O	SEGMENT output for LCD driving
COM0 to 3	36 to 39	O	COMMON output for LCD driving

●Block Diagrams / Pin Configurations / Pin Descriptions - continued

BU9795AFV

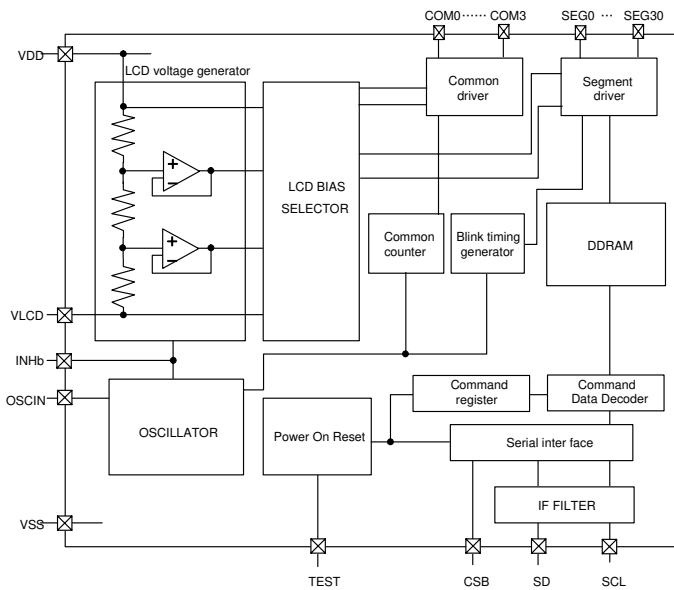


Figure 4. Block Diagram

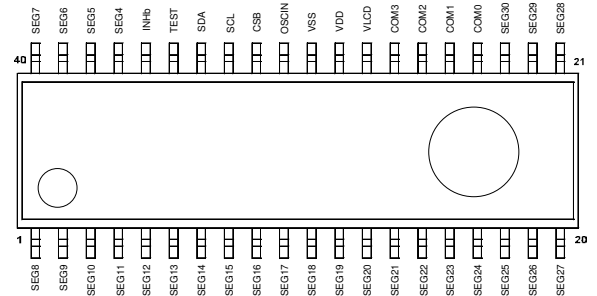


Figure 5. Pin Configuration (TOP VIEW)

Table 2 Pin Description

Pin name	Pin No.	I/O	Function
INHb	36	I	Input terminal for turn off display H : turn on display L : turn off display
TEST	35	I	Test input (ROHM use only) Must be connected to VSS
OSCIN	31	I	External clock input Ex clock and Int clock can be changed by command. Must be connected to VSS when using internal oscillation circuit.
SD	34	I	Serial data input
SCL	33	I	Serial data transfer clock
CSB	32	I	Chip select : "L" active
VSS	30		GND
VDD	29		Power supply
VLCD	28	I	Power supply for LCD driving
SEG4 to 30	1 to 23, 37 to 40	O	SEGMENT output for LCD driving
COM0 to 3	24 to 27	O	COMMON output for LCD driving

●Block Diagrams / Pin Configurations / Pin Descriptions - continued

BU9795AGUW

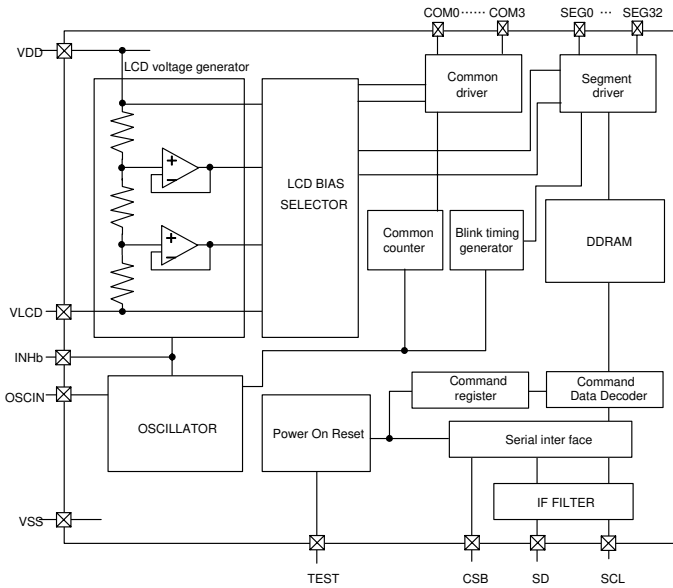


Figure 6. Block Diagram

	1	2	3	4	5	6	7
G	(NC)	SEG13	SEG15	SEG18	SEG20	SEG22	(NC)
F	SEG11	SEG12	SEG16	SEG17	SEG21	SEG23	SEG24
E	SEG9	SEG10	SEG14	SEG19	SEG25	SEG27	SEG26
D	SEG7	SEG6	SEG8	SEG5	SEG30	SEG28	SEG29
C	SEG4	SEG3	SEG2	CSB	COM3	SEG32	SEG31
B	X	INHb	SD	VSS	VDD	COM1	COM0
A	(NC)	TEST2	SCL	OSCIN	VLCD	COM2	(NC)

Figure 7. Pin Configuration (BOTTOM VIEW)

Table 3 Pin Description

Pin name	I/O	Function
INHb	I	Input terminal for turn off display H : turn on display L : turn off display
TEST	I	Test input (ROHM use only) Must be connected to VSS
OSCIN	I	External clock input Ex clock and Int clock can be changed by command. Must be connected to VSS when using internal oscillation circuit.
SD	I	Serial data input
SCL	I	Serial data transfer clock
CSB	I	Chip select : "L" active
VSS		GND
VDD		Power supply
VLCD	I	Power supply for LCD driving
SEG2 to 32	O	SEGMENT output for LCD driving
COM0 to 3	O	COMMON output for LCD driving

●Block Diagrams / Pin Configurations / Pin Descriptions – continued

BU9795AKS2

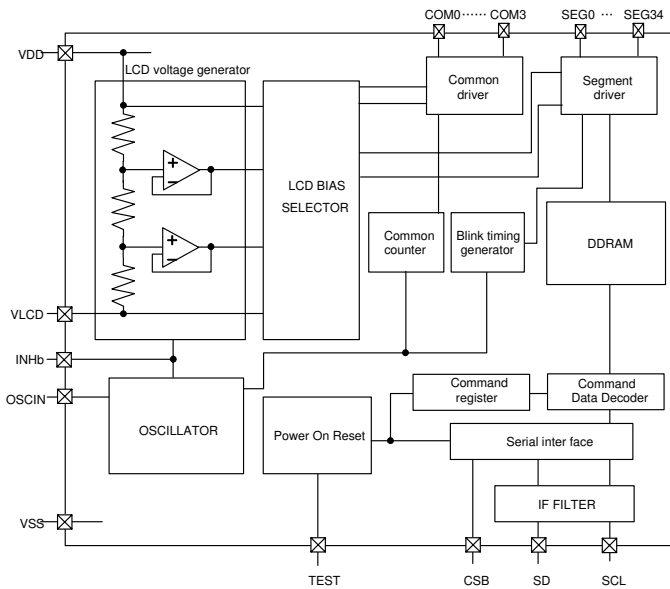


Figure 8. Block Diagram

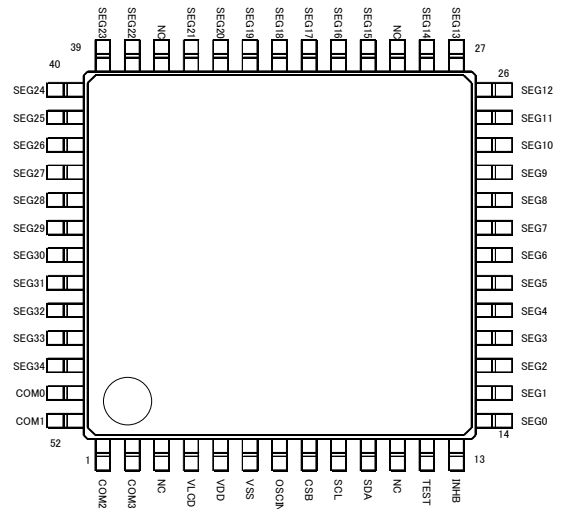


Figure 9. Pin Configuration (TOP VIEW)

Table 4 Pin Description

Pin name	Pin No.	I/O	Function
INHb	13	I	Input terminal for turn off display H : turn on display L : turn off display
TEST	12	I	Test input (ROHM use only) Must be connect to VSS
OSCIN	7	I	External clock input Ex clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SD	10	I	serial data input
SCL	9	I	serial data transfer clock
CSB	8	I	Chip select : "L" active
VSS	6		GND
VDD	5		Power supply
VLCD	4		Power supply for LCD driving
SEG0-34	14-28, 30-36 38-50	O	SEGMENT output for LCD driving
COM0-3	51-52, 1-2	O	COMMON output for LCD driving

## ● Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remark
Power supply voltage1	VDD	-0.5 to +7.0	V	Power supply
Power supply voltage2	VLCD	-0.5 to VDD	V	LCD drive voltage
Power dissipation	Pd	0.6	W	When use more than Ta=25°C, subtract 6mW per degree.(BU9795AKV) (Package only)
		0.7	W	When use more than Ta=25°C, subtract 7mW per degree (BU9795AFV) (Package only)
		0.27	W	When use more than Ta=25°C, subtract 2.7mW per degree (BU9795AGUW) (Package only)
		0.85	W	When use more than Ta=25°C, subtract 8.5mW per degree (BU9795AKS2) (Package only)
Input voltage range	VIN	-0.5 to VDD+0.5	V	
Operational temperature range	Topr	-40 to +85	°C	
Storage temperature range	Tstg	-55 to +125	°C	

## ● Recommended Operating Ratings(Ta=-40°C to +85°C,VSS=0V)

Parameter	Symbol	Ratings			Unit	Remark
		Min.	Typ.	Max.		
Power Supply voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply voltage2	VLCD	0	-	VDD -2.4	V	LCD drive voltage

\* Please use VDD-VLCD≥2.4V condition.

## ● Electrical Characteristics

DC Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C, unless otherwise specified)

Parameter	Symbol	Limits			Unit	Conditions	
		MIN	TYP	MAX			
"H" level input voltage	VIH	0.7VDD	-	VDD	V		
"L" level input voltage	VIL	VSS	-	0.3VDD	V		
"H" level input current	IIH	-	-	1	μA		
"L" level input current	IIL	-1	-	-	μA		
LCD Driver on resistance	SEG	RON	-	3.5	-	kΩ	Iload=±10μA
	COM	RON	-	3.5	-	kΩ	
VLCD supply voltage	VLCD	0	-	VDD -2.4	V	VDD-VLCD≥2.5V	
Standby current	Ist	-	-	5	μA	Display off, Oscillator off	
Power consumption 1	IDD1	-	12.5	30	μA	VDD=3.3V, Ta=25°C, Power save mode1, FR=70Hz 1/3 bias, Frame inverse	
Power consumption 2	IDD2	-	20	40	μA	VDD=3.3V, Ta=25°C, Normal mode, FR=80Hz 1/3 bias, Line inverse	

●Electrical Characteristics - continued

Oscillation Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Frame frequency	f <sub>CLK</sub>	56	80	104	Hz	FR = 80Hz setting
Frame frequency1	f <sub>CLK1</sub>	70	80	90	Hz	VDD=3.5V, 25°C

MPU interface Characteristics (VDD=2.5V to 5.5V, VSS=0V, Ta=-40°C to +85°C)

Parameter	Symbol	Limits			Unit	Conditions
		MIN	TYP	MAX		
Input rise time	t <sub>r</sub>	-	-	80	ns	
Input fall time	t <sub>f</sub>	-	-	80	ns	
SCL cycle time	t <sub>SCYC</sub>	400	-	-	ns	
"H" SCL pulse width	t <sub>SHW</sub>	100	-	-	ns	
"L" SCL pulse width	t <sub>SLW</sub>	100	-	-	ns	
SD setup time	t <sub>SDS</sub>	20	-	-	ns	
SD hold time	t <sub>SDH</sub>	50	-	-	ns	
CSB setup time	t <sub>CSS</sub>	50	-	-	ns	
CSB hold time	t <sub>CSH</sub>	50	-	-	ns	
"H" CSB pulse width	t <sub>CHW</sub>	50	-	-	ns	

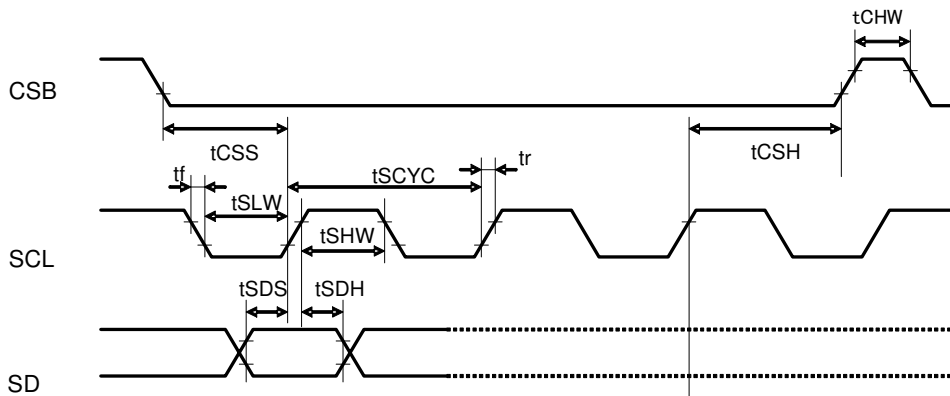


Figure 10. Interface Timing

●I/O equivalent circuit

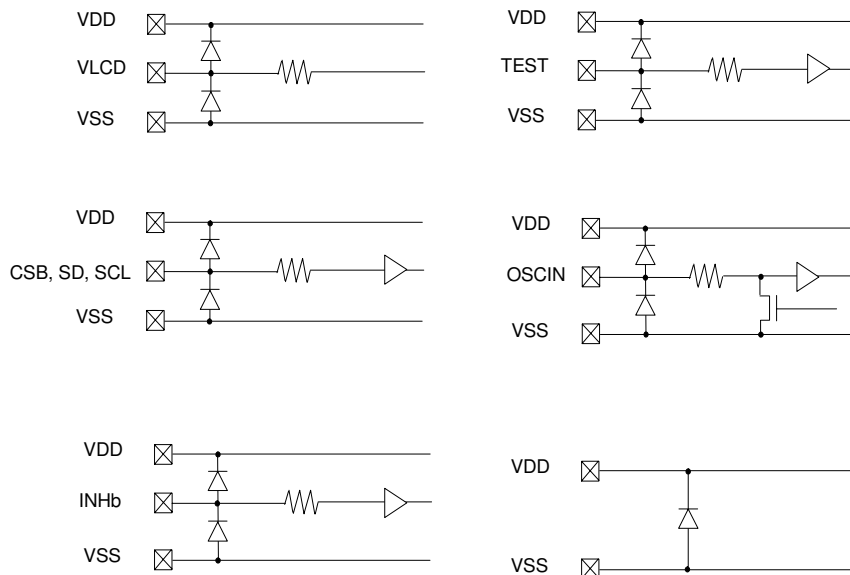
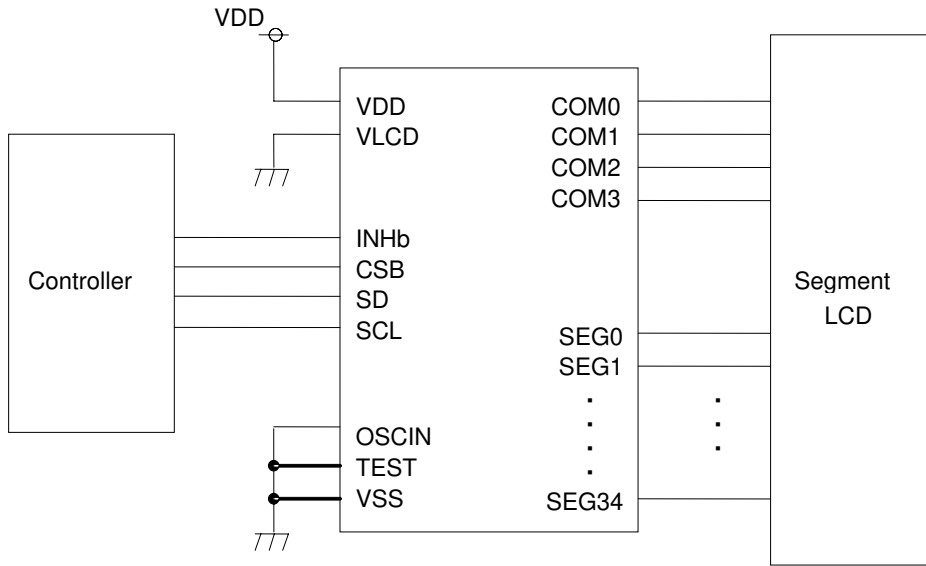


Figure 11. I/O equivalent circuit

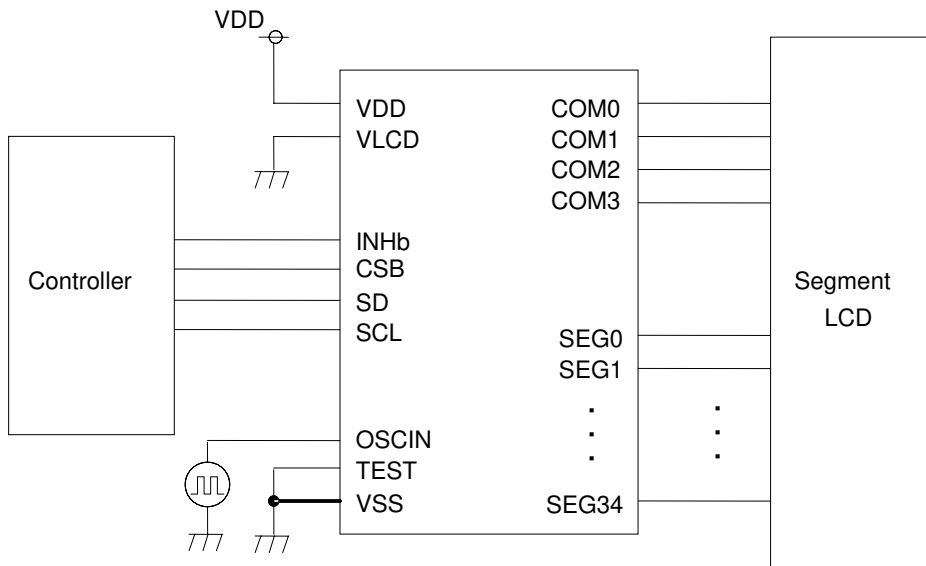


● Example of recommended circuit

<BU9795AKV/BU9795AKS2>



Using internal oscillator circuit mode

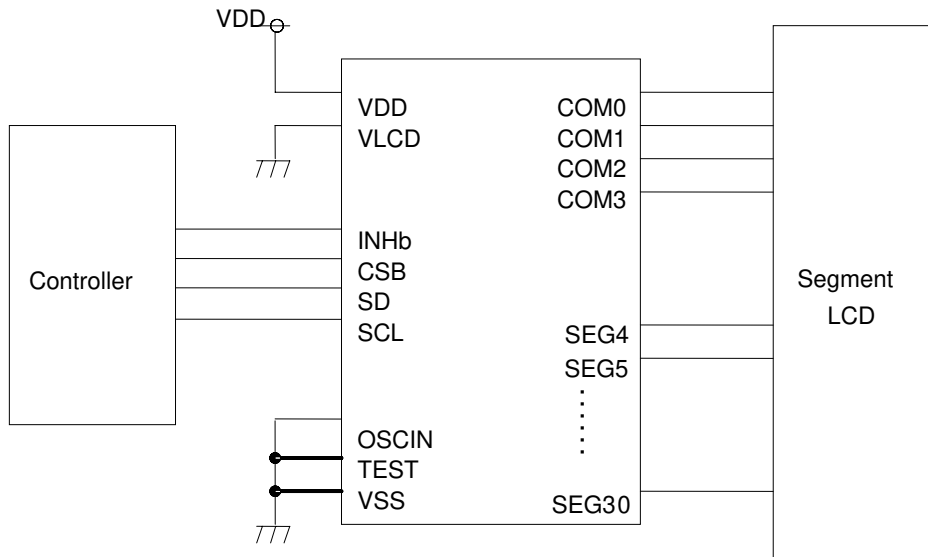


Using external oscillator mode

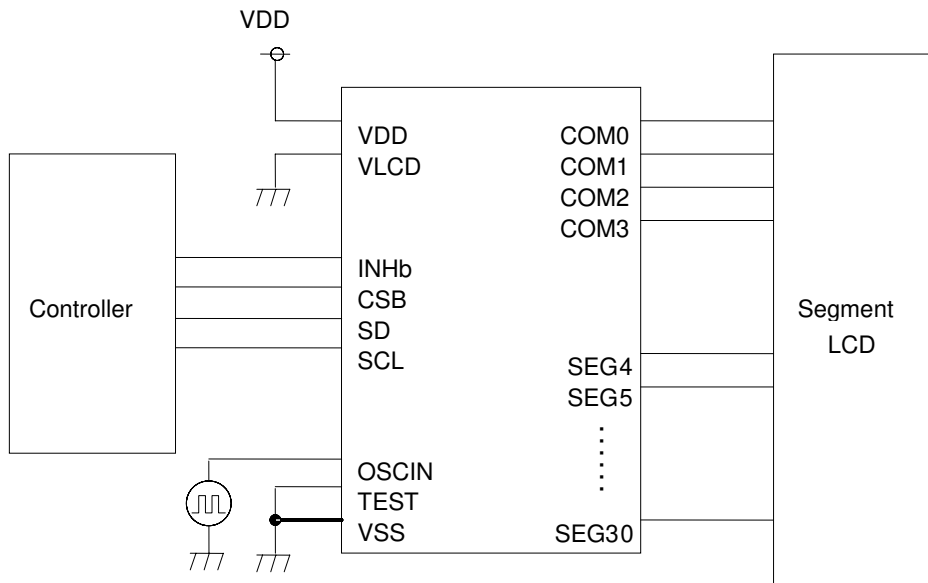
Figure 12. BU9795AKV/BU9795AKS2 recommended circuit

●Example of recommended circuit - continued

<BU9795AFV>



Using internal oscillator circuit mode

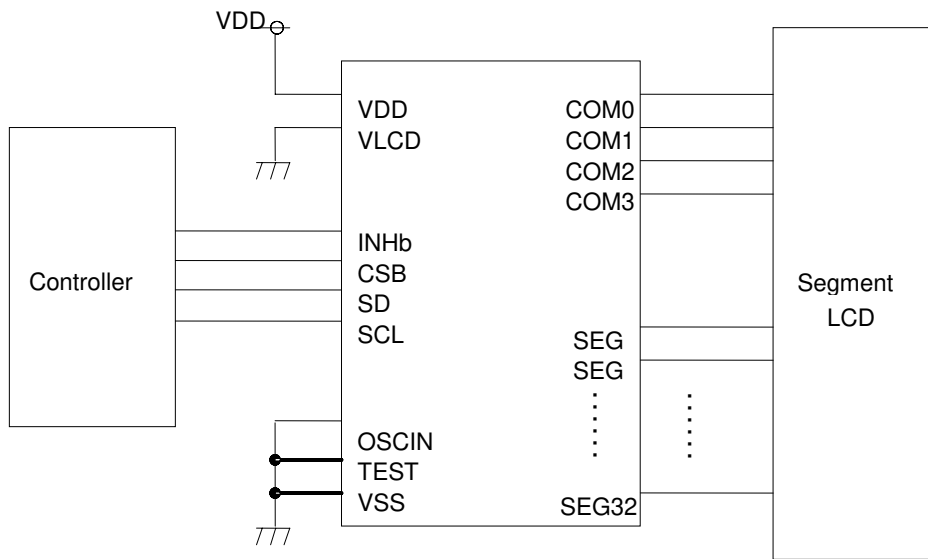


Using external oscillator mode

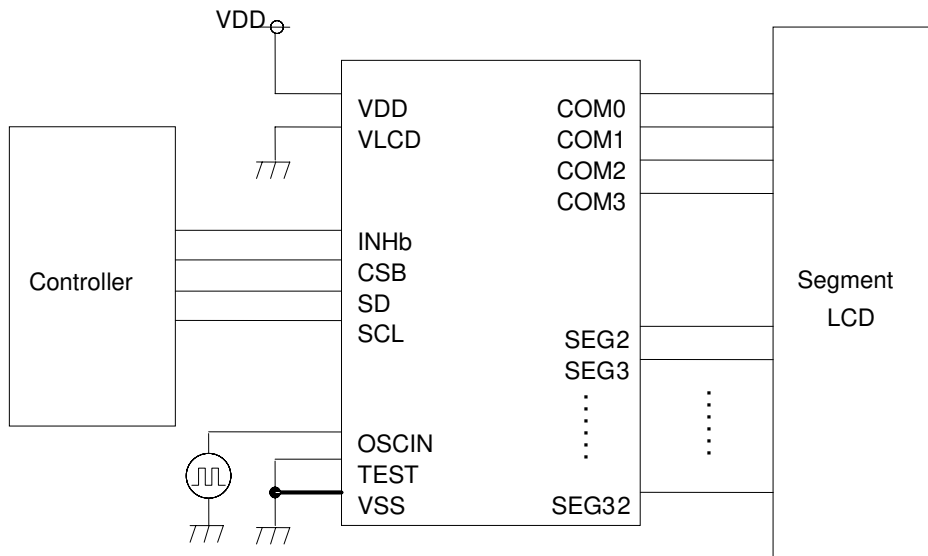
Figure 13. BU9795AFV example recommended circuit

●Example of recommended circuit - continued

<BU9795AGUW>



Using internal oscillator circuit mode



Using external oscillator mode

Figure14. BU9795AGUW example recommended circuit

●Function Description

○Command and data transfer method

○3-SPI (3wire Serial interface)

This device is controlled by 3-wire signal (CSB, SCL, and SD).

First, Interface counter is initialized with CSB="H", and CSB="L" makes SD and SCL input enable.

The protocol of 3-SPI transfer is as follows.

Each command starts with Command or Data judgment bit (D/C) as MSB data, followed by D6 to D0 during CSB = "L".

(Internal data is latched at the rising edge of SCL, it is converted to 8bits parallel data at the falling edge of 8th CLK.)

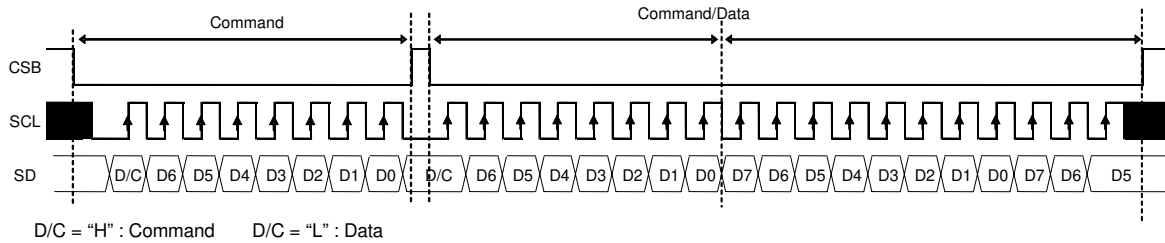


Figure 15. 3-SPI Command/Data transfer format

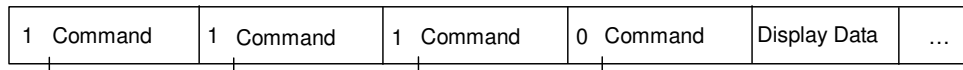
○Command transfer method

After CSB="H"→"L", 1st byte is always a command input.

MSB of the command input data will be judged that the next byte data, it is a command or display data (This bit is called "command or data judgment bit").

When set "command or data judge bit"='1', next byte will be (continuously) command.

When set "command or data judge bit"='0', next byte data is display data.



Once it becomes display data transfer condition, it will not be back to command input condition even if D/C=1.

So if you want to send command data again, please set CSB="L"→"H".

(CSB "L"→"H" will cancel data transfer condition.)

Command transfer is done by 8bits unit, so if CSB="L"→"H" with less than 8bits data transfer, command will be cancelled.

It will be able to transfer command with CSB="L" again.

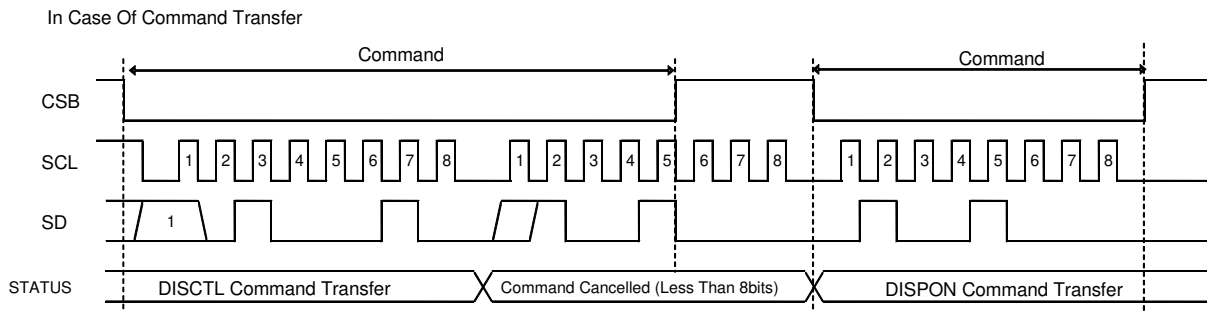
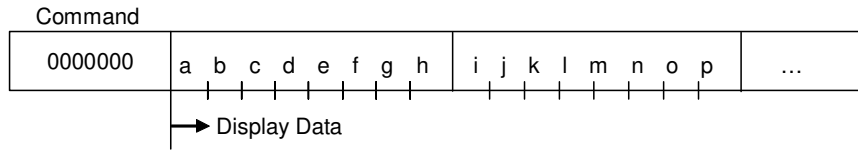


Figure 16. Command transfer format

○Write display data and transfer method  
 <BU9795AKV/BU9795AKS2>

This LSI has Display Data RAM (DDRAM) of 35×4=140bit.  
 The relationship between data input and display data, DDRAM data and address are as follows.



8 bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.  
 Data can be continuously written in DDRAM by transmitting Data continuously.  
 (When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function.)

		DDRAM address															
		00h	01h	02h	03h	04h	05h	06h	07h	.....	1Eh	1Fh	20h	21h	22h		
BIT	0	a	e	i	m	q	u									COM0	
	1	b	f	j	n	r	v									COM1	
	2	c	g	k	o	s	x									COM2	
	3	d	h	l	p	t	y									COM3	
		SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	.....	SEG 30	SEG 31	SEG 32	SEG 33	SEG 34		

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

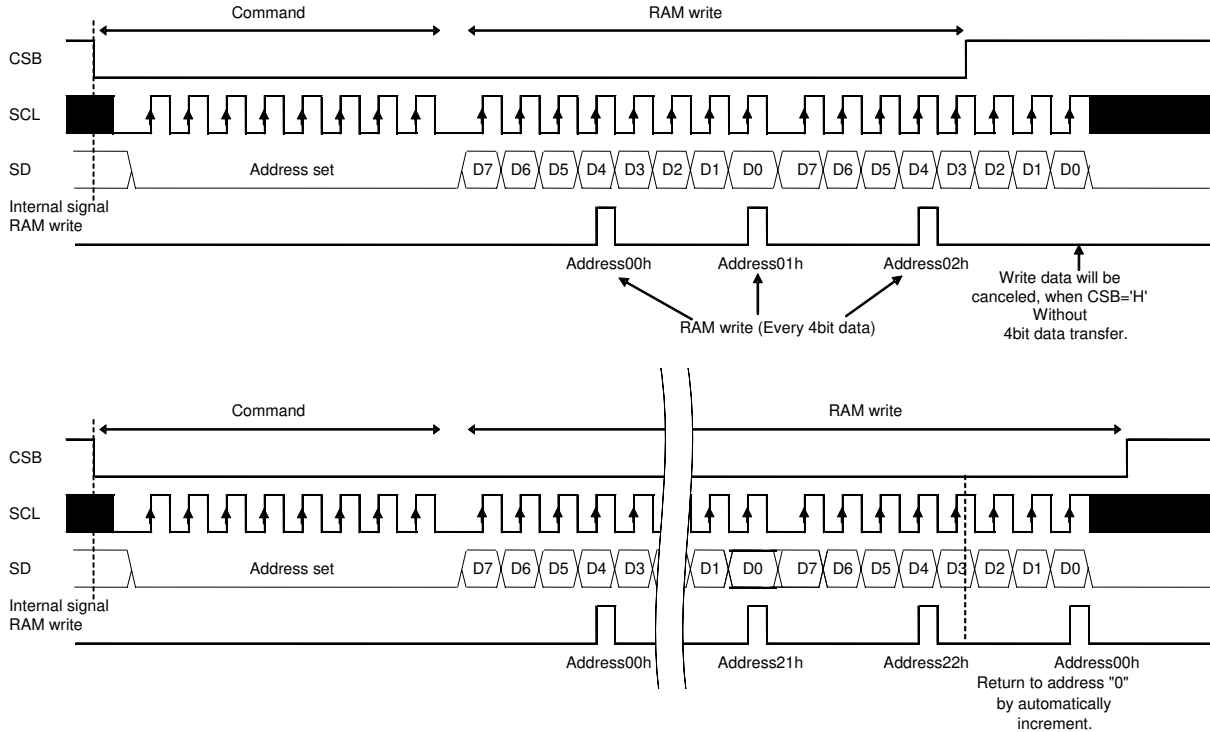
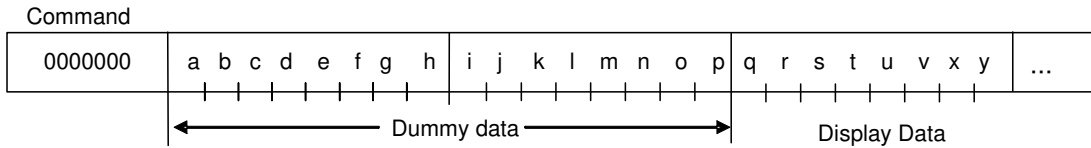


Figure 17. BU9795AKV/BU9795AKS2 Data Transfer Format

<BU9795AFV>

This LSI has Display Data RAM (DDRAM) of 27×4=108bit.  
 As SEG0, SEG1, SEG2, SEG3, SEG31, SEG32, SEG33, SEG34 are not output, these address will be dummy address.  
 The relationship between data input and display data, DDRAM data and address are as follows.



8 bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.  
 Data can be continuously written in DDRAM by transmitting Data continuously.  
 (When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function.)

BIT	Dummy data				DDRAM address												Dummy data									
	00h	01h	02h	03h	04h	05h	06h	07h	.....	1Eh	1Fh	20h	21h	22h												
0	a	e	i	m	q	u																				COM0
1	b	f	j	n	r	v																				COM1
2	c	g	k	o	s	x																				COM2
3	d	h	l	p	t	y																				COM3
	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	.....	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG	SEG		
	0	1	2	3	4	5	6	7	.....	30	31	32	33	34												

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

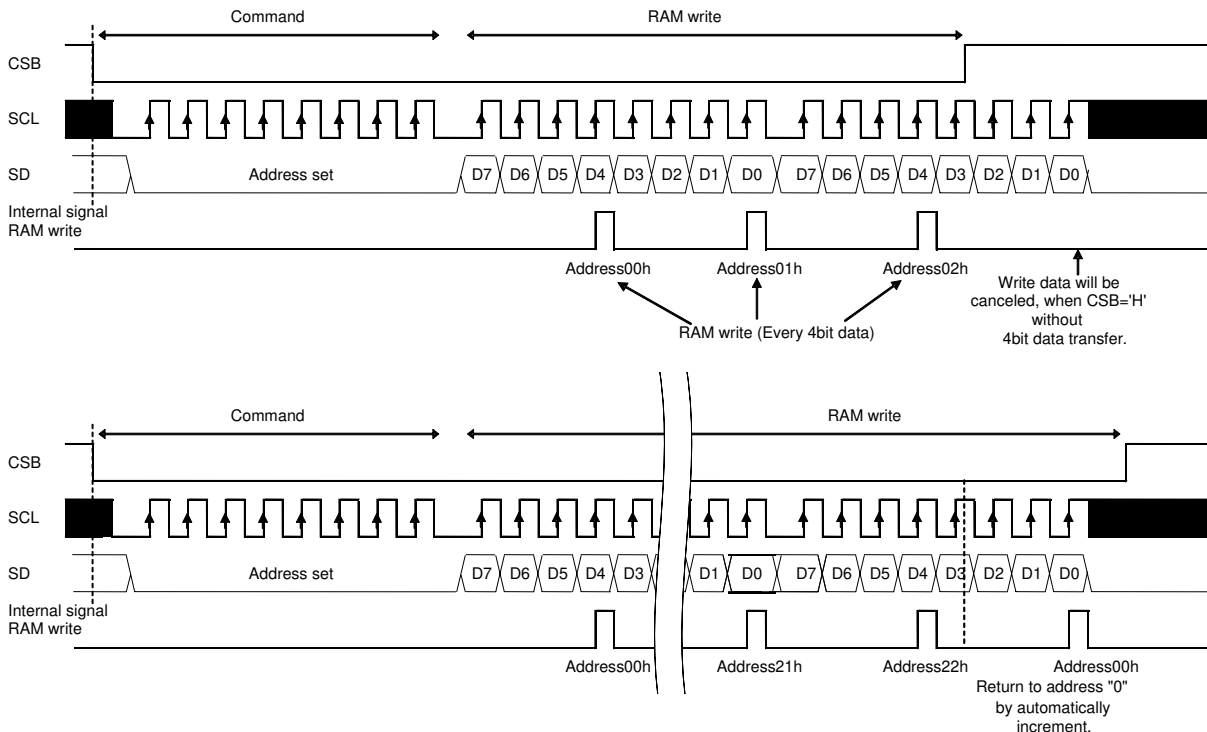
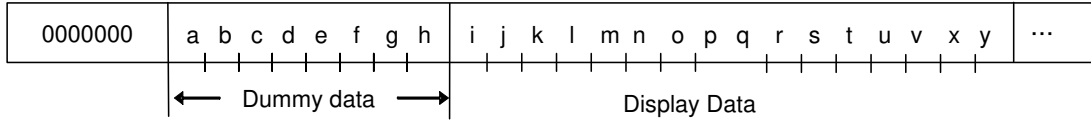


Figure 18. BU9795AFV Data Transfer Format

<BU9795AGUW>

This LSI has Display Data RAM (DDRAM) of 31×4=124bit.  
 As SEG0, SEG1, SEG33, SEG34 are not output, these address will be dummy address.  
 The relationship between data input and display data, DDRAM data and address are as follows.

Command



8 bit data will be stored in DDRAM. The address to be written is the address specified by ADSET command, and the address is automatically incremented in every 4bit data.  
 Data can be continuously written in DDRAM by transmitting Data continuously.  
 (When RAM data is written successively after writing RAM data to 22h (SEG34), the address is returned to 00h (SEG0) by the auto-increment function.)

		DDRAM address															
		00h	01h	02h	03h	04h	05h	06h	07h	.....	1Eh	1Fh	20h	21h	22h		
BIT	0	a	e	i	m	q	u									COM0	
	1	b	f	j	n	r	v									COM1	
	2	c	g	k	o	s	x									COM2	
	3	d	h	l	p	t	y									COM3	
		SEG 0	SEG 1	SEG 2	SEG 3	SEG 4	SEG 5	SEG 6	SEG 7	.....	SEG 30	SEG 31	SEG 32	SEG 33	SEG 34		

As data transfer to DDRAM happens every 4bit data, it will be cancelled if it changes CSB="L"→"H" before 4bits data transfer.

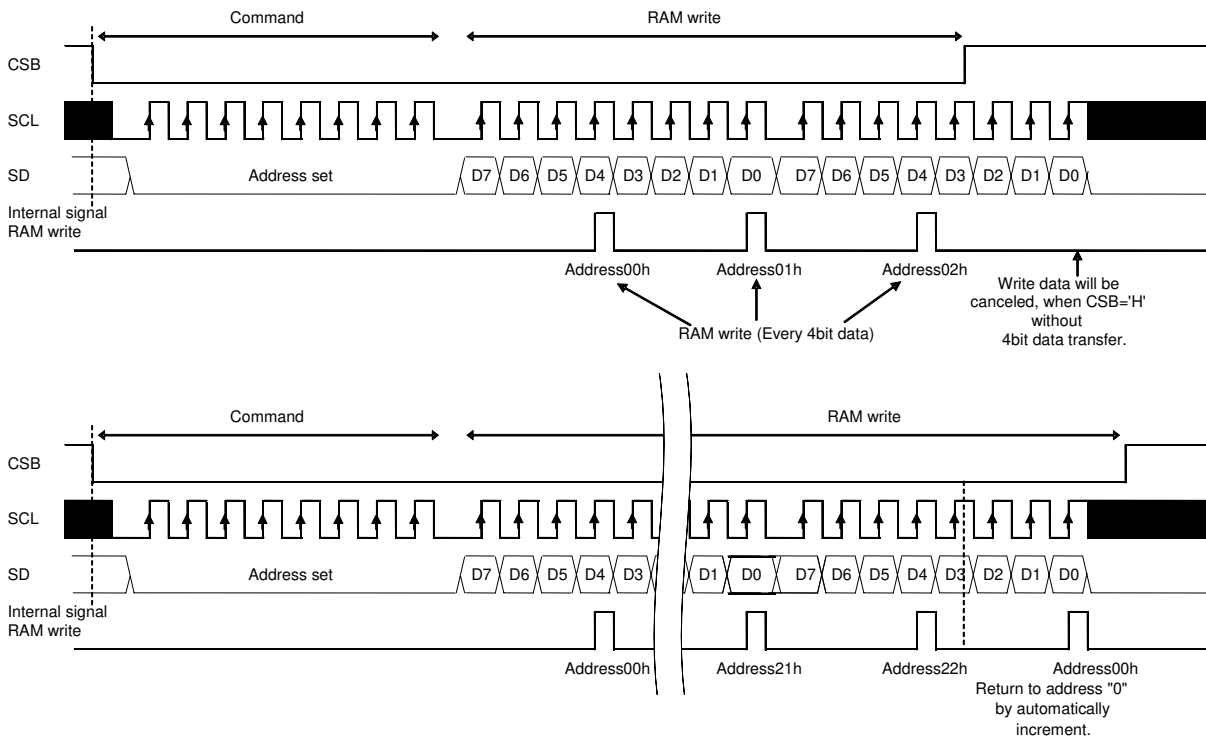
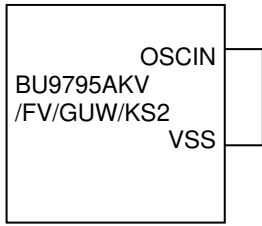


Figure 19. BU9795AGUW Data Transfer Format

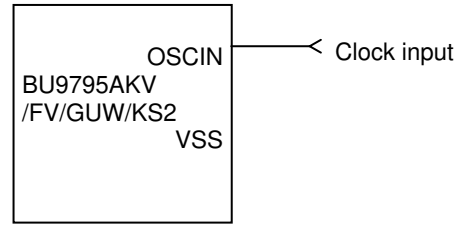
**OOSCILLATOR**

There are two kinds of clock for logic and analog circuit; from internal oscillator circuit or external clock input. If internal oscillator circuit will be used, OSCIN must be connected to VSS.

\*When you use external clock, execute ICSET command and connect OSCIN to external clock.



**Figure 20. Internal oscillator circuit mode**



**Figure 21. External clock mode**

**OLCD Driver Bias Circuit**

This LSI generates LCD driving voltage with on-chip Buffer AMP. And it can drive LCD at low power consumption.

\*1/3 and 1/2Bias can be set in MODESET command.

\*Line and frame inversion can be set in DISCTL command.

Refer to “LCD driving waveform” about each LCD driving waveform.

**OBlink timing generator**

This device has Blinking function.

\*This LSI is able to set blink mode with BLKCTL command.

Blink frequency varies widely by characteristic of fCLK, when internal oscillation circuit.

Refer to Oscillation Characteristics for more details on fCLK.

**OReset (initial) condition**

Initial condition after execute SOFTWARE RESET is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).

Refer to Command Description about initialize value of register.

**●Command / Function List**

Description List of Command / Function

No.	Command	Function
1	Mode Set (MODESET)	Set LCD drive mode
2	Address Set (ADSET)	Set LCD display mode 1
3	Display Control (DISCTL)	Set LCD display mode 2
4	Set IC Operation (ICSET)	Set IC operation
5	Blink Control (BLKCTL)	Set blink mode
6	All Pixel Control (APCTL)	Set pixel condition



●Detailed Command Description

D7 (MSB) is bit for command or data judgment.  
Refer to Command and data transfer method.

C : 0 : Next byte is RAM write data.  
1 : Next byte is command.

OMode Set (MODE SET)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

(\* : Don't care)

Set display ON and OFF

Setting	P3	Reset initialize condition
Display OFF(DISPOFF)	0	○
Display ON(DISPON)	1	

Display OFF : Regardless of DDRAM data, all SEGMENT and COMMON output will be stopped after 1 frame of data write. Display OFF mode will be finished by Display ON.

Display ON : SEGMENT and COMMON output will be active and start to read the display data from DDRAM.

(Note) It is not synchronize with display frame, when it will be controlled display ON/OFF with INHb terminal.

Set bias level

Setting	P2	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

Refer to LCD driving waveform.

OAddress set (ADSET)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

Address data is specified in P[4 : 0] and P2 (ICSET command) as follows.

	MSB			LSB
Internal register	Address [5]	Address [4]	...	Address [0]
Bit of each command	ICSET [P2]	ADSET [P4]	...	ADSET [P0]

The address is 00h in reset condition. The valid address is 00h to 22h.

Another address is invalid, (otherwise address will be set to 00h.)

P2 of ICSET command is only to define either MSB of address is "1" or "0".

Address counter will be set only when ADSET command is executed.

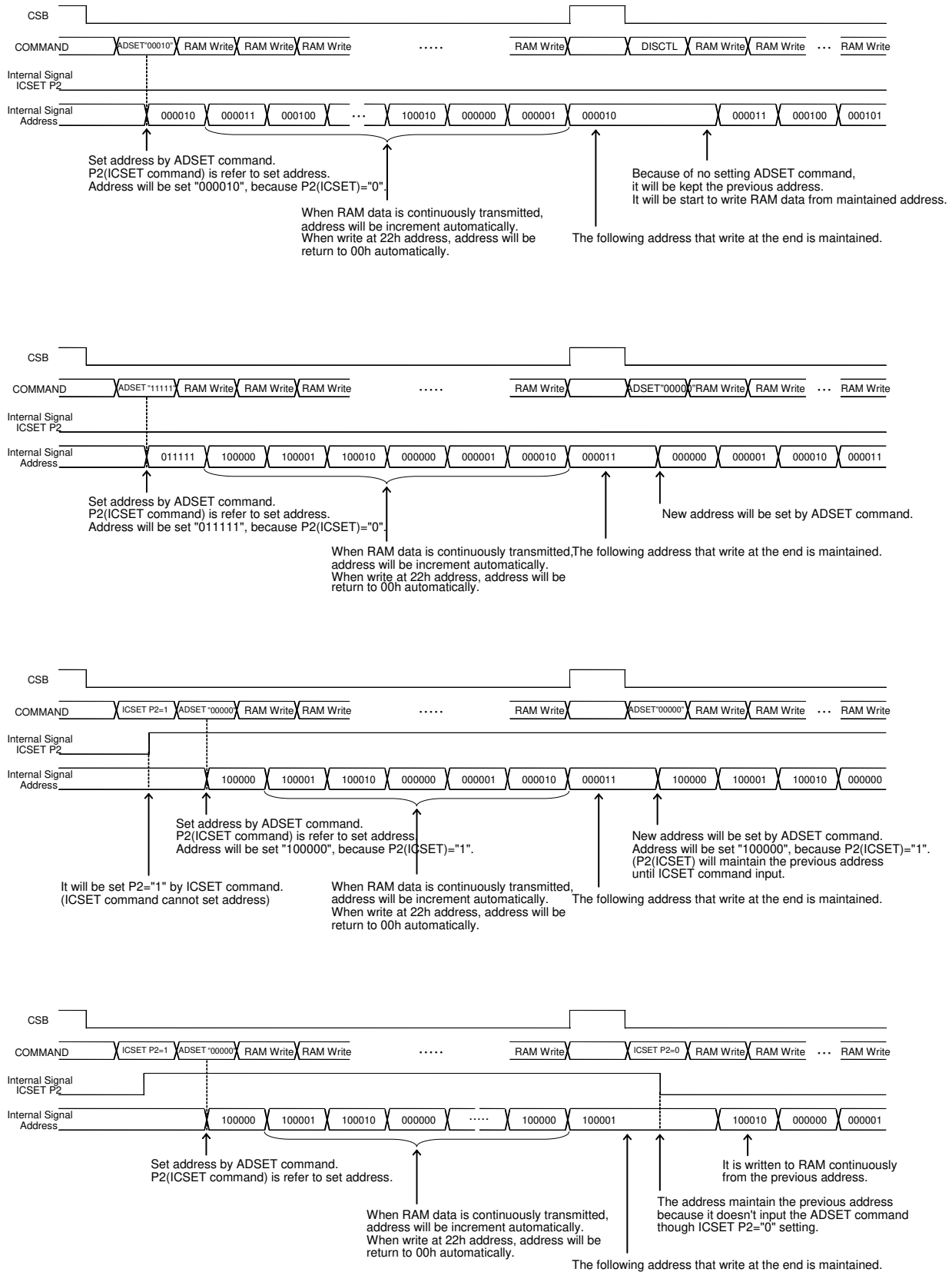


Figure 22. Address Set sequence

ODisplay control (DISCTL)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Frame frequency

Setting	P4	P3	Reset initialize condition
80Hz	0	0	○
71Hz	0	1	
64Hz	1	0	
53Hz	1	1	

\* About the characteristics of FR, refer to Oscillation characteristics.

Set LCD drive waveform

Setting	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

Set Power save mode

Setting	P1	P0	Reset initialize condition
Power save mode 1	0	0	
Power save mode 2	0	1	
Normal mode	1	0	○
High power mode	1	1	

\*VDD-VLCD≥3.0V is required for High power mode.

(Reference current consumption data)

Setting	Reset initialize condition
Power save mode 1	×0.5
Power save mode 2	×0.67
Normal mode	×1.0
High power mode	×1.8

\*Above current consumption data is reference value. It depends on panel load.

(Note) Frame rate FR / LCD drive waveform / Power save mode SR will effect display image.  
Select the best value in point of current consumption and display image using LCD panel (under real application).

Mode	Screen flicker	Display image / contrast
Frame frequency	○	-
LCD drive waveform	○	○
Power save mode	-	○

OSet IC Operation (ICSET)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	P2	P1	P0

P2 : MSB data of DDRAM address. Please refer to “ADSET” command.

Setting	P2	Reset initialize condition
Address MSB'0'	0	○
Address MSB'1'	1	

Set Software Reset condition

Setting	P1
No operation	0
Software Reset	1

When “Software Reset” is executed, this LSI will be reset to initial condition.

If software reset is executed, the value of P2 and P1 will be ignored and they will be set initialized condition. (Refer to “Reset initial condition”)

Switch between internal clock and external clock.

Setting	P0	Reset initialize condition
Internal clock	0	○
External clock input	1	

For internal clock : OSCIN is connected to VSS.

For external clock input : Input external clock into OSCIN.

<external Clock Frame frequency calculation>

DISCTL 80Hz select : Frame frequency [Hz] = external clock[Hz] / 512

DISCTL 71Hz select : Frame frequency [Hz] = external clock[Hz] / 576

DISCTL 64Hz select : Frame frequency [Hz] = external clock[Hz] / 648

DISCTL 53Hz select : Frame frequency [Hz] = external clock[Hz] / 768

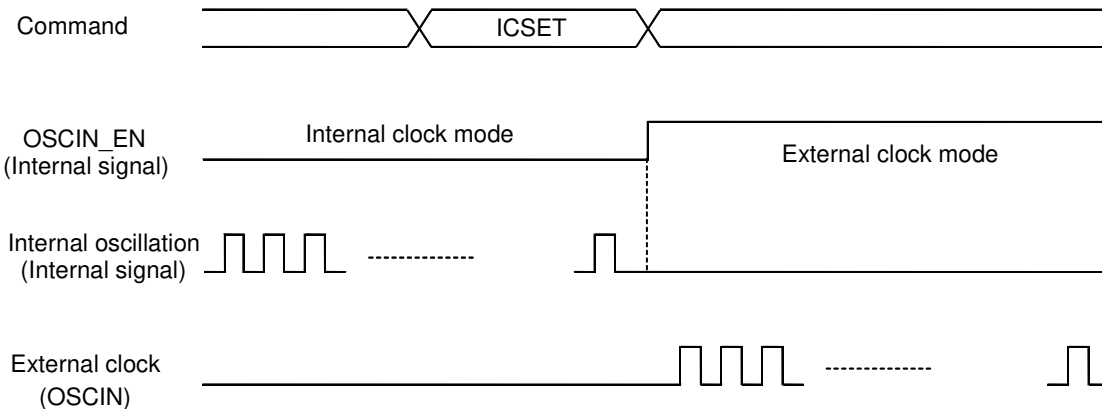


Figure 23. OSCMODE switching timing

OBlink control (BLKCTL)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

Set blink condition

Setting (Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

OAll pixel control (APCTL)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON. OFF

Setting	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

Setting	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

- All pixels ON : All pixels are ON regardless of DDRAM data.
- All pixels OFF : All pixels are OFF regardless of DDRAM data.

(Note) All pixels ON/OFF is effective only at the time of "Display ON" status.  
 The data of DDRAM do not change with this command.  
 If both P1 and P0=1', APOFF is selected. APOFF has higher priority than APON.

●LCD driving waveform

(1/3bias)

Line inversion

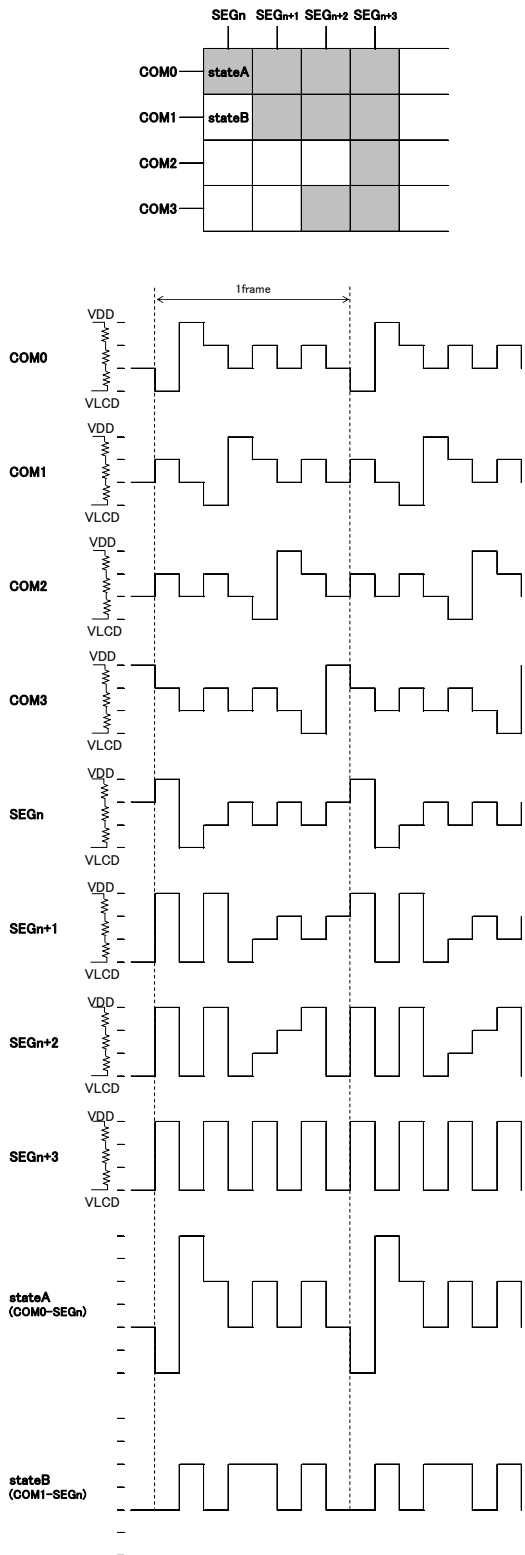


Figure 24. Line inversion waveform(1/3bias)

Frame inversion

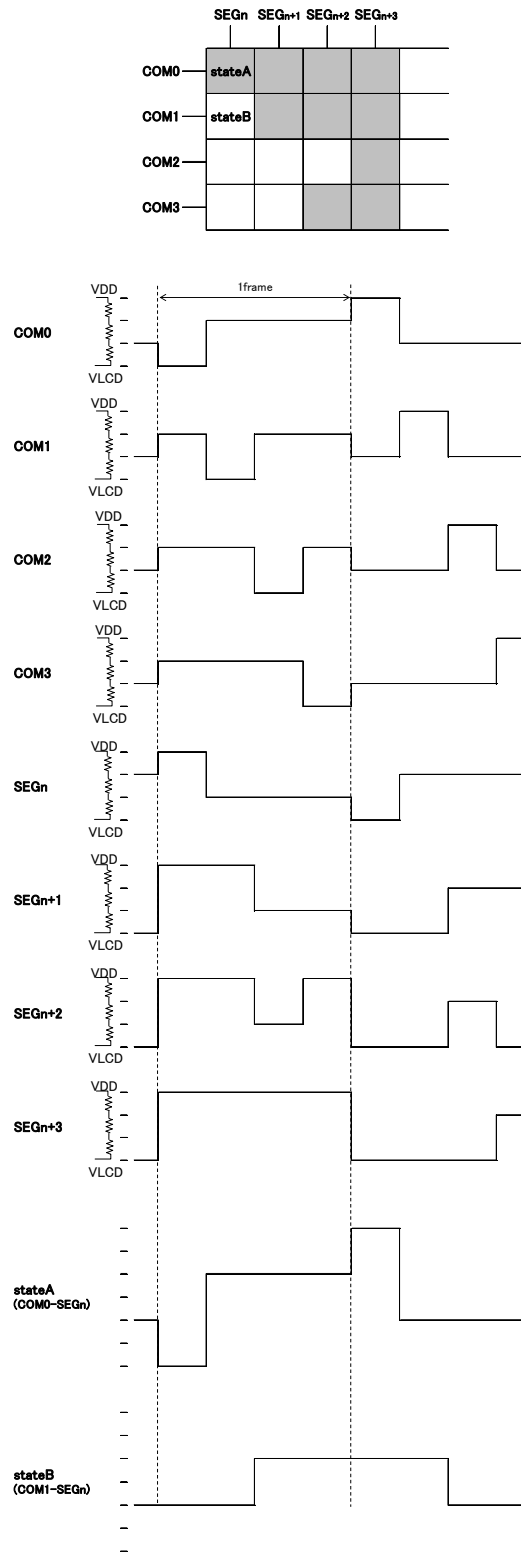


Figure 25. Frame inversion waveform(1/3bias)

(1/2bias)  
Line inversion

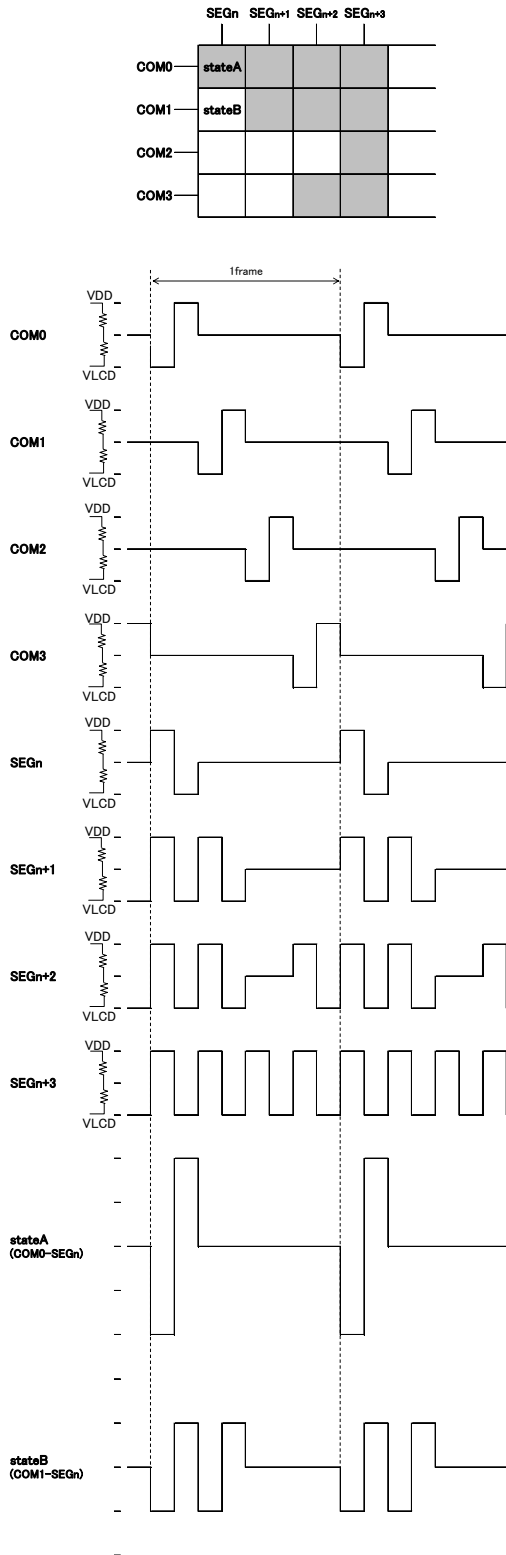


Figure 26. Line inversion waveform(1/2bias)

Frame inversion

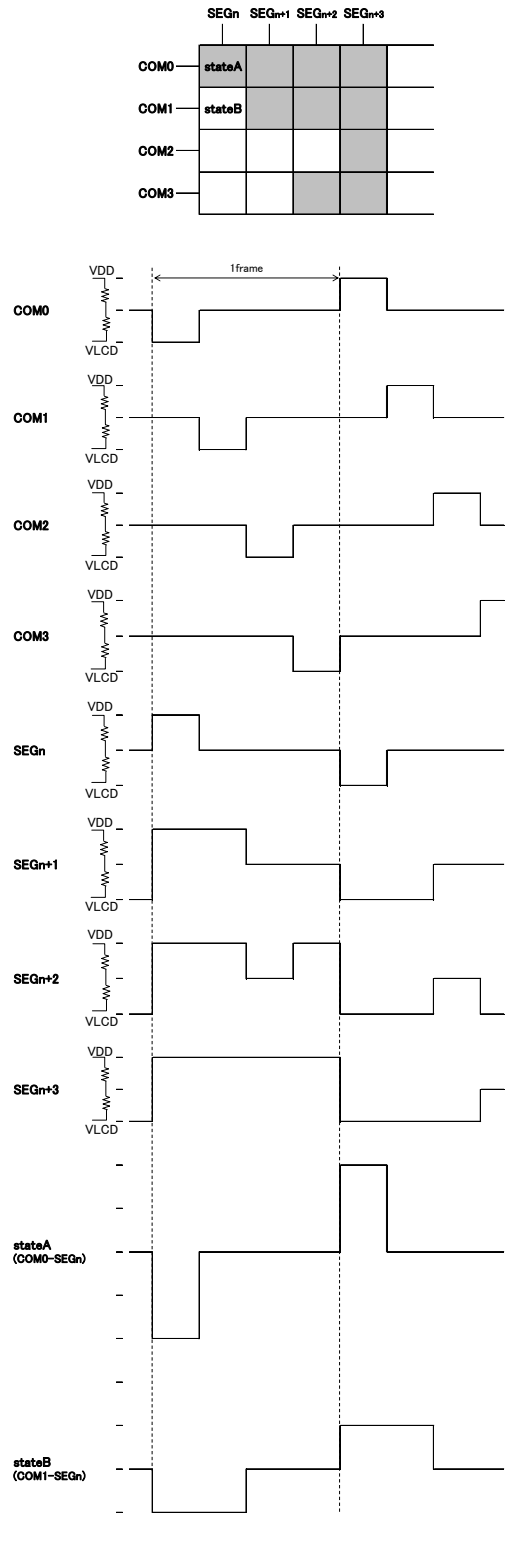


Figure 27. Frame inversion waveform(1/2bias)

●Example of display data

If LCD layout pattern is shown as in Figure28, Figure29 and DDRAM data is shown as in Table 5, display pattern will be shown as in Figure 30.

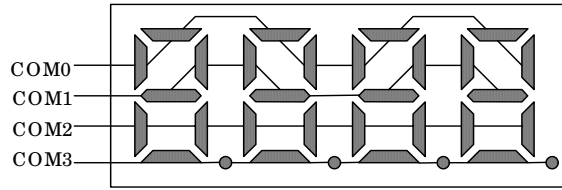


Figure 28. Example COM line pattern

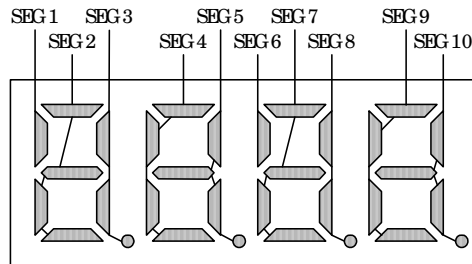


Figure 29. Example SEG line pattern



Figure 30. Example Display pattern

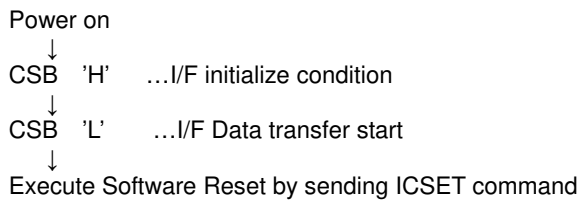
Table 5. DDRAM Data map

	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	
	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	
	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
COM0	D0	0	1	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	
COM1	D1	0	0	1	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	
COM2	D2	0	0	0	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	0	
COM3	D3	0	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	
Address		00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh	10h	11h	12h	13h



●Initialize sequence

Please follow sequence below after Power-On to set this device to initial condition.



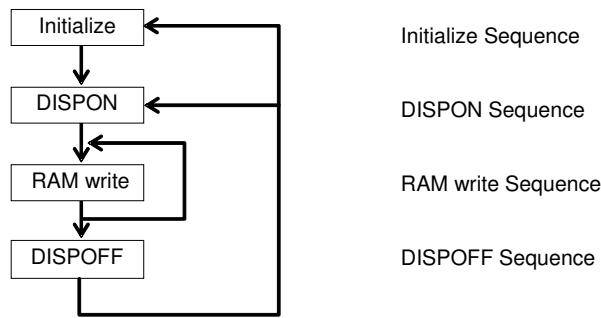
\* Each register value and DDRAM address, DDRAM data are random condition after power on till initialize sequence is executed.

●Start sequence

○Start sequence example 1

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0 to 5V (Tr=0.1ms)
	↓									
2	wait 100us									Initialize IC
	↓									
3	CSB 'H'									Initialize I/F data
	↓									
4	CSB 'L'									I/F Data transfer start
	↓									
5	ICSET	1	1	1	0	1	*	1	0	Software Reset
	↓									
6	BLKCTL	1	1	1	1	0	*	0	1	
	↓									
7	DISCTL	1	0	1	0	0	1	1	0	
	↓									
8	ICSET	1	1	1	0	1	0	0	0	RAM address MSB set
	↓									
9	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	address 00h to 01h
	Display Data	*	*	*	*	*	*	*	*	address 02h to 03h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	address 22h to 00h
	↓									
11	CSB 'H'									I/F Data transfer stop
	↓									
12	CSB 'L'									I/F Data transfer start
	↓									
13	MODESET	1	1	0	*	1	0	*	*	Display ON
	↓									
14	CSB 'H'									I/F Data transfer stop

○Start sequence example 2



This LSI is initialized with Initialize Sequence. And start to display with DISPON Sequence.  
 This LSI will update display data with RAM write Sequence.  
 And stop the display with DISPOFF sequence.  
 If you want to restart to display, This LSI will restart to display with DISPON Sequence.

**Initialize sequence**

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
Power on wait 100us CSB 'H' CSB 'L'									IC initialized I/F initialized
ICSET	1	1	1	0	1	0	1	0	Software Reset
MODESET	1	1	0	0	0	0	0	0	Display OFF
ADSET	0	0	0	0	0	0	0	0	RAM address set
Display Data	*	*	*	*	*	*	*	*	Display data
...									
CSB 'H'									

**DISPON sequence**

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB 'L'									
DISCTL	1	0	1	1	1	1	1	1	Display Control
BLKCTL	1	1	1	1	0	0	0	0	BLKCTL
APCTL	1	1	1	1	1	1	0	0	APCTL
MODESET	1	1	0	0	1	0	0	0	Display ON
CSB 'H'									

**RAM write sequence**

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB 'L'									
DISCTL	1	0	1	1	1	1	1	1	Display Control
BLKCTL	1	1	1	1	0	0	0	0	BLKCTL
APCTL	1	1	1	1	1	1	0	0	APCTL
MODESET	1	1	0	0	1	0	0	0	Display ON
ADSET	0	0	0	0	0	0	0	0	RAM address set
Display Data	*	*	*	*	*	*	*	*	Display data
...									
CSB 'H'									

**DISPOFF sequence**

Input	DATA								Description
	D7	D6	D5	D4	D3	D2	D1	D0	
CSB 'L'									
MODESET	1	1	0	0	0	0	0	0	Display OFF
CSB 'H'									