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Multi-function LCD Segment Drivers

BU97981xxx Series MAX 196 Segments (SEG49xCOM4)

Features

- Integrated RAM for Display Data (DDRAM): 49 x4 Bit (Max 196 Segment)
- LCD Drive Output: 4 Common Output, Max 49 Segment Output
- Integrated 3ch LED Driver Circuit
- Segment/ LED (Max 3port) Output Mode Selectable
- Segment/ GPO (Max 31port) Output Mode Selectable
- Support PWM Generation from Ext. or Internal Clock (Resolution: 8bit Mode/12bit Mode Selectable)
- Support Standby Mode
- Integrated Power-on-Reset Circuit (POR)
- Integrated Oscillator Circuit
- No External Component
- Low Power Consumption Design
- Independent Power Supply for LCD Driving
- Support Blink Function (Blink Frequency 1.6, 2.0, 2.6, 4.0Hz selectable)

Applications

- Telephone
- FAX
- Portable Equipment (POS, ECR, PDA etc.)
- DSC
- DVC
- Car audio
- Home Electrical Appliance
- Meter Equipment

etc.

Key Specifications

- Supply Voltage Range: +1.8V to +3.6V
- LCD Drive Power Supply Range: +3.3V to +5.5V
- Operating Temperature Range: -30°C to +75°C
- Max Segments:
  - BU97981KV 196 Segments
  - BU97981MUV 168 Segments
  - BU97981GU 196 Segments
- Max GPO Outputs:
  - BU97981KV 31port
  - BU97981MUV 27port
  - BU97981GU 31port
- Max LED Drive Outputs:
  - BU97981KV 3port
  - BU97981MUV 3port
  - BU97981GU 3port
- Display Duty: Static. 1/3, 1/4 Selectable
- Bias: Static, 1/3
- Integrated Regulator for LCD Drive: 3.2, 3.3, 3.4, 4.4, 4.5, 4.6, 5.0V Selectable
- Interface: 3wire Serial Interface

Typical Application Circuit

BU97981KV LED/GPO using case

LED : 3port
GPO : 5port
LCD :164seg

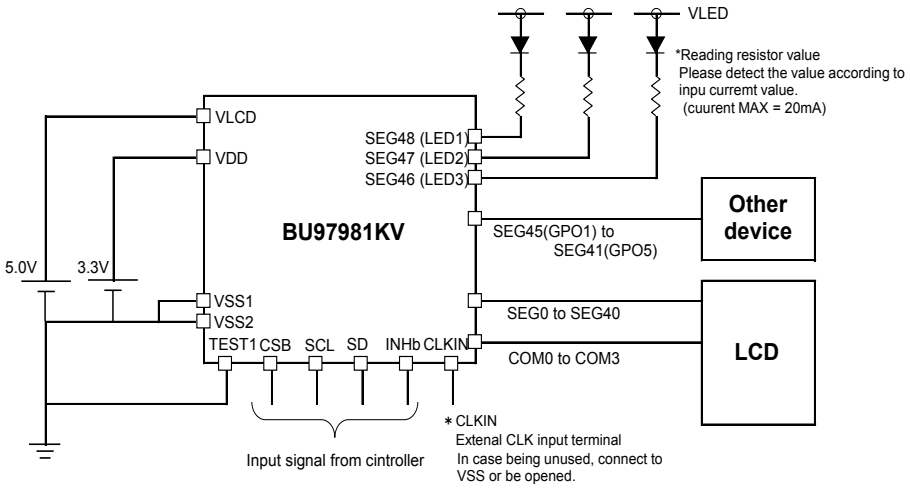


Figure 1. Typical Application Circuit

Block Diagram / Pin Arrangement / Pin Description

BU97981KV

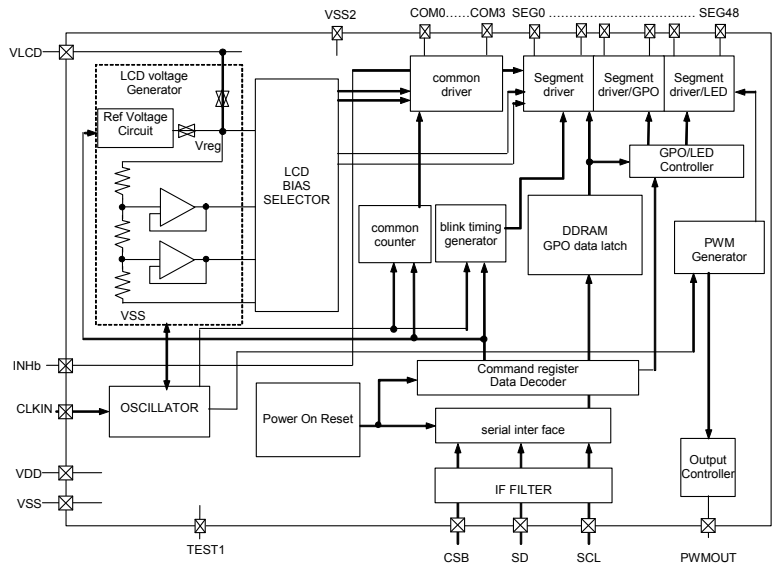


Figure 2. Block Diagram

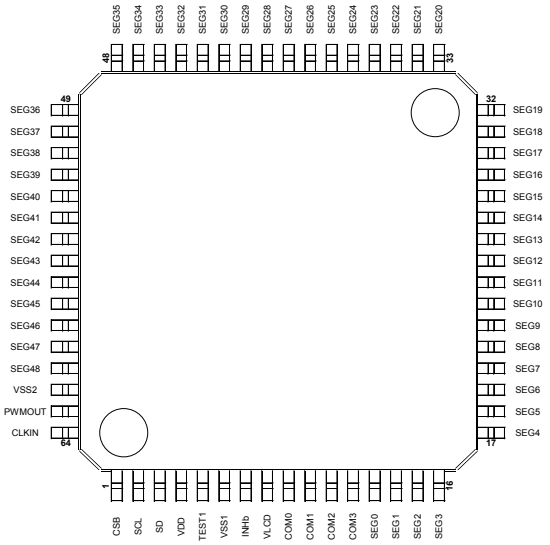


Figure 3. Pin Configuration (TOP VIEW)

Table 1. Pin Description

Terminal	Terminal number	I/O	Unused case	Function
CSB	1	I	-	Chip select: "L" active
SCL	2	I	-	Serial data transfer clock
SD	3	I	-	Input serial data
VDD	4	-	-	Power supply for LOGIC
CLKIN	64	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable) Support Hi-Z input mode at internal clock mode
TEST1	5	I	-	TEST terminal (Please connect VSS terminal)
VSS1	6	-	-	GND
VLCD	8	-	-	Power supply for LCD
INHb	7	I	VDD	Display turning on/off select terminal H: turning on display, L: turning off display INHb = “L”: All SEG/COM terminal : output VSS level GPO terminal : output VSS level LED drive terminal : output Hi-Z
PWMOUT	63	O	OPEN	PWM output for LED2 group
COM0 to 3	9 to 12	O	OPEN	COMMON output for LCD
SEG0 to 14	13 to 27	O	OPEN	SEGMENT output for LCD
SEG15 to 45	28 to 58	O	OPEN	SEGMENT output for LCD/GPO
SEG46 to 48	59 to 61	O	OPEN	SEGMENT output for LCD/LED driver
VSS2	62	-	GND	GND (for SEG46-48 / LED driver)

Block Diagram / Pin Arrangement / Pin Description

BU97981MUV

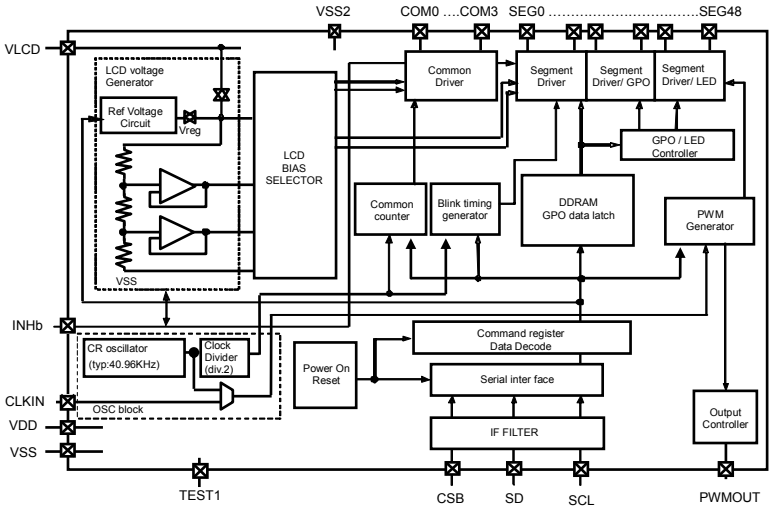


Figure 4. Block Diagram

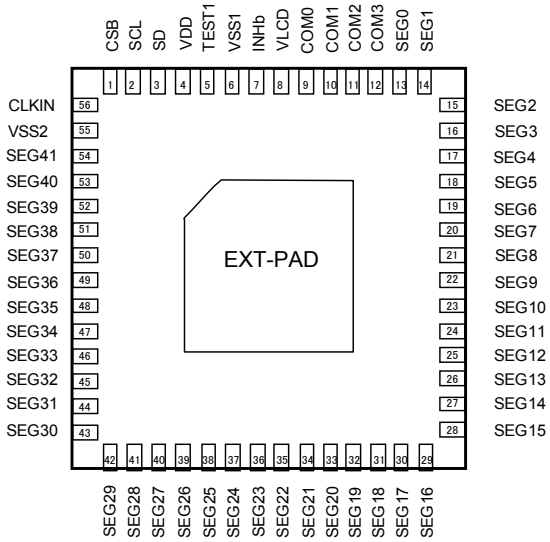


Figure 5. Pin Configuration (BOTTOM VIEW)

Table 2. Pin Description

Terminal	Terminal number	I/O	Unused case	Function
CSB	1	I	-	Chip select: "L" active
SCL	2	I	-	Serial data transfer clock
SD	3	I	-	Input serial data
VDD	4	-	-	Power supply for LOGIC
CLKIN	56	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable) Support Hi-Z input mode at internal clock mode
TEST1	5	I	-	TEST terminal (Please connect VSS terminal)
VSS1	6	-	-	GND
VLCD	8	-	-	Power supply for LCD
INHb	7	I	VDD	Display turning on/off select terminal H: turning on display, L: turning off display INHb = “L”: All SEG/COM terminal : output VSS level GPO terminal : output VSS level LED drive terminal : output Hi-Z
COM0~3	9-12	O	OPEN	COMMON output for LCD
SEG0~11	13-24	O	OPEN	SEGMENT output for LCD
SEG12~38	25-51	O	OPEN	SEGMENT output for LCD/GPO
SEG39~41	52-54	O	OPEN	SEGMENT output for LCD/LED driver
VSS2	55	-	GND	GND (for SEG39-41 / LED driver)
EXT-PAD	-(Note1)	-	VSS	substrate

(Note1) To radiate heat, please contact a board with the EXT-PAD which is located at the bottom side of VQFN56AV8080 package.
Please supply VSS level or Open state as the input condition for this PAD.

Block Diagram / Pin Arrangement / Pin Description

BU97981GU

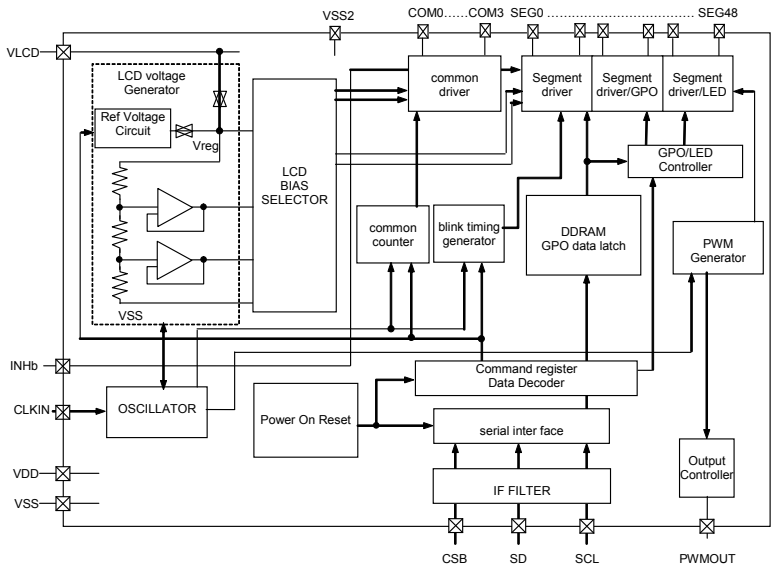


Figure 6. Block Diagram

	1	2	3	4	5	6	7	8
H	SEG4	SEG5	SEG9	SEG11	SEG14	SEG16	SEG18	SEG20
G	SEG2	SEG3	SEG7	SEG8	SEG12	SEG17	SEG19	SEG21
F	SEG0	SEG1	SEG6	SEG10	SEG13	SEG22	SEG23	SEG25
E	COM2	COM0	COM1	COM3	SEG15	SEG26	SEG24	SEG27
D	VLCD	VDD	INHB	SEG47	SEG31	SEG29	SEG28	SEG30
C	VSS1	SDA	SCL	SEG45	SEG42	SEG38	SEG33	SEG32
B	(NC)	CLKIN	VSS2	SEG44	SEG40	SEG39	SEG35	SEG34
A	CSB	PWM OUT	SEG48	SEG46	SEG43	SEG41	SEG37	SEG36

Figure 7. Pin Configuration (TOP VIEW)

Table 3. Pin Description

Terminal	I/O	Unused case	Function
CSB	I	-	Chip select: "L" active
SCL	I	-	Serial data transfer clock
SD	I	-	Input serial data
VDD	-	-	Power supply for LOGIC
CLKIN	I	OPEN / VSS	External clock input terminal (for display/PWM using selectable) Support Hi-Z input mode at internal clock mode
VSS1	-	-	GND
VLCD	-	-	Power supply for LCD
INHb	I	VDD	Display turning on/off select terminal H: turning on display, L: turning off display INHb = “L”: All SEG/COM terminal : output VSS level GPO terminal : output VSS level LED drive terminal : output Hi-Z
PWMOUT	O	OPEN	PWM output for LED2 group
COM0 to 3	O	OPEN	COMMON output for LCD
SEG0 to 14	O	OPEN	SEGMENT output for LCD
SEG15 to 45	O	OPEN	SEGMENT output for LCD/GPO
SEG46 to 48	O	OPEN	SEGMENT output for LCD/LED driver
VSS2	-	GND	GND (for SEG46-48 / LED driver)

Absolute Maximum Ratings (VSS=0V)

Parameter	Symbol	Ratings	Unit	Remarks
Power Supply Voltage 1	VDD	-0.3 to +4.5	V	Power supply
Power Supply Voltage 2	VLCD	-0.5 to +7.0	V	Power supply for LCD
Power Dissipation	Pd	1.0 (Note1)	W	BU97981KV
		3.6 (Note2)		BU97981MUV
		0.8 (Note3)		BU97981GU
Input Voltage Range	VIN	-0.5 to VDD+0.5	V	
Operational Temperature Range	Topr	-30 to +75	°C	
Storage Temperature Range	Tstg	-55 to +125	°C	
Output Current	Iout1	5	mA	SEG output
	Iout2	5	mA	COM output
	Iout3	10	mA	GPO output
	Iout4	50	mA	LED output

(Note1) When use more than Ta=25°C, subtract 10mW per degree. (using ROHM standard board)
(board size：70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only).
(Note2) When use more than Ta=25°C, subtract 36mW per degree. (using ROHM standard board)
(board size：74.2mm×74.2mm×1.6mm SEMI standard 4 layer board)
(Note3) When operated higher than Ta=25°C, subtract 8.0mW per degree. (using ROHM standard board)
(board size：114.3mm×76.2mm×1.6mm)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-30°C to +75°C,VSS=0V)

Parameter	Symbol	Ratings			Unit	Remarks
		Min	Typ	Max		
Power Supply Voltage 1	VDD	1.8	-	3.6	V	Power supply
Power Supply Voltage 2	VLCD	3.3	-	5.5	V	Power supply for LCD
LED Supply Voltage	VLED	1.0	-	VLCD	V	Power supply for LED
Output Current	Iout4	-	-	20	mA	Per LED port 1ch
	Iout4	-	-	60	mA	Total LED port current

Electrical Characteristics

DC characteristics (Ta=-30°C to +75°C, VDD=1.8V to 3.6V, VLCD=3.3V to 5.5V, VSS=0)
(BU97981KV,BU97981GU)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
“H” level Input Voltage	VIH	0.8VDD	-	VDD	V	SD, SCL, CSB, TEST1(Note4),CLKIN, INHb
“L” level Input Voltage	VIL	VSS	-	0.2VDD	V	SD, SCL, CSB, TEST1(Note4),CLKIN, INHb
Hysteresis Width	VH	-	0.2	-	V	SCL, INHb, VDD=3.3V, Ta=25°C
“H” Level Input Current	IIH1	-	-	5	μA	SD, SCL, CSB, CLKIN, INHb, VI=3.6V
“L” Level Input Current	IIL1	-5	-	-	μA	SD, SCL, CSB, CLKIN, INHb, TEST1(Note4), VI=0V
“H” Level Output Voltage (Note1&3)	VOH1	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V SEG0 to SEG48, Unused integrated regulator
	VOH2	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V, COM0 to COM3, Unused integrated regulator
	VOH3	VLCD -0.6	-	-	V	Iload=-1mA,VLCD=5.0V, SEG15 to SEG45 (GPO mode) Unused integrated regulator
	VOH4	VDD -0.6	-	-	V	Iload=-1mA, VDD=3.0V, PWMOUT
“L” Level Output Voltage (Note3)	VOL1	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, SEG0 to SEG48
	VOL2	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, COM0 to COM3
	VOL3	-	-	0.5	V	Iload=1mA, VLCD=5.0V, SEG15 to SEG45 (GPO mode), PWMOUT
	VOL4	-	0.11	0.5	V	Iload=20mA, VLCD=5.0V, SEG46 to 48 (LED drive mode)
Current Consumption (Note2)	IstVDD	-	3	10	μA	Input terminal ALL’L’, Display off, Oscillation off
	IstVLCD	-	0.5	5	μA	Input terminal ALL’L’, Display off, Oscillation off
	IVDD1	-	8	15	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM generate off, All output pin open
	IVDD2	-	90	130	μA	VDD=3.3V, Ta=25°C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open
	IVLCD1	-	10	15	μA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, Unused Integrated regulator, LED generate off, All output pin open
	IVLCD2	-	25	40	μA	VLCD=5.0V, Ta=25°C, 1/3bias, fFR=64Hz, Used Integrated regulator, LED generate off, All output pin open
	IVLCD3	-	30	48	μA	VLCD=5.0V, Ta=25°C,1/3bias, fFR=64Hz, Used Integrated regulator, PWM Frequency=500Hz setting, All output pin open

(Note1) Integrated regulator using case, please add load regulation value to output voltage listed above.
(Note2) Power save mode 1 and frame inversion setting
(Note3) Iload: In case, load current from only one port
(Note4) There is not TEST1 port in BU97981GU

Electrical Characteristics – Continued

DC characteristics (Ta=-30°C to +75°C, VDD=1.8V to 3.6V, VLCD=3.3V to 5.5V, VSS=0)
(BU97981MUV)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
“H” level Input Voltage	VIH	0.8VDD	-	VDD	V	SD, SCL, CSB, TEST1,CLKIN, INHb
“L” level Input Voltage	VIL	VSS	-	0.2VDD	V	SD, SCL, CSB, TEST1,CLKIN, INHb
Hysteresis Width	VH	-	0.2	-	V	SCL, INHb, VDD=3.3V, Ta=25°C
“H” level Input Current	IIH1	-	-	5	μA	SD, SCL, CSB, CLKIN, INHb, VI=3.6V
“L” level Input Current	IIL1	-5	-	-	μA	SD, SCL, CSB, CLKIN, INHb, TEST1, VI=0V
“H” Level Output Voltage (Note1&3)	VOH1	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V SEG0 to SEG41, Unused integrated regulator
	VOH2	VLCD -0.4	-	-	V	Iload=-50μA, VLCD=5.0V, COM0 to COM3, Unused integrated regulator
	VOH3	VLCD -0.6	-	-	V	Iload=-1mA,VLCD=5.0V, SEG12 to SEG38 (GPO mode) Unused integrated regulator
“L” Level Output Voltage (Note3)	VOL1	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, SEG0 to SEG41
	VOL2	-	-	0.4	V	Iload= 50μA, VLCD=5.0V, COM0 to COM3
	VOL3	-	-	0.5	V	Iload=1mA, VLCD=5.0V, SEG12 to SEG38 (GPO mode), PWMOUT
	VOL4	-	0.11	0.5	V	Iload=20mA, VLCD=5.0V, SEG39 to SEG41 (LED drive mode)
Current Consumption (Note2)	IstVDD	-	3	10	μA	Input terminal ALL’L’, Display off, Oscillation off
	IstVLCD	-	0.5	5	μA	Input terminal ALL’L’, Display off, Oscillation off
	IVDD1	-	8	15	μA	VDD=3.3V, Ta=25˚C, 1/3bias, fFR=64Hz, PWM generate off, All output pin open
	IVDD2	-	90	130	μA	VDD=3.3V, Ta=25˚C, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open
	IVLCD1	-	10	15	μA	VLCD=5.0V, Ta=25˚C, 1/3bias, fFR=64Hz, Unused Integrated regulator, LED generate off, All output pin open
	IVLCD2	-	25	40	μA	VLCD=5.0V, Ta=25˚C, 1/3bias, fFR=64Hz, Used Integrated regulator, LED generate off, All output pin open
	IVLCD3	-	30	48	μA	VLCD=5.0V, Ta=25˚C,1/3bias, fFR=64Hz, Used Integrated regulator, PWM Frequency=500Hz setting, All output pin open

(Note1) Integrated regulator using case, please add load regulation value to output voltage listed above.
(Note2) Power save mode 1 and frame inversion setting
(Note3) Iload: In case, load current from only one port

Electrical Characteristics – continued

Integrated Regulator Characteristics (Ta=-30°C to +75°C, VDD=1.8V to 3.6V, VLCD=3.3V to 5.5V, VSS=0)
(BU97981KV)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Output Voltage 1	Vreg1	4.35	4.5	4.65	V	4.5V setting (VLCD=5.5V, Ta=-30°C to 75°C) (Note1)
Output Voltage 2	Vreg2	4.42	4.5	4.58	V	4.5V setting (VLCD=5.5V, Ta=25°C) (Note1)
Load Regulation (Note2)	delta Vreg	-	-	0.3	V	Iout = -300μA

(Note1)In case integrated regulator using, please satisfy condition that Vreg output lower than VLCD - 0.5V.
(Note2) Load regulation: Vreg block load regulation only. Do not include other block ability.

(BU97981MUV)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Output Voltage 1	Vreg1	4.30	4.5	4.70	V	4.5V setting (VLCD=5.5V, Ta=-30°C to 75°C) (Note1)
Output Voltage 2	Vreg2	4.38	4.5	4.62	V	4.5V setting (VLCD=5.5V, Ta=25°C) (Note1)
Load Regulation (Note2)	delta Vreg	-	-	0.3	V	Iout = -300μA

(Note1)n case integrated regulator using, please satisfy condition that Vreg output lower than VLCD – 0.5V.
(Note2) Load regulation: Vreg block load regulation only. Do not include other block ability.

(BU97981GU)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Output Voltage 1	Vreg1	4.25	4.5	4.70	V	4.5V setting (VLCD=5.5V, Ta=-30°C to 75°C) (Note1)
Output Voltage 2	Vreg2	4.40	4.5	4.60	V	4.5V setting (VLCD=5.5V, Ta=25°C) (Note1)
Load Regulation (Note2)	delta Vreg	-	-	0.3	V	Iout = -300μA

(Note1)In case integrated regulator using, please satisfy condition that Vreg output lower than VLCD - 0.5V.
(Note2) Load regulation: Vreg block load regulation only. Do not include other block ability.

Oscillation Frequency Characteristics (Ta=-30°C to +75 °C, VDD=1.8V to 3.6V, VLCD=3.3V to 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Frame Frequency 1	fFR1	57.6	64	70.4	Hz	VDD=3.3V, Ta=25°C, fFR=64Hz setting
Frame Frequency 2	fFR2	51.2	64	73.0	Hz	VDD=2.5V to 3.6V fFR=64Hz setting
Frame Frequency 3	fFR3	45.0	-	64	Hz	VDD=1.8V to 2.5V fFR=64Hz setting
CLKIN Input Frequency	fCLK	-	2	4	MHz	

About detail function, please refer to the frame frequency setting of DISCTL command.

MPU Interface Characteristics (Ta=-30°C to +75 °C, VDD=1.8V to 3.6V, VLCD=3.3V to 5.5V, VSS=0)

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input Rise Time	tr	-	-	50	ns	
Input Fall Time	tf	-	-	50	ns	
SCL Cycle Time	tSCYC	250	-	-	ns	
“H” SCL Pulse Width	tSHW	50	-	-	ns	
“L” SCL Pulse Width	tSLW	50	-	-	ns	
SD Setup Time	tSDS	50	-	-	ns	
SD Hold Time	tSDH	50	-	-	ns	
CSB Setup Time	tCSS	50	-	-	ns	
CSB Hold Time	tCSH	50	-	-	ns	
“H” CSB Pulse Width	tCHW	50	-	-	ns	

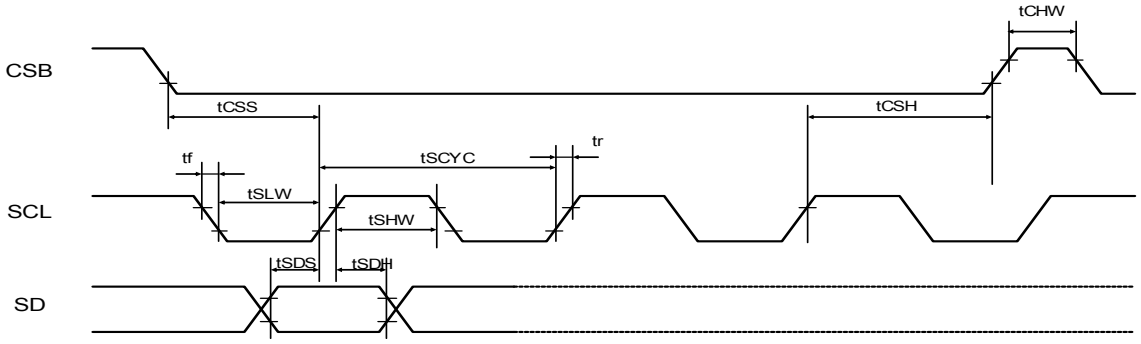


Figure 8. Serial Interface Timing

I/O Equivalence Circuit

(BU97981KV)

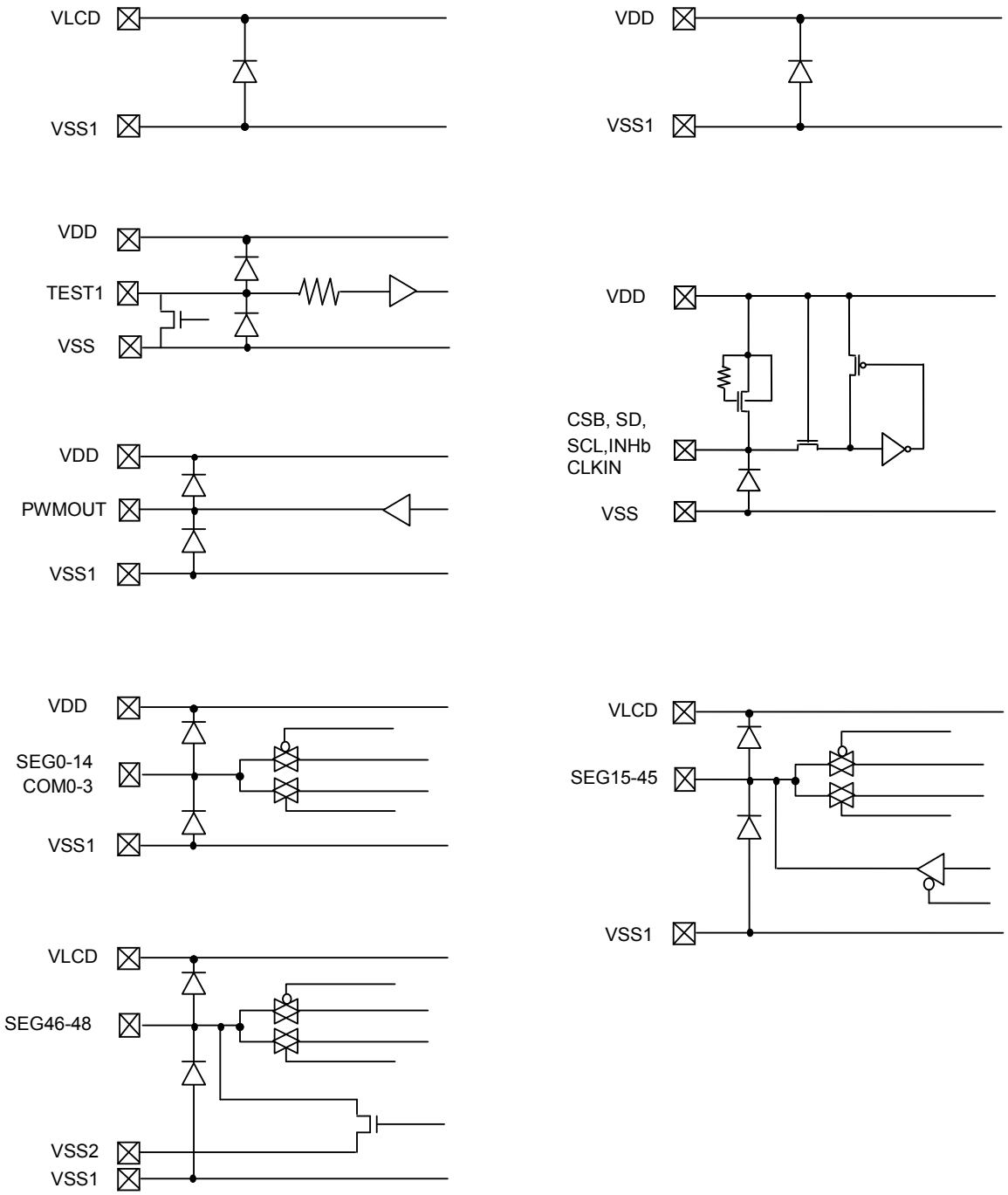


Figure 9. I/O Equivalence Circuit

I/O Equivalence Circuit - Continued

(BU97981MUV)

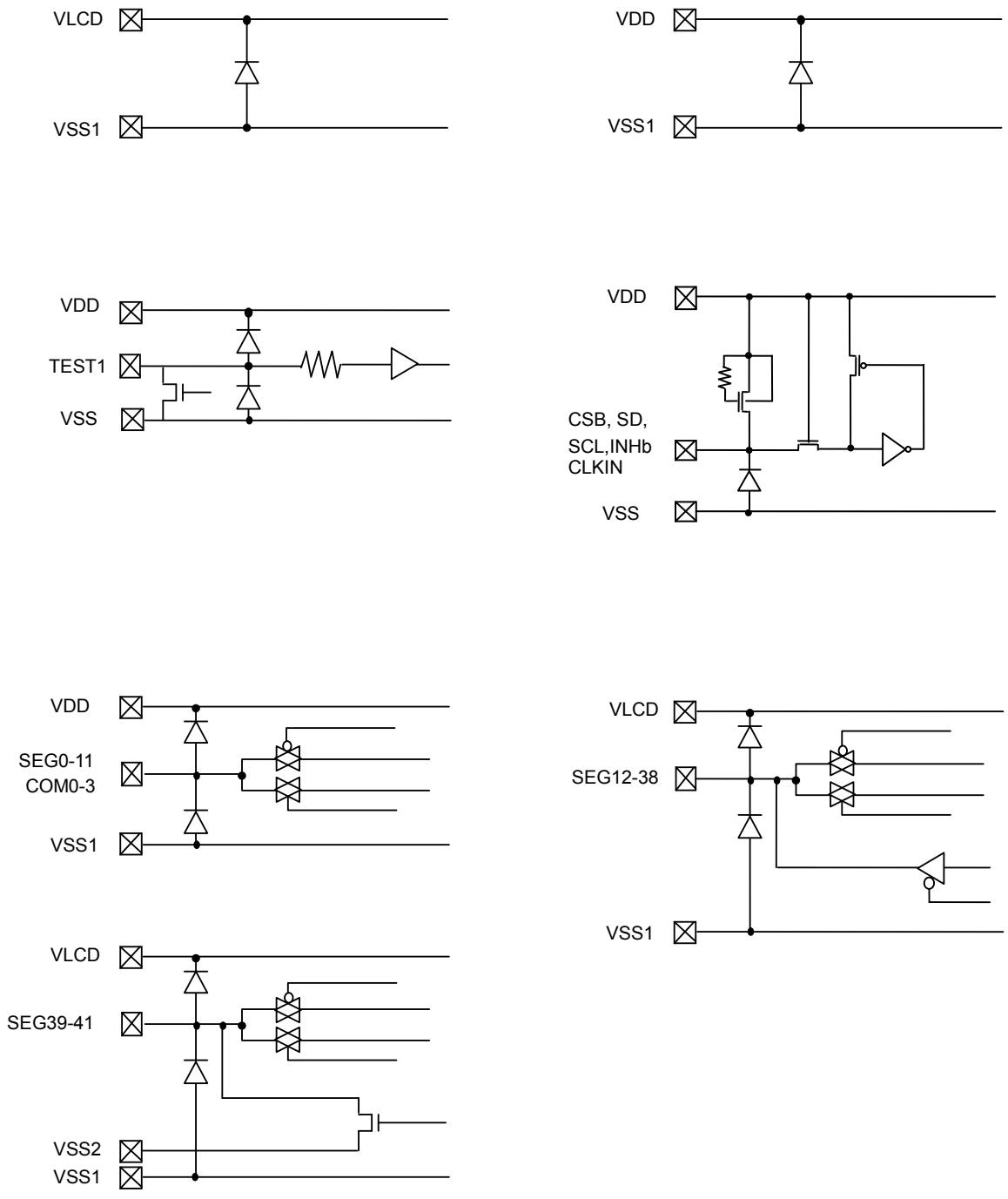


Figure 10. I/O Equivalence Circuit

I/O Equivalence Circuit - Continued

(BU97981GU)

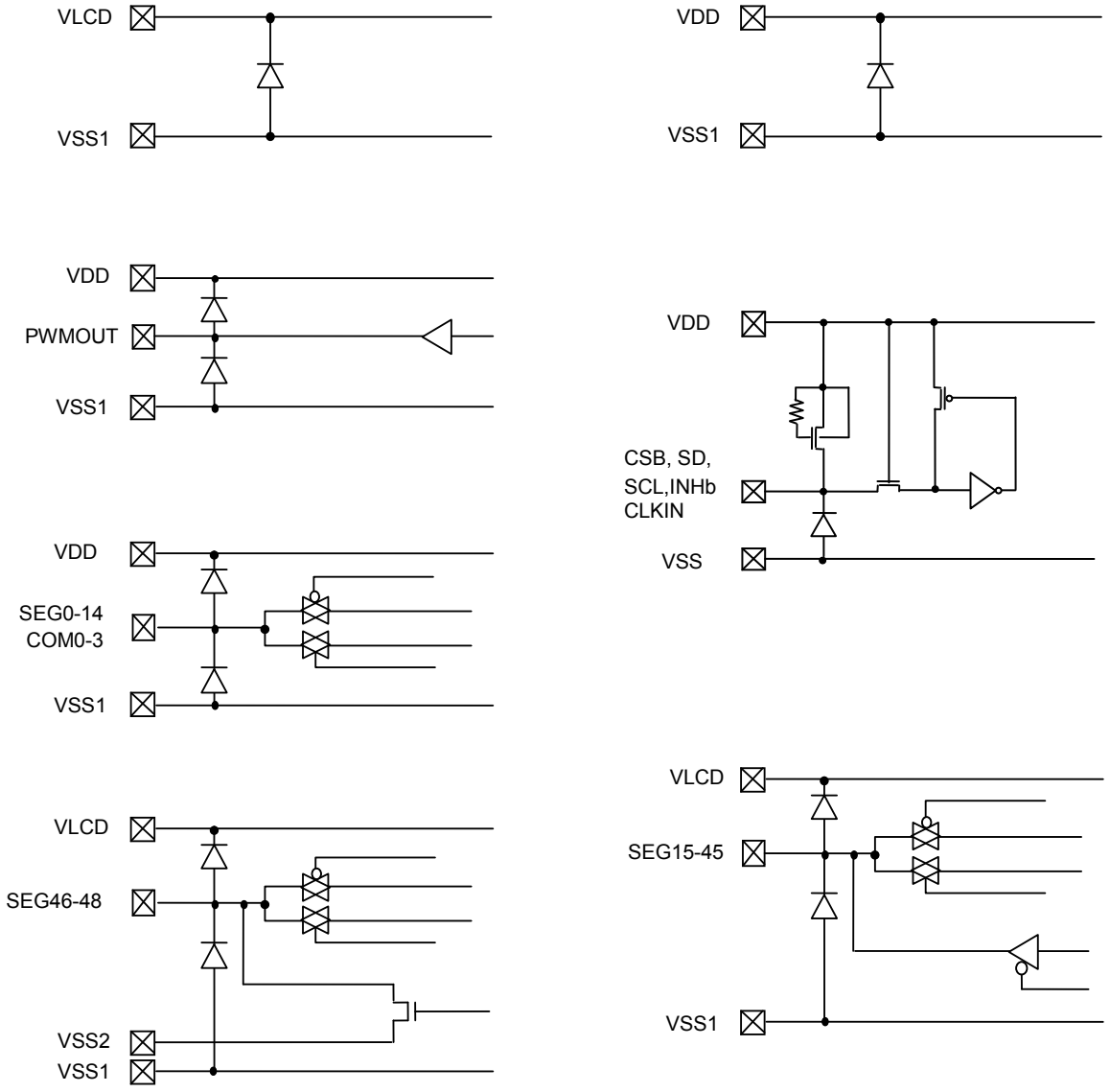
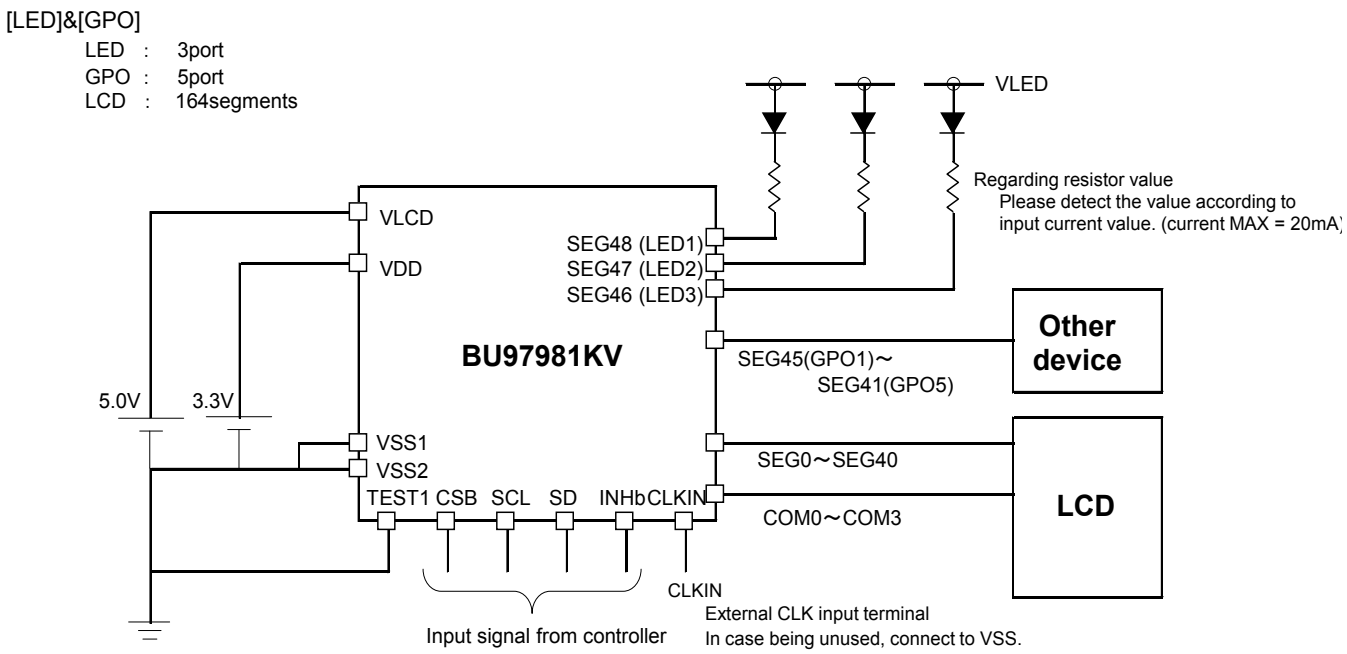


Figure 11. I/O Equivalence Circuit

Example of Recommended Circuit

(BU97981KV)

1. LED/GPO Using Case



2. SEG Output Only Case

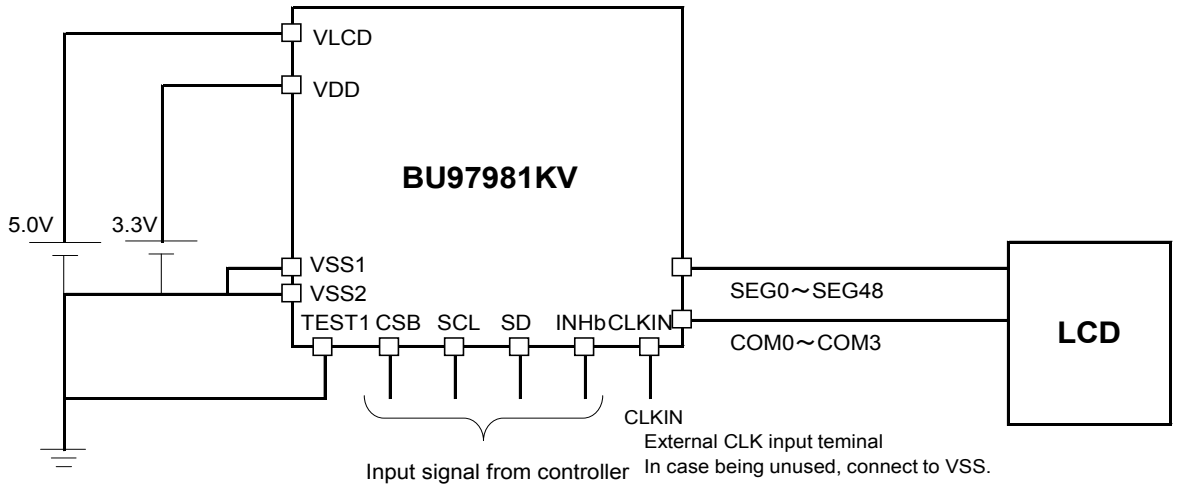
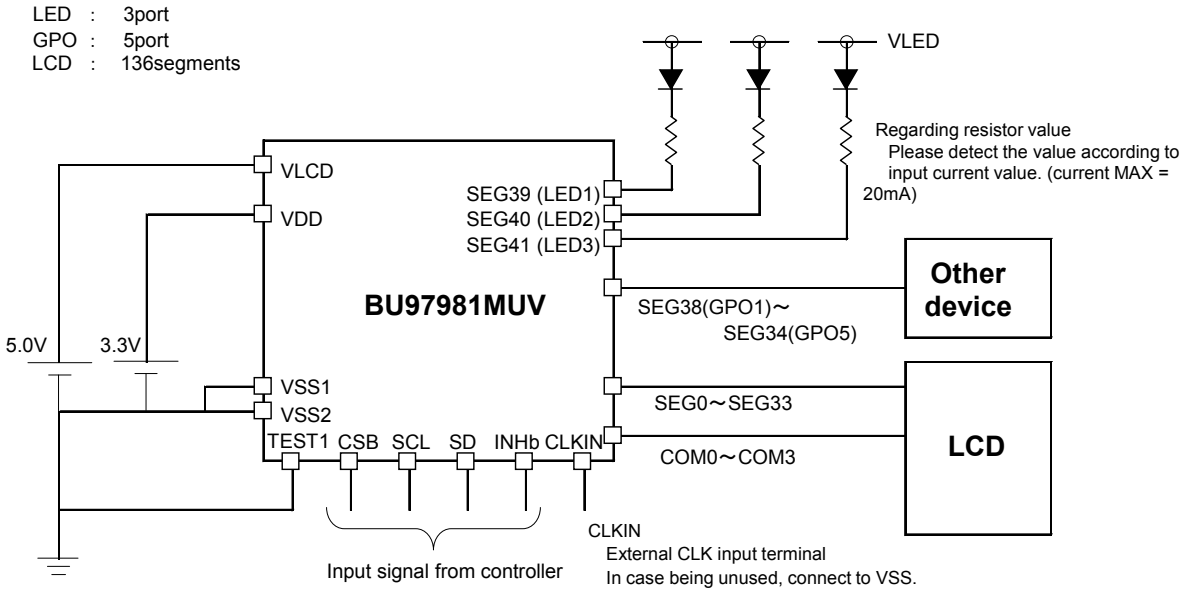


Figure 12. BU97981KV E.g. of Recommended Circuit

Example of Recommended Circuit – Continued

(BU97981MUV)

1. LED/GPO Using Case



2. SEG Output Only Case

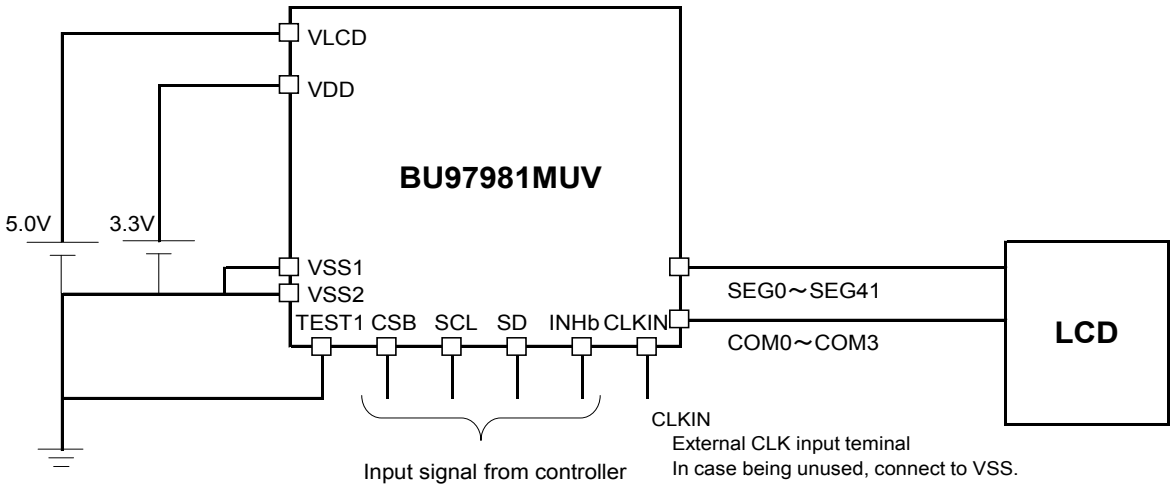
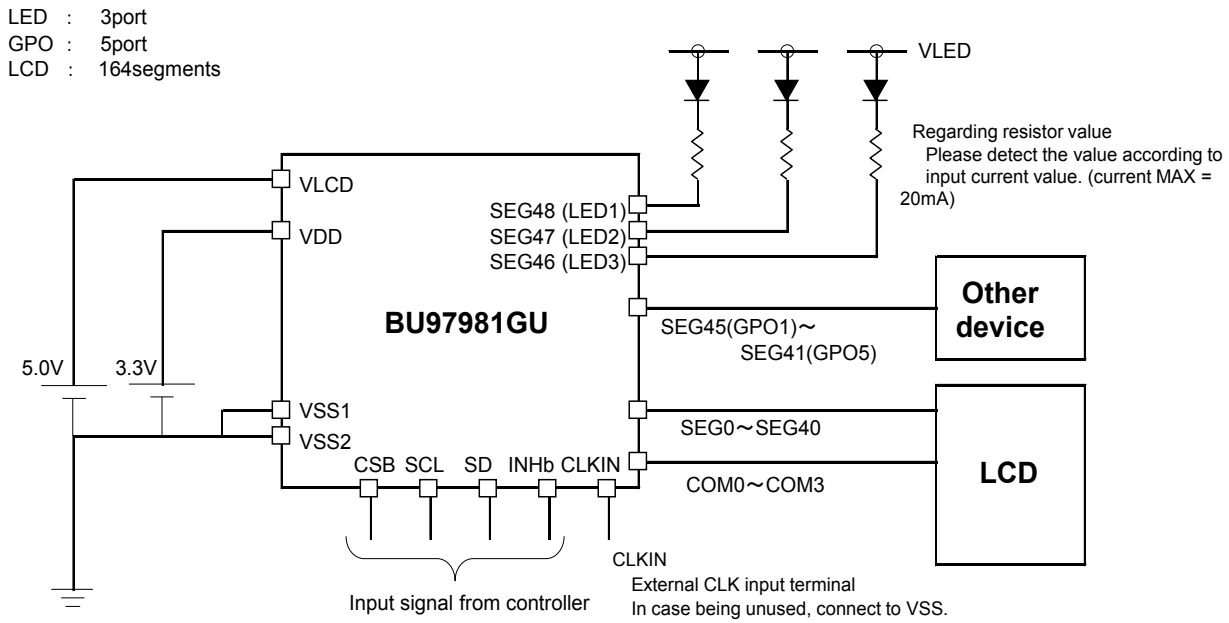


Figure 13. BU97981MUV E.g. of Recommended Circuit

Example of Recommended Circuit – Continued

(BU97981GU)

1. LED/GPO Using Case



2. SEG Output Only Case

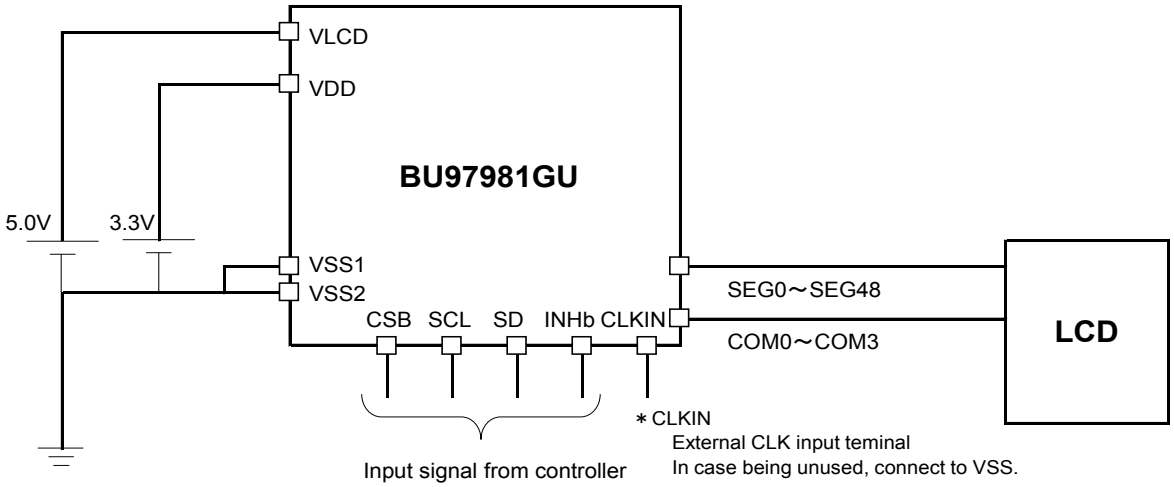


Figure 14. BU97981GU E.g. of Recommended Circuit

Function Descriptions

Command and Data Transfer Method

3-SPI (3 wire serial interface)
This device is controlled by 3-wire signal (CSB, SCL, and SD).
First, Interface counter is initialized with CSB="H",
and CSB="L" makes SD and SCL input enable.
The protocol of 3-SPI transfer is as follows.
Each command starts with Command or Data judgment bit (D/C) as MSB data,
and continuously in order of D6 to D0 are followed after CSB ="L".
(Internal data is latched at the rising edge of SCL, it converted to 8bits parallel data at the falling edge of 8th CLK.)

When CSB rise from "L" to "H", and at this time sending commands are less than 8bit, command and data transfer are canceled. To start sending command again, please fall CSB="L" and send command continuously.

After sending RAMWR or BLKWR or GPOSET command, BU97981KV/MUV is in the RAM data input mode. Under this mode, device can not accept new commands.

In this case, please rise CSB="H" and fall CSB="L", after this sequence device released from RAM data input mode, and can accept new command.

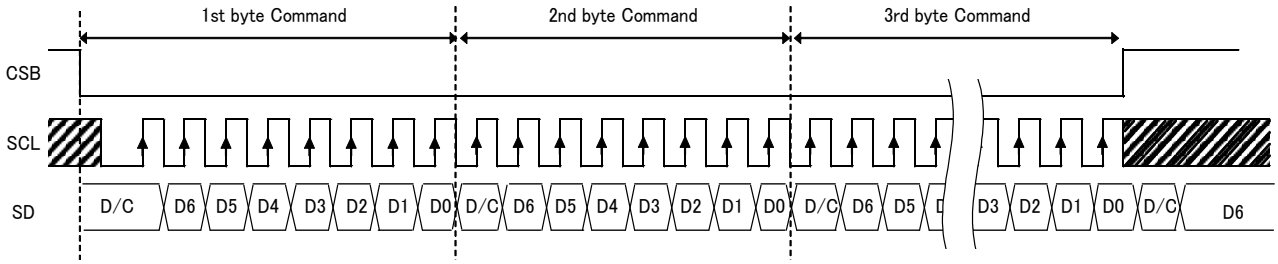
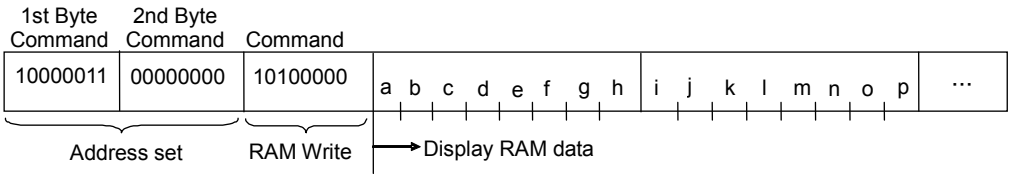


Figure 15. 3-SPI Data Transfer Format

8bit data, sending after RAMWR command, are display RAM data
8bit data, sending after BLKWR command, are blink RAM data
SCL and SD can be set to "H" or cleared to "L" during CSB="H"

Write Display Data and Transfer Method

This device has Display Data RAM (DDRAM) of 49×4=196bit.
The relationship between data input and display data, DDRAM data and address are as follows.

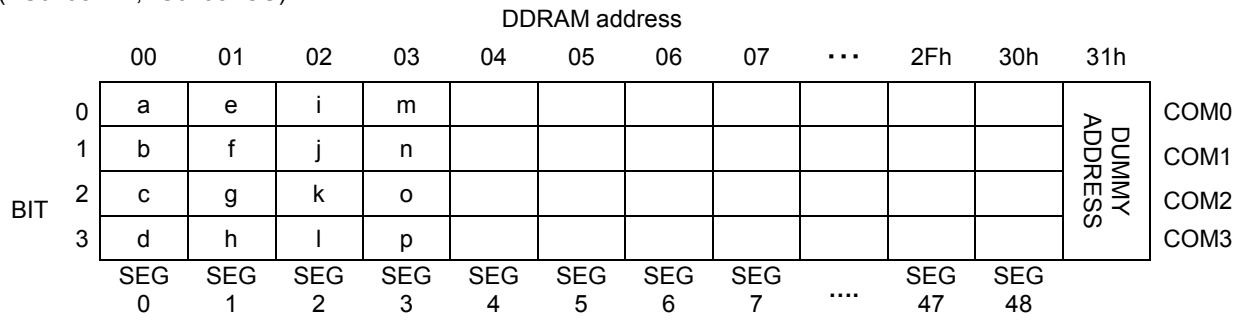


According to this command, 8bit binary data will write to DDRAM. The address which starts data writing is specified by "ADSET" command, and increment after finish writing display data every 4 bit.

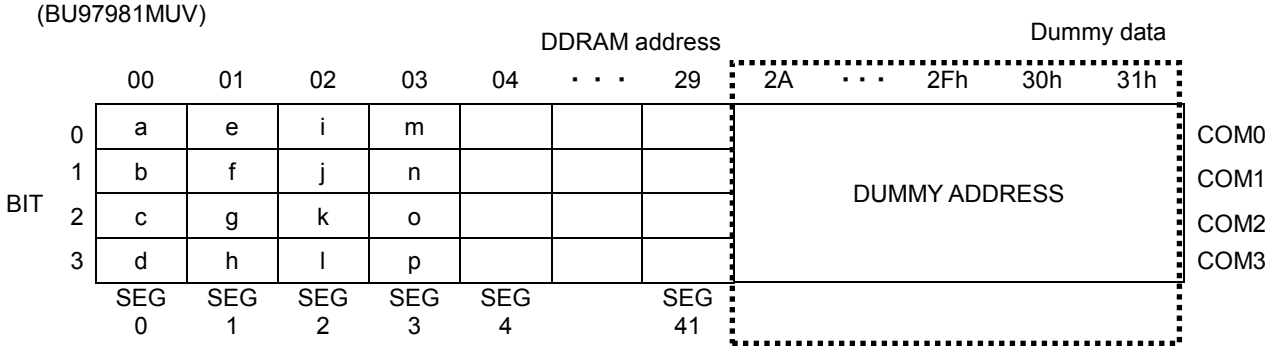
It is able to write to DDRAM by continuously sending data.
(In case data is sent continuously after write date at 30h (KV: SEG48), RAM data will be written to 31h (dummy address) and return to address 00h (SEG0) automatically.)

In case, SEG port assigned to GPO or LED port by OUTSET1 command, corresponding SEG address do not change and used as dummy address.

(BU97981KV,BU97981GU)



(BU97981MUV)



Display data write to DDRAM every 4bits.
In case CSB change from "L" to "H" before 4bits data transfer finish, RAM write is canceled.

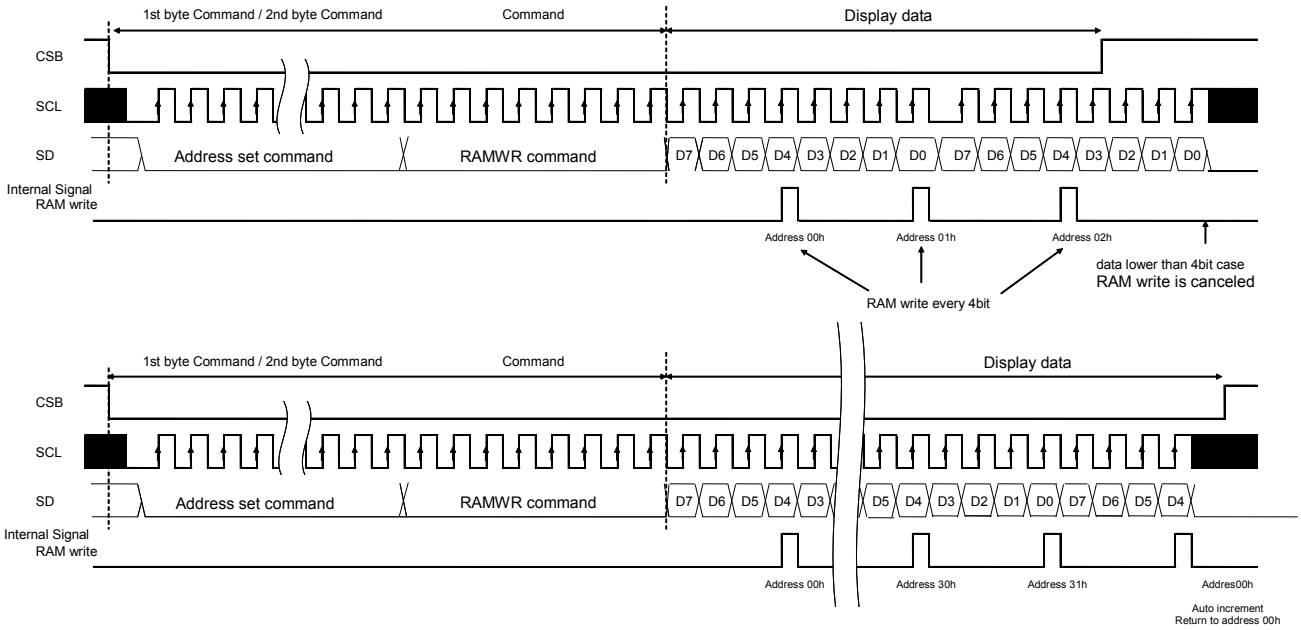


Figure 16. Display Data Transfer Method

Blink Function

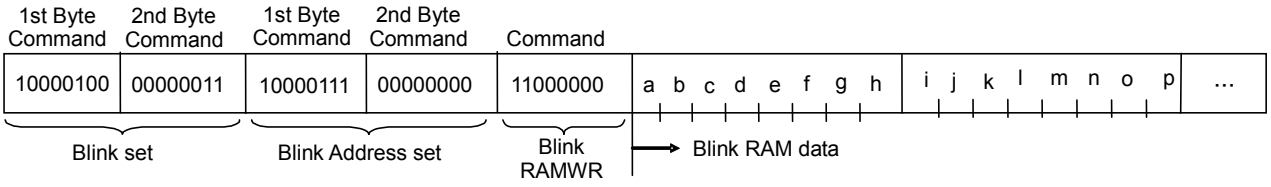
This device has Blink function. Blink function is able to set each segment port individually.
Blink ON/OFF and Blink frequency are set by the BLKSET command.
Blink frequency varies, according to fCLK characteristics.
Blink setup of each segments are controlled by BLKWR command.

The write start address is specified by “BLKADSET” command. And this address will increment after finish writing blink data every 4 bit. The relation of BLKWR command, blink ram data, and blinking segment port is below.

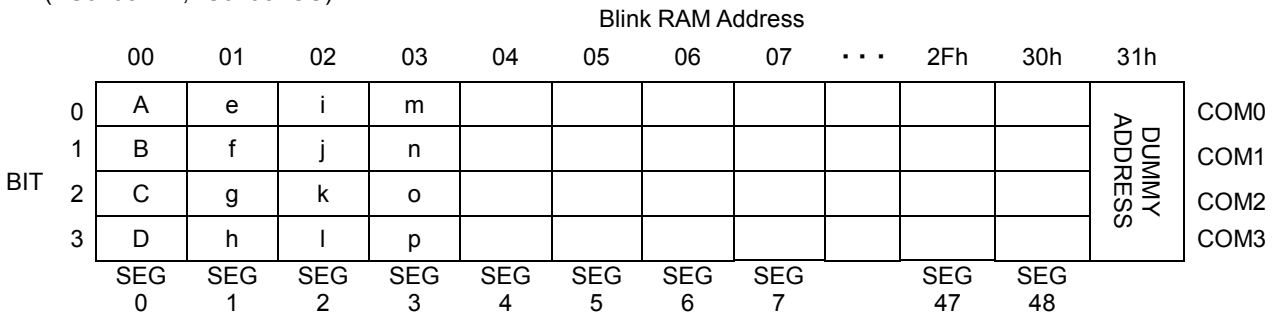
In case of data is “1”, segment will blink, on the other hand data is “0”, do not blink.
(In case data is written continuously, after write date at 30h (KV: SEG48), ram data will be written to 31h (dummy address) and return to address 00h (SEG0) automatically.)

Please refer to following figure about Blink operation of each segment.

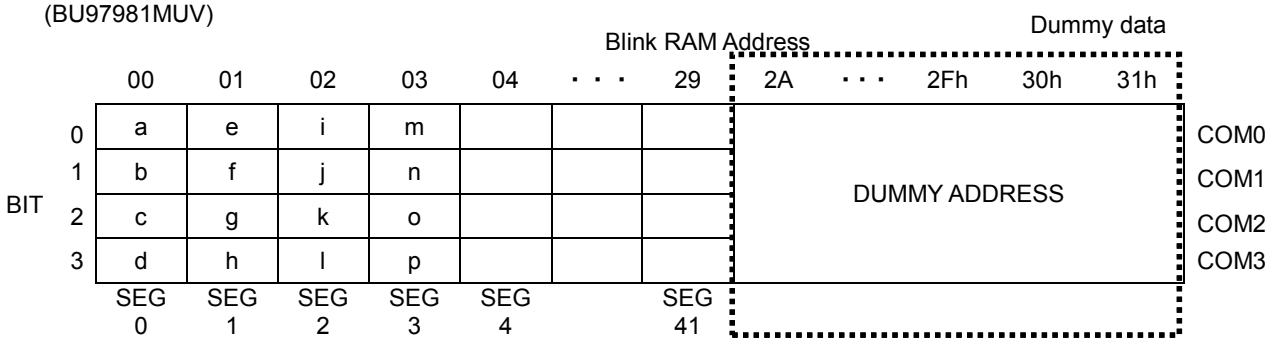
In case, SEG port assigned to GPO or LED port by OUTSET1 command, corresponding SEG address do not change and used as dummy address.



(BU97981KV,BU97981GU)



(BU97981MUV)



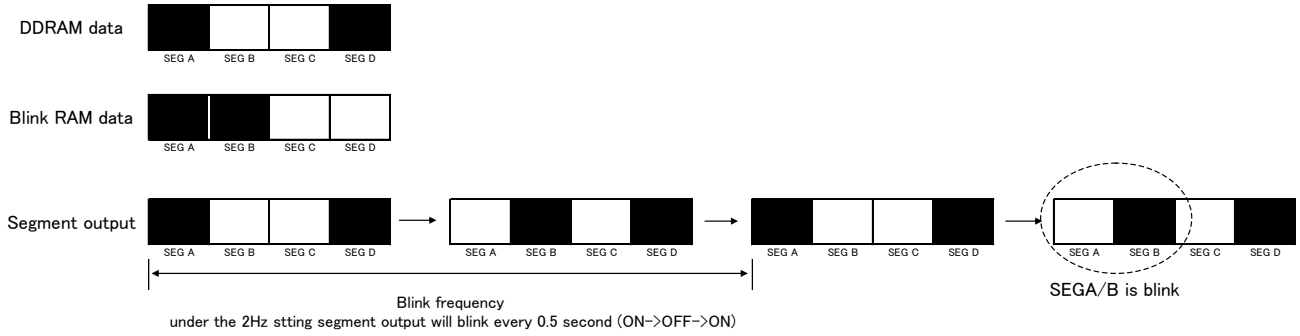


Figure 17. Blink Operation

LCD Driver Bias/Duty Circuit

This LSI generates LCD driving voltage with on-chip Buffer AMP.
And it can drive LCD at low power consumption
Line and frame inversion can be set in MODESET command.
1/4duty, 1/3duty and static mode can be set DISCTL command.
About each LCD driving waveform, please refer to “LCD driving waveform” descriptions.

Initial state

Initial state, after Software Reset command input
1. Display off
2. All command register value set Reset state.
3. DDRAM address data and Blink address data are initializing
(DDRAM data and Blink RAM data are not initializing.
Please write DDRAM data and Blink RAM data before Display on.)

Command / Function list

Function Description Table

NO	Command	Function
1	Mode Set (MODESET)	Set LCD drive mode (display on/off, current mode)
2	Display control (DISCTL)	Set LCD drive mode (frame freq., line/frame inversion)
3	Address set (ADSET)	Set display data RAM address for RAMWR command
4	Blink set (BLKSET)	Set Blink mode on/off
5	Blink address set (BLKADSET)	Set Blink data RAM address for BLKWR command
6	SEG/GPO port change (OUTSET1)	Select segment output/general purpose output (GPO)
7	SEG/LED port change (OUTSET2)	Select segment output/LED driving output
8	LED1 drive control (PWM1SET) (H piece adjustment of PWM1)	Set PWM1 signal “H” width for LED1 driving
9	LED2-3 drive control (PWM2SET) (H piece adjustment of PWM2)	Set PWM2 signal “H” width for LED2-3 driving
10	Display data RAM WRITE (RAMWR)	Write display data to display data RAM
11	Blink RAM WRITE (BLKWR)	Write Blink data to BLINK data RAM
12	All Pixel ON (APON)	Set all Pixel display on
13	All Pixel OFF (APOFF)	Set all Pixel display off
14	All Pixel On/Off mode off (NORON)	Set normal display mode (APON/APOFF cancel)
15	Software Reset (SWRST)	Software Reset
16	OSC external input (OSCSET)	Set External clock input
17	Integrated Regulator setup (REGSET)	Set integrated regulator voltage output
18	GPO output set (GPOSET)	Set GPO output data

Command Detail Descriptions

D/C, Data / Command judgment bit (MSB)
Detail, please refer to 3wire serial I/F

Mode Set (MODESET)

	MSB							LSB		
	D/C	D6	D5	D4	D3	D2	D1	D0	Hex	Reset
1st byte command	1	0	0	0	0	0	0	1	81h	-
2nd byte command	0	0	0	0	P3	P2	P1	P0	-	00h

Display Set

Condition	P3	Reset state
Display OFF	0	○
Display ON	1	

Display OFF : No LCD driving mode (Output: VSS Level)
Turn off OSC circuit and LCD power supply circuit. (Synchronized with frame freq)
Display ON : LCD driving mode
Turn on OSC circuit and LCD power supply circuit.
Read data from DDRAM and display to LCD.

LED port and GPO port output state are not influenced by a Display on/off state
Output state is decided by command setup (GPOSET, OUTSET1, OUTSET2, PWM1SET, PWM2SET) and INHb terminal state. About detail, please refer to each command description.

LCD drive mode set

Condition	P2	Reset state
Frame inversion	0	○
Line inversion	1	

Current mode set

Condition	P1	P0	Reset state
Power save mode1	0	0	○
Power save mode2	0	1	
Normal mode	1	0	
High power mode	1	1	

(Reference data of consumption current)

Condition	Current consumption
Power save mode 1	×1.0
Power save mode 2	×1.7
Normal mode	×2.7
High power mode	×5.0

The value changes according to the panel load.

Display Control (DISCTL)

	MSB D/C	D6	D5	D4	D3	D2	D1	LSB D0	Hex	Reset
1st byte Command	1	0	0	0	0	0	1	0	82h	-
2nd byte Command	0	0	0	0	P3	P2	P1	P0	-	02h

Duty Set

Condition	P3	P2	Reset state
1/4duty (1/3bias)	0	0	○
1/3duty (1/3bias)	0	1	
Static (1/1bias)	1	*	

*: Don't care

In 1/3duty, Display data and Blink data of COM3 is ineffective.
COM1 and COM3 output are same data.

Please be careful of transmission of display data and blink data.
The examples of SEG/COM output waveform, under the each Bias/Duty set up, are shown at "LCD Driver Bias/Duty Circuit" description.

Frame Frequency Set

Condition (1/4,1/3,1/1duty)	P1	P0	Reset state
(128Hz, 130Hz, 128Hz)	0	0	
(85Hz, 86hz, 64Hz)	0	1	
(64Hz, 65Hz, 48Hz)	1	0	○
(51Hz, 52Hz, 32Hz)	1	1	

Relation table, between Frame frequencies (FR), integrated oscillator circuit (OSC) and Divide number.

DISCTL (P1,P0)	Divide			FR [Hz] (Note1)		
	Duty set (P3,P2)			Duty set (P3,P2)		
	(0,0) 1/4duty	(0,1) 1/3duty	(1,*) 1/1duty	(0,0) 1/4duty	(0,1) 1/3duty	(1,*) 1/1duty
(0,0)	160	156	160	128	131.3	128
(0,1)	240	237	320	85.3	86.4	64
(1,0)	320	315	428	64	65	47.9
(1,1)	400	393	640	51.2	52.1	32

(Note1) FR is frame frequency, in case OSC frequency = 20.48KHz (typ).

The Formula, to calculate OSC frequency from Frame frequency is below.

" OSC frequency = Frame frequency (measurement value) x Divide number "
Divide number : Please decide by using the value of Frame Frequency Set (P1,P0) and duty setting (P3,P2).

Ex) (P1,P0) = (0,1) , (P3,P2) = (0,1) => Divide number= 237

Address Set (ADSET)

	MSB D/C	D6	D5	D4	D3	D2	D1	LSB D0	Hex	Reset
1st byte Command	1	0	0	0	0	0	1	1	83h	-
2nd byte Command	0	0	P5	P4	P3	P2	P1	P0	-	00h

Set start address to write DDRAM data.
The address can be set from 00h to 30h. (Address 31h is used at dummy address)
Do not set other address. (Except 00h to 31h address is not acceptable.)
In case, write data to DDRAM, please send RAMWR command certainly.

Blink Set (BLKSET)

	MSB D/C	D6	D5	D4	D3	D2	D1	LSB D0	Hex	Reset
1st byte Command	1	0	0	0	0	1	0	0	84h	-
2nd byte Command	0	0	0	0	0	P2	P1	P0	-	00h

Set Blink ON/OFF.
About detail, please refer to a “Blink function”.

Blink set

Blink mode(Hz)	P2	P1	P0	Reset state
OFF	0	0 / *	0 / *	○
1.6	1	0	0	
2.0	1	0	1	
2.6	1	1	0	
4.0	1	1	1	

*: Don’t care

Blink Address Set (BLKADSET)

	MSB D/C	D6	D5	D4	D3	D2	D1	LSB D0	Hex	Reset
1st byte Command	1	0	0	0	0	1	1	1	87h	-
2nd byte Command	0	0	P5	P4	P3	P2	P1	P0	-	00h

Set Blink data RAM start address to write.
The address can be set from 00h to 30h. (Address 31h is used at dummy address)
Do not set other address. (Except 00h-31h address is not acceptable.)
In case, write data to Blink RAM, please send BLKWR command certainly.

SEG/GPO Port Change (OUTSET1)

	MSB D/C	D6	D5	D4	D3	D2	D1	LSB D0	Hex	Reset
1st byte Command	1	0	0	0	1	0	0	0	88h	-
2nd byte Command	0	0	0	P4	P3	P2	P1	P0	-	00h

Set output mode, Segment output or GPO output.
P4 to P0: Select changing port number. (SEG15 to SEG45 ports are SEG mode/GPO mode selectable)

In case, GPO output is selected, Terminal output data is set by GPOSET command.

Ex) In case SEG45 port assigned to GPO,
If GPO1 data is “H”, GPO1 (SEG45) port outputs “H” (VLCD Level).
If GPO1 data is “L”, GPO1 (SEG45) port outputs “L” (VSS level).

Output terminal state under the P2 to P0 set condition is listed below

(BU97981KV ,BU97981GU)

Condition					SEG Terminal state (SEG output/GPO output)								
P4	P3	P2	P1	P0	SEG15 Terminal	SEG16 Terminal	SEG17 Terminal	SEG18 Terminal		SEG42 Terminal	SEG43 Terminal	SEG44 Terminal	SEG45 Terminal
0	0	0	0	0	SEG15	SEG16	SEG17	SEG18		SEG42	SEG43	SEG44	SEG45
0	0	0	0	1	SEG15	SEG16	SEG17	SEG18		SEG42	SEG43	SEG44	GPO1
0	0	0	1	0	SEG15	SEG16	SEG17	SEG18		SEG42	SEG43	GPO2	GPO1
0	0	0	1	1	SEG15	SEG16	SEG17	SEG18		SEG42	GPO3	GPO2	GPO1
0	0	1	0	0	SEG15	SEG16	SEG17	SEG18		GPO4	GPO3	GPO2	GPO1
		⋮							⋮				
1	1	0	1	1	SEG15	SEG16	SEG17	SEG18		GPO4	GPO3	GPO2	GPO1
1	1	1	0	0	SEG15	SEG16	SEG17	GPO28		GPO4	GPO3	GPO2	GPO1
1	1	1	0	1	SEG15	SEG16	GPO29	GPO28		GPO4	GPO3	GPO2	GPO1
1	1	1	1	0	SEG15	GPO30	GPO29	GPO28		GPO4	GPO3	GPO2	GPO1
1	1	1	1	1	GPO31	GPO30	GPO29	GPO28		GPO4	GPO3	GPO2	GPO1

(BU97981MUV)

Condition					SEG Terminal state (SEG output/GPO output)								
P4	P3	P2	P1	P0	SEG12 Terminal	SEG13 Terminal	SEG14 Terminal	SEG15 Terminal		SEG35 Terminal	SEG36 Terminal	SEG37 Terminal	SEG38 Terminal
0	0	0	0	0	SEG12	SEG13	SEG14	SEG15		SEG35	SEG36	SEG37	SEG38
0	0	0	0	1	SEG12	SEG13	SEG14	SEG15		SEG35	SEG36	SEG37	GPO1
0	0	0	1	0	SEG12	SEG13	SEG14	SEG15		SEG35	SEG36	GPO2	GPO1
0	0	0	1	1	SEG12	SEG13	SEG14	SEG15		SEG35	GPO3	GPO2	GPO1
0	0	1	0	0	SEG12	SEG13	SEG14	SEG15		GPO4	GPO3	GPO2	GPO1
		⋮							⋮				
1	0	1	1	1	SEG12	SEG13	SEG14	SEG15		GPO4	GPO3	GPO2	GPO1
1	1	0	0	0	SEG12	SEG13	SEG14	GPO24		GPO4	GPO3	GPO2	GPO1
1	1	0	0	1	SEG12	SEG13	GPO25	GPO24		GPO4	GPO3	GPO2	GPO1
1	1	0	1	0	SEG12	GPO26	GPO25	GPO24		GPO4	GPO3	GPO2	GPO1
1	1	0	1	1	GPO27	GPO26	GPO25	GPO24		GPO4	GPO3	GPO2	GPO1
11100 – 11111					GPO27	GPO26	GPO25	GPO24		GPO4	GPO3	GPO2	GPO1

In case, the SEG port is switched to the GPO port, DDRAM address and Blink RAM address do not change.
In this case, DDRAM address and Blink RAM address, selected GPO output mode, is dummy address.

Change Command of a SEG/LED port (OUTSET2)

	MSB D/C	D6	D5	D4	D3	D2	D1	LSB D0	Hex	Reset
1st byte Command	1	0	0	0	1	0	0	1	89h	-
2nd byte Command	0	0	0	0	0	P2	P1	P0	-	00h

This command affects segment port/LED port selection and PWM resolution set up.

P2: Resolution setting

Setting	P2	Reset condition
12bit resolution mode	0	○
8bit resolution mode	1	

P1 to P0: select SEG driving mode or LED driving mode, this command affect at SEG46 to SEG48 port.
The effective address is 00h to 03h. In case LED driving mode is selected, output turns into “NMOS Open Drain” from segment output.

The state of the output terminal in case P1 to P0 are setup is shown below
(BU97981KV, BU97981GU)

Setting		SEG Terminal state (SEG output/LED output)		
P1	P0	SEG46 Terminal	SEG47 Terminal	SEG48 Terminal
0	0	SEG46	SEG47	SEG48
0	1	SEG46	SEG47	LED1
1	0	SEG46	LED2	LED1
1	1	LED3	LED2	LED1

(BU97981MUV)

Setting		SEG Terminal state (SEG output/LED output)		
P1	P0	SEG39 Terminal	SEG40 Terminal	SEG41 Terminal
0	0	SEG39	SEG40	SEG41
0	1	SEG39	SEG40	LED1
1	0	SEG39	LED2	LED1
1	1	LED3	LED2	LED1

In this case, DDRAM address and a Blink RAM address of SEG port that set up to LED port, do not change.
The address assigned to LED port is used as dummy address respectively.

The output state of GPO, LED, and PWMOUT port under the INHb H/L, display on/off, and RESET state are listed below.

Control port	INHb		DISPLAY		RESET state
	H	L	ON	OFF	
GPO	According to GPOSET command	Low Fix	According to GPOSET command	According to GPOSET command	GPO unselected (All SEG output)
PWMOUT	According to PWM2SET command	Low Fix	According to PWM2SET command	According to PWM2SET command	Low Fix
LED	According to PWM1/PWM2SET command	Hi-Z	According to PWM1/PWM2SET command	According to PWM1/PWM2SET command	LED unselected (All SEG output)