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Real-Time Clock (RTC) series

I²C BUS Serial Interface RTC with High-precision Oscillation Adjustment

BU9873

Outline

The BU9873 is a CMOS real-time clock, which has a built-in interrupt generation function. This product is connected to the CPU via I²C interface, and configured to perform serial transmission of time and calendar data to the CPU. A high-precision oscillation adjustment circuit is also integrated, which is capable of adjusting time counts with digital method, and correcting deviations in the oscillation frequency of the crystal oscillator.

Important Characteristics

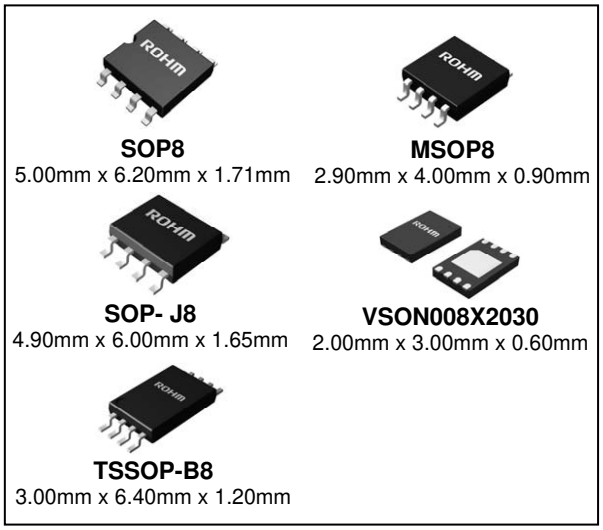
- Time Keeping Voltage 1.45V to 5.5V
- Time Keeping Current 1 (V$_{DD}$=3V, Ta=+25°C) 0.4µA (Typ)
- Time Keeping Current 2 (V$_{DD}$=3V, Ta=-40°C to +85°C) 1.0µA (Max)
- Power Supply Voltage 1.8V to 5.5V
- Access Frequency 1 (V$_{DD}$=1.8V to 2.5V) 100kHz (Max)
- Access Frequency 2 (V$_{DD}$=2.5V to 5.5V) 400kHz (Max)

Features

- Connected to the CPU via I²C Interface
- Time (Hour・Minute・Second, Selectable 12-Hour and 24-Hour Mode Setting)
- Calendar (Year・Month・Day・Week)
- Periodic Interrupt Function (Output from INTRB, Ranging from 1 Second to 1 Month)
- Alarm Interrupt Function (Day-of-Week・Hour・Minute in Setting Format, Output from INTRB)
- Oscillation Halt Sensing Function
- 32.768 kHz Clock Output (Output from 32KOUT with Control Pin)
- ±30 Second Adjustment Function
- Automatic Leap Year Recognition up to the Year 2099
- Built-in Oscillation Stabilizing Capacitors (C$_G$, C$_D$)
- High-Precision Oscillation Adjustment Circuit

Package

W (Typ) x D (Typ) x H (Max)



SOP8
5.00mm x 6.20mm x 1.71mm

MSOP8
2.90mm x 4.00mm x 0.90mm

SOP- J8
4.90mm x 6.00mm x 1.65mm

VSON008X2030
2.00mm x 3.00mm x 0.60mm

TSSOP-B8
3.00mm x 6.40mm x 1.20mm

○Product structure: Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Typical Application Circuit

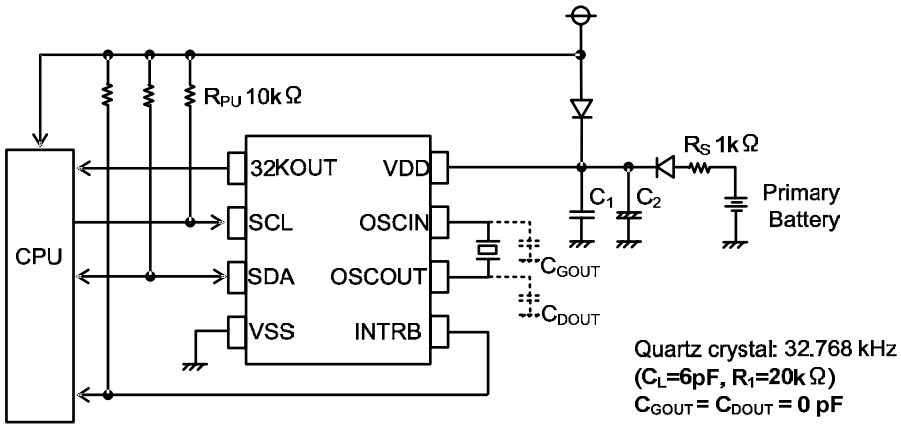


Figure 1. Typical application circuit (with primary battery)

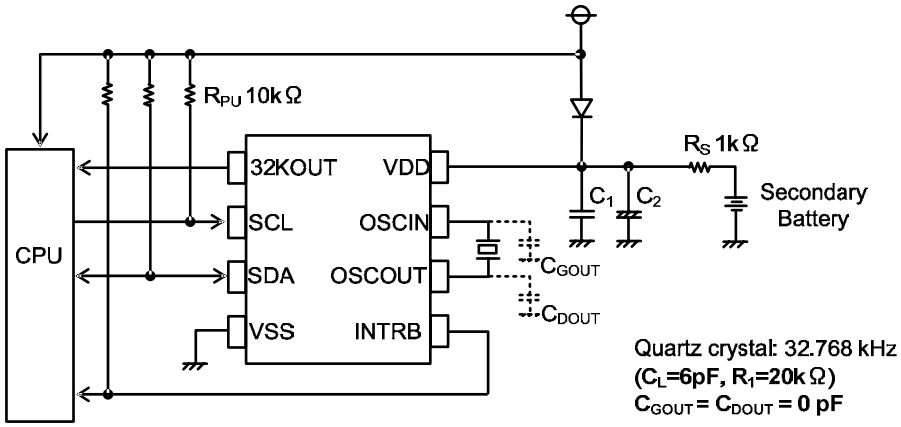


Figure 2. Typical application circuit (with secondary battery)

Pin Configuration

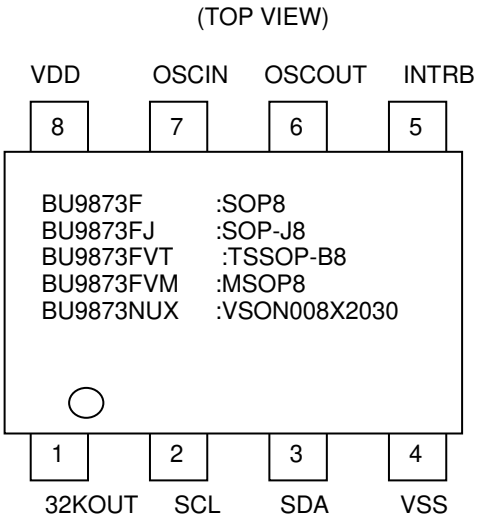


Figure 3. Pin configuration

Pin Description

Pin No.	Symbol	Input/Output	Function
1	32KOUT	Output	The 32KOUT pin is used to output 32.768 kHz clock pulses, which is controlled by an internal register. This pin is enabled during power-on from 0V, and is CMOS push-pull output.
2	SCL	Input	The SCL pin is used to input clock pulses synchronizing the input/output data from SDA pin.
3	SDA	Input/Output	The SDA pin is used to input and output data for writing and reading, which is synchronized with SCL pin. This pin is N-channel open drain output.
4	VSS	-	The VSS pin is grounded.
5	INTRB	Output	The INTRB pin is used to output periodic interrupt, or alarm interrupt (Alarm_A, Alarm_B) to the CPU. This pin is disabled during power-on from 0V, and is also N-channel open drain output.
6	OSCOUT	-	The OSCIN and OSCOUT pins are used to connect the 32.768 kHz crystal oscillator (Beside the crystal, all other oscillation circuit components is already integrated in this IC).
7	OSCIN	-	
8	VDD	-	The VDD pin is connected to the power supply.

Block Diagram

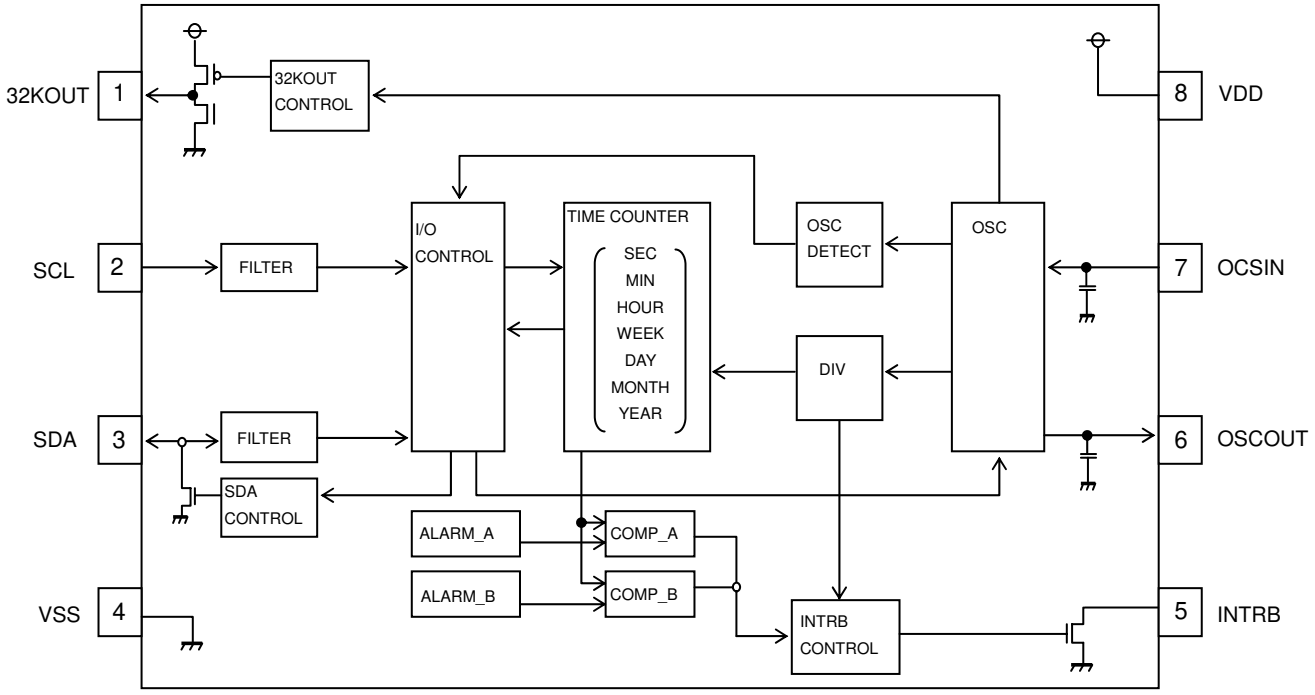


Figure 4. Block diagram

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Remark
Supply Voltage	V_{DD}	−0.3 to +6.5	V	
Power Dissipation	Pd	0.45 (SOP8)	W	When using above Ta=25, decreased by 4.5mW/°C.
		0.45 (SOP-J8)		When using above Ta=25, decreased by 4.5mW/°C.
		0.33 (TSSOP-B8)		When using above Ta=25, decreased by 3.3mW/°C.
		0.31 (MSOP8)		When using above Ta=25, decreased by 3.1mW/°C.
		0.30 (VSON008X2030)		When using above Ta=25, decreased by 3.0mW/°C.
Storage Temperature	Tstd	−55 to +125	°C	
Operating Temperature	Topt	−40 to +85	°C	
Terminal Voltage	—	-0.3 to V_{DD} +0.3	V	The Max value of Terminal Voltage is not over 6.5V. When the pulse width is 50ns or less, the Min value of Terminal Voltage is not lower than -0.8V.

Caution: Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings

Recommended Operating Conditions

Item	Symbol	Rating	Unit
Supply Voltage	V_{DD}	1.8 to 5.5	V
Timekeeping Voltage(Note 1)	V_{CLK}	1.45 to 5.5	V
Input Voltage	V_{IN}	0 to V_{DD}	V

(Note1) For minimum time keeping voltage, C_{GOUT} = C_{DOUT} = 0 pF; Quartz crystal unit: C_L (load capacitor) = 6 pF to 12.5 pF, Maximum value of R_1 (equivalent series resistance) = 80 KΩ.

DC Characteristics

Item	Symbol	Pin Name	Spec			Unit	Conditions
			Min	Typ	Max		
"H" Input Voltage	V_{IH}	SCL, SDA	$0.7V_{DD}$	—	V_{DD}+0.3	V	
"L" Input Voltage	V_{IL}	SCL, SDA	-0.3	—	$0.3V_{DD}$	V	
"H" Output Current	I_{OH}	32KOUT	—	—	-0.5	mA	$V_{OH}=V_{DD}$-0.5V
"L" Output Current	I_{OL1}	INTRB, 32KOUT	1	—	—	mA	V_{OL1}=0.4V
	I_{OL2}	SDA	6	—	—	mA	V_{OL2}=0.4V
Input Leakage Current	I_{ILK}	SCL	-1	—	1	μA	V_{IN}=5.5V or V_{SS}, V_{DD}=5.5V
Output Off State Leakage Current	I_{OZ}	SDA, INTRB, 32KOUT	-1	—	1	μA	V_{OUT}=5.5V or V_{SS}, V_{DD}=5.5V
Standby Current (time keeping current)	I_{DD1}	VDD	—	0.4	0.6	μA	V_{DD}=3V, Topt=25°C, SCL, SDA=3V, $C_{GOUT}=C_{DOUT}$=0pF, Output=Open(Note1)
	I_{DD2}	VDD	—	—	1.0	μA	V_{DD}=3V, Topt=-40°C to +85°C, SCL, SDA=3V, $C_{GOUT}=C_{DOUT}$=0pF, Output=Open(Note1)
	I_{DD3}	VDD	—	—	1.35	μA	V_{DD}=5.5V, Topt=-40°C to +85°C, SCL, SDA=5.5V, $C_{GOUT}=C_{DOUT}$=0pF, Output=Open(Note1)
Internal Oscillation Capacitance 1	C_G	OSCIN	—	10	—	pF	
Internal Oscillation Capacitance 2	C_D	OSCOUT	—	10	—	pF	

Unless otherwise specified: Vss=0V, V_{DD}=3V, Topt=−40°C to +85°C, Oscillation frequency=32.768 kHz
(load capacitance C_L=6pF, equivalent series resistance R_1=20kΩ)

(Note 1) In this mode, 32KOUT is disabled and no clock is output from this pin.
For time keeping current when outputting 32-kHz pulse from 32KOUT pin (this pin without loading), please refer to "P.7 Typical Performance Curves".

AC Characteristics

Item	Symbol	V_{DD} ≥1.8V			V_{DD} ≥2.5V			Unit
		Min	Typ	Max	Min	Typ	Max	
SCL Clock Frequency	f_{SCL}	0	—	100	0	—	400	kHz
SCL Clock “L” Time	t_{LOW}	4.7	—	—	1.3	—	—	µs
SCL Clock “H” Time	t_{HIGH}	4.0	—	—	0.6	—	—	µs
Start Condition Hold Time	$t_{HD:STA}$	4.0	—	—	0.6	—	—	µs
Stop Condition Setup Time	$t_{SU:STO}$	4.0	—	—	0.6	—	—	µs
Start Condition Setup Time	$t_{SU:STA}$	4.7	—	—	0.6	—	—	µs
Data Setup Time	$t_{SU:DAT}$	250	—	—	100	—	—	ns
“H” Data Hold Time	$t_{HDH:DAT}$	0	—	—	0	—	—	ns
“L” Data Hold Time	$t_{HDL:DAT}$	35	—	—	35	—	—	ns
SDA “L” Stable Time After Falling of SCL	$t_{PL:DAT}$	—	—	2.0	—	—	0.9	µs
SDA Off Stable Time After Falling of SCL	$t_{PZ:DAT}$	—	—	2.0	—	—	0.9	µs
Rising Time of SCL and SDA (Input)	t_R	—	—	1000	—	—	300	ns
Falling Time of SCL and SDA (Input)	t_F	—	—	300	—	—	300	ns
Spike Width that can be Filtered	t_{SP}	—	—	50	—	—	50	ns

Unless additional specified: V_{SS}=0V, Topt=−40°C to +85°C

(Note1) Not 100% TESTED Condition

Input data level: $V_{IL}=0.2\times V_{DD}$ $V_{IH}=0.8\times V_{DD}$
Input data timing reference level: $0.3\times V_{DD}/0.7\times V_{DD}$
Output data timing reference level: $0.3\times V_{DD}/0.7\times V_{DD}$
Rise/Fall time: ≦20ns

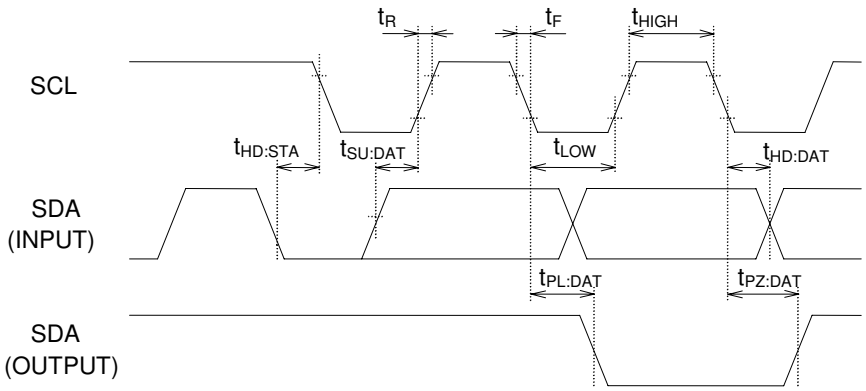


Figure 5. Input and output timing

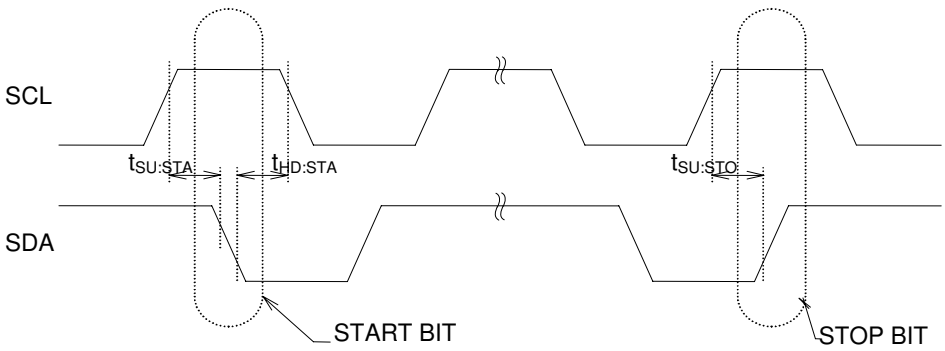


Figure 6. Start and stop condition

Typical Performance Curves

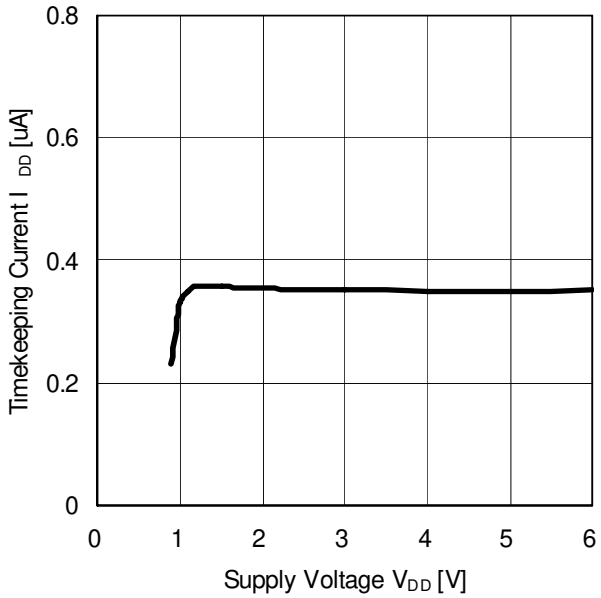


Figure 7. Timekeeping Current vs. Supply Voltage
(with no 32-kHz clock output, output pins open)
(C_{GOUT}=C_{DOUT}=0pF, Topt=25°C)

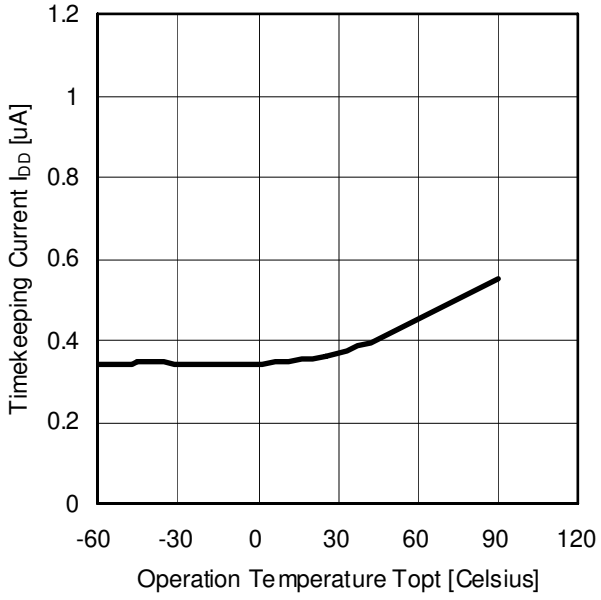


Figure 8. Timekeeping Current vs. Operating Temperature
(with no 32-kHz clock output, output pins open)
(C_{GOUT}=C_{DOUT}=0pF, V_{DD}=3V)

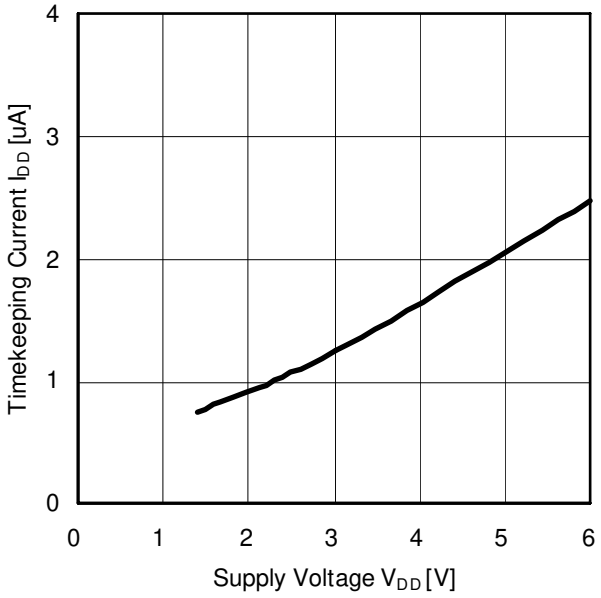


Figure 9. Timekeeping Current vs. Supply Voltage
(with 32-kHz clock output, output pins open)
(C_{GOUT}=C_{DOUT}=0pF, Topt=25°C)

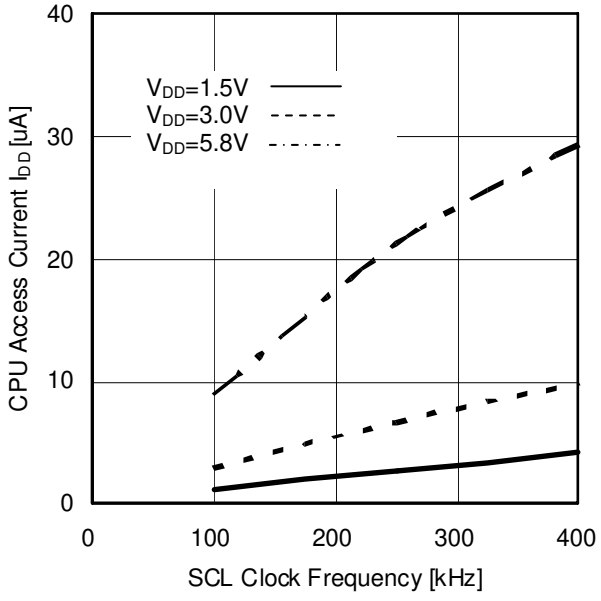


Figure 10. CPU Access Current vs. SCL Clock Frequency
(with no 32-kHz clock output, SDA="H")
(other pins open, C_{GOUT}=C_{DOUT}=0pF, Topt=25°C)

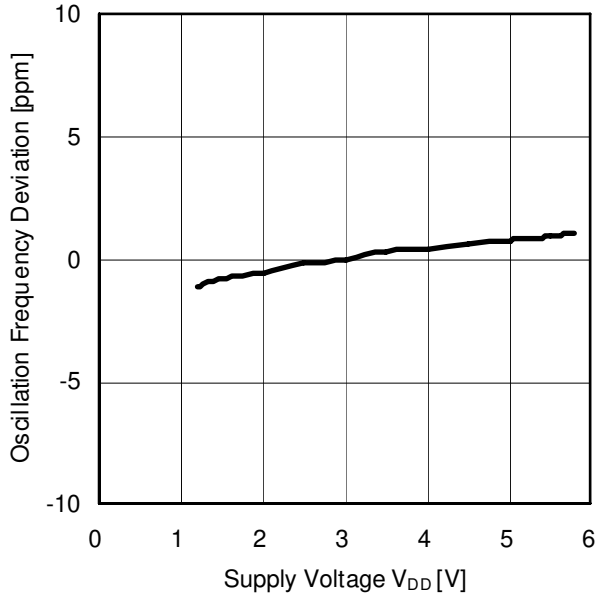


Figure 11. Oscillation Frequency Deviation vs. Supply Voltage
(V_{DD}=3V, Topt=25°C as standard)

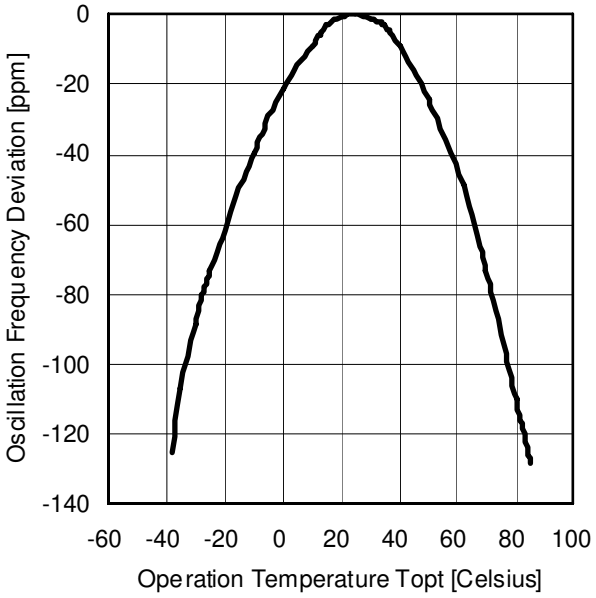


Figure 12. Oscillation Frequency Deviation vs. Operating Temperature
(V_{DD}=3V, Topt=25°C as standard)

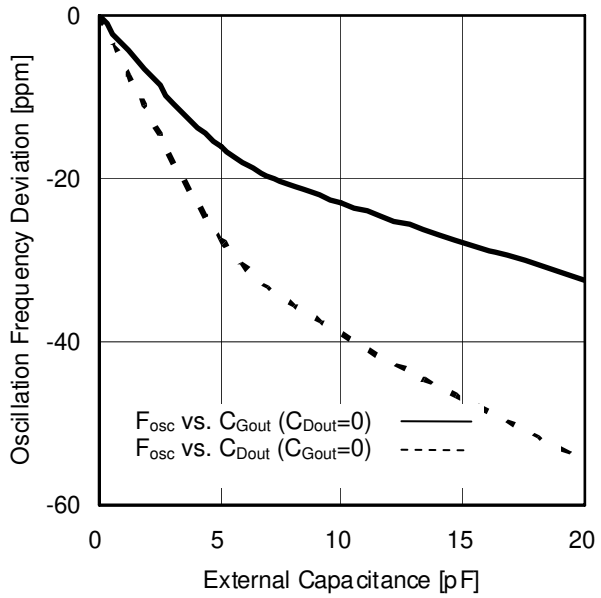


Figure 13. Oscillation Frequency Deviation vs. External C_G and C_D
(V_{DD}=3V, Topt=25°C as standard)

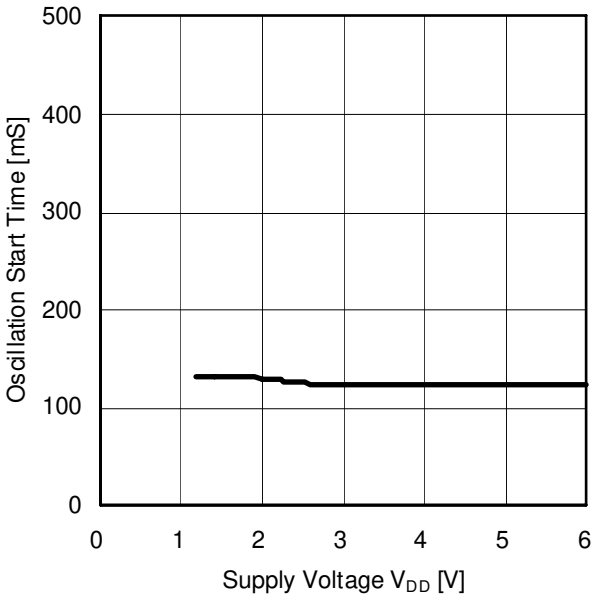


Figure 14. Oscillation Start Time vs. Supply Voltage
(Topt=25°C)

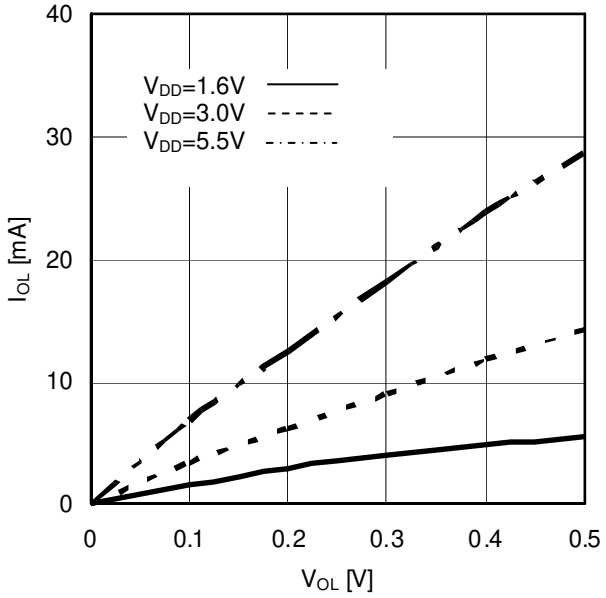


Figure 15. I_{OL} vs. V_{OL} INTRB pin
(Topt=25°C)

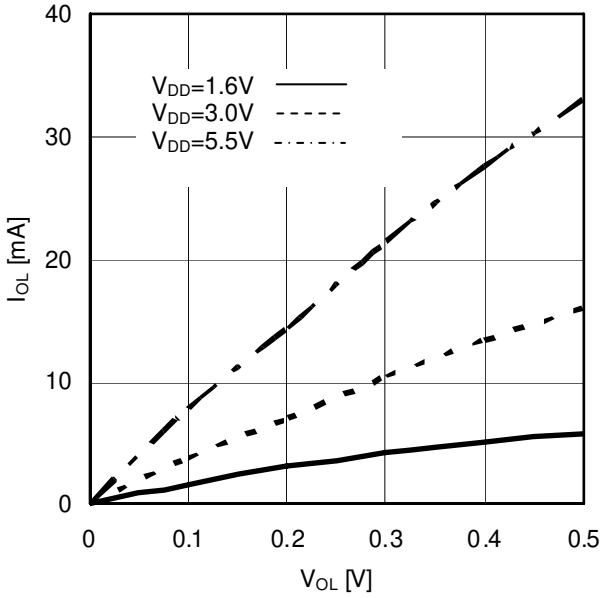


Figure 16. I_{OL} vs. V_{OL} SDA pin
(Topt=25°C)

Function Description

IC function will be explained as the following sequence.

1. Communication interface
2. Address mapping of internal register
3. Clock and calendar function
4. Oscillation adjustment function with digital method
5. Alarm interrupts function
6. Periodic interrupt function
7. Test bit
8. ±30 second adjust function
9. Oscillation halts sensing function
10. 32-kHz clock output function

1. Communication Interface

This product can read/write data from I^2C bus interface with 2-wires: SDA (data) and SCL (clock). Since the output of SDA pin is open-drain, data transferring between CPU with different supply voltage is possible by adopting a pull-up resistor on the circuit board.

1-1. I^2C BUS Communication

I^2C BUS data communication starts by a start condition input, and ends by a stop condition input. The data length is 8-bit, and acknowledges signal is always required after each byte.

I^2C BUS carries out data transmission between plural devices connected by 2-wires: serial data (SDA) and serial clock (SCL). Among these devices, there is “master” that generates clock and control the start and end signal, and “slave” that is controlled by unique device address. RTC is “slave”. And the device that outputs data to bus during data transferring is called “transmitter”, and the device that receives data is called “receiver”.

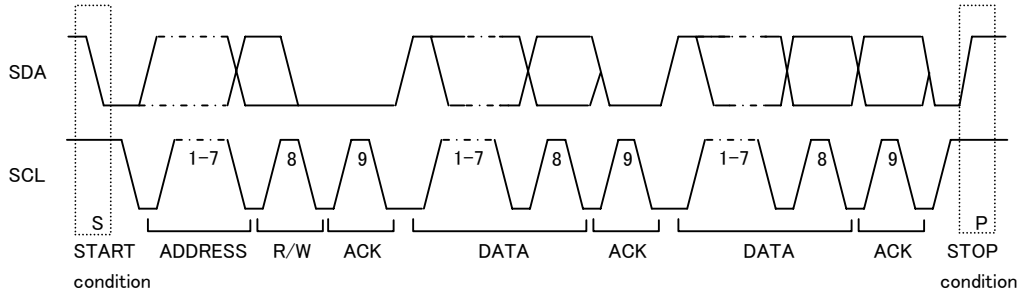


Figure 17. I^2C BUS communication

1-2. Start Condition (start bit recognition)

Before executing any command, start condition (start bit) is necessary, where SDA goes from “H” down to “L” when SCL is “H”.

This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this condition is satisfied, no command will be executed.

1-3. Stop Condition (stop bit recognition)

Every command can be ended by stop condition (stop bit), where SDA rising from “L” to “H” when SCL is “H”.

1-4. Acknowledge (ACK) Signal

- This acknowledge (ACK) signal is a software rule to judge whether data transfer has been executed successfully or not. For master and slave, the device (μ-COM during inputting slave address of write command, read command, and this IC during outputting data of read command) at the transmitter side releases the bus after outputting 8-bit data.
- The device (this IC during inputting slave address of write command, read command, and μ-COM during outputting data of read command) at the receiver side sets SDA “L” during the ninth clock cycle, and outputs acknowledge signal (ACK) showing that it has received the 8-bit data.
- This IC outputs acknowledge signal (ACK) “L” after recognizing start condition and 8-bit slave address.
- Every write action outputs acknowledge signal (ACK) “L” after receiving 8-bit data (word address and write data).
- Every read action outputs 8-bit data (read data), and detects acknowledge signal (ACK) “L”. When acknowledge signal (ACK) is detected, and stop condition is not sent from the master (μ-COM) side, this IC will continue to output data. When acknowledge signal (ACK) is not detected, this IC will stop data transfer, and end read action after recognizing stop condition (stop bit). Then, this IC will get in off-status.

1-5. Write Command

Write command is illustrated as following: Firstly, input start condition; then, enter the 7-bit slave address. Slave address of this IC is (0110010). Thereafter, enter “L” for the R/$\overline{W}$ bit, which indicates the direction of data transmission.

In the next byte, input the internal address pointer (4-bit) and transmission format (4-bit) to the IC. For write operation, only one transmission format (0000) is available. The 3_{rd} byte transmits data that will be written to the address specified by the internal address pointer. Internal address pointer settings will also be automatically incremented for 4byte and after. Note that when the internal address pointer is Fh, it will change to 0h during transmitting the next byte.

Example of write command (when writing to internal address Eh to Fh)

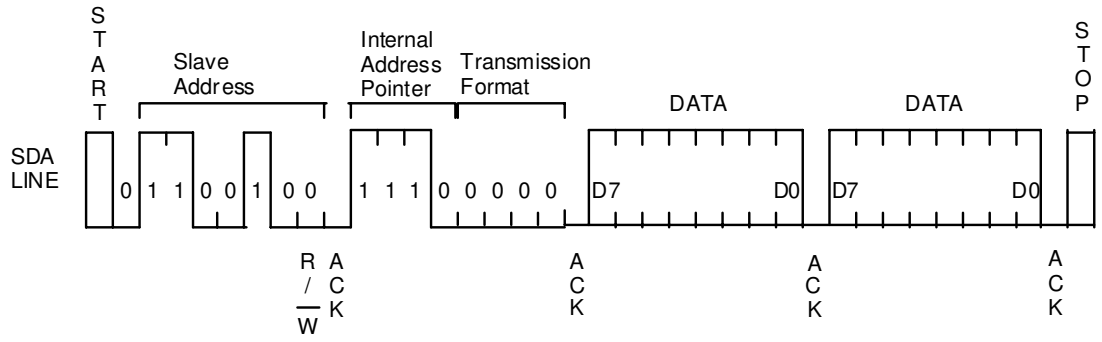


Figure 18. Write command

1-6. Read Command

This IC allows the following three methods of reading data from an internal register.

1-6-1. Read from a Specified Internal Address

The first method uses data write command to specify the internal address pointer and transfer format, and then repeat the start condition again. After the 7-bit slave address, enter “H” for the R/$\overline{W}$ bit, which indicates the direction of data transmission. In the next byte, data from the specified internal address will be output. If entering “L” during the timing of ACK, the data from the next address will be output continuously. The read operation will not be ended until entering “H” during the timing of ACK and following a stop condition.

The internal address pointer is reset to Fh when a stop condition is met. Therefore, this read method allows no insertion of stop condition before the end of read.

Example 1 of data read (when data is read from 2h to 3h)

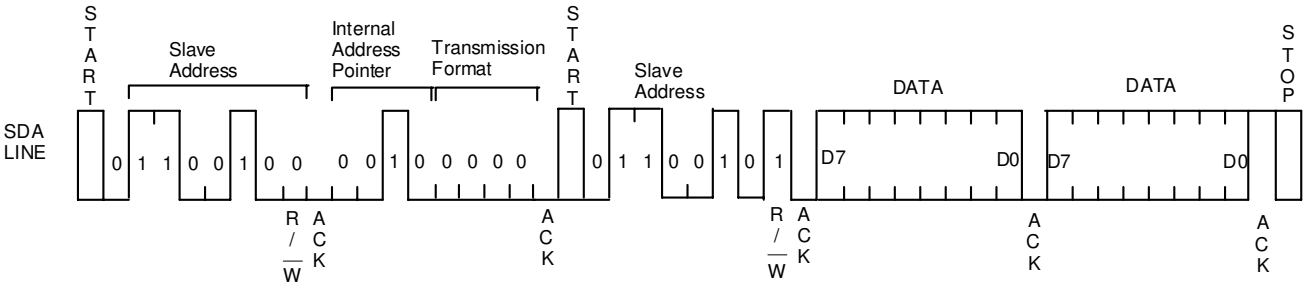


Figure 19. Read from a specified internal address

1-6-2. Fast Read from a Specified Internal Address (with changing transmission format)

The second method uses data write command to specify the internal address pointer, but the transfer format is designated to be (0100). In the next byte, data from the specified internal address will be output immediately. If entering “L” during the timing of ACK, the data from the next address will be output continuously. The read operation will not be ended until entering “H” during the timing of ACK and following a stop condition.

Example 2 of data read (when data is read from internal addresses Eh to 1h)

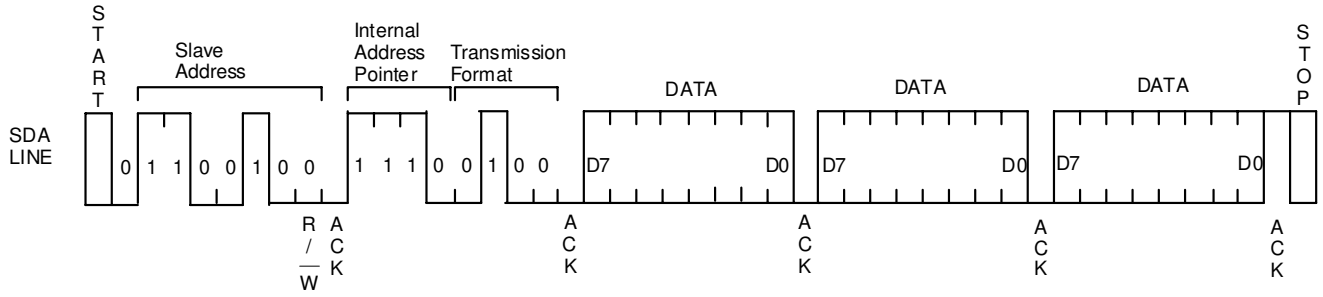


Figure 20. Fast read from a specified internal address

1-6-3. Read from Address Fh (without specifying the internal address)

The third method starts with a start condition, and then enters the 7-bit slave address and “H” for the R/$\overline{W}$ bit, which indicates the direction of data transmission.

In the next byte, data from address Fh will be output immediately. If entering “L” during the timing of ACK, the data from the next address will be output continuously. The read operation will not be ended until entering “H” during the timing of ACK and following a stop condition

Since the internal address pointer is set to Fh by a stop condition, this method is only effective when reading is started from the internal address Fh.

Example 3 of data read (when data is read from internal addresses Fh to 3h)

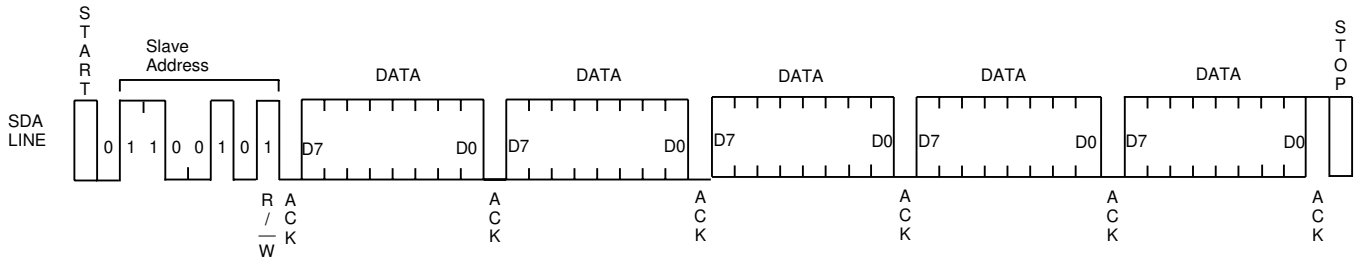


Figure 21. Read from address Fh

1-7. Notes during RTC Data Transmission

To avoid invalid read and write, two features should be noted when accessing the RTC.

Hold function of clock carry-up

While read and write operation is executed (at the same time, RTC clock is still counting-up), this IC temporarily holds the clock carry-up from start condition to stop condition, to prevent invalid read and write. If clock carry-up happens during this period (read or write from start condition to stop condition), it will be adjusted within approx. 61µs after stop condition.

Automatic release function of access

When 0.5 to 1.0 second elapses after start condition, any access to the RTC will be automatically terminated, to release the temporarily holding of clock carry-up, set Fh to the address pointer, and access from the CPU is forced to be stopped (as long as stop condition is received, the same action will be made: automatic release function from the I^2C bus interface).

Therefore, one access must be completed within 0.5 seconds. The automatic release function prevents delay in SCL clock, even if SCL is stopped because of system sudden failure during read operation.

In addition, a second start condition (after the first start condition and ahead of the stop condition) is regarded as the "repeated start condition". Therefore, when 0.5 to 1.0 seconds elapses after the first start condition, access to the RTC will also be released automatically.

If access is tried after automatic release function is activated, no acknowledge signal will be output for writing while FFh will be output for reading.

The following points should be noted during accessing the RTC.

(1) No stop condition shall be generated until clock and calendar data read/write is started and completed

Bad example of time read
(Start condition) → (Read of seconds) → (Read of minutes) → (Stop condition) → (Start condition) → (Read of hours) → (Stop condition)

Assuming read is started at 05:59:59 P.M. and while reading seconds and minutes the time advanced to 06:00:00 P.M. During this time, second digit is hold so the read result is 05:59:59. Then the IC confirms stop condition and carries second digit that is being hold and the time changes to 06:00:00 P.M. Thus, when the hour digit is read, it changes to be 6. The invalid results of 06:59:59 will be read.

(2) One cycle of read/write operation shall be completed within 0.5 seconds.

(3) Do not send start condition within 61µs from stop condition, because the clock carry-up that is hold during I^2C access will be adjusted within approx.61µs from stop condition.

2. Address Mapping of Internal Register

	Internal address				Contents	Data							
	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Second Counter	— (Note1)	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1
1	0	0	0	1	Minute Counter	—	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1
2	0	0	1	0	Hour Counter	—	—	H_{20} P/AB	H_{10}	H_8	H_4	H_2	H_1
3	0	0	1	1	Day-of-week Counter	—	—	—	—	—	W_4	W_2	W_1
4	0	1	0	0	Day Counter	—	—	D_{20}	D_{10}	D_8	D_4	D_2	D_1
5	0	1	0	1	Month Counter	—	—	—	MO_{10}	MO_8	MO_4	MO_2	MO_1
6	0	1	1	0	Year Counter	Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1
7	0	1	1	1	Time Trimming Register	—	F_6	F_5	F_4	F_3	F_2	F_1	F_0
8	1	0	0	0	Alarm_A (Minute Register)	—	AM_{40}	AM_{20}	AM_{10}	AM_8	AM_4	AM_2	AM_1
9	1	0	0	1	Alarm_A (Hour Register)	—	—	AH_{20} AP/AB	AH_{10}	AH_8	AH_4	AH_2	AH_1
A	1	0	1	0	Alarm_A (Day-of-week Register)	—	AW_6	AW_5	AW_4	AW_3	AW_2	AW_1	AW_0
B	1	0	1	1	Alarm_B (Minute Register)	—	BM_{40}	BM_{20}	BM_{10}	BM_8	BM_4	BM_2	BM_1
C	1	1	0	0	Alarm_B (Hour Register)	—	—	BH_{20} BP/AB	BH_{10}	BH_8	BH_4	BH_2	BH_1
D	1	1	0	1	Alarm_B (Day-of-week Register)	—	BW_6	BW_5	BW4	BW_3	BW_2	BW_1	BW_0
E	1	1	1	0	Control Register 1	AALE	BALE	—	—	TEST (Note4)	CT_2	CT_1	CT_0
F	1	1	1	1	Control Register 2	—	—	12B/24	ADJ (Note2) XSTP (Note3)	CLENB	CTFG	AAFG	BAFG

(Note1) The "–" mark indicates data which can be read only and set to "0" when it is read.
(Note2) For the ADJ/XSTP bit of control register 2, ADJ will be set to "1" if writing "1", while XSTP will be set to "0" if writing "0" during normal oscillation. Conversely, setting ADJ=0 and XSTP=1 cause no event. The value of XSTP bit is output when it is read.
(Note3) When XSTP is set to "1", the internal register F6 to F0, CT2 to CT0, AALE, BALE, CLENB will be reset to "0".
(Note4) The TEST bit of control register 1 is for shipment testing. Please always set TEST = 0. If this bit is set to "1" accidentally, it will be reset to "0" after stop condition is input.

3. Clock and Calendar Function

The clock and calendar function is available in this IC, ranging from seconds to years (the last two digits of a year).
Every register is configured in BCD code, and assigned to the following address respectively.
Second counter (internal address 0h)
Minute counter (internal address 1h)
Hour counter (internal address 2h)
Day-of-week counter (internal address 3h)
Day counter (internal address 4h)
Month counter (internal address 5h)
Year counter (internal address 6h)

3-1. Clock Counter (second counter, minute counter and hour counter)

Time digit in BCD code is displayed as follows.
Second counter: be reset to “00” and carried to minute digits when incremented from 59 to 00.
Minute counter: be reset to “00” and carried to hour digits when incremented from 59 to 00.
Hour counter: be reset to “00” and carried to day and day-of-the-week digits when incremented from 23 to 00 (in 24-hour mode).
If non-existent time has been written, any carry from lower digits may cause the time counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent time data.
Users can choose to display time in 12-hour mode or 24-hour mode by setting the 12B/24 bit (internal address Fh).

12B/24-hour mode selection bit

12B/24	Description
0	12- hour time display system (separate for morning and afternoon)
1	24- hour time display system

Time Display Table

24-hour mode	12-hour mode	24-hour mode	12-hour mode
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

Setting the 12-hour or 24-hour mode should precede writing time data.

3-2. Day-of-week Counter

Day-of-week digits are incremented by 1 corresponding to the 7 days of week, e.g. (W4, W2, W1) = (0, 0, 0) → (0, 0, 1) → … → (1, 1, 0) → (0, 0, 0)
The relation between the days of week and day-of-week digits is user definable. (e.g. Sunday=0, 0, 0)
(W4, W2, W1) should not be set to (1, 1, 1).

3-3. Calendar Counter (day counter, month counter and year counter)

The automatic calendar function provides the calendar digit displayed in BCD code.
Day digits: Range from 1 to 31 (for January, March, May, July, August, October, and December)
Range from 1 to 30 (for April, June, September, and November)
Range from 1 to 29 (for February in leap years)
Range from 1 to 28 (for February in ordinary years)
Carried to month digits when reset to 1
Month digits: Range from 1 to 12 and carried to year digits when reset to 1.
Year digits: Range from 00 to 99 and 00, 04, 08… 92 and 96 are counted as leap years.
If non-existent time has been written, any carry from lower digits may cause the time counters to malfunction. Therefore, such incorrect writing should be replaced with the writing of existent time data.

3-4. Automatic Judgment of Leap Year

Automatic judgment function of leap year is included in this IC. Leap year is defined as follows.
The year that can be divided by 4 is leap year.
The year that can be divided by 100 is ordinary year.
The year that can be divided by 400 is leap year.
For example, year 2000 is a leap year while year 2100 is ordinary year.

Because the year register of this IC only supports the last two digits, a year will be automatically recognized as a leap year if it is a multiple of 4. Therefore, year 2100 or 2000 will be determined as leap year because the last two digits are “00”. This result in automatic judgment of leap years only can be up to the year 2099 in this IC.

4. Oscillation Adjustment Function with Digital Method

This IC has built-in oscillation capacitance C_G and C_D, the oscillation circuit can be configured easily by connecting an external crystal oscillator. However, due to some variations such as parasitic capacitance, it is hardly for RTC to oscillate at 32,768 Hz exactly.

Therefore, if you want to achieve high-precision clock, it is necessary to use the error correction method. By using this feature, you can achieve high-precision clock with only ±1.5ppm mismatch at a specified temperature. Because the crystal oscillator has temperature dependency, the clock mismatch will increase when the temperature changes.

The clock adjustment step is about 3ppm and the total range is ±189ppm.

As following, some application is possible:

(1) If the temperature sensor is integrated in system, by setting the clock adjustment function in accordance with the variation of temperature, it is possible to realize high-precision clock that does not depend on the temperature.

(2) By storing seasonal temperature information to the system, and using the clock adjustment function with this temperature information, the realization of high-precision clock is available throughout the year.

4-1. Function Description

In the IC, counting up to seconds is made once per 32,768 of clock pulse generated by the oscillator. If oscillation frequency is not 32,768 Hz which does not match with the number of clock counts, the time error will happen. This function is designated to compensate the clock mismatch.

The adjustment function adds 2 clock pulses every 20 seconds: 2/(32,768×20)=3.051ppm, which delays the clock by approx. 3ppm. Likewise, decrementing 2 clock pulses advances the clock by 3ppm. Thus the clock may be adjusted to the precision of ±1.5ppm. and the total range is ±189.2ppm (±124 steps) according to the internal 7-bit trim register. The time trimming circuit adjusts one second count based on this register when second digit is 00, 20 or 40 seconds. Note that the time trimming function only adjust clock timing and oscillation frequency and 32-kHz clock output is not adjusted.

Setting data to internal register (internal address 7h) activates the time trimming circuit. And bit F6 decides either increasing or decreasing the clock pulse.

The clock counts will be increased as ((F5, F4, F3, F2, F1, F0)−1) ×2 when F6 is set to “0”.
The clock counts will be decreased as ((/F_6, /F_5, /F_4, /F_3, /F_2, /F_1, /F_0)+1) ×2 when F6 is set to “1”.
Counts will not change when (F6, F5, F4, F3, F2, F1, F0) are set to (＊, 0, 0, 0, 0, 0, ＊)

For example, when 32.768 kHz crystal is used:
When (F6, F5, F4, F3, F2, F1, F0) are set to (0, 0, 0, 0, 1, 1, 1), counts will change as: 32,768+(7−1) ×2=32,780 (clock will be delayed) when second digit is 00, 20 or 40.

When (F6, F5, F4, F3, F2, F1, F0) are set to (0, 0, 0, 0, 0, 0, 1), counts will remain 32,768 without changing when second digit is 00, 20 or 40.

When (F6, F5, F4, F3, F2, F1, F0) are set to (1, 1, 1, 1, 1, 1, 0), counts will change as: 32,768+(−2) ×2=32,764 (clock will be advanced) when second digit is 00, 20 or 40.

4-2. Configuration Method of Time Adjustment

Time adjustment amount can be calculated following the rules below.

Case 1:
When oscillation frequency (Note1) >target frequency (Note2) (clock gains)

$$\text{Adjustment amount}^{(Note3)} = \frac{(\text{Oscillation frequency} - \text{Target frequency} + 0.1)}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\approx (\text{Oscillation frequency} - \text{Target frequency}) \times 10 + 1$$

(Note1) Oscillation frequency : Clock frequency output from the 32KOUT pin at room temperature.
(Note2) Target frequency : A frequency to be adjusted to.
Since temperature characteristics of a 32.768 kHz crystal oscillator generally generates the highest frequency at a room temperature, we recommend to set the target frequency to approx. 32768.00Hz to 32768.10Hz (+3.05ppm to 32768Hz).
Note that this value may differ based on the environment or place where the device will be used.
(Note3) Adjustment amount: A value to be set finally to F6 to F0 bits. This value is expressed in 7bit binary digits with sign bit.

Example of Calculations

When oscillation frequency=32768.85 kHz; target frequency=32768.05 kHz

Oscillation adjustment value = (32768.85 - 32768.05 + 0.1) / (32768.85 × 3.051 × 10^{-6})

≈ (32768.85 - 32768.05) × 10 + 1

= 9.001 ≈ 9

In this instance, write the settings (DEV, F6, F5, F4, F3, F2, F1, F0) = (0, 0, 0, 0, 1, 0, 0, 1) in the oscillation adjustment register. Thus, an appropriate oscillation adjustment value in the presence of any time count gain represents a distance from 01h.

Case 2:
When oscillation frequency=target frequency (no clock gain or loss)
(F6, F5, F4, F3, F2, F1, F0) = (*, 0, 0, 0, 0, 0, *).
In this case, the correction is not performed.

Case 3:
When oscillation frequency<target frequency (clock loses)

$$\text{Adjustment amount} = \frac{(\text{Oscillation frequency} - \text{Target frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\approx (\text{Oscillation frequency - Target frequency}) \times 10$$

Example of Calculations

When actual oscillation frequency=32763.95 kHz; target frequency=32768.05 kHz

Oscillation adjustment value = (32763.95 - 32768.05) / (32768.05 × 3.051 × 10^{-6})

≈ (32763.95 - 32768.05) × 10 + 1

= -41.015 ≈ -41

To express -41 in 7bit binary digits with sign bit, subtract 41 (29h) from 128 (80h) in the above case, 80h-29h=57h. Thus, set (F6, F5, F4, F3, F2, F1, F0) to (1, 0, 1, 0, 1, 1, 1). As this example shows, adjustments to be used when the clock loses shall be distance from 80h.

5. Alarm Interrupt Function

The BU9873 has an alarm function that outputs an interrupt signal from INTRB pin to CPU when the day of the week, hour or minute match with the preset time. There are two systems of alarms (Alarm_A, Alarm_B), and each may output interrupt signal separately at a specified time. The alarm may be selectable between on and off for each day of the week, thus allowing outputting alarm everyday or on a specific day of the week. Polling is possible for each alarm function

5-1. Usage of Alarm Interrupt Function

Users can set the time to generate an alarm interrupt. There are two systems of alarms, Alarm_A register (internal address 8h to Ah), Alarm_B register (internal address Bh to Dh), covering the day of the week, hour and minute.

Because Alarm_A and Alarm_B are the same function, only Alarm_A is explained as example.

	Internal address				Contents	Data							
	A3	A2	A1	A3		D7	D6	D5	D4	D3	D2	D1	D0
8	1	0	0	0	Alarm_A (Minute Register)	—	AM_{40}	AM_{20}	AM_{10}	AM_8	AM_4	AM_2	AM_1
9	1	0	0	1	Alarm_A (Hour Register)	—	—	AH_{20} AP/AB	AH_{10}	AH_8	AH_4	AH_2	AH_1
A	1	0	1	0	Alarm_A (Day-of-week Register)	—	AW_6	AW_5	AW_4	AW_3	AW_2	AW_1	AW_0

Alarm_A, Alarm_B hour register D5 is set to for PM in the 12-hour display system at AP/AB. The register D5 indicates 10 digit of hour digit in 24-hour display system at AH20.
To activate alarm operation, any imaginary alarm time setting should not be left to avoid un-matching.
AW0 to AW6 correspond to the day-of-the-week counter (W4, W2, W1) being set at (0, 0, 0) to (1, 1, 0).
No alarm pulses are output when all of AW0 to AW6 are set to 0.

Example of alarm time settings

Alarm Time Settings	Day-of-the-week							12-hour svstem				24-hour system			
	Sun	Mon	Tue	Wed	Thu	Fri	Sat	10 hour	1 hour	10 min	1 min	10 hour	1 hour	10 min	1 min
	AW0	AW1	AW2	AW3	AW4	AW5	AW6								
0:00AM every day	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
1:30AM every day	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
11:59AM every day	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00PM on Monday through Friday	0	1	1	1	1	1	1	3	2	0	0	1	2	0	0
1:30PM on Sunday	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
11:59PM Monday Wednesday,and Friday	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

Designation of day-of-the-week and AW0 to AW6 in the above table is an example.

The alarm interruption is enabled only when the AALE, BALE bits are set to “1” (internal address Eh).

Alarm_A, Alarm_B enable bits

AALE, BALE	Description	
0	Alarm_A (Alarm_B) Correspondence action invalid	Default
1	Alarm_A (Alarm_B) Correspondence action valid	

5-2. Alarm Interrupt Output

Alarm interrupt output is from INTRB pin and the outputting is “L”. In addition, by monitoring the value of AAFG, BAFG bits (internal address Fh), the state of alarm can be checked.

Alarm_A (Alarm_B) Flag Bit

AAFG, BAFG	Description	
0	Unmatched alarm register with clock counter	Default
1	Matched alarm register with clock counter	

The flag bit turns to “1” and INTRB is “L” when matched time is sensed for each alarm.
The AAFG, BAFG bit may be set only to “0”. Setting this bit to“0” sets the INTRB to OFF status (“H”). When this bit is set to“1” nothing happens. When the AALE, BALE bit is set to“0”, alarm operation is disabled and “0“is read from the AAFG, BAFG bit.

Output timing between AAFG, BAFG bit and INTRB

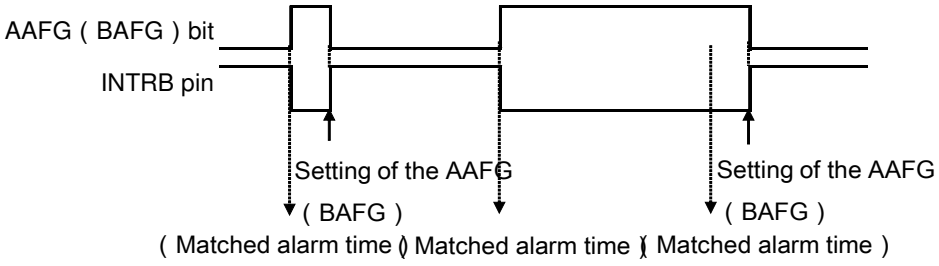


Figure 22. Output timing between AAFG (BAFG) bit and INTRB

If time matching happened, AAFG (BAFG) bit will be kept high until it is set to “0”.

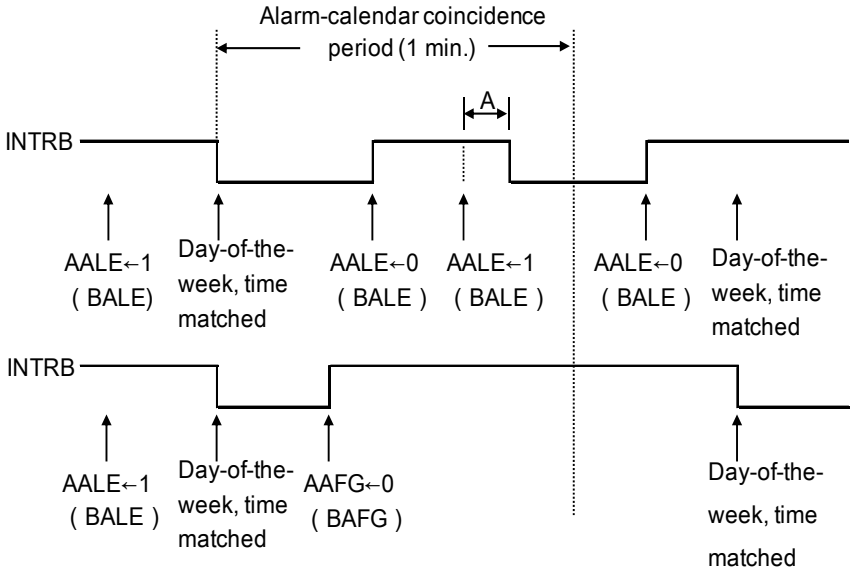


Figure 23. Output timing between AALE (BALE) bit, AAFG (BAFG) bit and INTRB

5-3. INTRB Output Control

Alarm interrupt and periodic interrupt are both outputted from INTRB pin, so there are totally three types of signal from this pin.
If more than one signal is triggered at the same time, the output becomes a NOR waveform of these signals.

Example: When Alarm_A and Alarm_B are output from the INTRB pin

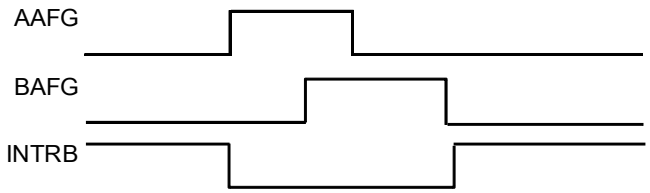


Figure 24. INTRB output control

By checking the flag bit, which interrupt outputted from INTRB pin can be distinguished.

	Flag bit	Enable bit
Alarm_A	AAFG (D1 at Fh)	AALE (D7 at Eh)
Alarm_B	BAFG (D0 at Fh)	BALE (D6 at Eh)
Periodic interrupt	CTFG (D2 at Fh)	Disabled at CT2=CT1=CT0=0 (D2 to D0 at Eh)

6. Periodic Interrupt Function

The BU9873 can output periodic interrupt pulses in addition to alarm function from the INTRB pin. Output wave form for periodic interrupt may be selected from regular pulse waveform (2Hz and 1Hz) and waveforms (every second, every minute, every hour and every month) that are appropriate for CPU level interrupt. The condition of periodic interrupt signals can be monitored with using a polling function.

6-1. Usage of Periodic Interrupt Function

Periodic interrupt function selection with setting value to register (internal address Eh)

CT2	CT1	CT0	Description		
			Wave From Mode	Cycle and Falling Timing	
0	0	0	—	OFF (Default)	Default
0	0	1	—	Fixed at “L”	
0	1	0	Pulse mode	2Hz (Duty50%)	
0	1	1	Pulse mode	1Hz (Duty50%)	
1	0	0	Level mode	Every second (synchronized with second count-up)	
1	0	1	Level mode	Every minute (at 00 second of every minute)	
1	1	0	Level mode	Every hour (at 00 :00 of every hour)	
1	1	1	Level mode	Every month (1st day, 00:00:00 a.m. of every month)	

(1) Pulse mode：Outputs 2Hz, 1Hz clock pulses (duty 50%). Since counting up of second counter is delayed by approximately 92μs from the falling edge of clock pulse, time reading immediately after the falling edge of clock pulse may appear to lag behind the time counts of the real-time clocks by approximately 1 second.

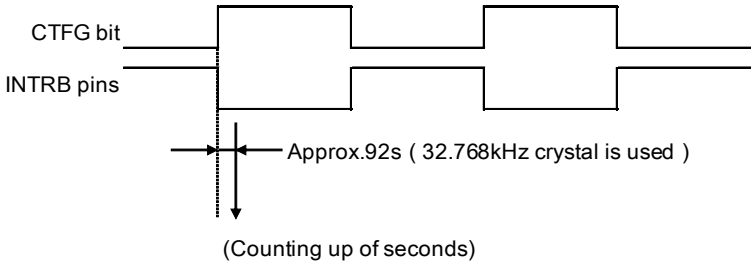


Figure 25. Output timing of pulse mode

(2) Level mode：One second, one minute or one month may be selected for an interrupt cycle. Counting up of seconds is matched with falling edge of interrupt output. INTRB pin will be kept “L” until CTFG bit is set to “0”.

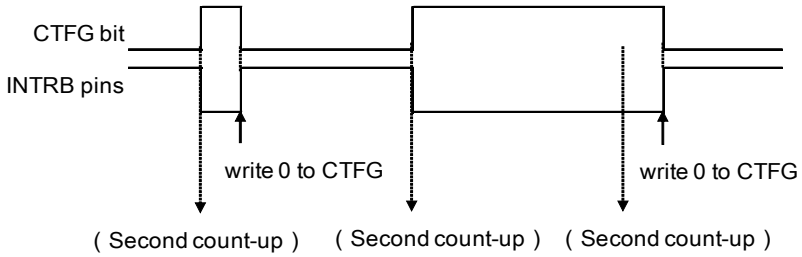


Figure 26. Output timing of level mode

(3) When the time trimming circuit is used, periodic interrupt cycle changes every 20 seconds.
Pulse mode: “L” duration of output of output pulses may change in the maximum rang of ±3.784ms.
For example, Duty will be 50±0.3784％at 1Hz.
Level mode: Frequency in one second may change in the maximum range of：±3.784ms.

6-2. Periodic Interrupt Output

Besides the alarm interrupts function, the periodic interrupt is also outputted from INTRB terminal. If more than one signal is triggered at the same time, the output becomes a NOR waveform of these signals. Further, by reading data from CTFG bit (internal address Fh), it is possible to check the state of interrupt function.

Periodic Interrupt Flag Bit

CTFG	Description	
0	Periodic Interrupt output=OFF (“H”)	Default
1	Periodic Interrupt output=ON (“L”)	

This bit is set to “1” when periodic interrupt pulses are output (“L”). The CTFG bit may be set only to “0” in the interrupt level mode. Setting this bit to “0” sets the INTRB to OFF (“H”). When this bit is set to “1”, nothing happens.

7. Test Bit

The TEST bit is for shipment testing in the factory. Please always set TEST = 0. If this bit is set to “1” accidentally, it will be reset to “0” after stop condition is input.

Test Bit

TEST	Description	
0	normal mode	Default
1	test mode	

8. ±30 Second Adjust Function

±30 Second Adjust Bit

ADJ	Description	
0	Ordinary operation	Default
1	Second digit adjustment	

The following operations are performed by setting the second ADJ bit (internal address Fh) to 1.

(1) For second digits ranging “00”to“29”seconds.
Clock counters smaller than seconds are reset and second digits are set to”00”.

(2) For second digits ranging “30”to“59”seconds.
Clock counters smaller than seconds are reset and second digits are set to”00”. Minute digits are incremented by 1.

Second digits are adjusted within122μs from writing operation to ADJ.
The ADJ bit is for write only and allows no read operation.

9. Oscillation Halt Sensing Function

This IC has a built-in oscillation halt detection circuit, and store the status in XSTP bit (internal address Fh). If initial power on from 0V or supply voltage drops without back-up battery, the XSTP bit will be set to "1" automatically. This function can be applied to judge clock data validity.

Oscillator Halt Sensing Bit

XSTP	Description	
0	Ordinary oscillation	
1	Oscillator halt sensing	Default

When oscillation is halted after initial power on from 0V or supply voltage drops, the bit will be set to"1" and remain to be "1"even if oscillation is restarted. This bit may be used to judge validity of clock and calendar data after power on or supply voltage drops. The XSTP bit can be written to "0" during ordinary oscillation.
When this bit is set to"1", F_6～F_0, CT_2～CT_0, AALE, BALE, CLENB bits will be reset to "0". INTRB output will stop and the 32KOUT will output 32-kHz clock pulses.

In order to prevent invalid detection of oscillation halt, the points should be noted as the following.
(1) Instantaneous disconnection of V_{DD}
(2) Condensation on the crystal oscillator
(3) Generation of noise on the PCB in the crystal oscillator
(4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC

10. 32-kHz Clock Output Function

The IC can generate clock pulses of 32-kHz from the 32KOUT pin.
When power on (XSTP=1), 32-kHz clock pulses are output from 32KOUT, which is CMOS push-pull output. The pin is changed to be high impedance by setting the CLENB (internal address Fh) bit to "1".

32-kHz Clock Output Bit

CLENB	Description	
0	32-kHz clock output enabled	Default
1	32-kHz clock output disabled	

By setting this is bit to "0", outputting clock pulses with the same frequency of crystal oscillator is enabled. 32-kHz clock output will not be affected from settings in the clock adjustment register.

The timing of 32KOUT with CLENB control is shown below.

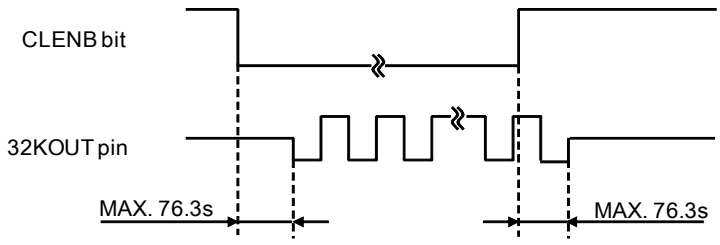


Figure 27. Output timing between 32KOUT and CLENB bit

Configuration of Application Circuit

1. Quartz Crystal

Typical frequency of quartz crystal is 32.768 kHz. Generally, quartz crystal units have basic characteristics including an equivalent series resistance (R_1) indicating the oscillation margin and a load capacitance (C_L) indicating the degree of their center frequency. We recommended characteristics of crystal units for the BU9873 as follows:

(1) Max. R_1 is up to 80kΩ.
(2) C_L value of 6 to 12.5pF.

The stability of quartz crystal units' oscillation depends on the parasitic capacitance of the circuit board and external oscillator capacitors (C_{Gout} and C_{Dout}). The best C_L value we recommended is 6 to 8pF, but if C_L value is more than 8pF, please use the oscillation adjustment method and refer to P17 “Oscillation Adjustment Function with Digital Method”.

Install the quartz crystal unit in the closest position to the real-time clock ICs. Avoid using any long parallel lines to wire the OSCIN and OSCOUT pins. Avoid laying any signal lines or power lines in the vicinity of the oscillation circuit.

2. Pull Up Resistor R_{PU}

(1) Pull up resistance of SDA and INTRB terminal

SDA and INTRB output is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU}, the larger is the consumption current.

(a) Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

- SDA rise time to be determined by the capacitance (C_{BUS}) of bus line of R_{PU} and SDA should be t_R or lower. And AC timing should be satisfied even when SDA rise time is slow.
- The bus electric potential Ⓐ to be determined by input leak total (I_L) of device connected to bus at output of 'H' to the SDA line and R_{PU} should sufficiently secure the input 'H' level (V_{IH}) of microcontroller and EEPROM including recommended noise margin 0.2Vcc.

$$V_{CC} - I_L R_{PU} - 0.2V_{CC} \geq V_{IH}$$

$$\therefore R_{PU} \leq \frac{0.8V_{CC} - V_{IH}}{I_L}$$

Ex.) Vcc =3V I_L=10μA V_{IH}=0.7 Vcc
thus

$$\therefore R_{PU} \leq \frac{0.8 \times 3 - 0.7 \times 3}{10 \times 10^{-6}}$$

$$\leq 30 \quad [k\Omega]$$

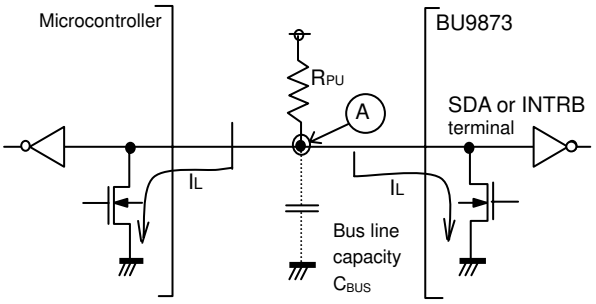


Figure 28. I/O circuit diagram

(b) Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

- When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=1mA.

$$\frac{V_{CC} - V_{OL}}{R_{PU}} \leq I_{OL}$$

$$\therefore R_{PU} \geq \frac{V_{CC} - V_{OL}}{I_{OL}}$$