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Digital Video Encoders

Video bus interface


BU9969KN

No.09067EAT02

•Description

BU9969KN is a digital video encoder IC for NTSC/PAL (ITU-R BT.601, ITU-R BT.656).

It allows captured images (e.g. downloaded or on mobile phones) to be viewed on a TV monitor. In addition, a digital filter is built in for high image quality, and both multifunction and simple types are available for greater compatibility.

•Features

- Video Format
 - NTSC-M
 - PAL-B/D/G/H/I
- Bus Interface
 - 656 input mode YCbCr 8 bit (included in EAV, SAV)
 - 601 input mode YCbCr 16 bit or RGB 16 bit (with Hsync, Vsync input)
- Input Data Format
 - YCbCr 4:2:2 (656 mode or 601 mode)
 - RGB R: 5bit, G: 6bit, B: 5bit (601 mode)
- Input Range
 - YCbCr:
 - 1) Y: 16-235, CbCr: 16-240 SCALE_M* = "1"
 - 2) YCbCr : 1-254 SCALE_M* = "0" (601 mode)

*SCALE_M is 1st bit of Sub-Address x'04.
 - RGB: R, B: 0 - 31, G: 0 - 63
- NTSC/PAL Standard Video Output Support
- Trap Filter Built In
- x4 System Clock Over Sampling Function Built In
- 10-bit Video DAC Built In
- PLL Built In
- 2-Wire Serial Interface
- 2 Supply Voltage Operation: (DVDD = PVDD = 1.8V : Typ, IOVDD = AVDD = 3.0V : Typ)
- Package: VQFN36

•Application

Cell Phone

•Absolute Maximum Ratings

Table.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
[1.8V Power Source System]			
Digital Core Power Source Voltage	DVDD	-0.2 to 2.5	V
PLL Power Source Voltage	PVDD		
[3.0V Power Source System]			
Digital I/O power source voltage	IOVDD	-0.2 to 4.5	V
DAC Power Source Voltage	AVDD		
Power Dissipation1	Pd1	450 (Note.1)	mW
Power Dissipation2	Pd2	700 (Note.2)	mW
Storage temperature range	Tstg	-25 to 125	°C

Note 1 : When not mounted on any board at Ta = 25°C.

Note 2 : When mounted on 50mm*58mm*1.6mm glass epoxy board. In the case to use at Ta = 25°C or higher, 11.3 mW should be decreased per 1°C. This value is an actually measured value, and not a guaranteed value.

•Recommended Operation Range

Table.2 Recommended Operation Range

Item	Symbol	Range	Unit
[1.8V Power Source System]			
Digital Core Power Source Voltage	DVDD	1.80 ± 0.1	V
PLL Power Source Voltage	PVDD		
[3.0V Power Source System]			
Digital I/O power source voltage*	IOVDD	3.00 ± 0.3	V
DAC Power Source Voltage	AVDD		
Operation temperature range	Topr	-20 to 70	°C

*Connect the pull-up resistance of the serial interface to the digital I/O power source voltage.

*Supply the power source voltage to all power source pins within 100 μ sec.

This procedure is same, when stopping to supply the power source.

●Recommended Operating Conditions

Table.3 Recommended Operating Conditions

(Unless otherwise specified Ta=25°C, DVDD=PVDD=1.8V, IOVDD=AVDD=3.0V, GND=0V)

Item	Symbol	Min	Typ	Max	Unit	Condition
<Image data interface>						
SYSCLK frequency 1	fsysclk1	–	27	–	MHz	656 input mode
SYSCLK frequency 2	fsysclk2	–	13.5	–	MHz	601 input mode
SYSCLK frequency deviation 1	dfsysclk1	–100	–	100	ppm	27MHz at 656 input mode
SYSCLK frequency deviation 2	dfsysclk2	–100	–	100	ppm	13.5MHz at 601 input mode
SYSCLK rise time	t2r	–	–	5	ns	*1
SYSCLK fall time	t2f	–	–	5	ns	*1
SYSCLK duty	dutysclk	45	–	55	%	*1
<Serial interface>						
SCLK frequency	f _{SCLK}	–	–	400	kHz	
SCLK rise time	t1sr	–	–	300	ns	*1
SCLK fall time	t1sf	–	–	300	ns	*1
SDI rise time	t1dr	–	–	300	ns	*1
SDI fall time	t1df	–	–	300	ns	*1
SCLK "L" pulse width	t1wl	1.3	–	–	us	*1
SCLK "H" pulse width	t1wh	0.6	–	–	us	*1

*1 Refer to Fig.5 the serial interface–timing chart on page 9.

●Electric Characteristics 1

Table 4.1 Electric Characteristics 1

(Unless otherwise specified Ta=25°C, DVDD=PVDD=1.8V, IOVDD=AVDD=3.0V, GND=0V)

Item	Symbol	Min	Typ	Max	Unit	Condition
<Image data interface>						
Data setup time	t2sd	5	–	–	ns	*1
Data hold time	t2hd	8	–	–	ns	*1
HS, VS setup time	t2sc	5	–	–	ns	*1
HS, VS hold time	t2hc	8	–	–	ns	*1
<Serial interface>						
Data hold time	t1h	0	–	0.9	us	*2
Data setup time	t1s	100	–	–	ns	*2
Hold time (START)	t1hSTA	0.6	–	–	us	*2
Setup time (STOP)	t1sSTO	0.6	–	–	us	*2
Setup time (START)	t1sSTA	0.6	–	–	us	*2
Bus free time Between "STOP" condition and "START" condition	tBUF	1.3	–	–	us	*2

*1 Refer to Fig.3., the image data and synchronous signal–timing chart on page 8.

*2 Refer to Fig.5., the serial interface timing chart on page 9.

●Electric Characteristics 2

Table 4.2 Electric Characteristics 2

(Unless otherwise specified Ta=25°C, DVDD=PVDD=1.8V, IOVDD=AVDD=3.0V, GND=0V)

Item	Symbol	Min	Typ	Max	Unit	Condition
<Video encoder digital portion>						
Digital core dynamic current	IDDCO	–	20	50	mA	*1
Digital I/O dynamic current	IDDIO	–	0.5	10.0	mA	
Digital core static current	ISTDCO	–	1.5	8	μA	*2
Digital I/O static current	ISTDIO	–	0.5	2	μA	*3
“H” input voltage	V _{IH}	IOVDD *0.8	–	IOVDD +0.2	V	*4
“L” input voltage	V _{IL}	–0.2	–	IOVDD *0.2	V	*4
L input leak current 1	I _{ILL1}	–10	–	10	μA	*5
L input leak current 2	I _{ILL2}					
H input leak current 1	I _{IHL}	–10	–	10	μA	*6
H input leak current 2	I _{IHT}	10	–	500	μA	*7
SDI “L” output voltage	V _{OL}	0	–	0.5	V	*8 IOL=2mA

*1 Internal Color Bar output mode at 27MHz operation.

*2 RESETB = Low

*3 RESETB = Low and All inputs pins = Low

*4 The following pins are applied.

SYSCLK, DATA[15:0], HS, VS, TEST[3:0], SCLK and SDI.

*5 The following pins are set to “Low”.

SYSCLK, DATA[15:0], HS, VS, TEST[3:0], SCLK and SDI.

*6 The following pins are set to “High (IOVDD)”.

SYSCLK, DATA[15:0], HS, VS, SCLK and SDI.

*7 The following pins are set to “High (IOVDD)”.

TEST [3:0]

*8 The SDI pin is applied.

●Electric Characteristics 3

Table 4.3 Electric Characteristics 3

(Unless otherwise specified Ta=25°C, DVDD=PVDD=1.8V, IOVDD=AVDD=3.0V, GND=0V)

Item	Symbol	Min	Typ	Max	Unit	Condition
<Video DAC portion>						
Video DAC resolution	RES	–	–	10	bit	
Video DAC dynamic current	IDDV	–	40	55	mA	R _L =37.5Ω, R _{IREF} =1.2kΩ *1
Video DAC static current	ISTV	–	1	5	μA	RESETB=L *2
Integral linearity error	INL	–	±8.0	±15.0	LSB	R _L =37.5Ω, R _{IREF} =1.2kΩ *1
Differential linearity error	DNL	–	±1.0	±4.0	LSB	R _L =37.5Ω, R _{IREF} =1.2kΩ *1
Full scale voltage	V _{FS}	1.1	1.25	1.4	V	R _L =37.5Ω, R _{IREF} =1.2kΩ *1
<PLL portion>						
PLL dynamic current	IDDP	–	1	2.5	mA	SYSCLK=27MHz input
PLL static current	ISTP	–	1	5	μA	*2

*1 R_L=37.5Ω shows the value at measurement.*2 Set the RESETB or 1st bit of register PWD_M to “Low”.

●Block Diagram

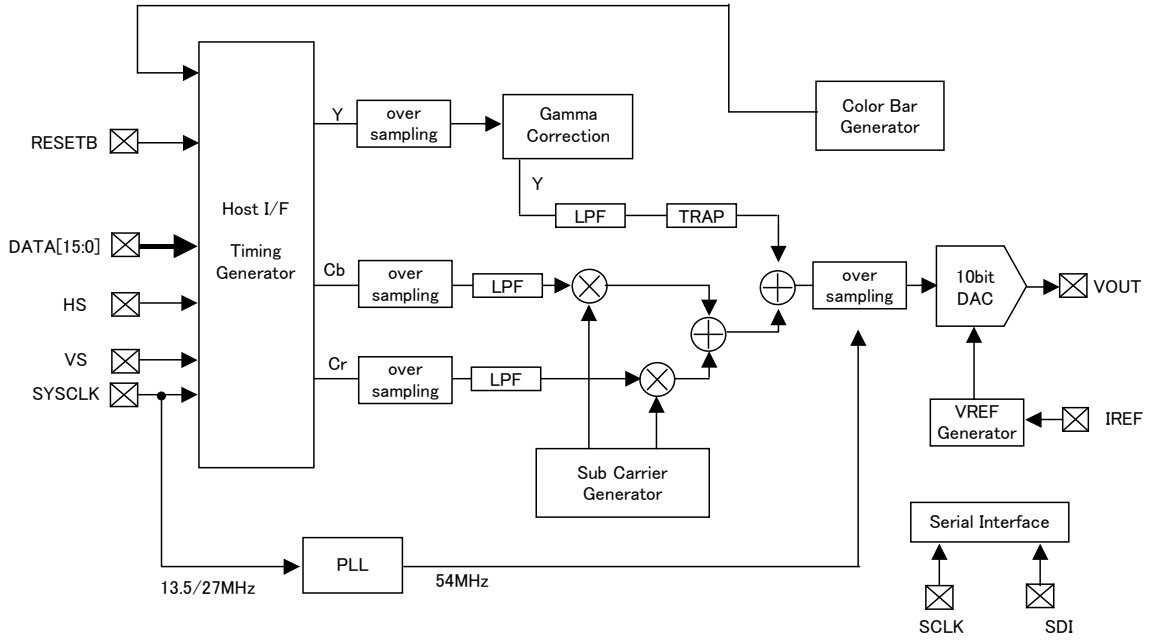


Fig.1. BU9969KN Block Diagram

●Terminal Functions

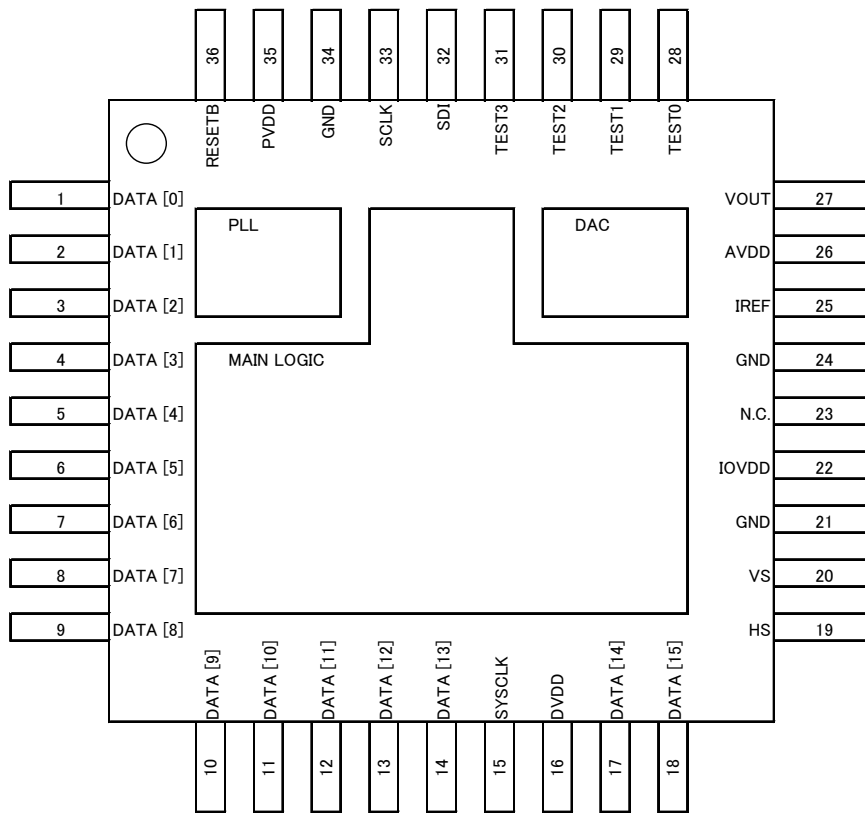


Fig 2. BU9969KN Terminal Layout

●Terminal Functions

Table 5. BU9969KN Terminal Functions

Terminal No.	Terminal name	Description of terminals			I/O *1
		RGB input (601 input mode)	YCbCr input (601 input mode)	YCbCr input (656 input mode)	
1	DATA [0]	R[0] data	Y[0] data	YCbCr[0] data	I
2	DATA [1]	R[1] data	Y[1] data	YCbCr[1] data	I
3	DATA [2]	R[2] data	Y[2] data	YCbCr[2] data	I
4	DATA [3]	R[3] data	Y[3] data	YCbCr[3] data	I
5	DATA [4]	R[4] data	Y[4] data	YCbCr[4] data	I
6	DATA [5]	G[0] data	Y[5] data	YCbCr[5] data	I
7	DATA [6]	G[1] data	Y[6] data	YCbCr[6] data	I
8	DATA [7]	G[2] data	Y[7] data	YCbCr[7] data	I
9	DATA [8]	G[3] data	CbCr[0] data	Connected to GND	I
10	DATA [9]	G[4] data	CbCr[1] data	Connected to GND	I
11	DATA [10]	G[5] data	CbCr[2] data	Connected to GND	I
12	DATA [11]	B[0] data	CbCr[3] data	Connected to GND	I
13	DATA [12]	B[1] data	CbCr[4] data	Connected to GND	I
14	DATA [13]	B[2] data	CbCr[5] data	Connected to GND	I
15	SYCLK	System clock (Image data transfer clock)			I(S)
16	DVDD	Digital core power source			P
17	DATA [14]	B[3] data	CbCr[6] data	Connected to GND	I
18	DATA [15]	B[4] data	CbCr[7] data	Connected to GND	I
19	HS	Horizontal synchronous signal input (To be used only at 16-bit input mode)			I(S)
20	VS	Vertical synchronous signal input (To be used only at 16-bit input mode)			I(S)
21	GND	GND for I/O power source and Digital core power source			G
22	IOVDD	I/O power source			P
23	N.C.	Non Connection			-
24	GND	GND for Analog power source			G
25	IREF	DAC reference current setting terminal			O
26	AVDD	Analog power source			P
27	VOUT	Composite signal output			O
28	TEST0	Test terminal. It connects with GND.			I(PD)
29	TEST1	Test terminal. It connects with GND.			I(PD)
30	TEST2	Test terminal. It connects with GND.			I(PD)
31	TEST3	Test terminal. It connects with GND.			I(PD)
32	SDI	Serial data input			I(S)/O *2
33	SCLK	Serial clock input			I(S)
34	GND	GND for PLL power source			G
35	PVDD	PLL power source			P
36	RESETB	Reset input (L: reset)			I(S)

*1 ABBR:

I(S) : input I/O with schmitt, I(PD) : input I/O with Pull Up register, O : output, P : power source, G : ground.

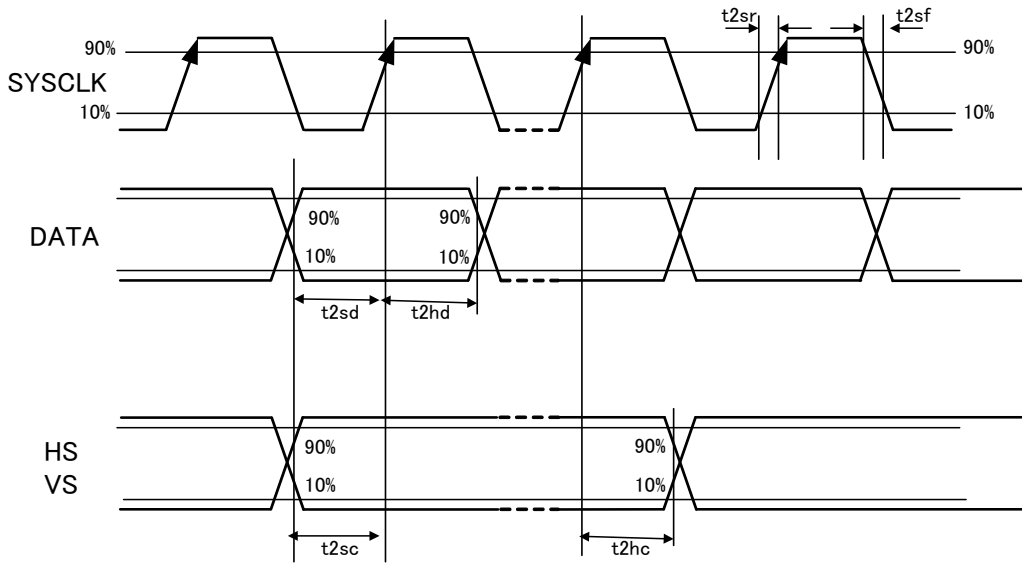
*2 At reset mode, the bidirectional I/O pin is set to the input mode.

•Terminal Equivalent Circuit

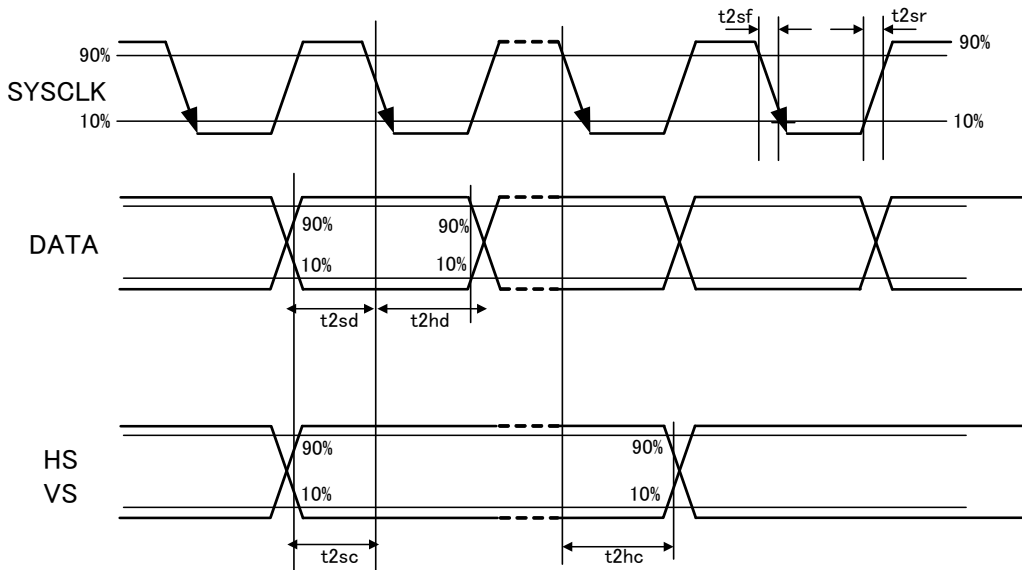
Table 6. Terminal Equivalent Circuit

Terminal name	Equivalent circuit diagram	Terminal name	Equivalent circuit diagram
DATA[15:0]		IREF	
SYSCLK SCLK VS HS RESETB		VOUT	
SDI		DVDD PVDD	
TEST0 TEST1 TEST2 TEST3		IOVDD AVDD	
		GND	

•Input Timing Chart



Data latched by the rising edge of SYSCLK



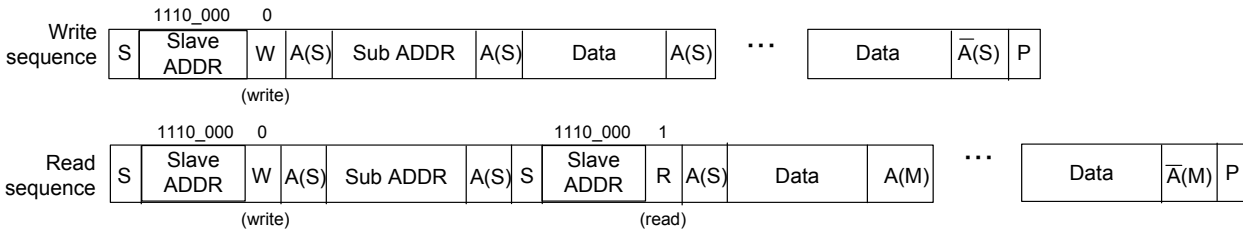
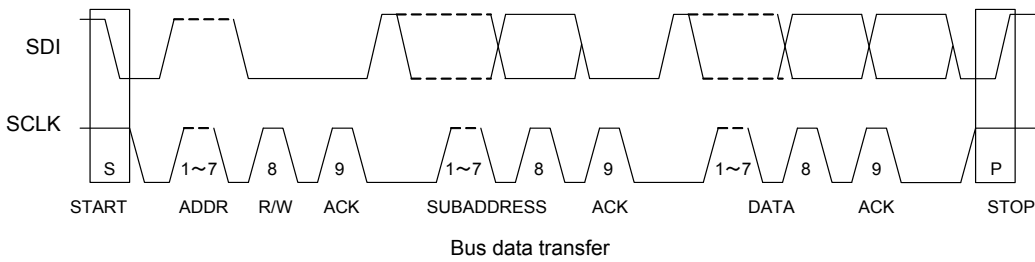
Data latched by the falling edge of SYSCLK

Fig.3. Image data and synchronous signal timing chart

It can be controlled by 3rd bit of register SYCPOL_M that is latched by the rising or falling of SYSCLK.

●Serial Interface Format

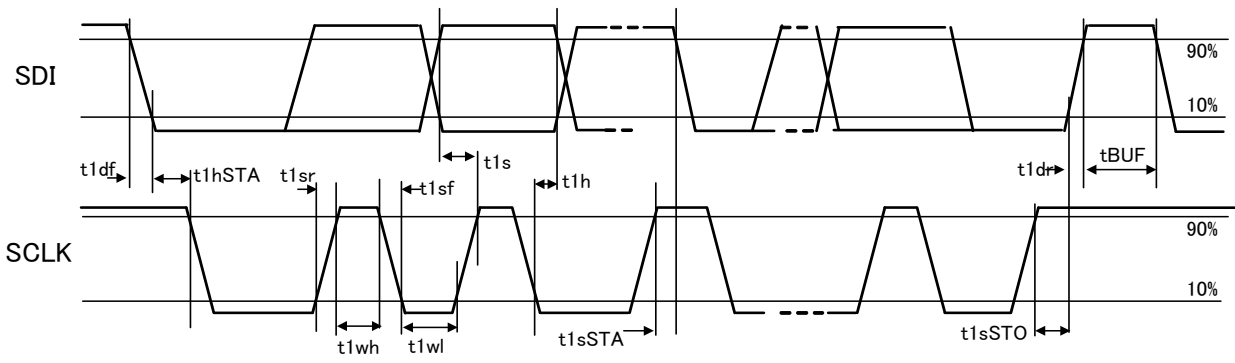
The slave address of the device is E0h.



Write / read sequence
 S = start bit A(S) = acknowledge by slave $\bar{A}(S)$ = no acknowledge by slave
 P = stop bit A(M) = acknowledge by master $\bar{A}(M)$ = no acknowledge by master

Fig.4. Serial Interface Format

●Serial Interface Timing

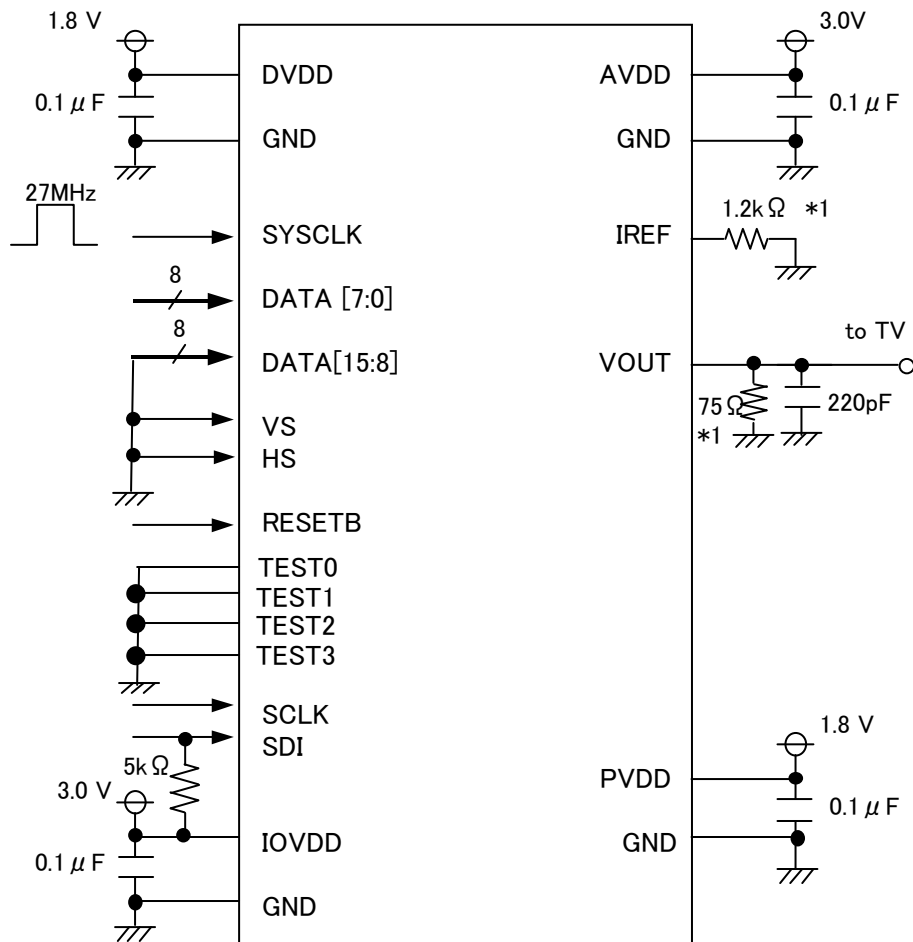


t1s: DATA set-up time t1h: DATA hold time
 t1wl: SCLK "L" pulse width t1wh: SCLK "H" pulse width
 t1hSTA: Hold time START condition t1sSTA: Set-up time for a repeated START condition
 t1sSTO: Set-up time for STOP condition

*Please change the SDA after SCLK is stabilized in Low except the condition "START" and "STOP".

Fig.5. Serial Interface Timing Diagram

●Application circuit diagram 1



656 input mode

Fig.6. Application Circuit Diagram Example

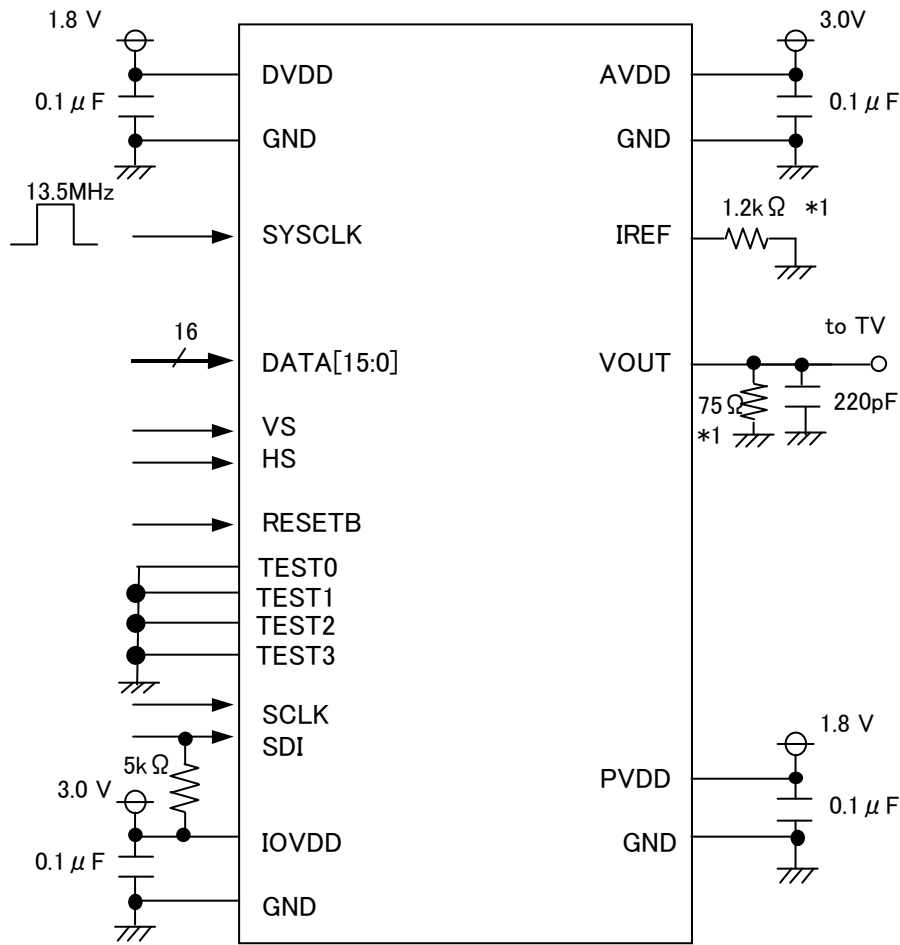
*1 Use 75Ω resistor and 1.2kΩ resistor with precision ±1%.

Application example

The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

●Application circuit diagram 2



601 input mode

Fig.7. Application Circuit Diagram Example

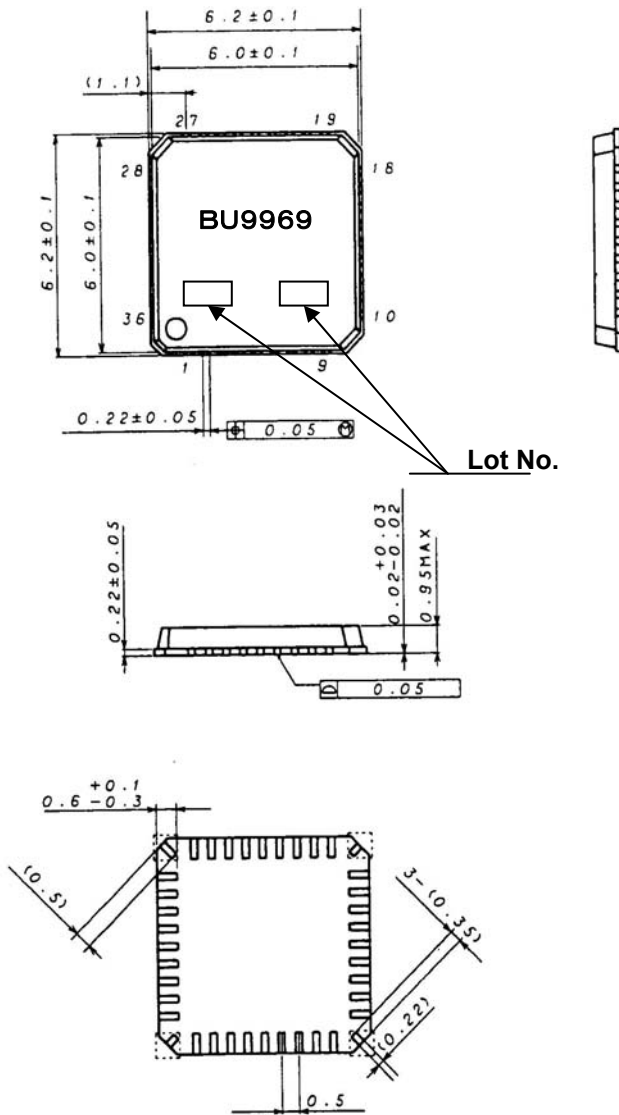
*1 Use 75Ω resistor and 1.2kΩ resistor with precision ±1%.

Application example

The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.

When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.

●External Dimensional Drawing



Lot No.

(Note) It must not be mounted at the dotted line part.

Figure number : EX346-5001-3

Fig.8. BU9969KN External Dimensional Drawing

●Ordering part number

B	U
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Part No.

9	9	6	9
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Part No.

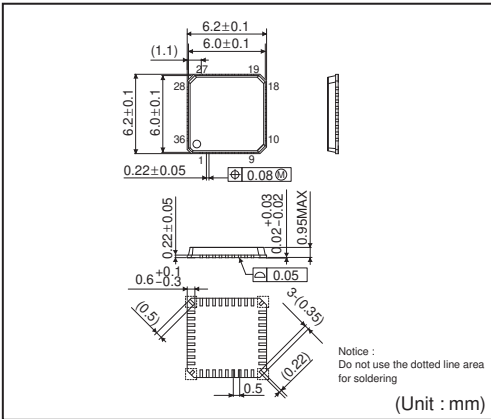
K	N
---	---

Package
KN: VQFN36

-	E	2
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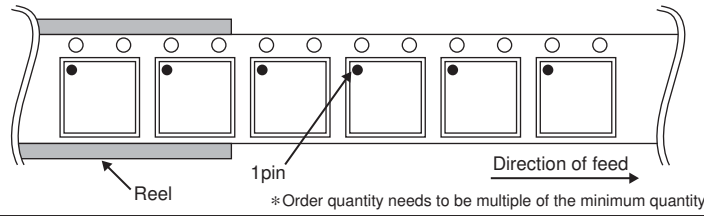
Packaging and forming specification
E2: Embossed tape and reel

VQFN36



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1 pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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