Chipsmall

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We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Digital Video Encorders

CPU bus interface

BU9972GU

No.09067EAT01

ROHM Electronic Components

Pb Free

RoHS Directive Compliance

●Description

BU9972GU is a digital video encoder IC for CPU bus interface.

It allows captured images (e.g. downloaded or on mobile phones) to be viewed on a TV monitor. In addition, a digital filter is built in for high image quality, and both multifunction and simple types are available for greater compatibility.

●Features

Video Format： NTSC-M, PAL-B/D/G/H/I standard compliant

Input Image Data Format： YCbCr 4:2:2 8 bits/16 bits, RGB 16 bits (R: 5 bits/G: 6 bits/B: 5 bits)

BUS I/F： Master / Slave mode Support

10-bit Video-DAC Built-in, PLL Built-in

Image Expansion Function, Image Display Position Adjustment Function

● Absolute Maximum Ratings   (Ta = 25℃)

Parameter	Symbol	Ratings	Unit
Digital supply voltage	DVDD	-0.2 ～ 2.5	V
PLL supply voltage	PVDD	-0.2 ～ 2.5	V
DAC supply voltage	AVDD	-0.2 ～ 4.5	V
I/O supply voltage	IOVDD	-0.2 ～ 4.5	V
Power dissipation (*1)	Pd	570	mW
Storage temperature range	Tstg	-25 ～ ＋125	℃

(*1)   A measured value at mounting on a board（Size: 114.3mm x 76.2mm x 1.6mm, 4-layer）implemented in relation to SEMI.

In the case of exceeding Ta=25℃, 5.7mW should be reduced per 1℃.

* The radiation-resistance design is not carried out.

* Operation is not guaranteed.

●Operating Conditions (Ta= -20～＋70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	DVDD	1.7	1.8	1.9	V
PLL supply voltage	PVDD	1.7	1.8	1.9	V
DAC supply voltage	AVDD	2.7	2.85	3.0	V
I/O supply voltage (*1)	IOVDD	1.7	1.8	1.9	V
		2.7	2.85	3.0	V

(*1) Usage limitation: IOVDD = 1.8V±0.1V or 2.85V±0.15V

2009.03 - Rev.A

●Electrical characteristics

（Unless otherwise noted, Ta=25℃、DVDD=PVDD=1.8V、IOVDD=2.85V、AVDD=2.85V、DVSS=PVSS=IOVSS=AVSS=GND=0V）

Parameter	Symbol	Mi.	Typ.	Max.	Unit	Conditions
Digital Operating Current	IDDCO	-	40	60	mA	Ta=25℃ (*1)
I/O Operating Current	IDDIO	-	5	10	mA	Ta=25℃ (*1)
Digital Static Current	ISTDCO	-	10	25	μA	RESETB=GND、Ta=25℃
I/O Static Current	ISTDIO	-	5	15	μA	RESETB=GND、Ta=25℃ Fix input terminals to GND.
H Input Voltage	VIH	IOVDD *0.8	-	IOVDD +0.2	V	
L Input Voltage	VIL	-0.2	-	IOVDD *0.2	V	
H/L Input Leak Current	IIL	-3	-	3	μA	VIN=IOVDD/GND
H Input Current	IIHT	10	-	200	μA	VIN=IOVDD
H Output Voltage	VOH	IOVDD -0.4	-	IOVDD	V	IOH=2mA
L Output Voltage	VOL	IOVSS	-	0.4	V	IOL=2mA
Video DAC Resolution	RES	-	-	10	Bits	
Video DAC Operating Current	IDDV	-	38	45	mA	R_L=37.5Ω、R_{IREF}=1.2kΩ
Video DAC Static Current	ISTV	-	1	5	μA	RESETB=GND、Ta=25℃
PLL Operating Current	IDDP	-	0.5	1.5	mA	
PLL Static Current	ISTP	-	1	5	μA	RESETB=GND、Ta=25℃

(*1) A measured value at QVGA color-bar image output in expand mode.
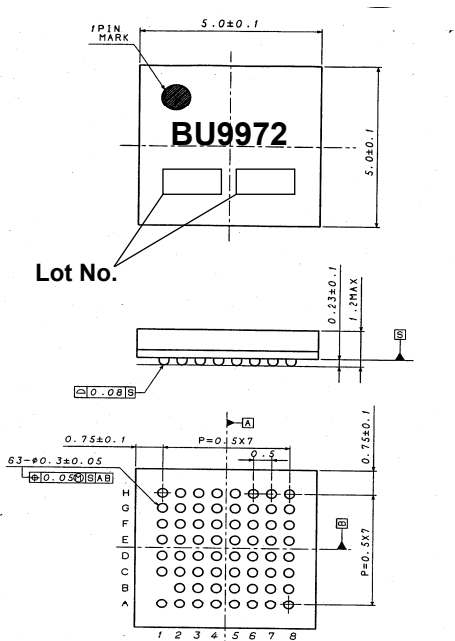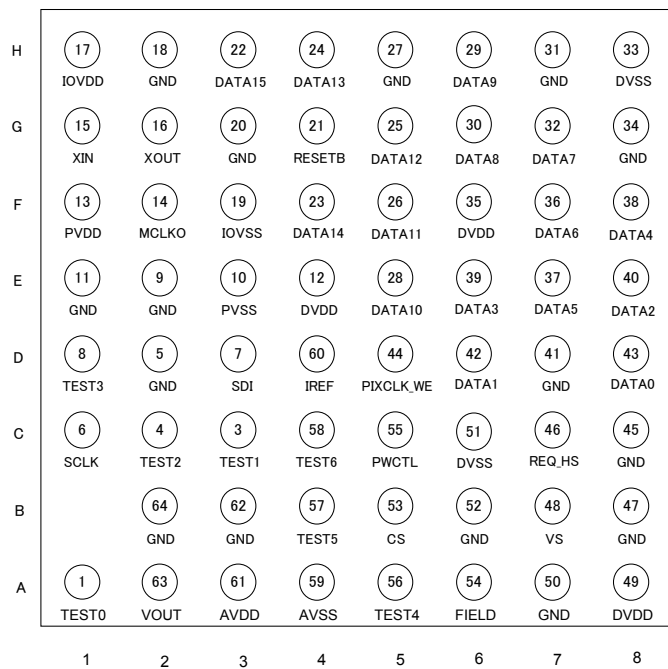
●Block diagram
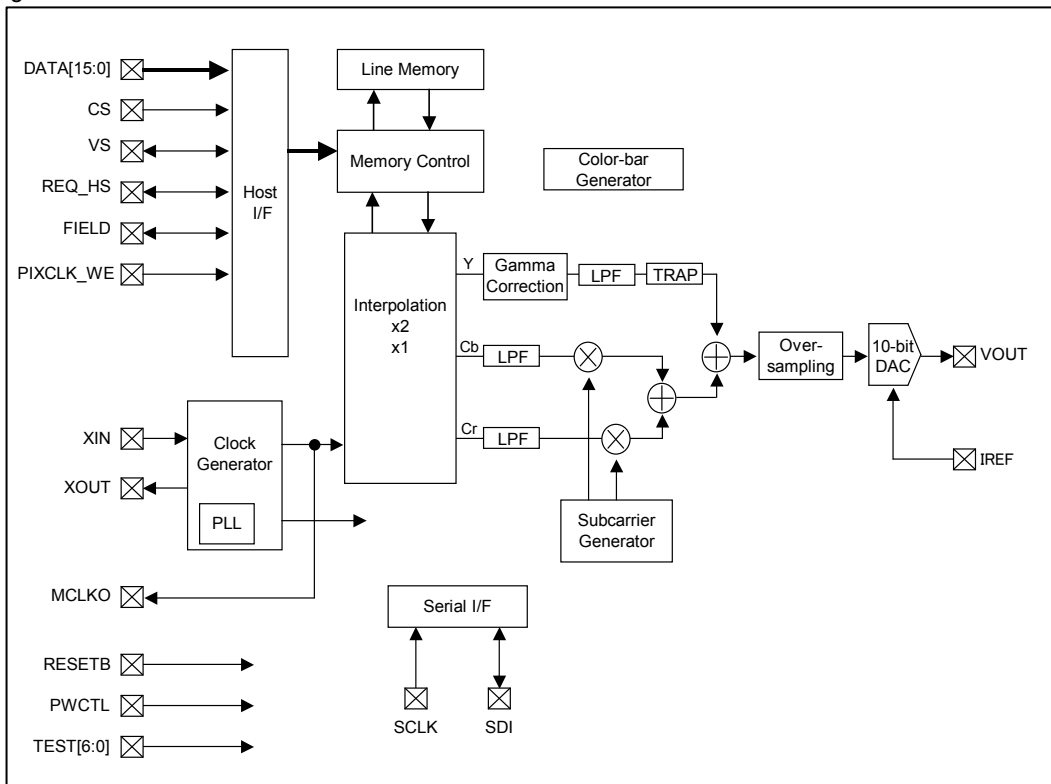
●Terminal functions

Terminal	Terminal	Description	Terminal	Terminal	Description	Terminal	Terminal	Description
1	TEST0	Test pin.	23	DATA14	Pixel data input.	45	GND	Connect to ground.
2	N.C.	No Connection.	24	DATA13	Pixel data input.	46	REQ_HS	Data request / Horizontal synchronizing signal.
3	TEST1	Test pin.	25	DATA12	Pixel data input.	47	GND	Connect to ground.
4	TEST2	Test pin.	26	DATA11	Pixel data input.	48	VS	Vertical synchronizing signal.
5	GND	Connect to ground.	27	GND	Connect to ground.	49	DVDD	Digital power supply.
6	SCLK	Serial clock.	28	DATA10	Pixel data input.	50	GND	Connect to ground.
7	SDI	Serial data.	29	DATA9	Pixel data input.	51	DVSS	Connect to ground.
8	TEST3	Test pin.	30	DATA8	Pixel data input.	52	GND	Connect to ground.
9	GND	Connect to ground.	31	GND	Connect to ground.	53	CS	Identify whether input pixel data is valid or not.
10	PVSS	PLL ground.	32	DATA7	Pixel data input.	54	FIELD	Field identification signal.
11	GND	Connect to ground.	33	DVSS	Connect to ground.	55	PWCTL	Power down control input.
12	DVDD	Digital power supply.	34	GND	Connect to ground.	56	TEST4	Test pin.
13	PVDD	PLL power supply.	35	DVDD	Digital power supply.	57	TEST5	Test pin.
14	MCLKO	System clock signal output.	36	DATA6	Pixel data input.	58	TEST6	Test pin.
15	XIN	PLL reference clock output / connect to oscillator.	37	DATA5	Pixel data input.	59	AVSS	DAC ground.
16	XOUT	Oscillator output.	38	DATA4	Pixel data input.	60	IREF	Reference voltage output for DAC.
17	IOVDD	I/O power supply.	39	DATA3	Pixel data input.	61	AVDD	DAC power supply.
18	GND	Connect to ground.	40	DATA2	Pixel data input.	62	GND	Connect to ground.
19	IOVSS	Connect to ground.	41	GND	Connect to ground.	63	VOUT	Analog composite video
20	GND	Connect to ground.	42	DATA1	Pixel data input.	64	GND	Connect to ground.
21	RESETB	System reset input.	43	DATA0	Pixel data input.			
22	DATA15	Pixel data input.	44	PIXCLK_WE	Pixel clock input.			

●Package outline

VBGA063T050 (Unit : mm)

●Ball assignment　（Bottom View）

	1	2	3	4	5	6	7	8
H	17 IOVDD	18 GND	22 DATA15	24 DATA13	27 GND	29 DATA9	31 GND	33 DVSS
G	15 XIN	16 XOUT	20 GND	21 RESETB	25 DATA12	30 DATA8	32 DATA7	34 GND
F	13 PVDD	14 MCLKO	19 IOVSS	23 DATA14	26 DATA11	35 DVDD	36 DATA6	38 DATA4
E	11 GND	9 GND	10 PVSS	12 DVDD	28 DATA10	39 DATA3	37 DATA5	40 DATA2
D	8 TEST3	5 GND	7 SDI	60 IREF	44 PIXCLK_WE	42 DATA1	41 GND	43 DATA0
C	6 SCLK	4 TEST2	3 TEST1	58 TEST6	55 PWCTL	51 DVSS	46 REQ_HS	45 GND
B		64 GND	62 GND	57 TEST5	53 CS	52 GND	48 VS	47 GND
A	1 TEST0	63 VOUT	61 AVDD	59 AVSS	56 TEST4	54 FIELD	50 GND	49 DVDD

●**Cautions on use**

（1）Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

（2）Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

（3）Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

（4）Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

（5）GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

（6）Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

（7）Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

（8）Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

（9）Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.
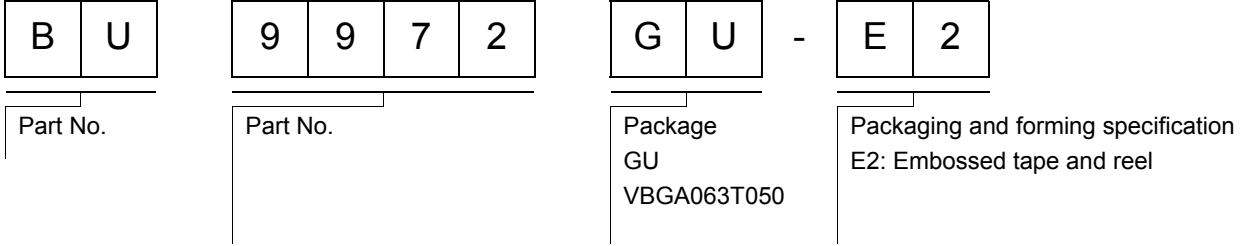
（10）Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.
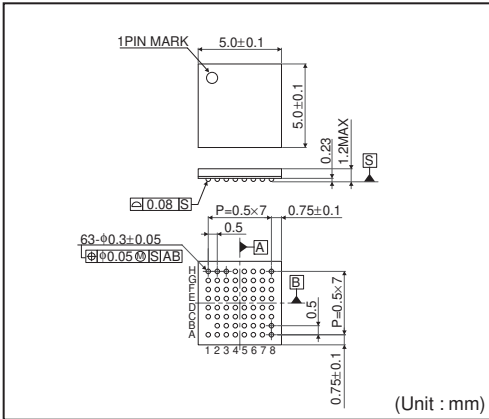
（11）External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●**Ordering part number**

| B | U | | 9 | 9 | 7 | 2 | | G | U | - | E | 2 |

Part No.

Part No.

Package
GU
VBGA063T050

Packaging and forming specification
E2: Embossed tape and reel

VBGA063T050

1PIN MARK   5.0±0.1

5.0±0.1

0.23

1.2MAX

S

0.08 S

P=0.5×7   0.75±0.1

0.5

63-φ0.3±0.05

φ0.05 S A B

A

B

0.5   P=0.5×7

H G F E D C B A

1 2 3 4 5 6 7 8

0.75±0.1

(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

1pin

Direction of feed

Reel

＊Order quantity needs to be multiple of the minimum quantity.
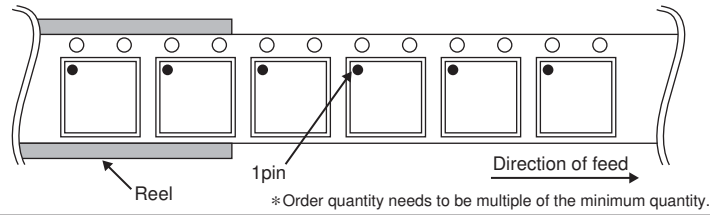
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