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IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors

founded by NXP

BUJ302AD

NPN power transistor

11 October 2016 — Product data sheet

1. General description

High voltage, high speed planar passivated NPN power switching transistor in a SOT428 (DPAK) surface mountable plastic package.

2. Features and benefits

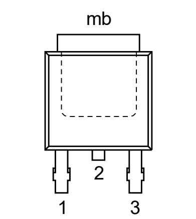
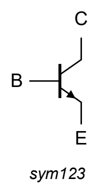
- Fast switching
- Low thermal resistance
- Surface mountable package
- Very high voltage capability
- Very low switching and conduction losses

3. Applications

- DC-to-DC converters
- High frequency electronic lighting ballasts
- Inverters
- Motor control systems

4. Pinning information

Table 1. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	B	base	 DPAK (SOT428)	
2	C	collector[1]		
3	E	emitter		
mb	C	mounting base; connected to collector		

[1] it is not possible to make a connection to pin 2 of the SOT428 (DPAK) package

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
BUJ302AD	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CESM}	collector-emitter peak voltage	V_{BE} = 0 V		-	1050	V
V_{CEO}	collector-emitter voltage	I_B = 0 A		-	400	V
V_{EBO}	emitter-base voltage	I_C = 0 A; I_E = 2 A; t_p < 10 ms		-	24	V
I_C	collector current	Fig. 1; Fig. 2; Fig. 3		-	4	A
I_{CM}	peak collector current			-	8	A
I_B	base current			-	2	A
I_{BM}	peak base current			-	4	A
P_{tot}	total power dissipation	T_{mb} ≤ 25 °C; Fig. 4		-	80	W
T_{stg}	storage temperature			-65	150	°C
T_j	junction temperature			-	150	°C

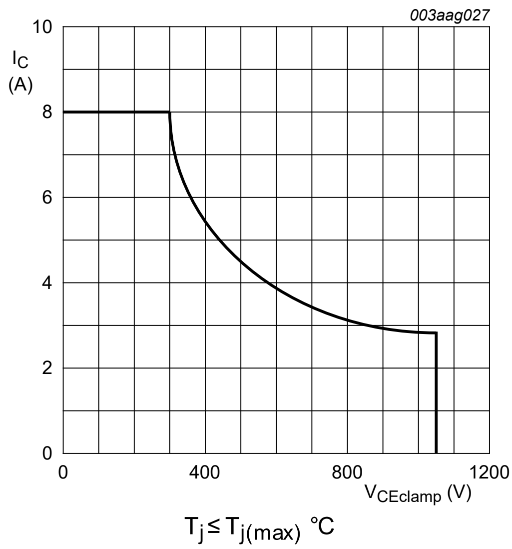
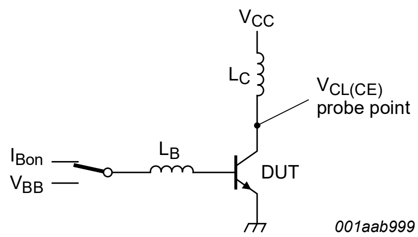


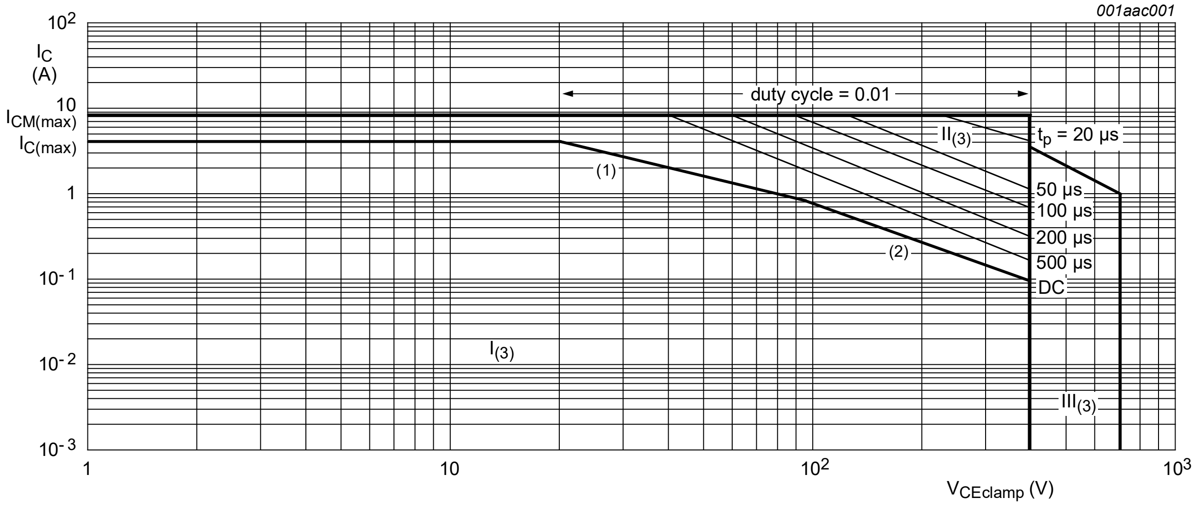
Fig. 1. Reverse bias safe operating area



$V_{CL(CE)} \leq 1000$ V; $V_{CC} = 150$ V; $V_{BB} = -5$ V;

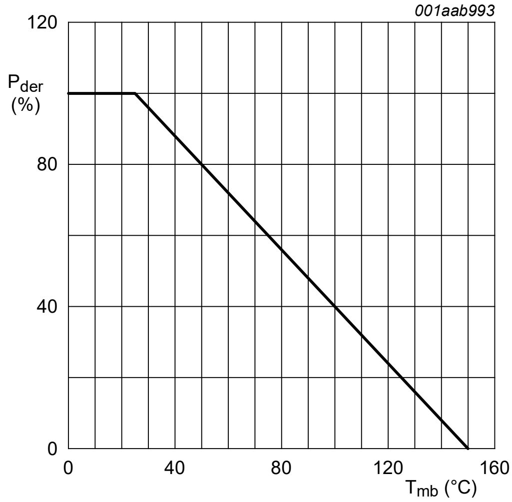
$L_B = 1\ \mu H$; $L_C = 200\ \mu H$

Fig. 2. Test circuit for reverse bias safe operating area



1)Ptot maximum and Ptot peak maximum lines
2)Second breakdown limits
3) I = Region of permissable DC operation
II = Extension for repetitive pulse operation
III = Extension during turn-on in single transistor converters
provided that RBE ≤ 100 Ω and tp ≤ 0.6 μs

Fig. 3. Forward bias safe operating area for Tmb ≤ 25 °C



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 4. Normalized total power dissipation as a function of mounting base temperature

7. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	1.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board (FR4) mounted; minimum footprint		-	75	-	K/W

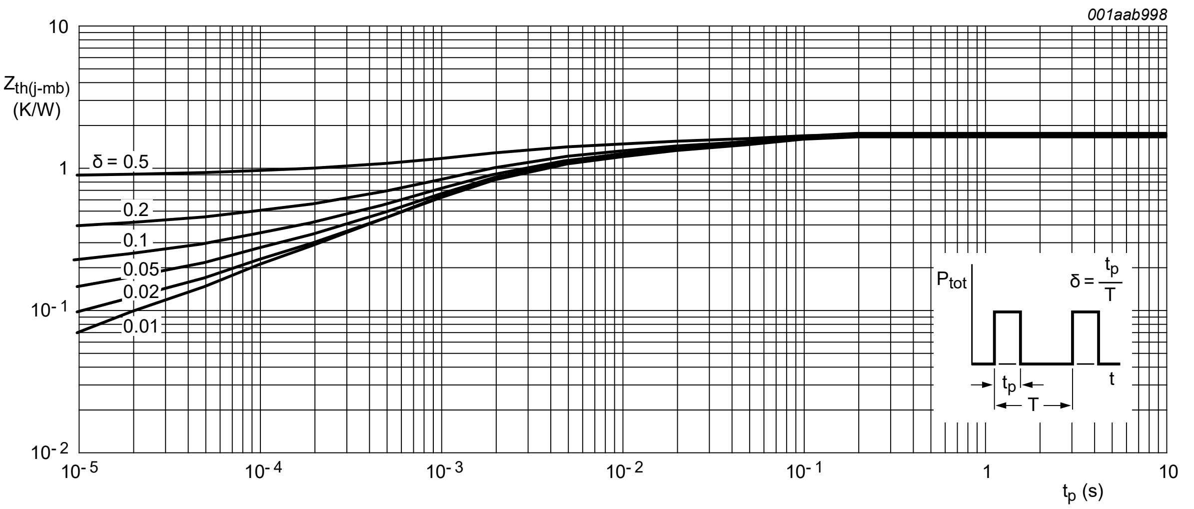


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse width

8. Characteristics

Table 5. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{CES}	collector-emitter cut-off current (base shorted)	V_{BE} = 0 V; V_{CE} = 1050 V		-	0.2	10	µA
I_{CEO}	collector-emitter cut-off current (base open)	V_{CE} = 400 V; I_B = 0 A; T_{mb} = 25 °C		-	10	250	mA
$V_{(BR)EBO}$	emitter-base breakdown voltage (collector open)	I_B = 1 mA; I_C = 0 A; T_{mb} = 25 °C		15	19	-	V
V_{CEOsus}	collector-emitter sustaining voltage (base open)	I_B = 0 A; I_C = 10 mA; L_C = 25 mH; T_{mb} = 25 °C; Fig. 6; Fig. 7	[1]	400	470	-	V
V_{CEsat}	collector-emitter saturation voltage	I_C = 1 A; I_B = 0.2 A; T_{mb} = 25 °C; Fig. 8; Fig. 9	[1]	-	0.15	0.5	V
		I_C = 3.5 A; I_B = 1 A; T_{mb} = 25 °C; Fig. 8; Fig. 9	[1]	-	0.6	1.5	V
V_{BEsat}	base-emitter saturation voltage	I_C = 3.5 A; I_B = 1 A; T_{mb} = 25 °C; Fig. 10	[1]	-	1.1	1.5	V
h_{FE}	DC current gain	I_C = 0.1 A; V_{CE} = 5 V; T_{mb} = 25 °C; Fig. 11	[1]	48	66	100	
		I_C = 0.8 A; V_{CE} = 3 V; T_{mb} = 25 °C; Fig. 12	[1]	25	42	50	
Dynamic characteristics							
t_s	storage time	I_C = 2.5 A; I_{Bon} = 0.5 A; I_{Boff} = -0.5 A; R_L = 60 Ω; V_{BB} = -5 V; T_{mb} = 25 °C; resistive load; t_p = 300 µs; Fig. 13; Fig. 14		-	-	3.5	µs
t_f	fall time			-	-	500	ns

[1] Pulse test: pulse duration ≤ 300 µs, duty cycle ≤ 2 %

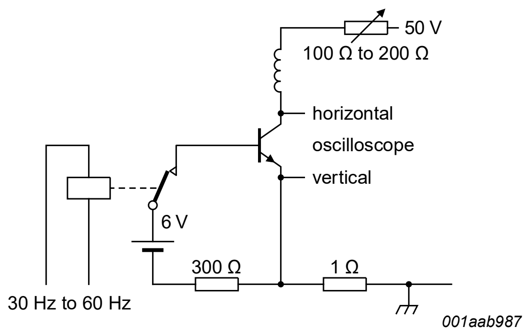


Fig. 6. Test circuit for collector-emitter sustaining voltage

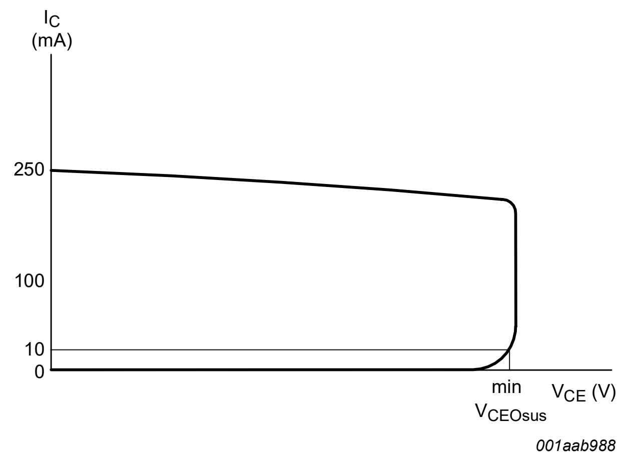


Fig. 7. Oscilloscope display for collector-emitter sustaining voltage test waveform

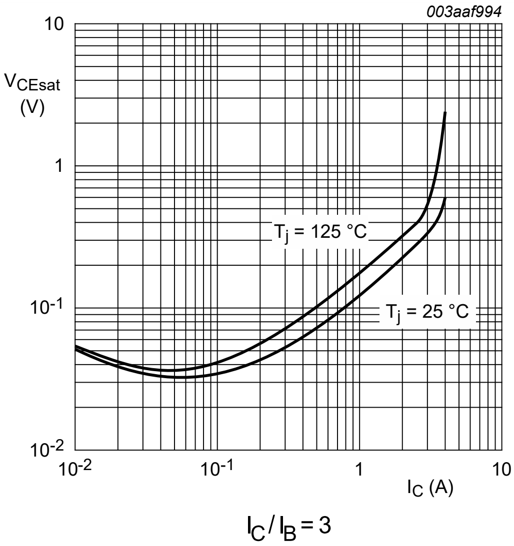


Fig. 8. Collector-emitter saturation voltage as a function of collector current; typical values

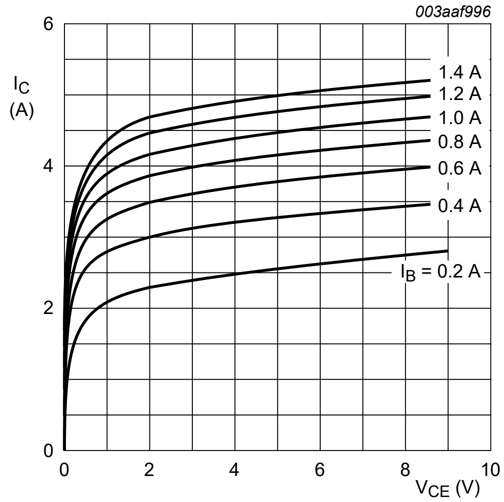


Fig. 9. Collector current as a function of collector-emitter voltage; typical values

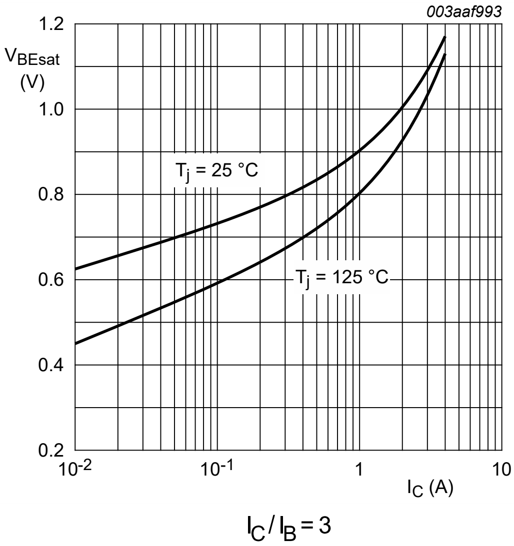


Fig. 10. Base-emitter saturation voltage as a function of collector current; typical values

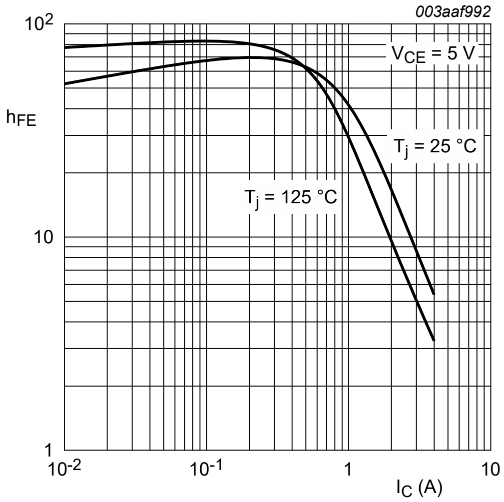


Fig. 11. DC current gain as a function of collector current; typical values

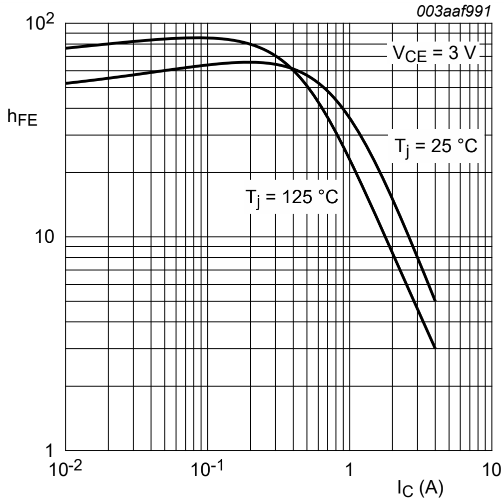
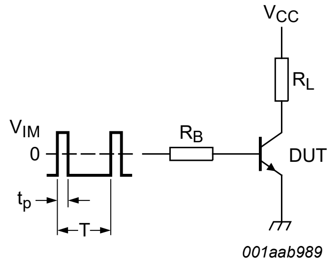


Fig. 12. DC current gain as a function of collector current; typical values



$V_{IM} = -6$ to $+8$ V; $V_{CC} = 250$ V; $t_p = 20$ µs; $\delta = \frac{t_p}{T} = 0.01$

R_B and R_L calculated from I_{Con} and I_{Bon} requirements.

Fig. 13. Test circuit for resistive load switching

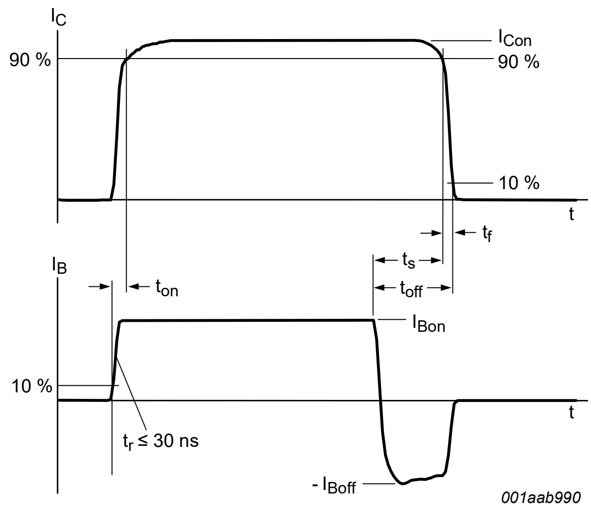
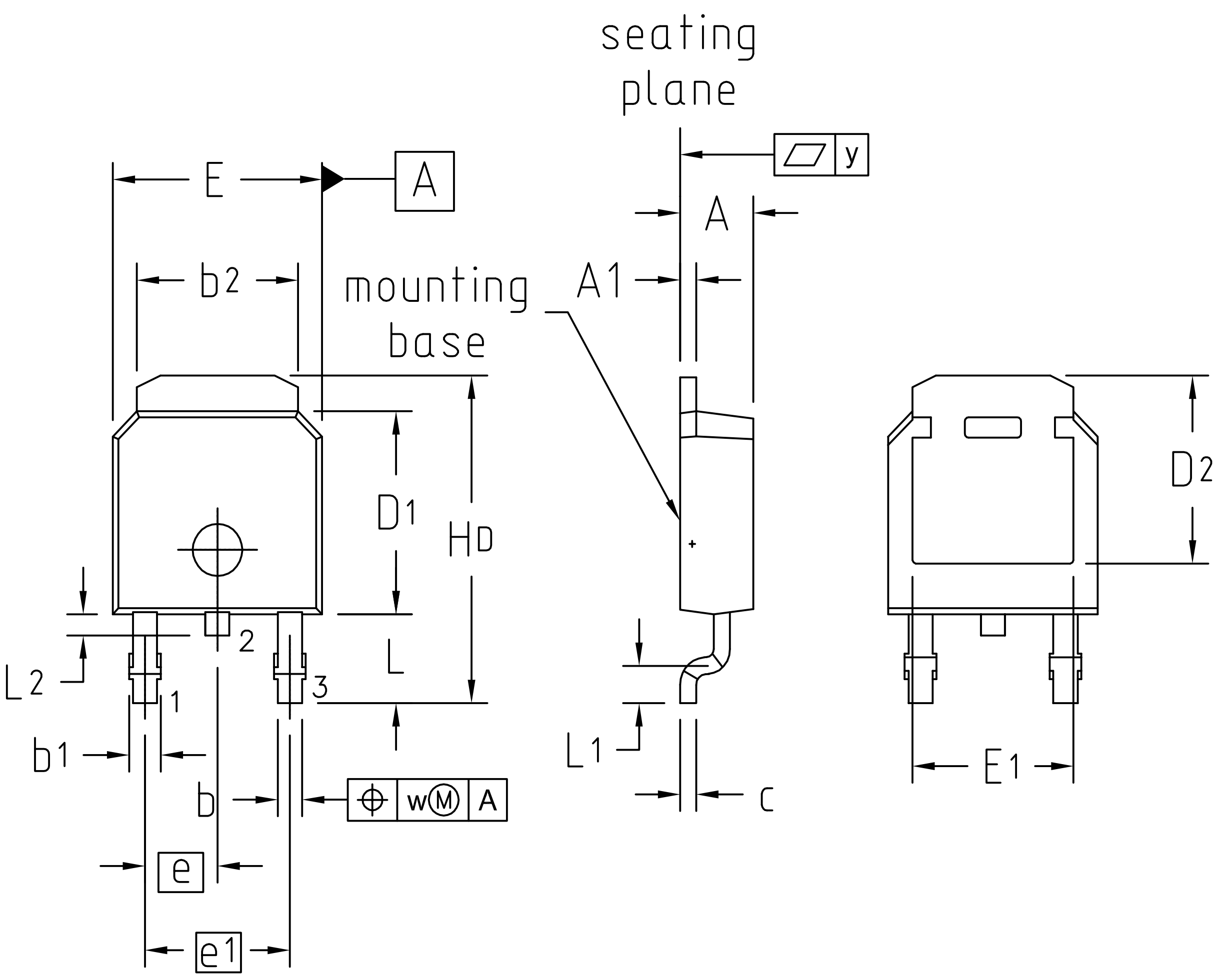


Fig. 14. Switching times waveforms for resistive load

9. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428



UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2	E	E_1	e	e_1	H_D	L	L_1	L_2	w	y
mm	2.38	0.93	0.89	1.1	5.46	0.56	6.22	4.00	6.73	4.45	2.285	4.57	10.40	2.95	0.5	0.90	0.2	0.20
	2.22	0.46	0.71	0.9	5.00	0.20	5.98	min.	6.47	min.			9.60	2.55	min.	0.50		max.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428		TO-252				

Fig. 15. Package outline DPAK (SOT428)

10. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 11 October 2016