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BUK7E1R9-40E

N-channel TrenchMOS standard level FET 19 May 2016

Product data sheet

General description

Standard level N-channel MOSFET in a SOT226 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

Features and benefits 2.

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with V_{GS(th)} rating of greater than 1 V at 175 °C

Applications

- 12 V Automotive systems
- Electric and electro-hydraulic power steering
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	[1]	-	-	120	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	324	W
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 ^{\circ}\text{C};$ Fig. 11		-	1.5	1.9	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 13; Fig. 14		-	34.7	-	nC

^[1] Continuous current is limited by package.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D I
2	D	drain		
3	S	source		G
mb	D	mounting base; connected to drain		mbb076 S
			I2PAK (SOT226)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK7E1R9-40E	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226		

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7E1R9-40E	BUK7E1R9-40E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	40	V
V_{GS}	gate-source voltage	DC; T _j ≤ 175 °C		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	324	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 2</u>	[1]	-	120	Α
		V _{GS} = 10 V; T _{mb} = 100 °C; <u>Fig. 2</u>	[1]	-	120	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 \text{ °C}$; Fig. 3		-	1198	Α
T _{stg}	storage temperature			-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
Tj	junction temperature			-55	175	°C
Source-drain	diode			1	'	,
Is	source current	T _{mb} = 25 °C	[1]	-	120	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	1198	Α
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 120 A; $V_{sup} \le 40$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[2][3]	-	801	mJ

- [1] Continuous current is limited by package.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.

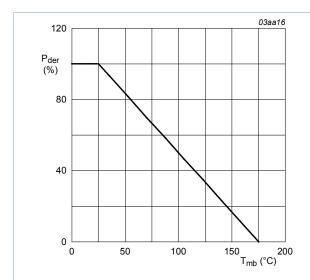
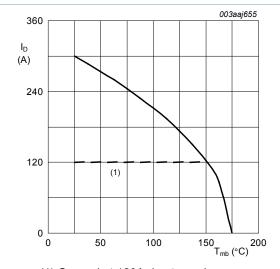


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



(1) Capped at 120A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

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N-channel TrenchMOS standard level FET

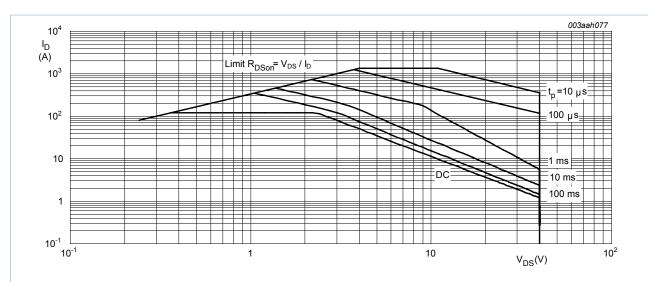
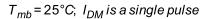


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



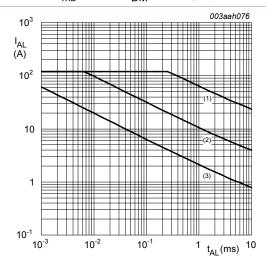


Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1)
$$T_{j(init)} = 25$$
°C; (2) $T_{j(init)} = 150$ °C; (3) Repetitive Avalanche

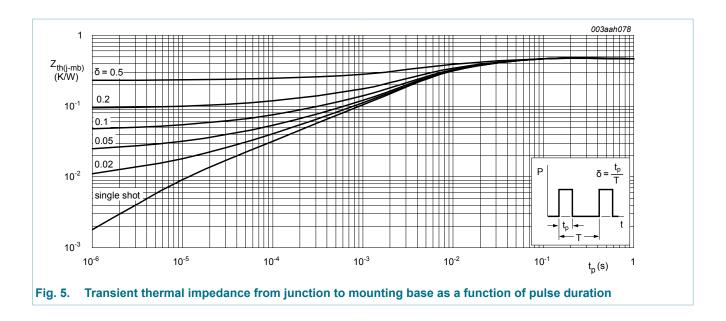
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	0.46	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	65	-	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	cteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	40	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	36	-	-	V
V _{GS(th)}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; <u>Fig. 9</u> ; <u>Fig. 10</u>	2.4	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = -55 °C; Fig. 10	-	-	4.5	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 10	1	-	-	V
I _{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	0.27	3	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	1.5	1.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12; Fig. 11	-	-	3.6	mΩ
Dynamic ch	aracteristics					
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V;	-	118	-	nC
Q _{GS}	gate-source charge	Fig. 13; Fig. 14	-	29.3	-	nC
Q_{GD}	gate-drain charge		-	34.7	-	nC

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C _{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; Fig. 15$		-	7873	10472	pF
C _{oss}	output capacitance			-	1410	1692	pF
C _{rss}	reverse transfer capacitance			-	851	1165	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$		-	35	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega$		-	49	-	ns
t _{d(off)}	turn-off delay time			-	87	-	ns
t _f	fall time			-	52	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to center of die		-	2.5	-	nH
L _S	internal source inductance	from source lead to source bonding pad		-	7.5	-	nΗ
Source-dra	in diode				'		
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}; Fig. 16$		-	0.79	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	46	-	ns
Q _r	recovered charge	V _{DS} = 25 V		-	62	-	nC

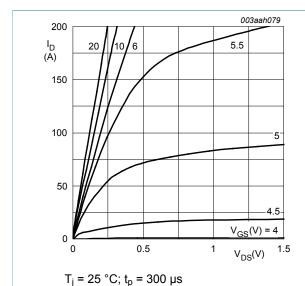


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

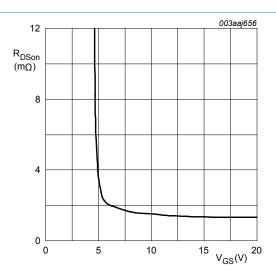


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25$$
°C; $I_D = 25A$

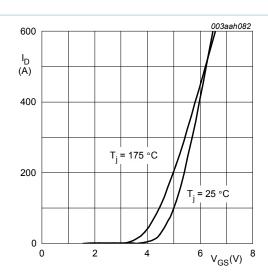


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values



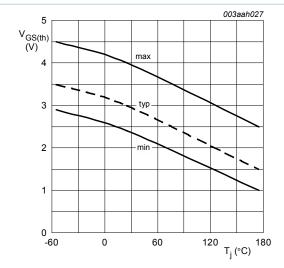


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$$I_D$$
 = 1 mA; V_{DS} = V_{GS}

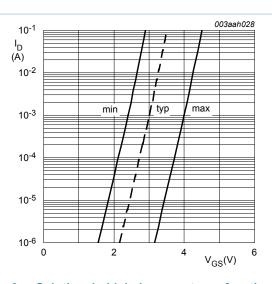


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$$T_i = 25$$
°C; $V_{DS} = 5V$

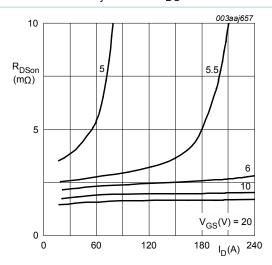


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

 T_j = 25 °C; t_p = 300 μs

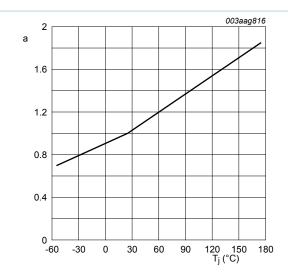


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25 °C)}}$$

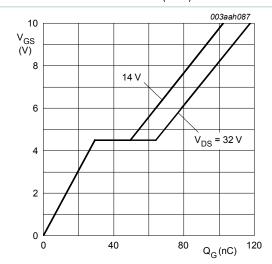


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

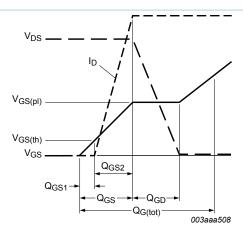


Fig. 13. Gate charge waveform definitions

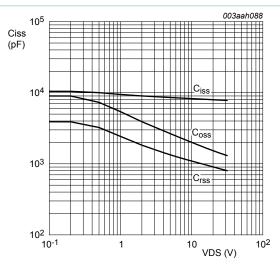


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V$$
; $f = 1MHz$

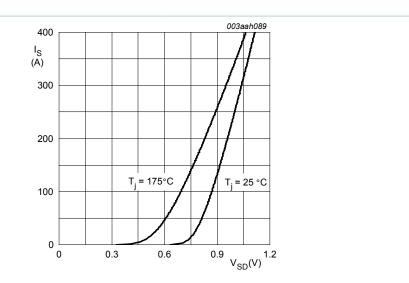


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values $V_{\rm GS} = 0V$

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11. Package outline

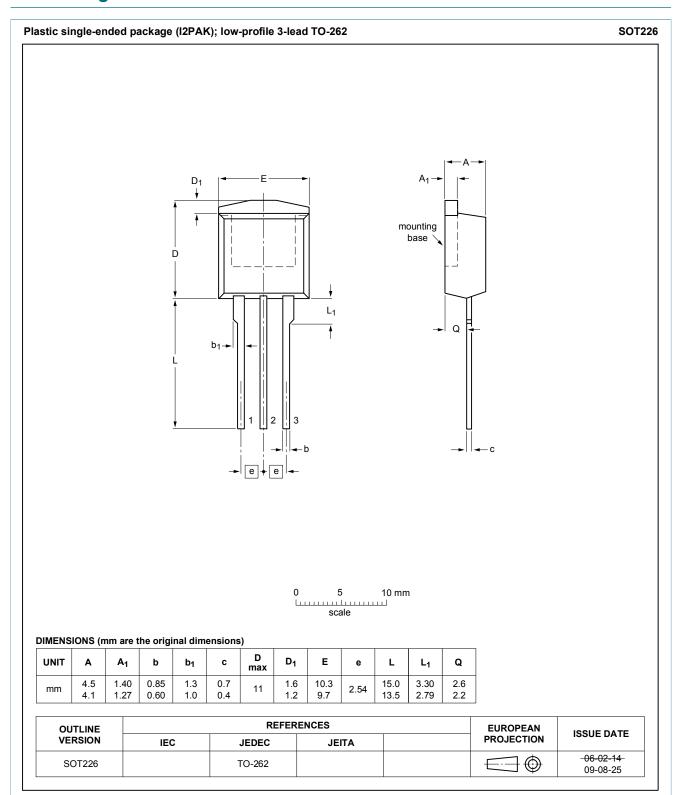


Fig. 17. Package outline I2PAK (SOT226)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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