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BUK7K23-80E

Dual N-channel 80 V, 23 mΩ standard level MOSFET

17 August 2017

Product data sheet

1. General description

Dual Standard level N-channel MOSFET in an LFPK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)}$ rating of greater than 1 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

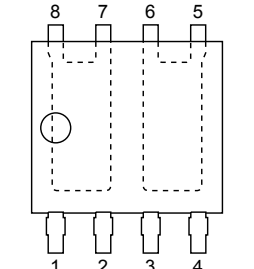
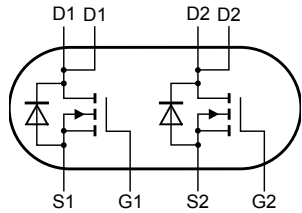
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Limiting values FET1 and FET2						
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	-	-	17	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	-	53	W
Static characteristics FET1 and FET2						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ °C};$ Fig. 11	-	17.6	23	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}; V_{DS} = 64\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ °C};$ Fig. 13 ; Fig. 14	-	7.5	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K23-80E	LFPAK56D	plastic, single ended surface mounted package (LFPAK56D); 8 leads; 1.27 mm pitch; 4.7 mm x 5.3 mm x 1.05 mm body	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K23-80E	72380E

8. Limiting values

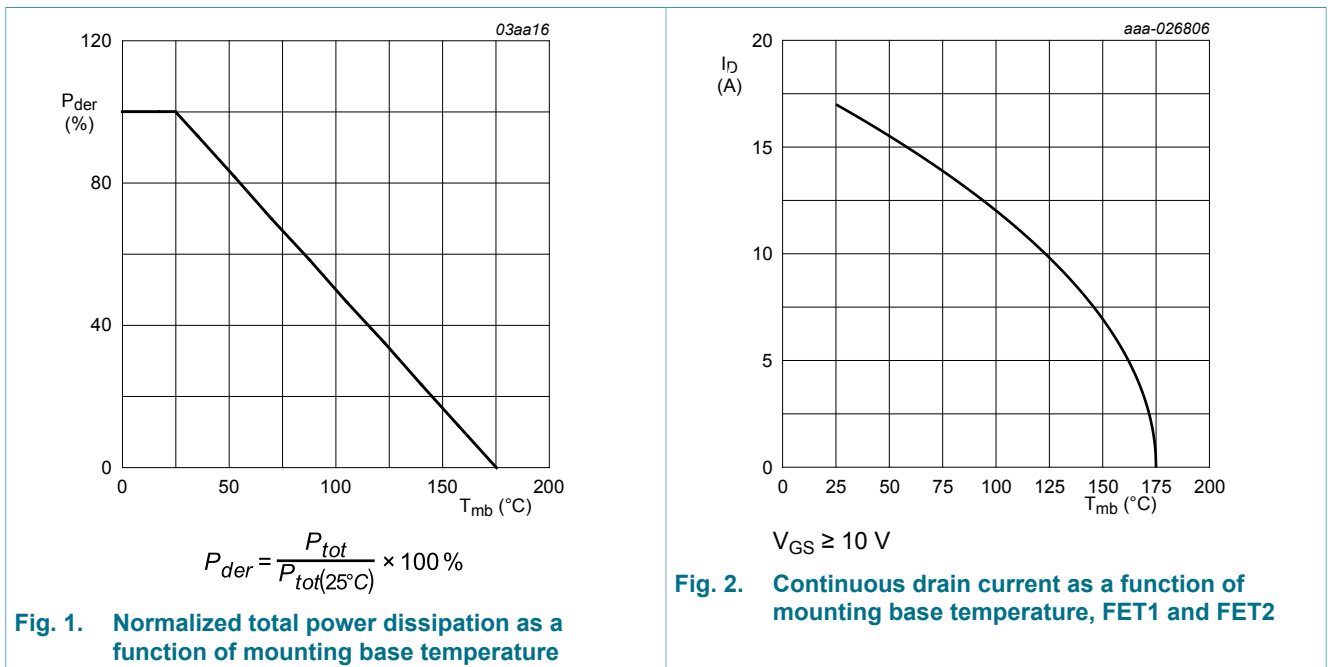
Table 5. Limiting values

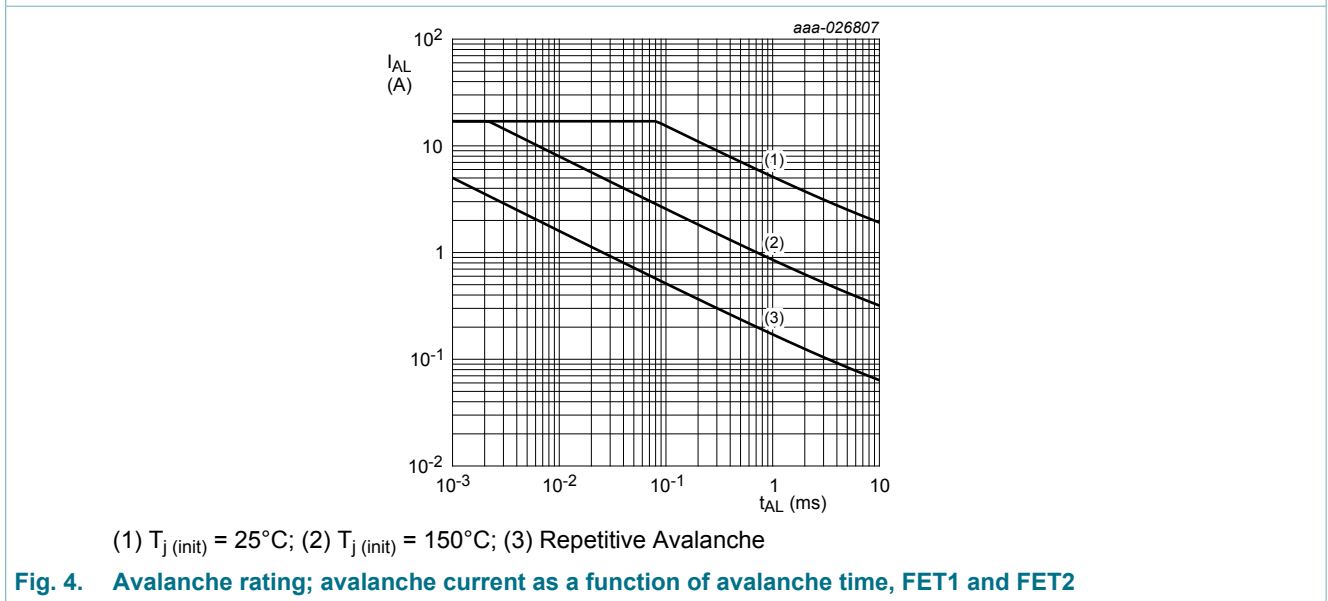
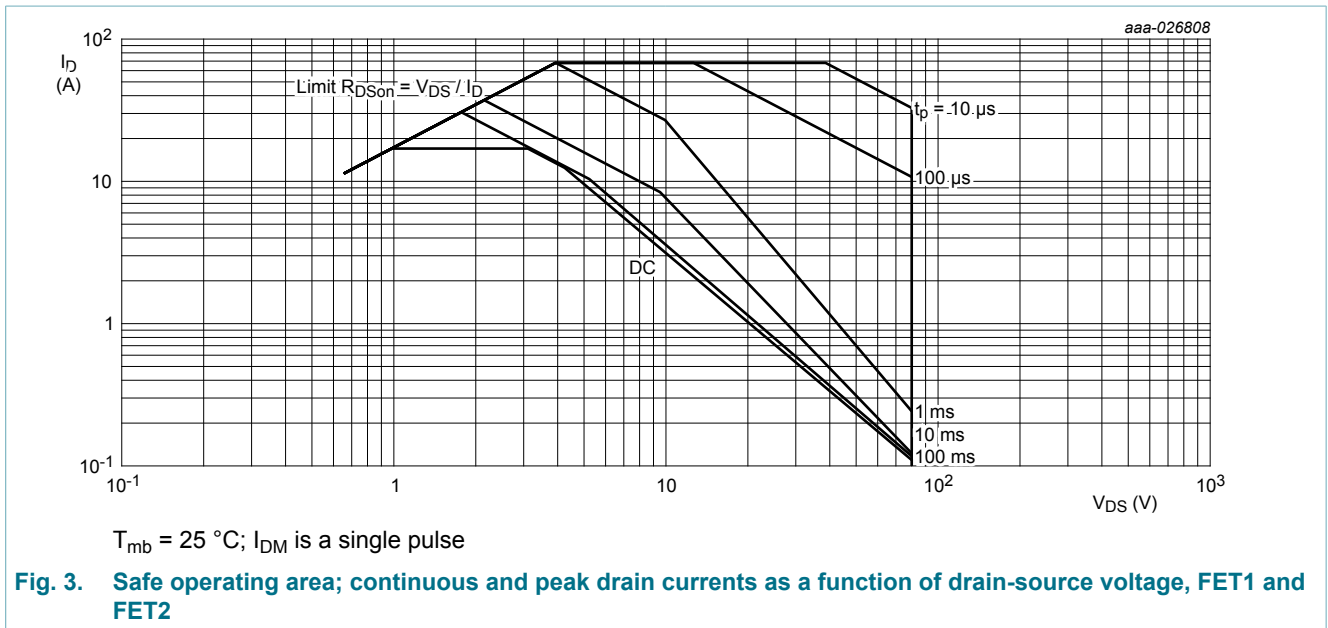
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Limiting values FET1 and FET2					
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	53	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	17	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	12	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	68	A

Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode FET1 and FET2					
I _S	source current	T _{mb} = 25 °C	-	17	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	68	A
Avalanche ruggedness FET1 and FET2					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 17 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(initial)} = 25 °C; unclamped; Fig. 4	[1] [2]	72	mJ

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

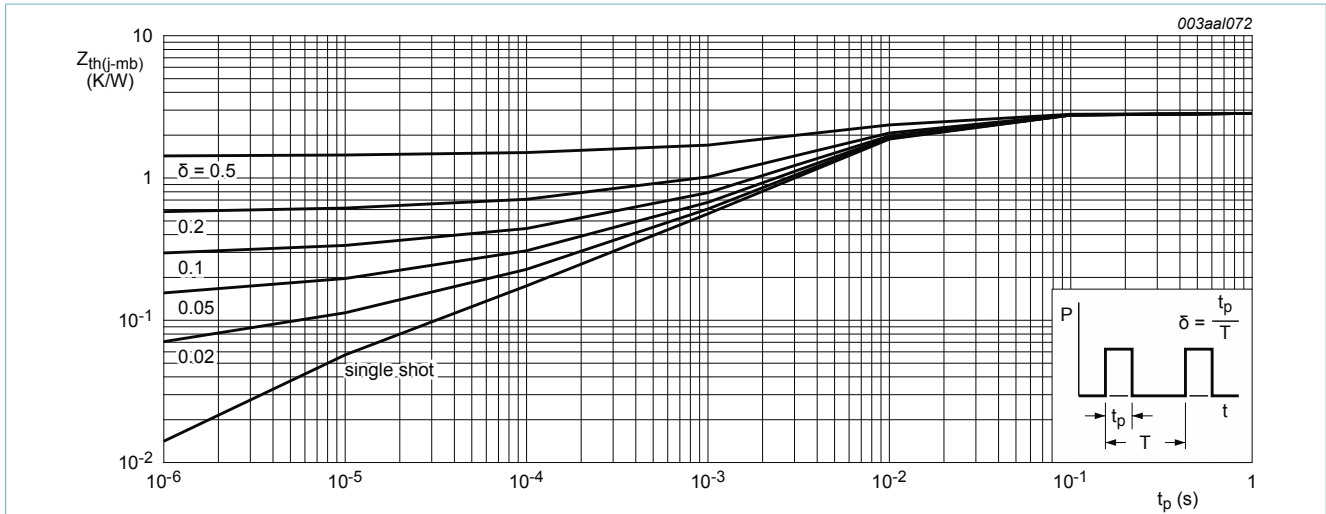


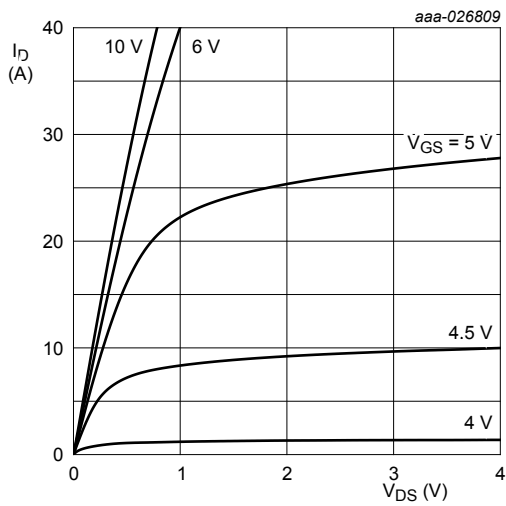
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

10. Characteristics

Table 7. Characteristics

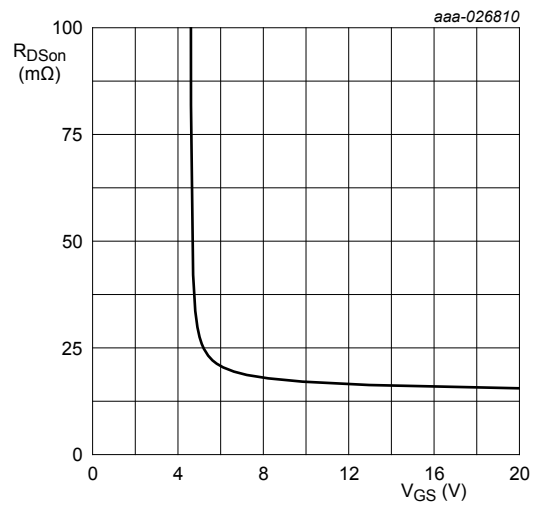
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}; \text{ Fig. 10}$	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 10}$	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 10}$	1	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	-	17.6	23	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 12}$	-	-	58	mΩ
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 10 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 13}; \text{ Fig. 14}$	-	22.8	-	nC
Q_{GS}	gate-source charge		-	5	-	nC
Q_{GD}	gate-drain charge		-	7.5	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C; \text{ Fig. 15}$	-	1159	1542	pF
C_{oss}	output capacitance		-	130	156	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rSS}	reverse transfer capacitance		-	78	107	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 60\text{ V}; R_L = 5\ \Omega; V_{GS} = 10\text{ V};$ $R_{G(ext)} = 5\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	6.4	-	ns
t_r	rise time		-	8.9	-	ns
$t_{d(off)}$	turn-off delay time		-	16.9	-	ns
t_f	fall time		-	10.9	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	27.3	-	ns
Q_r	recovered charge		-	29.8	-	nC



$T_j = 25\text{ }^\circ\text{C}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2



$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2

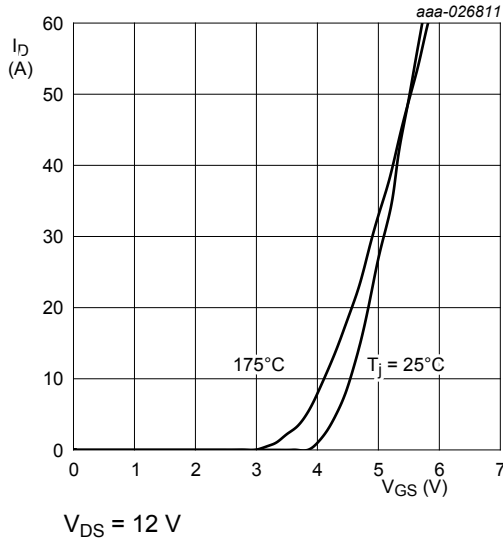


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

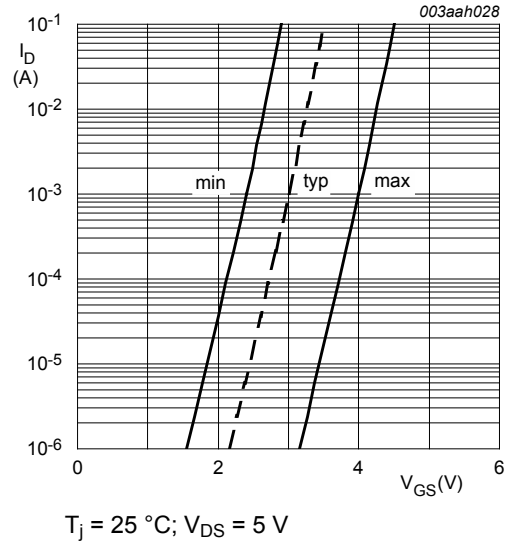


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

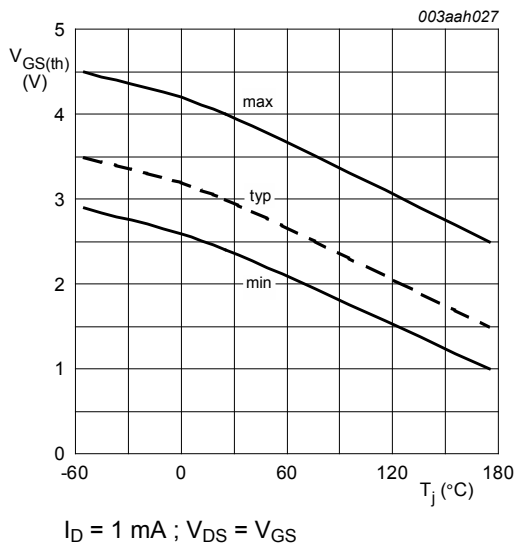


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

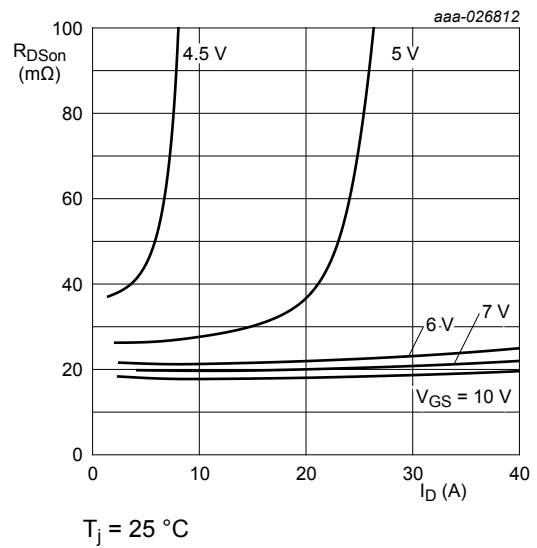
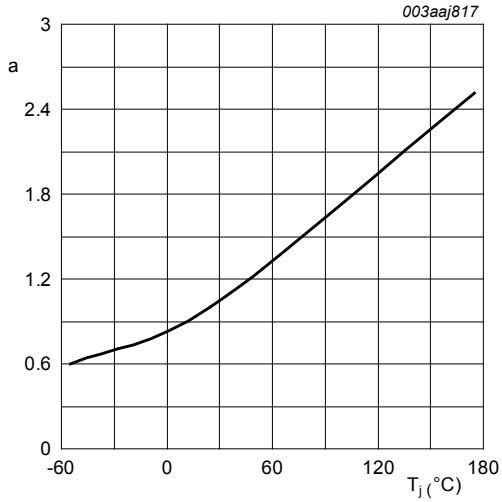
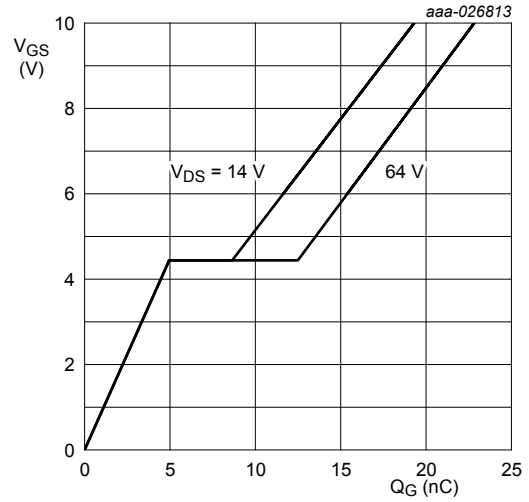


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2



$T_j = 25^{\circ}\text{C}; I_D = 10\text{A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

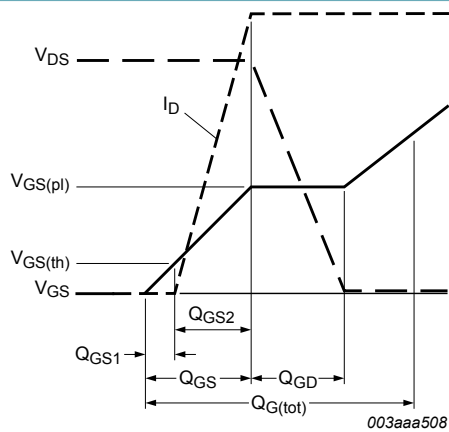
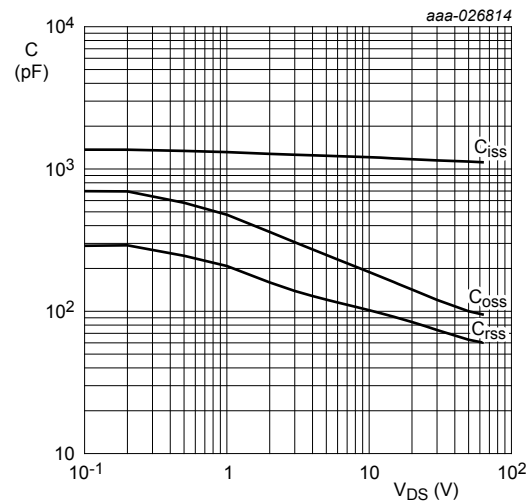
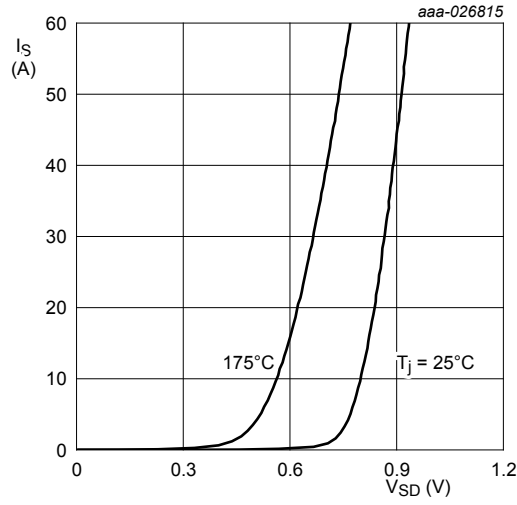


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

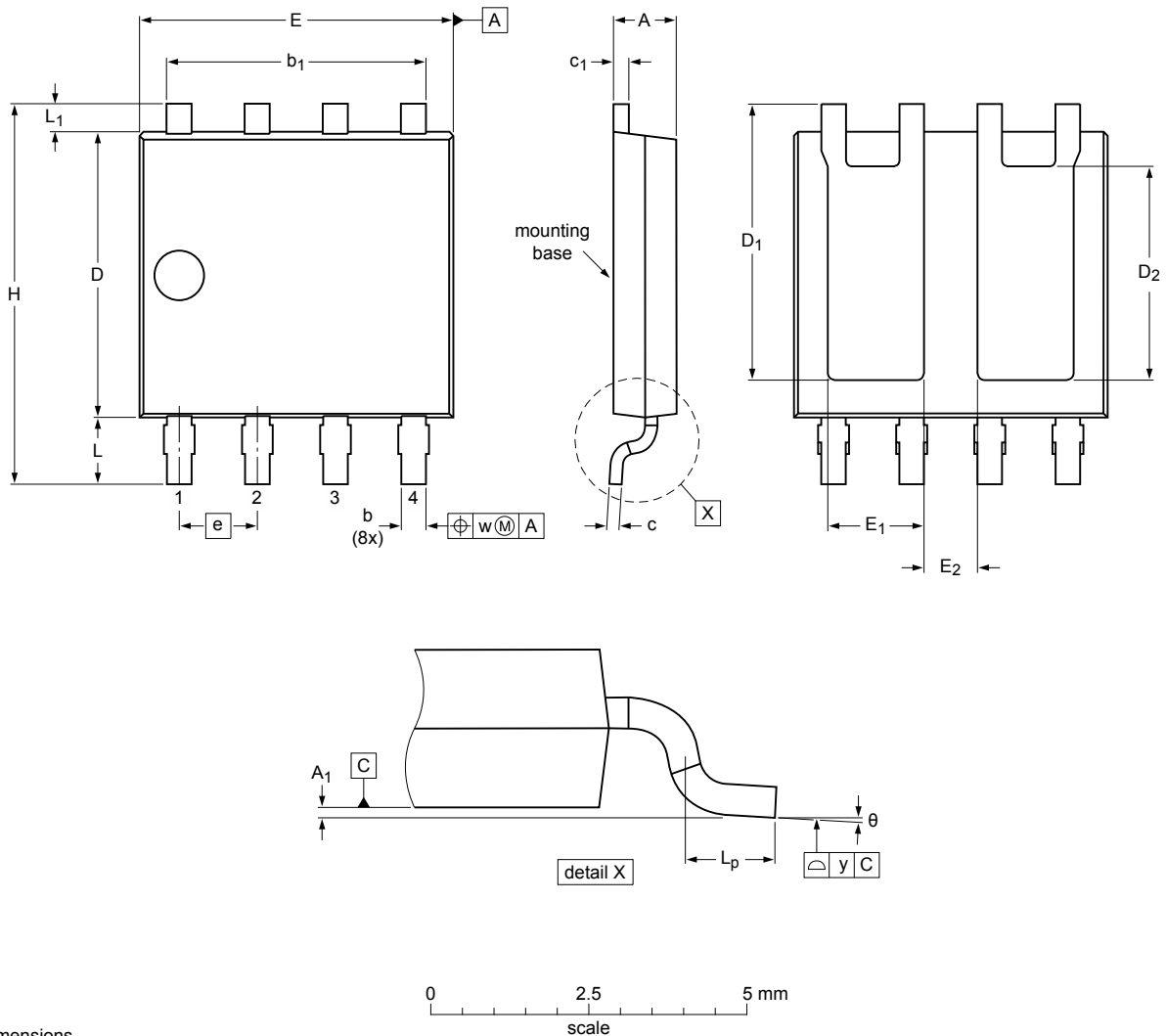


$V_{GS} = 0$ V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

11. Package outline

Plastic single ended surface mounted package LFAK56D; 8 leads SOT1205



Dimensions

Unit	A	A ₁	b	b ₁	c	c ₁	D ⁽¹⁾	D ₁ ⁽¹⁾	D ₂ ^(ref)	E ⁽¹⁾	E ₁ ⁽¹⁾	E ₂	e	H	L	L ₁	L _p	w	y	θ		
max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85		0.25	0.1	8°	
nom													1.27									
min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40				0°	

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1205					-14-08-21- 14-10-28

Fig. 17. Package outline LFAK56D (SOT1205)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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