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BUK7K52-60E

Dual N-channel 60 V, 45 mΩ standard level MOSFET

10 December 2013

Product data sheet

1. General description

Dual standard level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)}$ of greater than 1 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

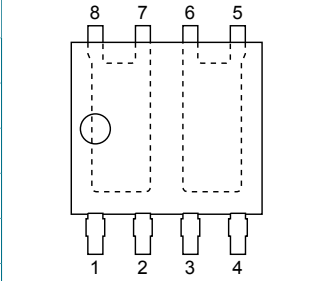
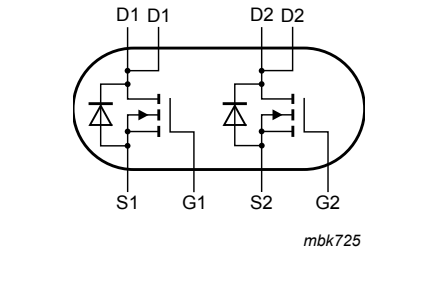
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	60	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	15.4	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	32	W
Static characteristics FET1 and FET2						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	35	45	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 5\text{ A}; V_{DS} = 48\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	-	3.5	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K52-60E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K52-60E	75260E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC	-20	20	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	15.4	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	12.6	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 4	-	71	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 2	-	32	W

Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
Source-drain diode FET1 and FET2					
I _S	source current	T _{mb} = 25 °C	-	15.4	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	71	A
Avalanche Ruggedness FET1 and FET2					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 15.4 A; V _{sup} ≤ 60 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 3	[1][2]	-	11.6 mJ

- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

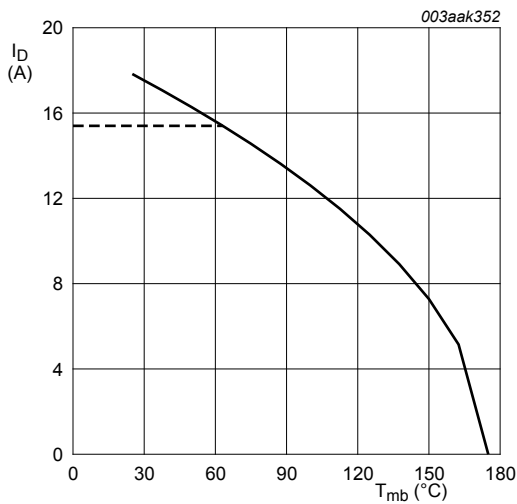


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

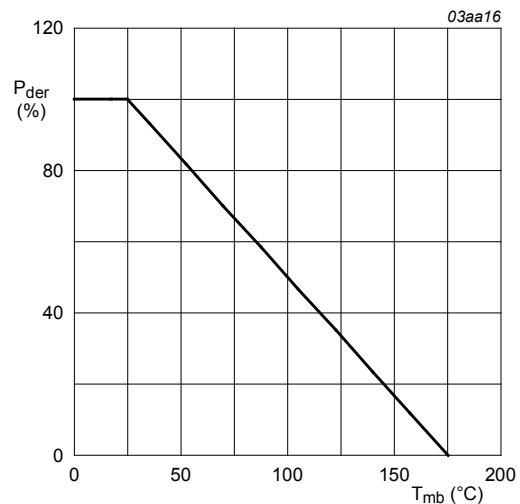


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

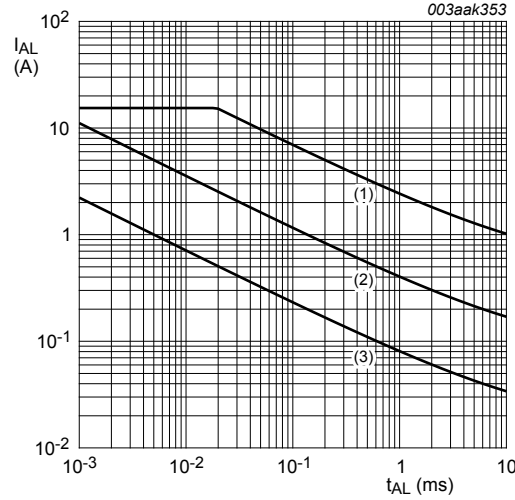


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (int)} = 25^{\circ}C$; (2) $T_{j (int)} = 150^{\circ}C$; (3) Repetitive Avalanche

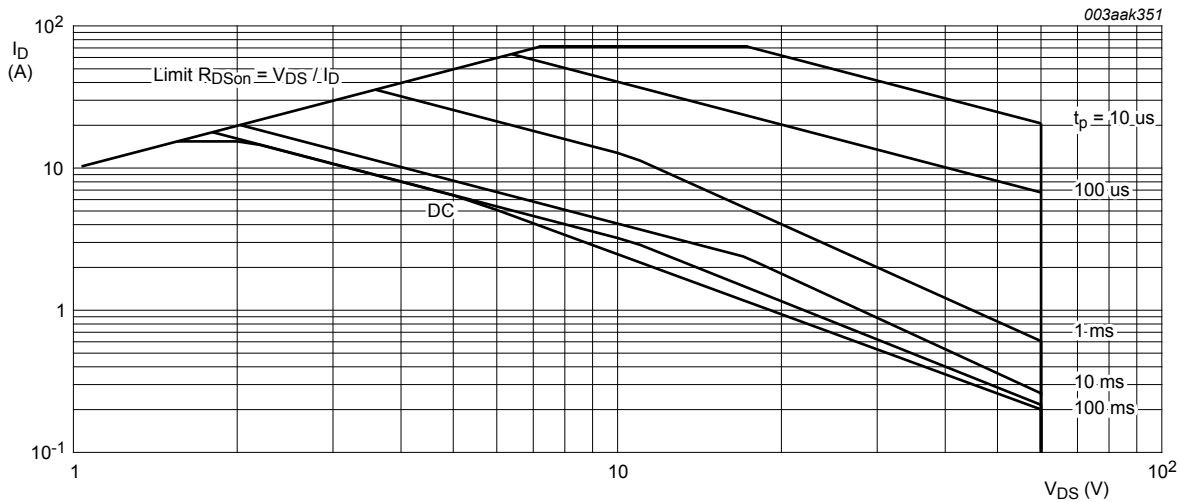


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	4.68	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

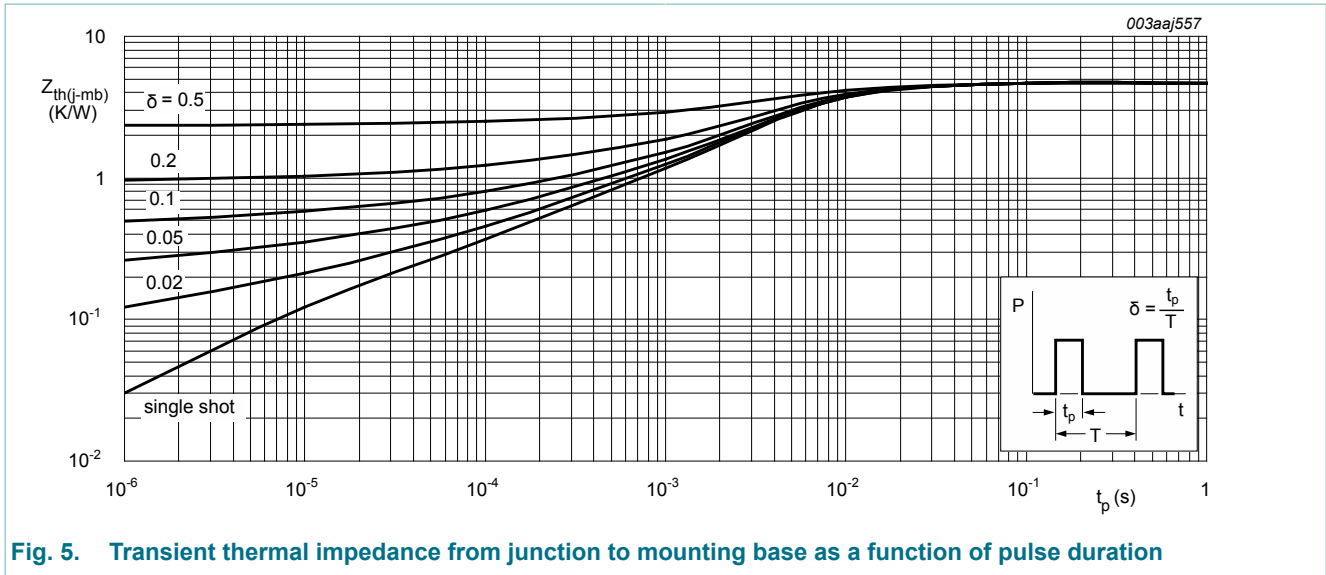


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9; Fig. 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 9; Fig. 10	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 9; Fig. 10	-	-	4.5	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 5 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	35	45	mΩ
		$V_{GS} = 10 V; I_D = 5 A; T_j = 175 \text{ }^\circ C;$ Fig. 12; Fig. 11	-	78	101	mΩ
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 5 A; V_{DS} = 48 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14	-	9.2	-	nC
Q_{GS}	gate-source charge		-	2	-	nC
Q_{GD}	gate-drain charge		-	3.5	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 5\text{ A}$; $V_{DS} = 48\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	5	-	V
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$; Fig. 15	-	401	535	pF
C_{oss}	output capacitance		-	73	87	pF
C_{rss}	reverse transfer capacitance		-	53	72	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 48\text{ V}$; $R_L = 5\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$; $T_j = 25\text{ °C}$; $I_D = 5\text{ A}$	-	4.3	-	ns
t_r	rise time		-	5.1	-	ns
$t_{d(off)}$	turn-off delay time		-	8.4	-	ns
t_f	fall time		-	5.4	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; Fig. 16	-	0.83	1.2	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 30\text{ V}$; $T_j = 25\text{ °C}$	-	17.6	-	ns
Q_r	recovered charge		-	12.3	-	nC

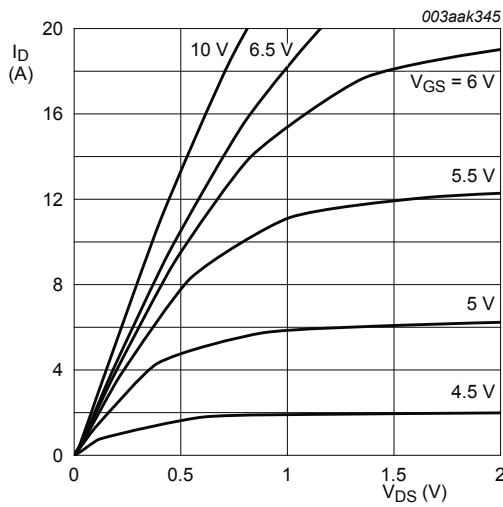


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ °C}$

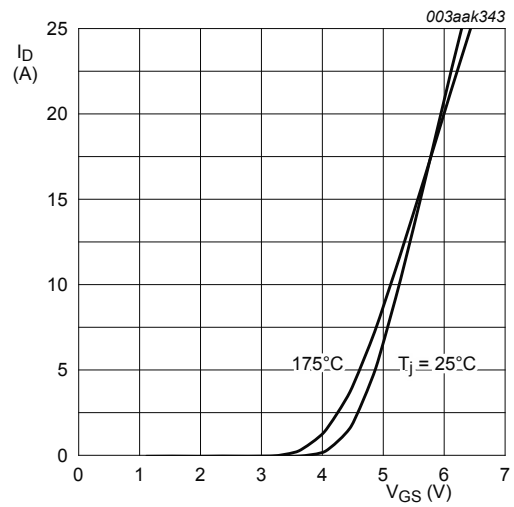


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

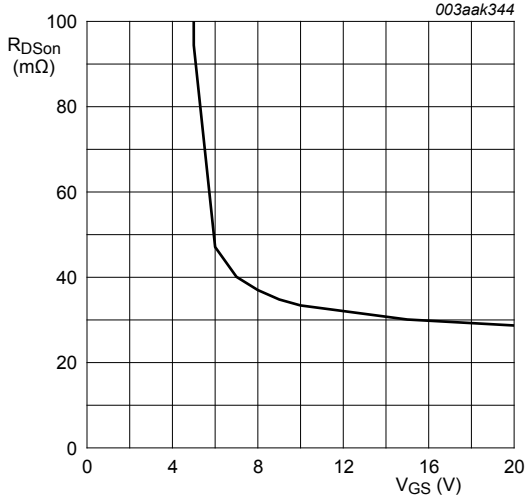


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 5\text{A}$

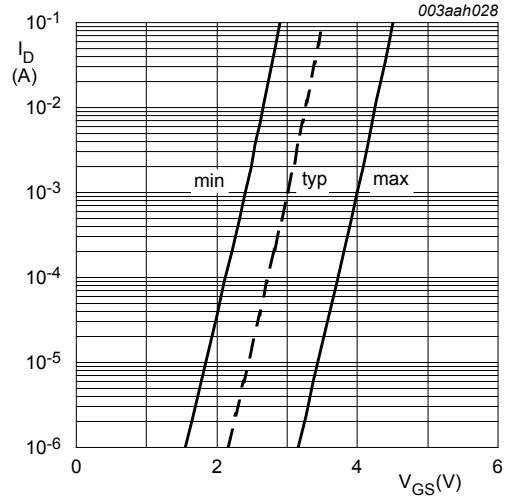


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

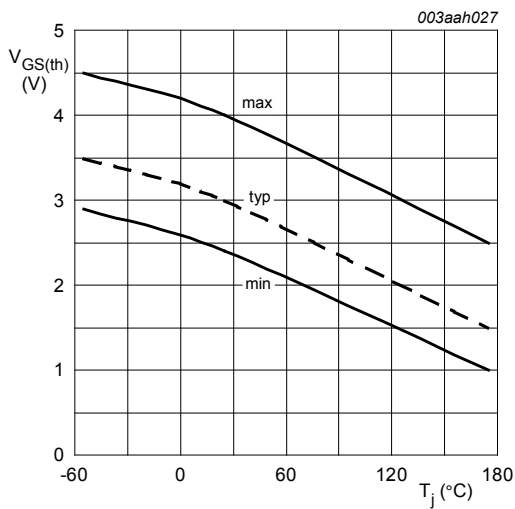


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

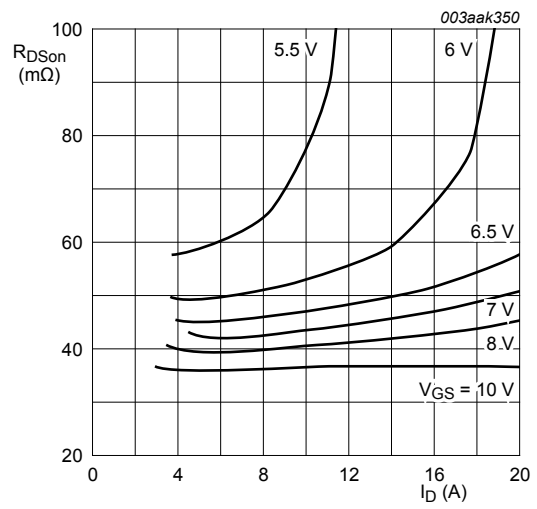


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

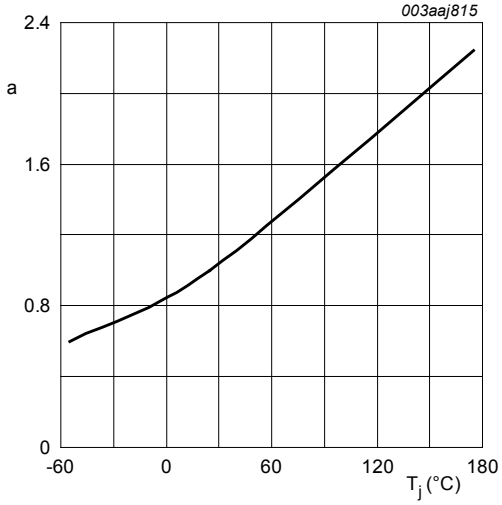


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

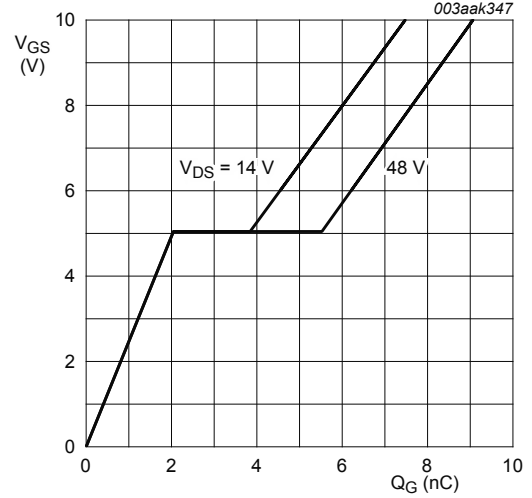


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 5\text{ A}$

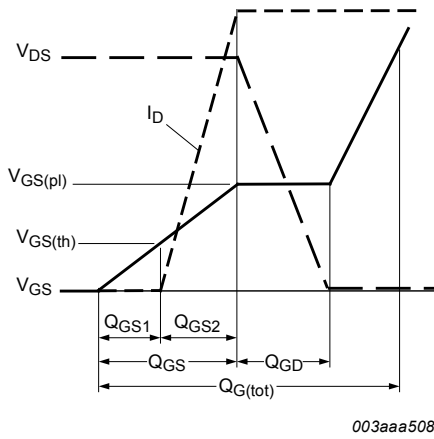


Fig. 14. Gate charge waveform definitions

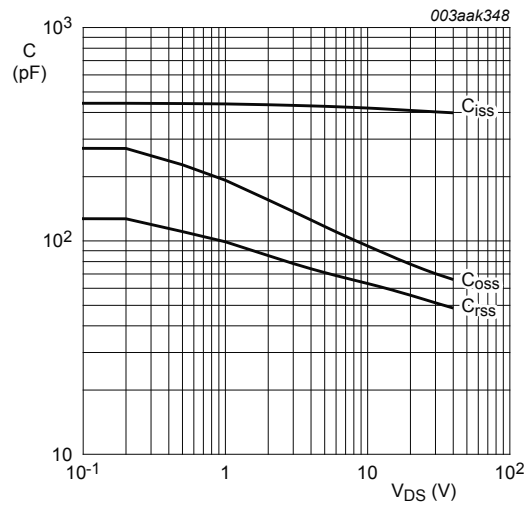
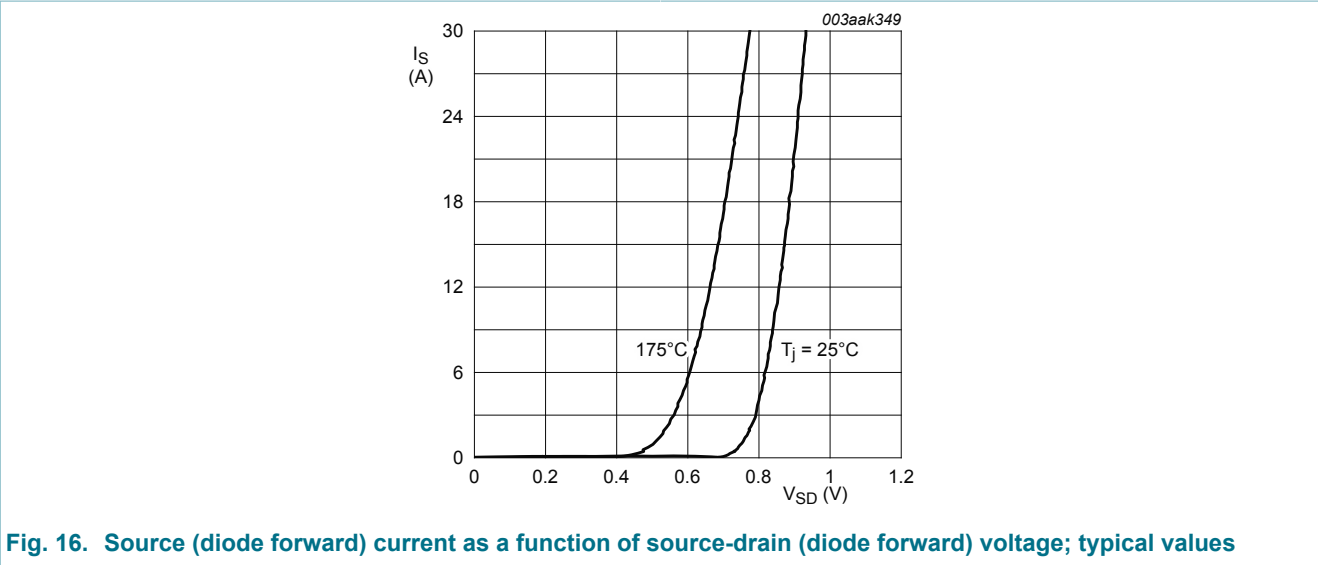


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$



11. Package outline

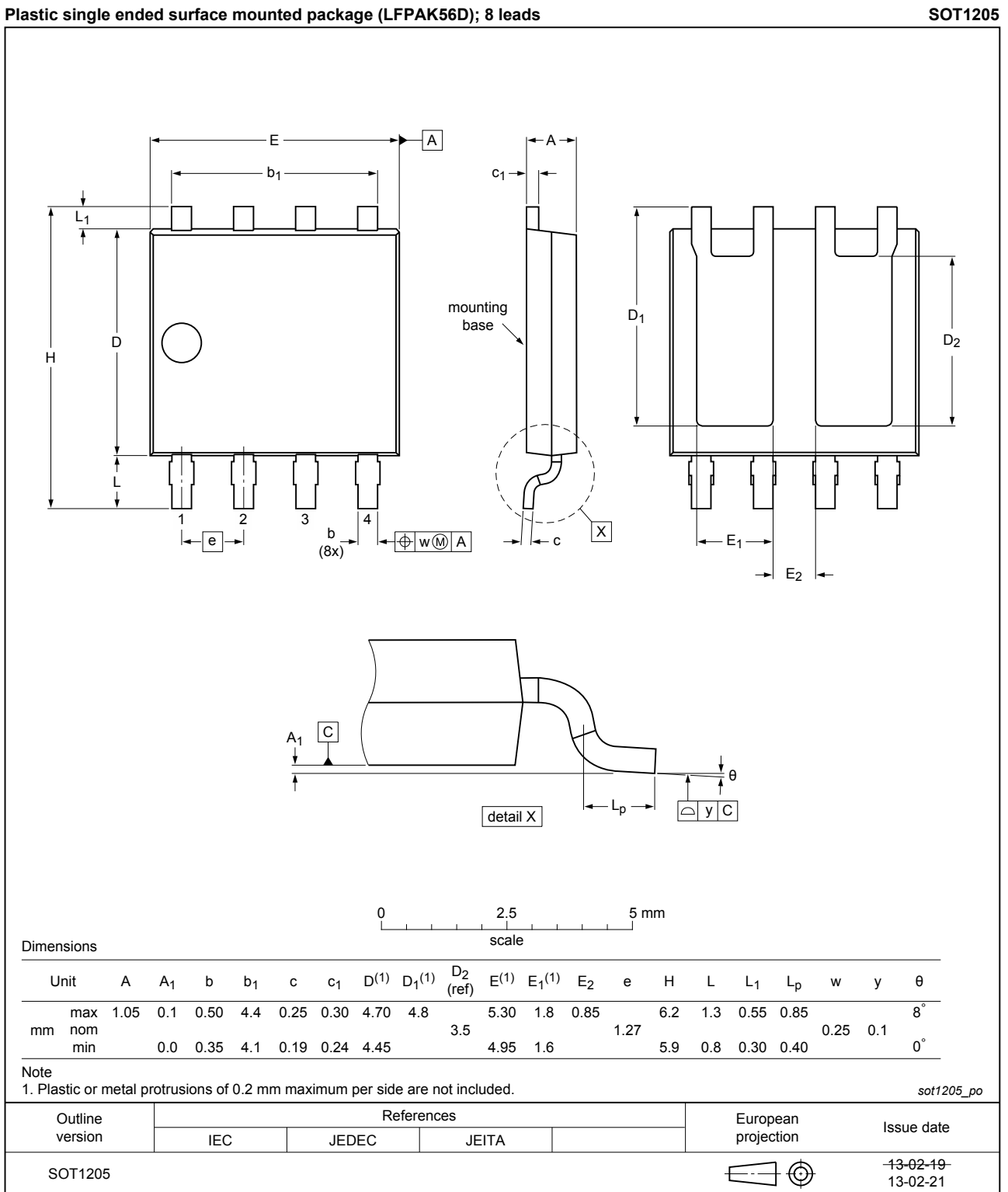


Fig. 17. Package outline LPAK56D (SOT1205)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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