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# BUK7K6R8-40E

Dual N-channel 40 V, 6.8 mΩ standard level MOSFET

6 November 2013

Product data sheet

## 1. General description

Dual standard level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with  $V_{GS(th)}$  of greater than 1 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

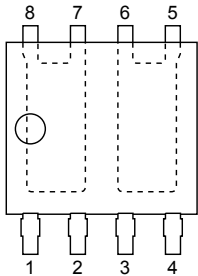
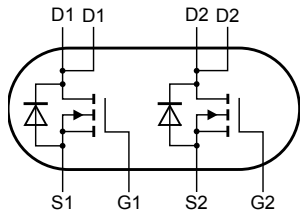
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	40	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	-	64	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C}; \text{Fig. 12}$	-	5.8	6.8	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 20\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 20\text{ V}; T_j = 25\text{ °C}; \text{Fig. 14}; \text{Fig. 15}$	-	9.1	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K6R8-40E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K6R8-40E	76E840

## 8. Limiting values

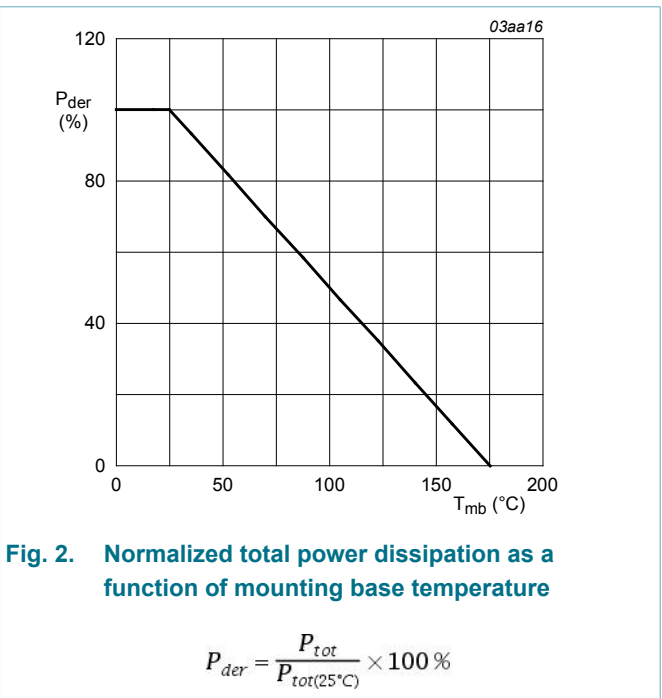
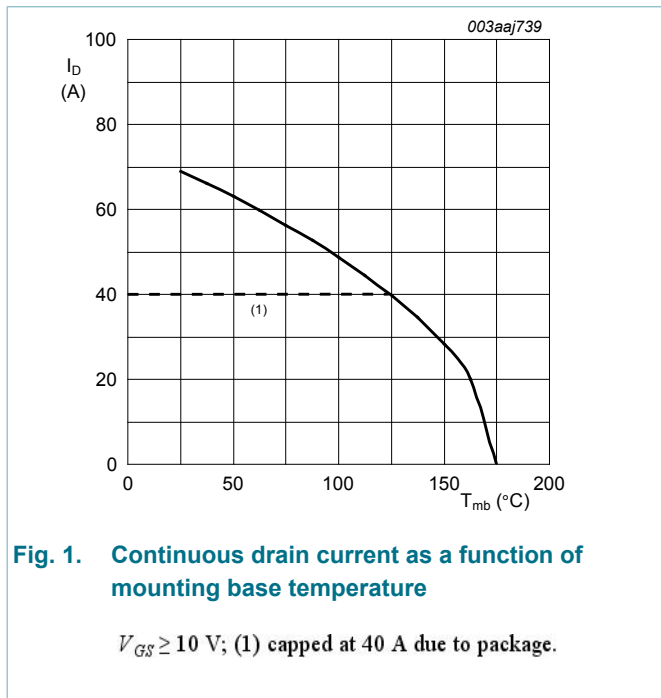
Table 5. Limiting values

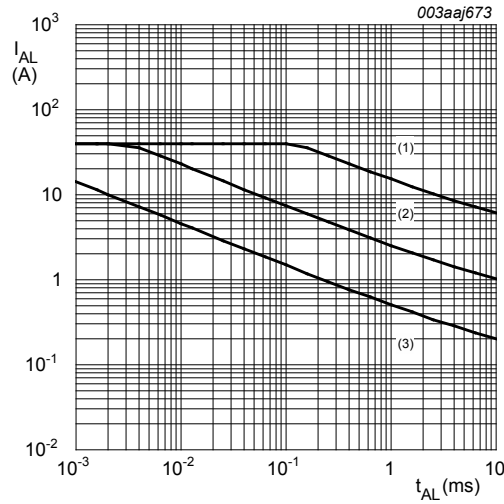
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$ ; $T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	40	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC	-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 1	-	40	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; Fig. 1	-	40	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	276	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 2	-	64	W

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode FET1 and FET2</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	40	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	276	A
<b>Avalanche Ruggedness FET1 and FET2</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 40 A; V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; <a href="#">Fig. 3</a>	[1][2]	-	130 mJ

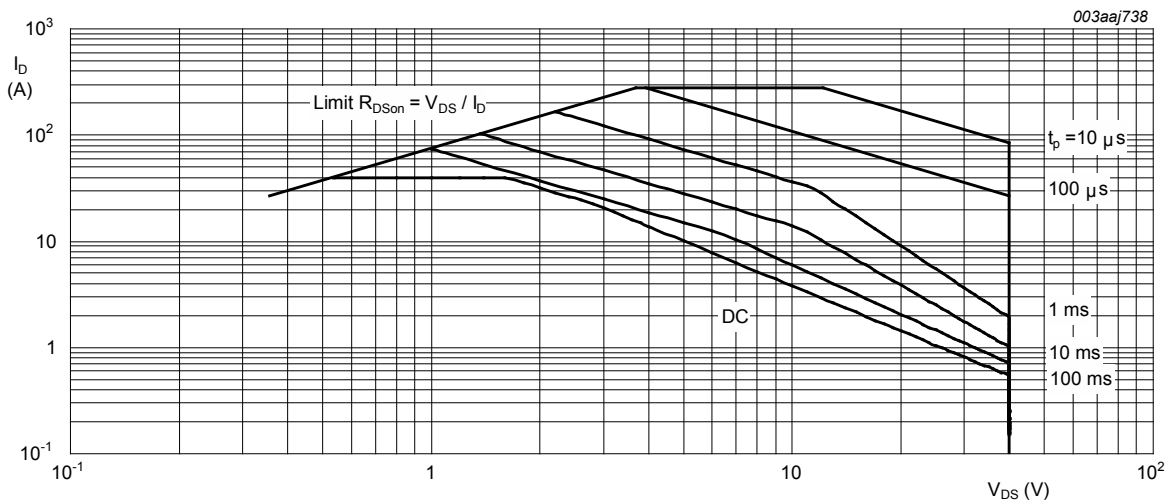
- [1] Refer to application note AN10273 for further information
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C





**Fig. 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2**

- (1) Single-pulse;  $T_j = 25\text{ }^\circ\text{C}$ .
- (2) Single-pulse;  $T_j = 150\text{ }^\circ\text{C}$ .
- (3) Repetitive.



**Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25\text{ }^\circ\text{C}$ ;  $I_{DM}$  is a single pulse; (1) Capped at 40 A due to package

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.36	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

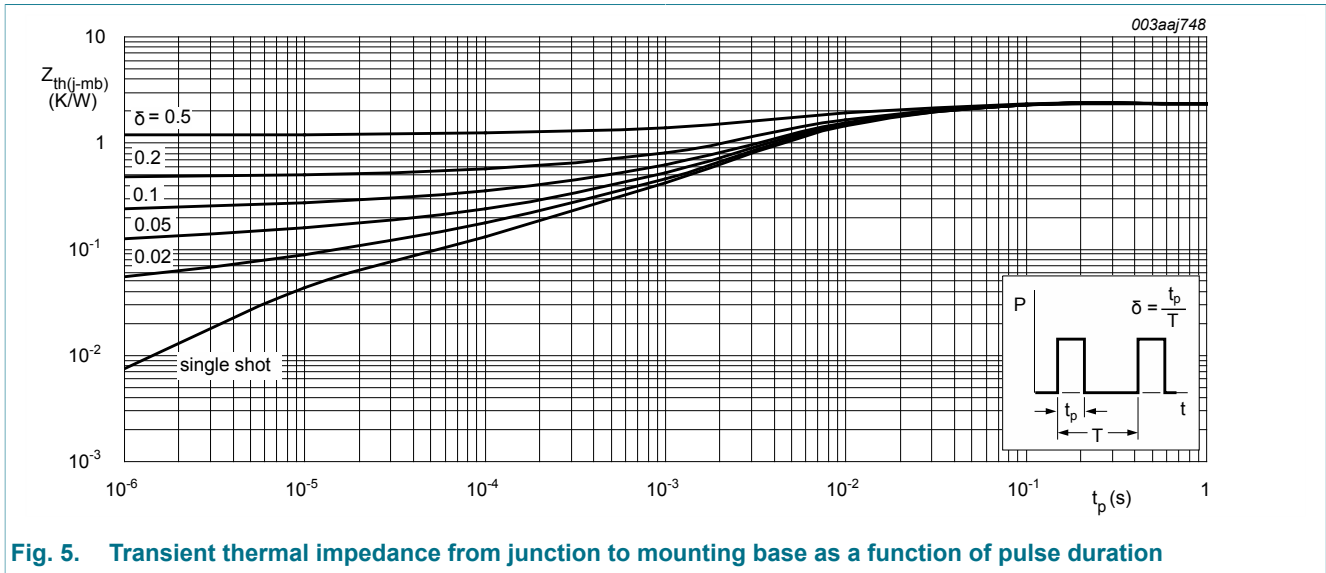


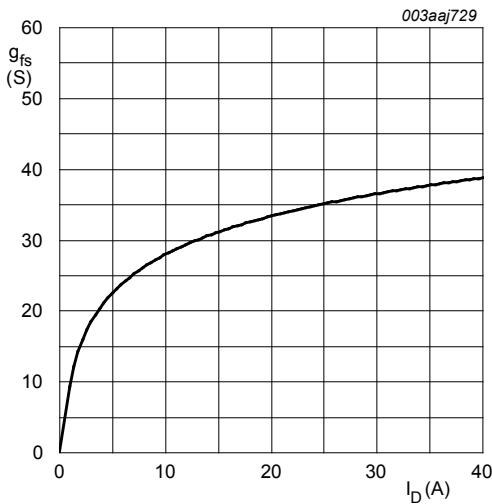
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

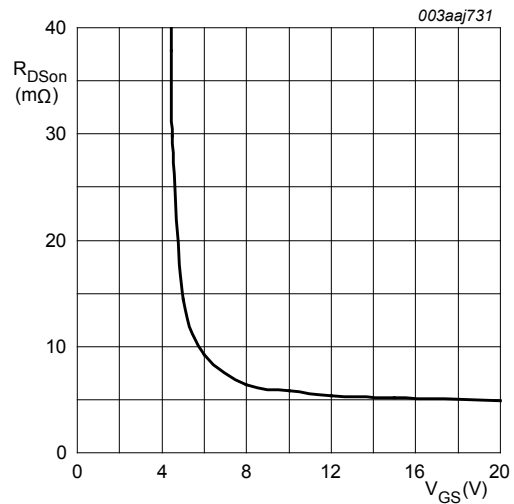
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	4.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 20 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 12</a>	-	5.8	6.8	mΩ
		$V_{GS} = 10 V; I_D = 20 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 13</a>	-	11	13.4	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 20 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	28.9	-	nC
$Q_{GS}$	gate-source charge		-	7	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 20 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 20 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	9.1	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	1460	1947	pF
$C_{oss}$	output capacitance		-	324	389	pF
$C_{rss}$	reverse transfer capacitance		-	197	270	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 32 \text{ V}; R_L = 1.6 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(\text{ext})} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}; I_D = 20 \text{ A}$	-	8.9	-	ns
$t_r$	rise time		-	15.4	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	19.4	-	ns
$t_f$	fall time		-	16.5	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 17</a>	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$ $V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	20.6	-	ns
$Q_r$	recovered charge		-	11.3	-	nC



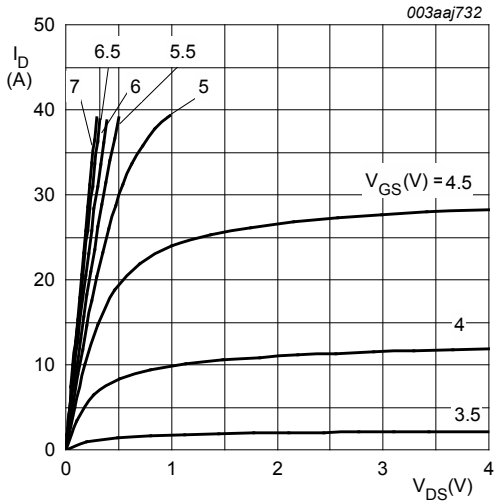
**Fig. 6. Forward transconductance as a function of drain current; typical values**

$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 15 \text{ V}$



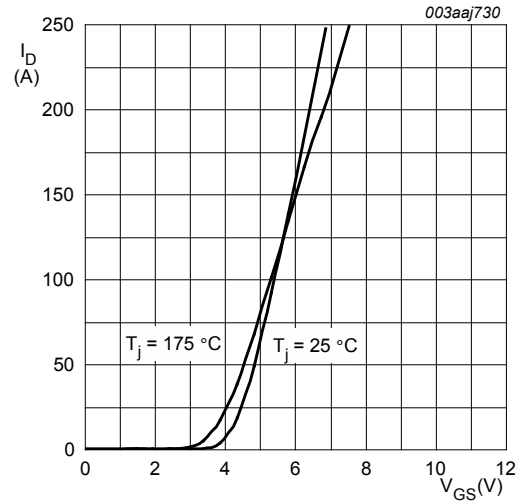
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25 \text{ }^\circ\text{C}; I_D = 20 \text{ A}$



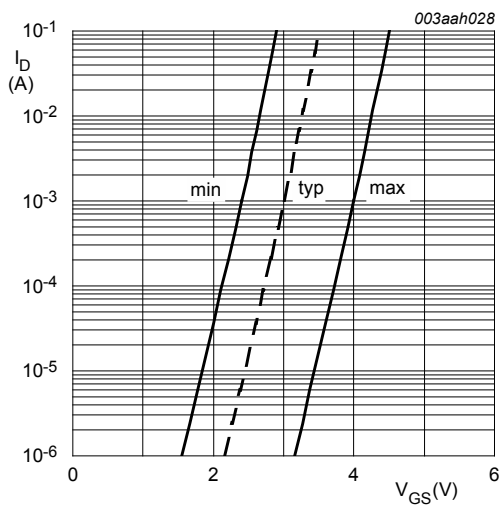
**Fig. 8. Output characteristics: drain current as a function of drain-source voltage; typical values**

$T_j = 25^\circ\text{C}$



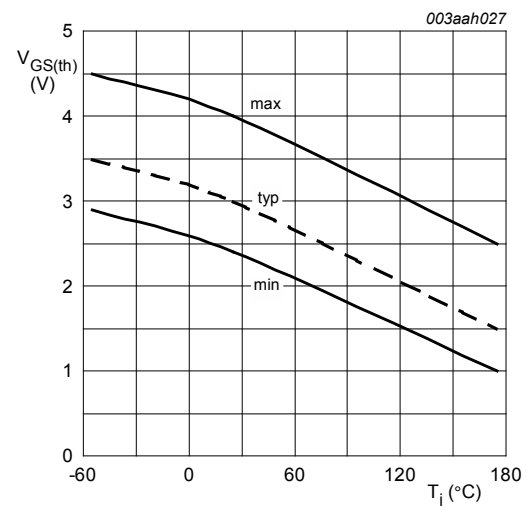
**Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10\text{ V}$



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$



**Fig. 11. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$



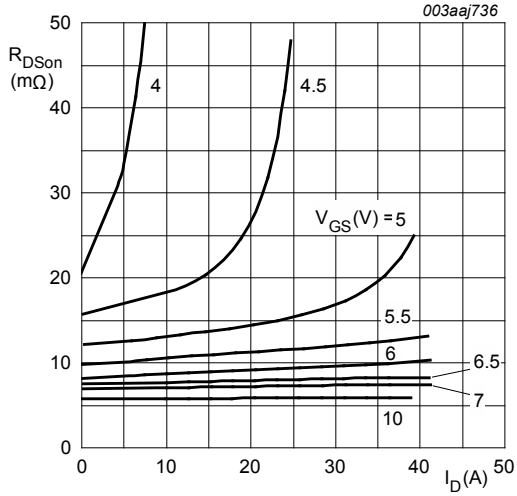


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}$

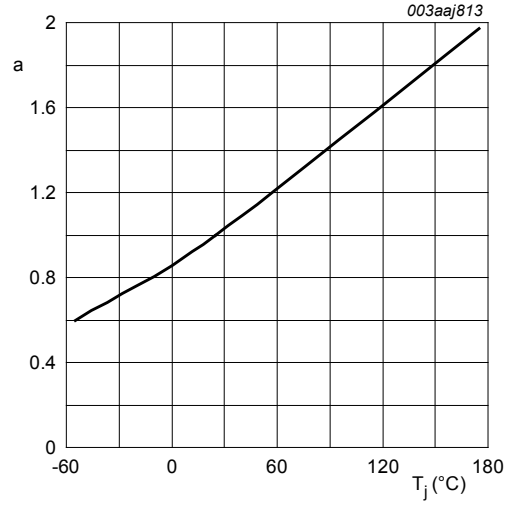


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

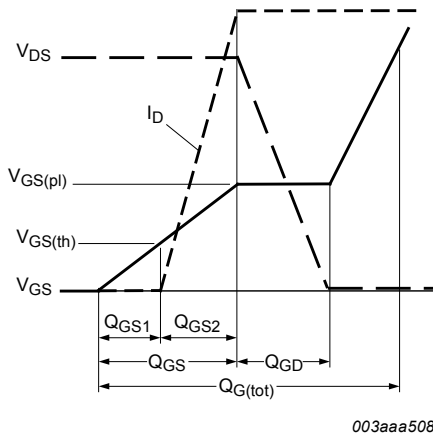


Fig. 14. Gate charge waveform definitions

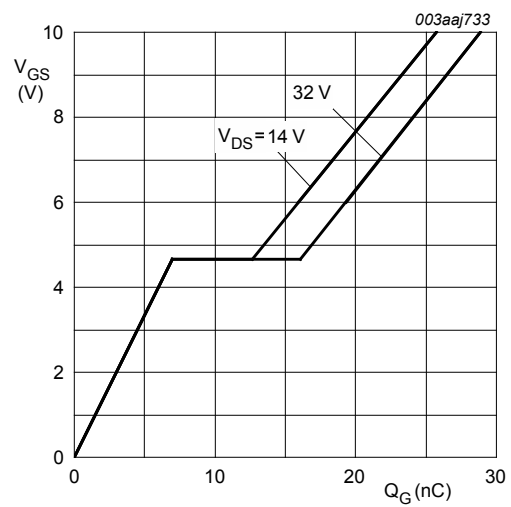
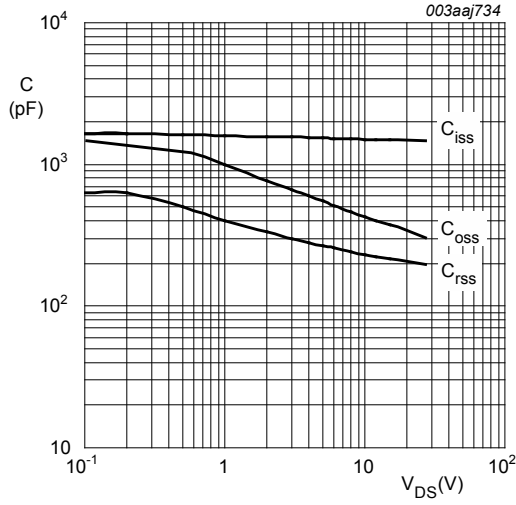


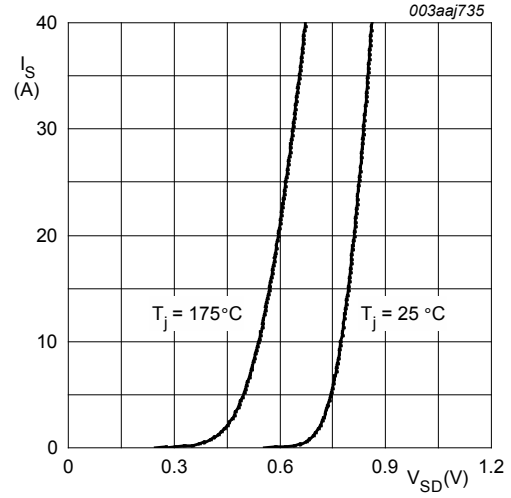
Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 20\text{A}$



**Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

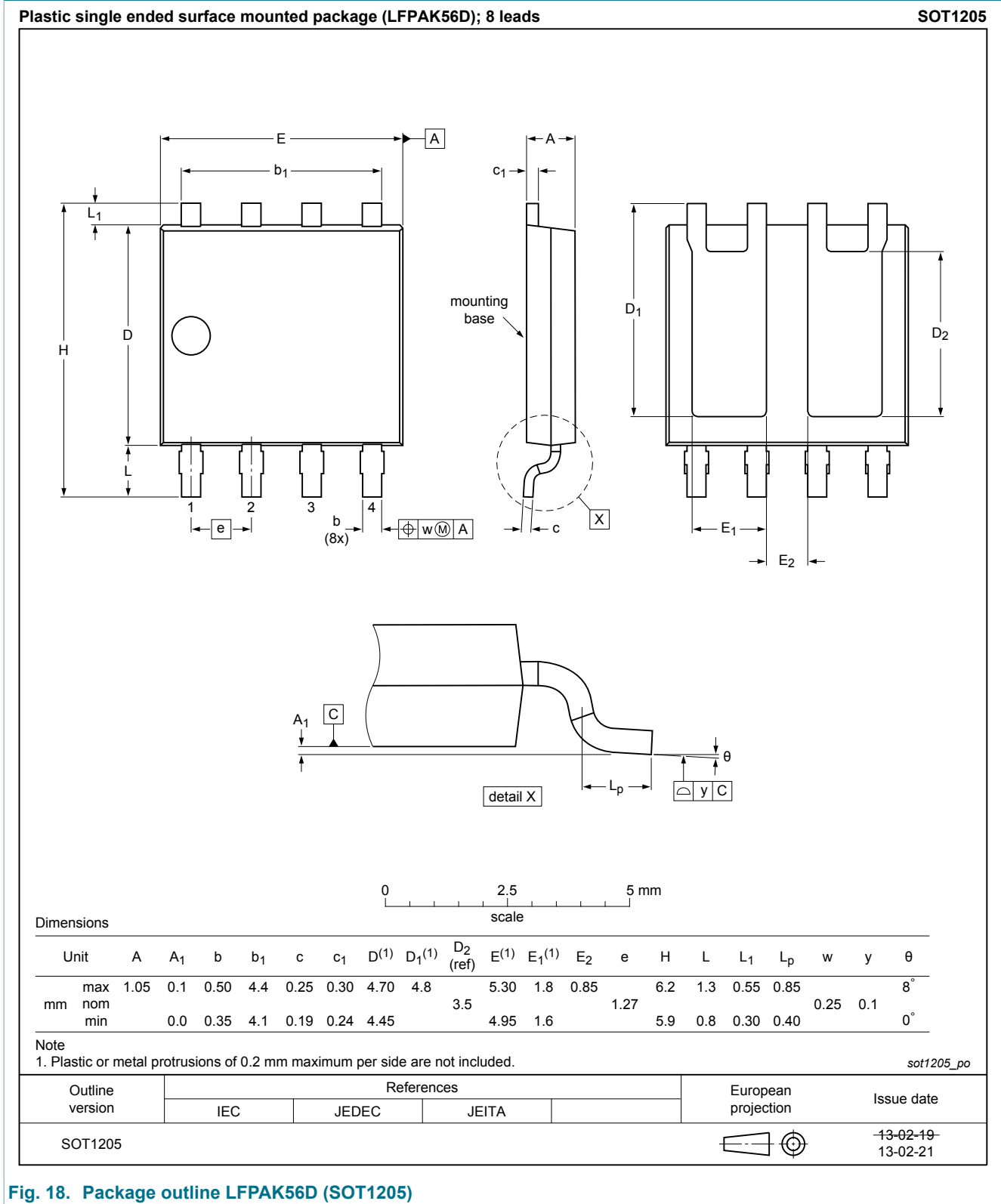
$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$



**Fig. 17. Source current as a function of source-drain voltage; typical values**

$$V_{GS} = 0\text{ V}$$

### 11. Package outline



**Fig. 18. Package outline LPAK56D (SOT1205)**

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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## 13. Contents

1	General description .....	1
2	Features and benefits .....	1
3	Applications .....	1
4	Quick reference data .....	1
5	Pinning information .....	2
6	Ordering information .....	2
7	Marking .....	2
8	Limiting values .....	2
9	Thermal characteristics .....	4
10	Characteristics .....	5
11	Package outline .....	10
12	Legal information .....	11
12.1	Data sheet status .....	11
12.2	Definitions .....	11
12.3	Disclaimers .....	11
12.4	Trademarks .....	12

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Date of release: 06 November 2013