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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



TrenchMOS™ transistor Logic level FET

BUK9520-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using 'trench' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

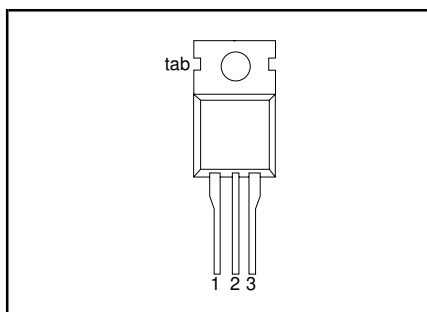
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	52	A
P_{tot}	Total power dissipation	116	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 5\text{ V}$	20	mΩ

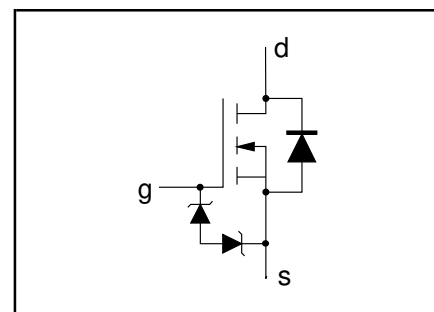
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	52	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	37	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	208	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	116	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	1.29	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	in free air	60	-	K/W

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STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55°C	55 50	- -	- -	V V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA T _j = 175°C T _j = -55°C	1 0.5 -	1.5 - -	2 - 2.3	V V V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175°C	-	0.05	10	μA
I _{GSS}	Gate source leakage current	V _{GS} = ±5 V; V _{DS} = 0 V T _j = 175°C	-	0.02	500	μA
±V _{(BR)GSS}	Gate-source breakdown voltage	I _G = ±1 mA; T _j = 175°C	10	-	10	μA V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A T _j = 175°C	- -	15 -	20 42	mΩ mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g _{fs}	Forward transconductance	V _{DS} = 25 V; I _D = 25 A	20	-	-	S
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	1800	2400	pF
C _{oss}	Output capacitance		-	350	420	pF
C _{riss}	Feedback capacitance		-	170	235	pF
t _{d on}	Turn-on delay time	V _{DD} = 30 V; I _D = 25 A; V _{GS} = 5 V; R _G = 10 Ω Resistive load	-	28	40	ns
t _r	Turn-on rise time		-	110	160	ns
t _{d off}	Turn-off delay time		-	95	135	ns
t _f	Turn-off fall time		-	70	90	ns
L _d	Internal drain inductance	Measured from contact screw on tab to centre of die	-	3.5	-	nH
L _d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	-	4.5	-	nH
L _s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

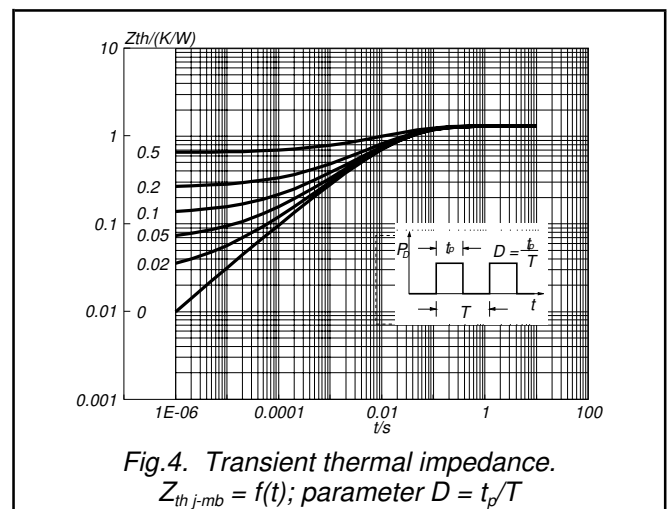
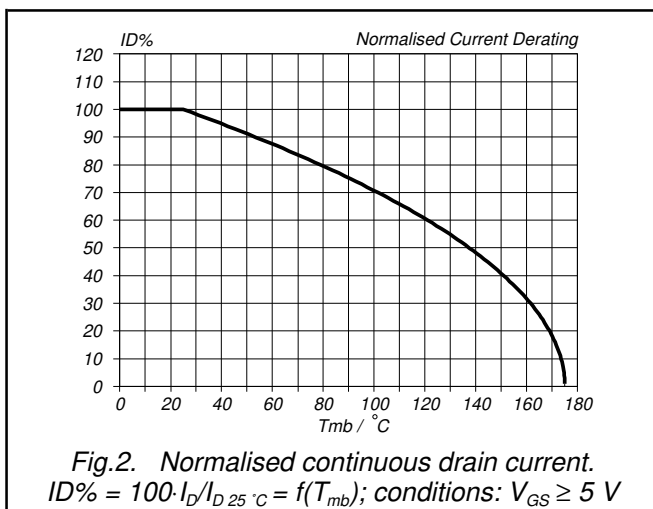
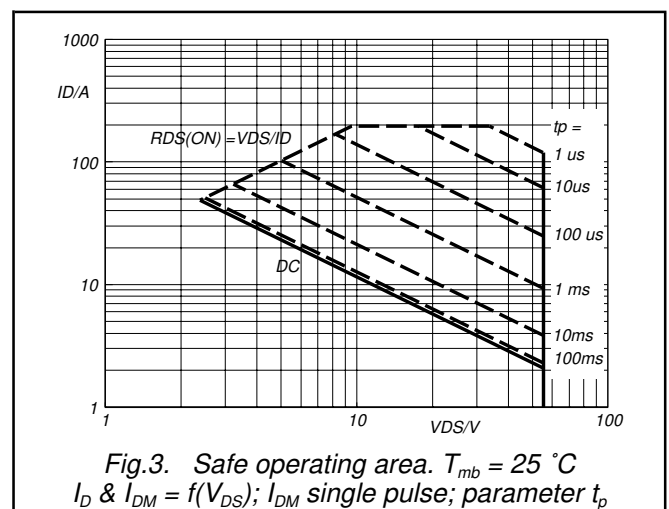
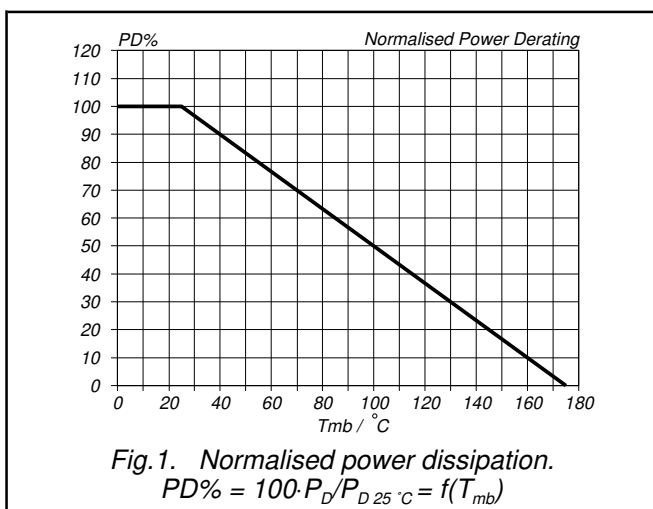
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{DR}	Continuous reverse drain current		-	-	52	A
I _{DRM}	Pulsed reverse drain current		-	-	208	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V I _F = 40 A; V _{GS} = 0 V	- -	0.95 1.0	1.2 -	V
t _{rr}	Reverse recovery time	I _F = 40 A; -di _F /dt = 100 A/μs;	-	47	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = -10 V; V _R = 30 V	-	0.15	-	μC

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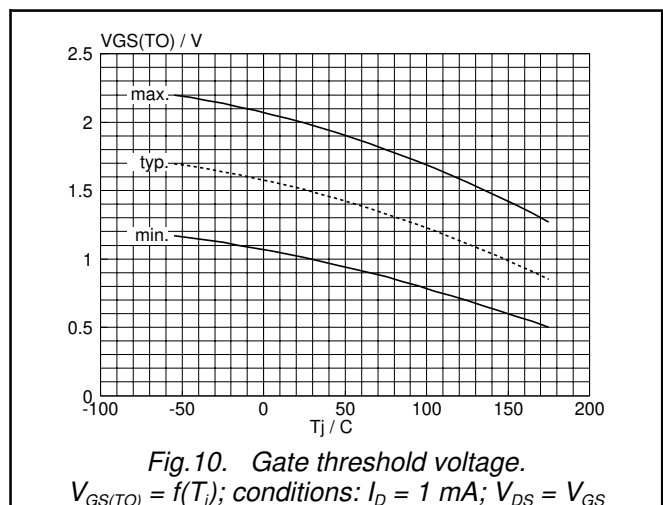
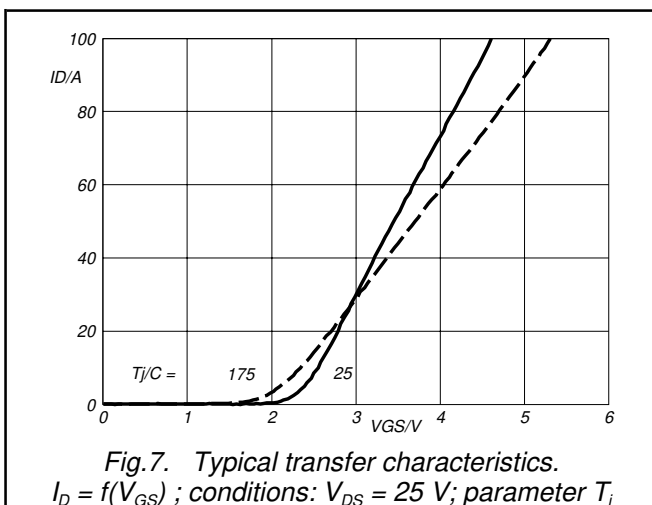
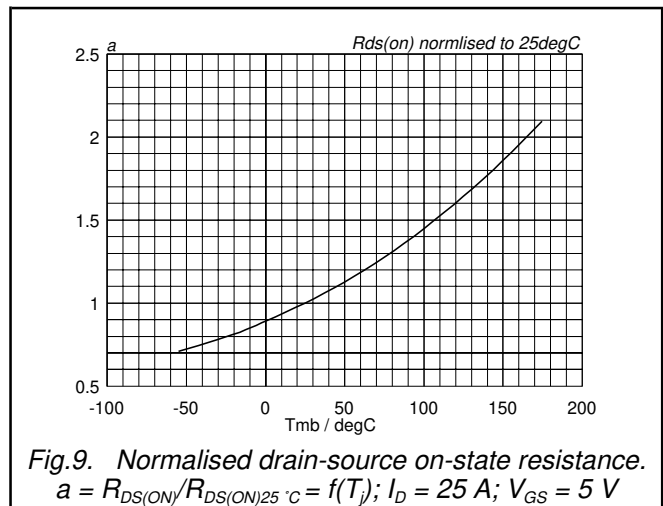
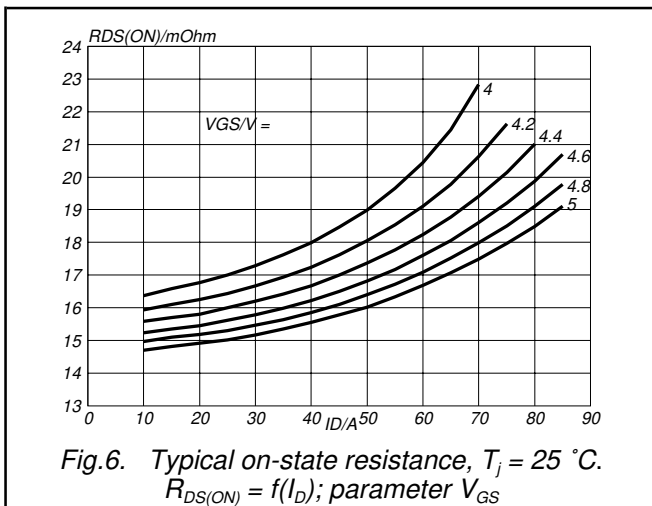
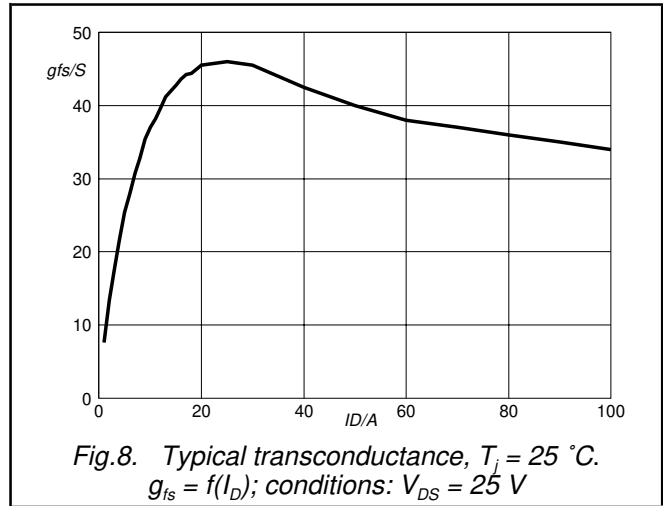
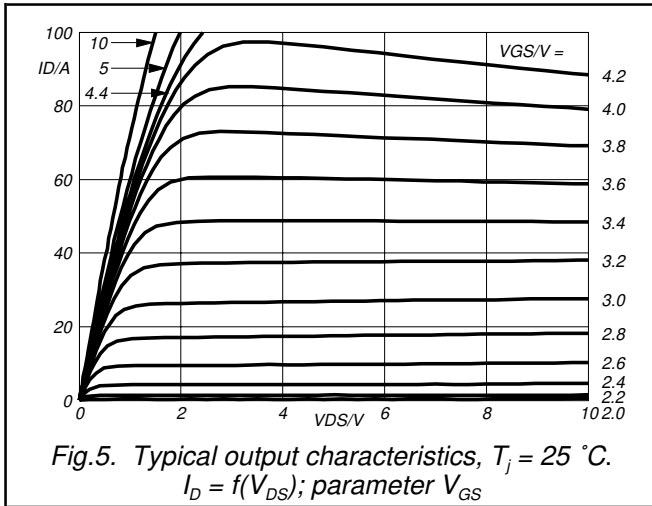
AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 45 \text{ A}; V_{DD} \leq 25 \text{ V}; V_{GS} = 5 \text{ V}; R_{GS} = 50 \text{ } \Omega; T_{mb} = 25 \text{ } ^\circ\text{C}$	-	-	110	mJ



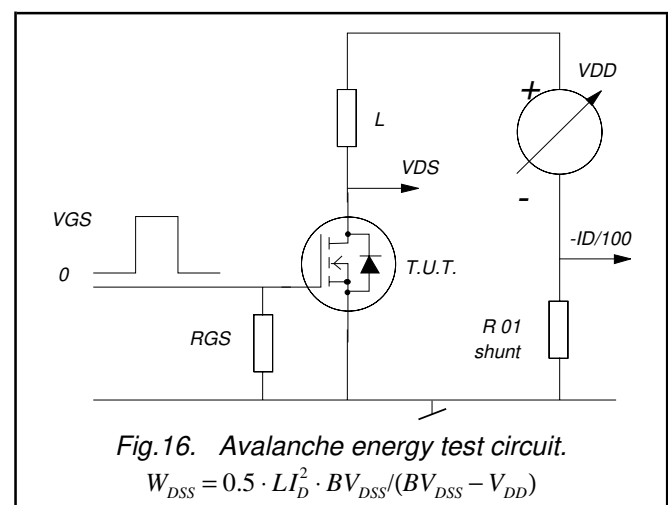
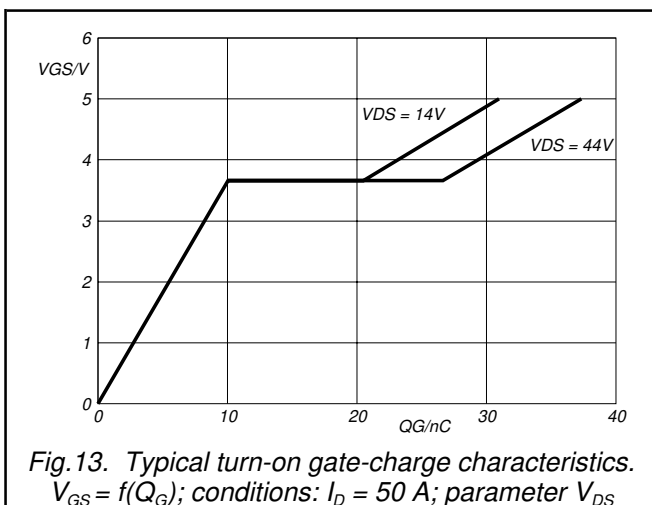
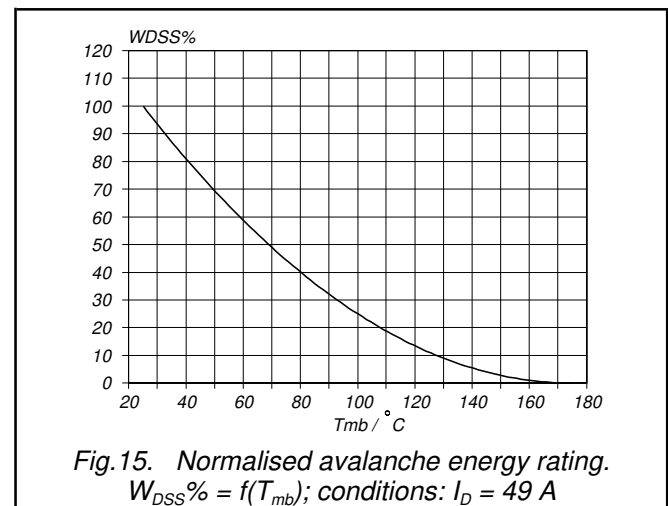
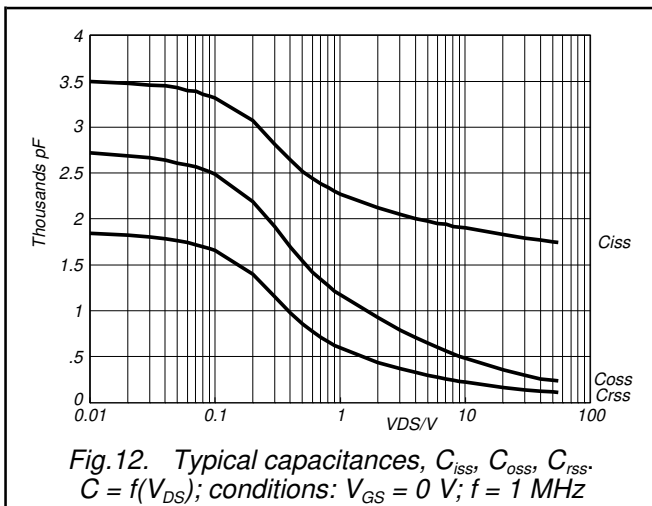
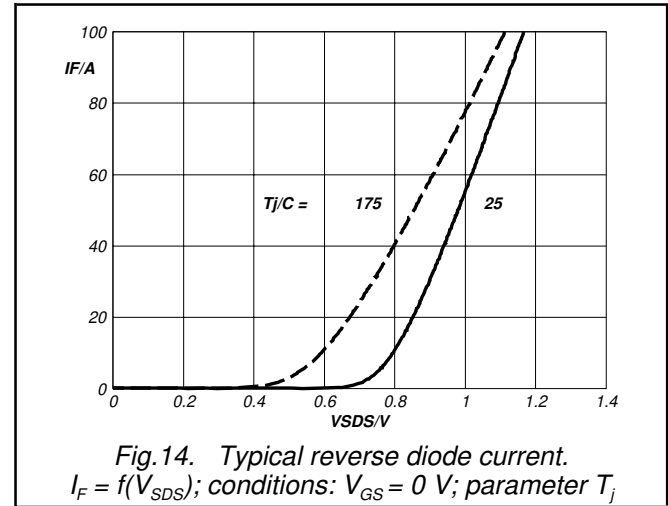
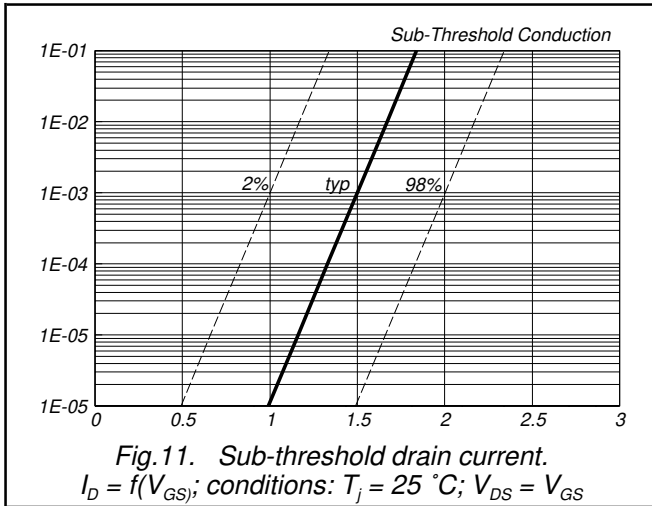
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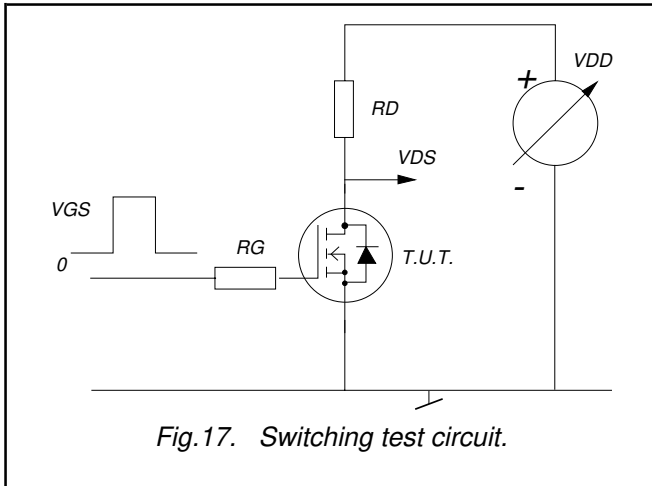
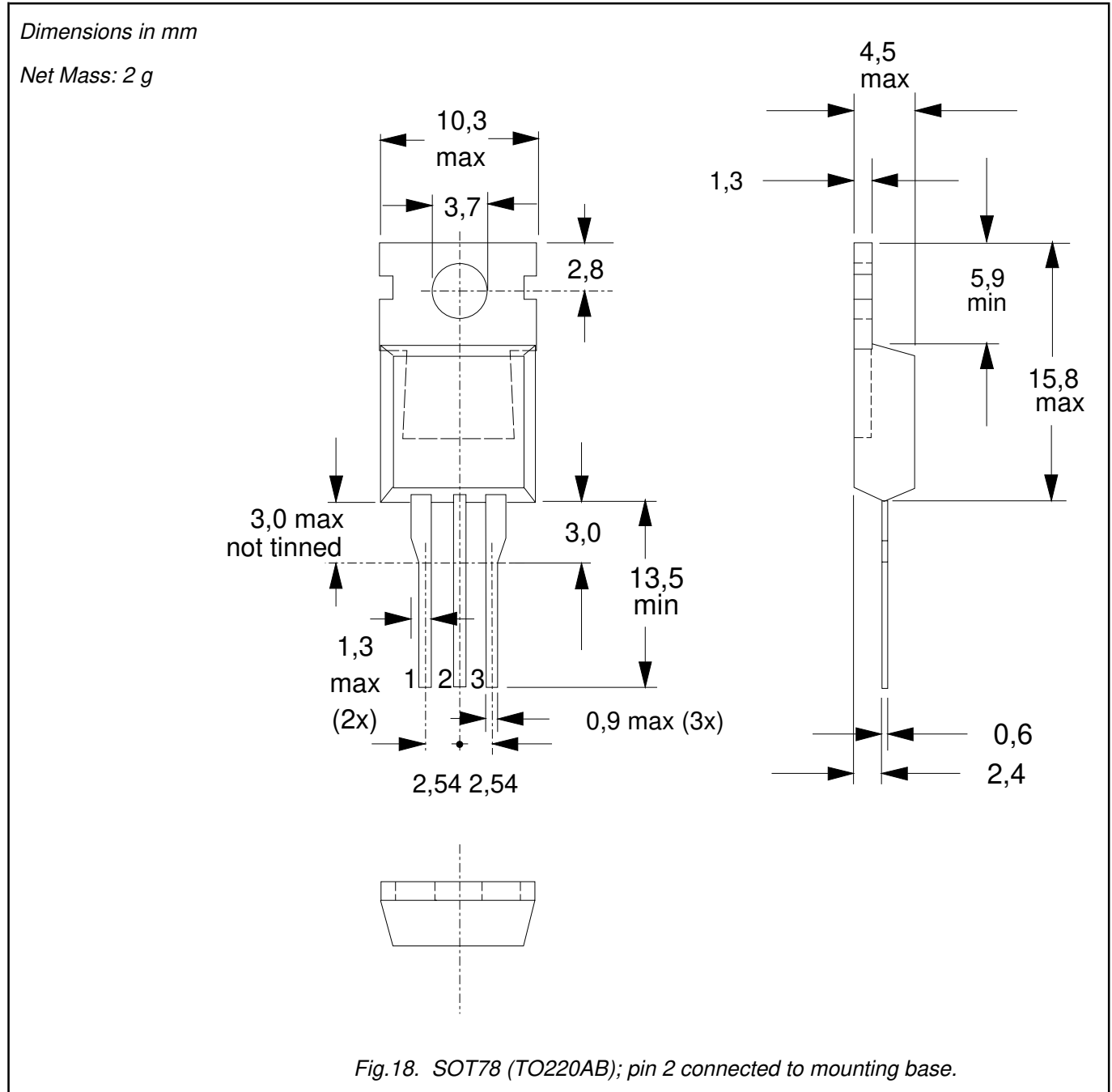


Fig.17. Switching test circuit.

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MECHANICAL DATA



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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