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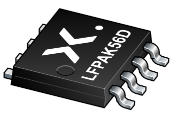


BUK9K30-80E

Dual N-channel 80 V, 30 mΩ logic level MOSFET

12 May 2018 Product data sheet

1. General description

Dual Logic level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

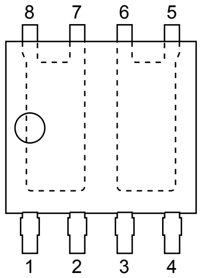
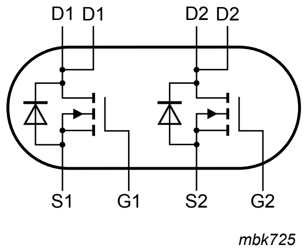
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Limiting values FET1 and FET2							
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	80	V
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	-	17	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	53	W
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 11		-	21	30	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	I_D = 5 A; V_{DS} = 64 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 13; Fig. 14		-	6.2	-	nC
Source-drain diode FET1 and FET2							
Q_r	recovered charge	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C		-	30.8	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D (SOT1205)	
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K30-80E	LFPAK56D	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K30-80E	93080E

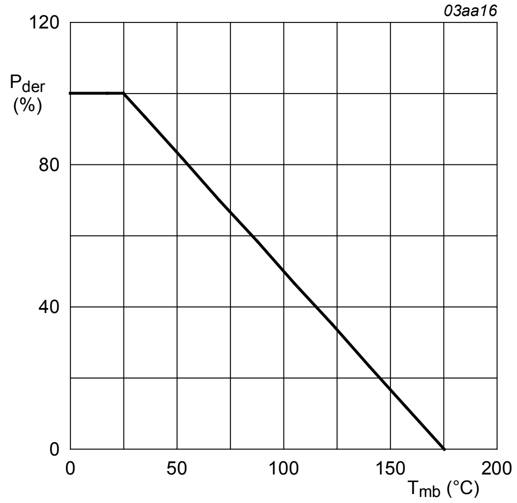
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

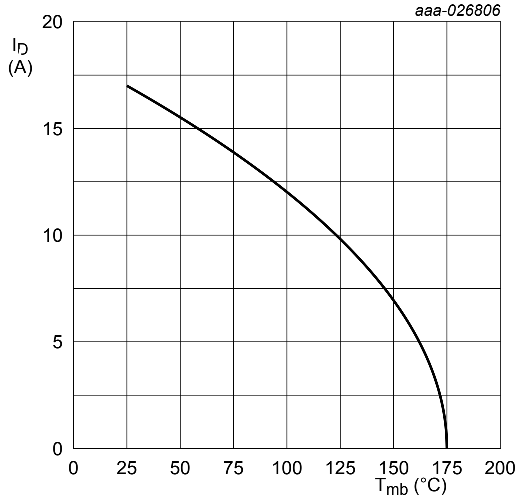
Symbol	Parameter	Conditions		Min	Max	Unit
Limiting values FET1 and FET2						
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	80	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	80	V
V_{GS}	gate-source voltage	DC; T_j ≤ 175 °C		-10	10	V
		Pulsed; T_j ≤ 175 °C	[1] [2]	-15	15	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	53	W
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; Fig. 2		-	17	A
		V_{GS} = 5 V; T_{mb} = 100 °C; Fig. 2		-	12	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	68	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I_S	source current	T_{mb} = 25 °C		-	17	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	68	A
Avalanche ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 17 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[3] [4]	-	72	mJ

[1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm.
[2] Significantly longer life times are achieved by lowering T_j and or V_{GS}.
[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[4] Refer to application note AN10273 for further information.



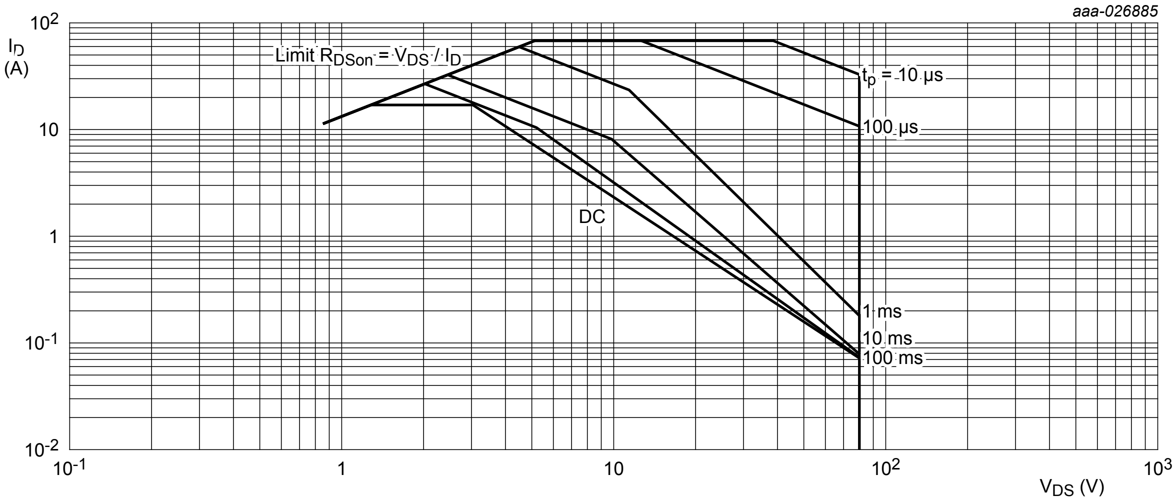
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



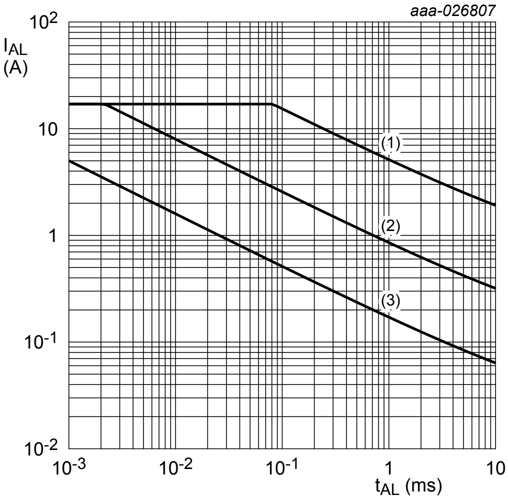
$V_{GS} \geq 5$ V

Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2



(1) $T_{j\ (init)}$ = 25°C; (2) $T_{j\ (init)}$ = 150°C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board		-	95	-	K/W

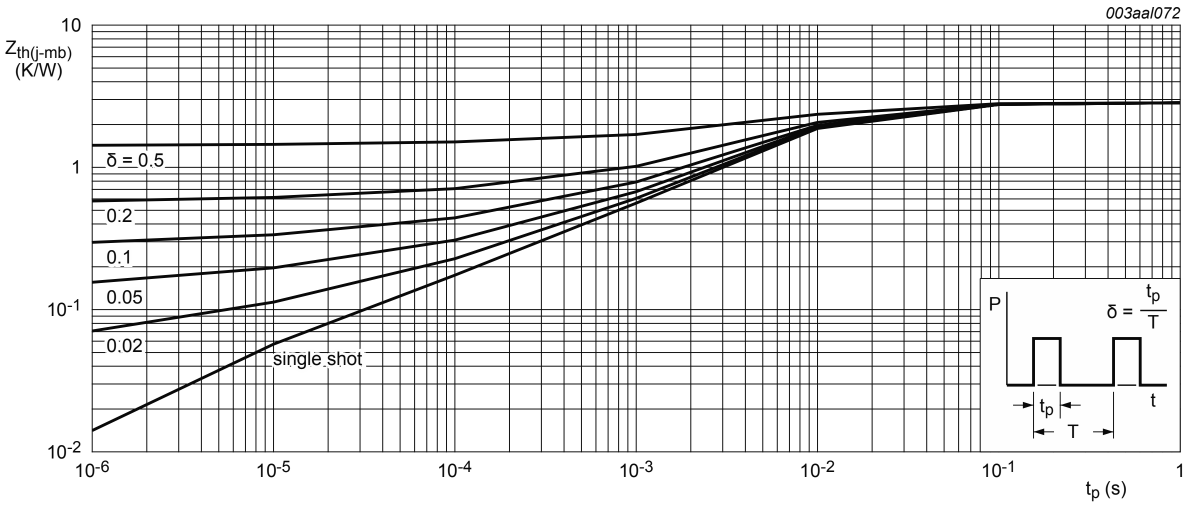
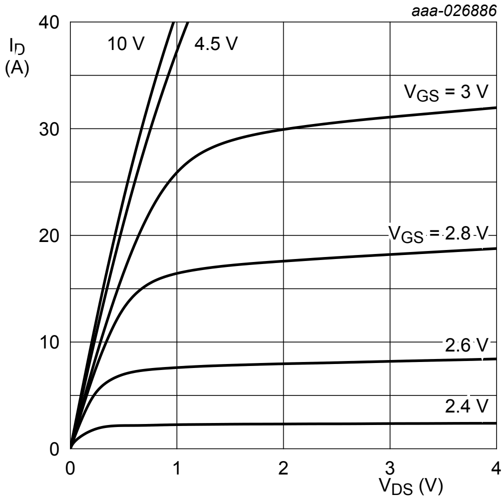


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

10. Characteristics

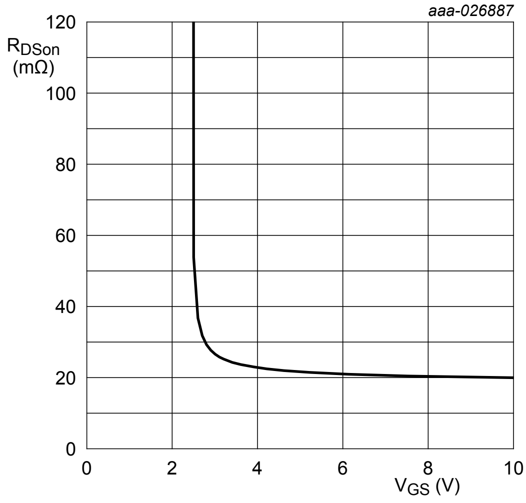
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics FET1 and FET2							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		80	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 9; Fig. 10		1.4	1.7	2.1	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.45	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 10		0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	1	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 5 A; T_j = 25 °C; Fig. 11		-	21	30	mΩ
		V_{GS} = 10 V; I_D = 5 A; T_j = 25 °C; Fig. 11		-	20	26	mΩ
		V_{GS} = 5 V; I_D = 5 A; T_j = 175 °C; Fig. 12		-	-	75	mΩ
Dynamic characteristics FET1 and FET2							
$Q_{G(tot)}$	total gate charge	I_D = 5 A; V_{DS} = 64 V; V_{GS} = 5 V; T_j = 25 °C; Fig. 13; Fig. 14		-	17.5	-	nC
Q_{GS}	gate-source charge			-	3.9	-	nC
Q_{GD}	gate-drain charge			-	6.2	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		-	1727	2297	pF
C_{oss}	output capacitance			-	126	151	pF
C_{rss}	reverse transfer capacitance			-	68	93	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 60 V; R_L = 12 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	10.4	-	ns
t_r	rise time			-	14.8	-	ns
$t_{d(off)}$	turn-off delay time			-	24.7	-	ns
t_f	fall time			-	15	-	ns
Source-drain diode FET1 and FET2							
V_{SD}	source-drain voltage	I_S = 5 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.78	1.2	V
t_{rr}	reverse recovery time	I_S = 5 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 25 V; T_j = 25 °C		-	27.2	-	ns
Q_r	recovered charge			-	30.8	-	nC



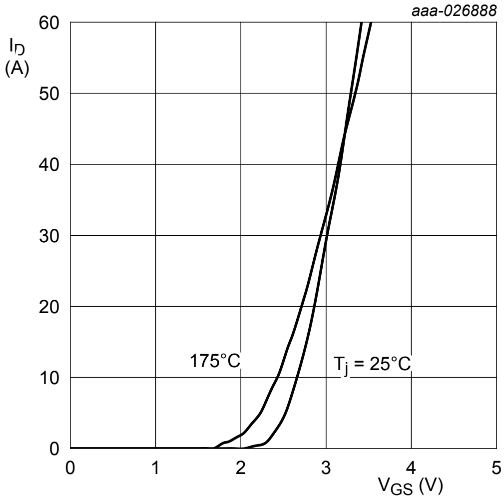
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2



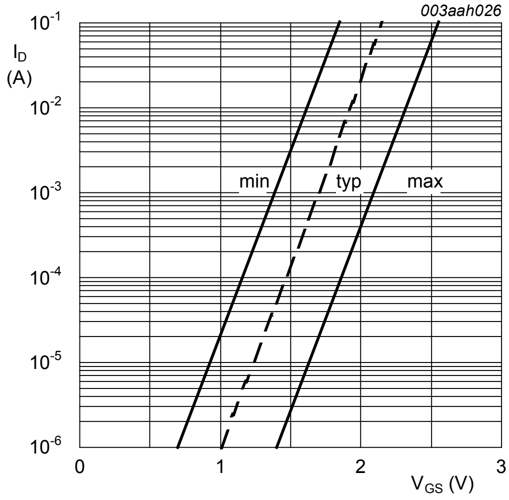
T_j = 25 °C; I_D = 5 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2



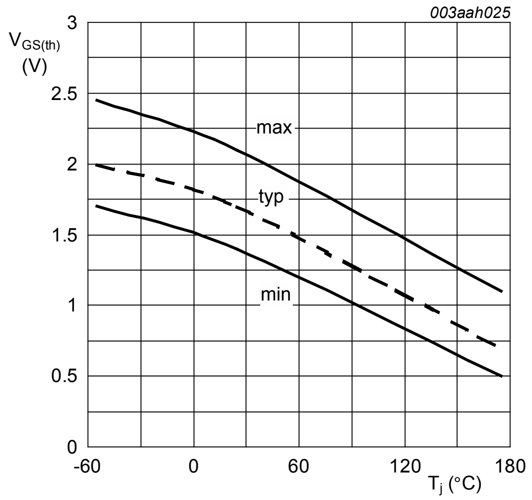
V_{DS} = 12 V

Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2



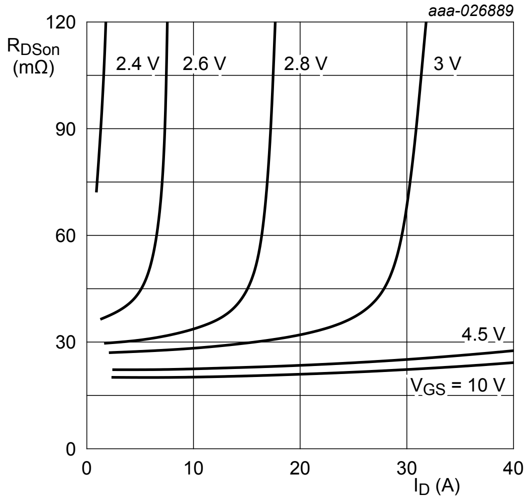
T_j = 25 °C; V_{DS} = 5 V

Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2



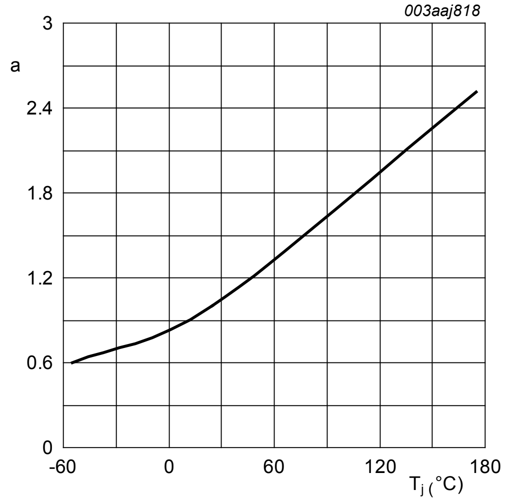
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2



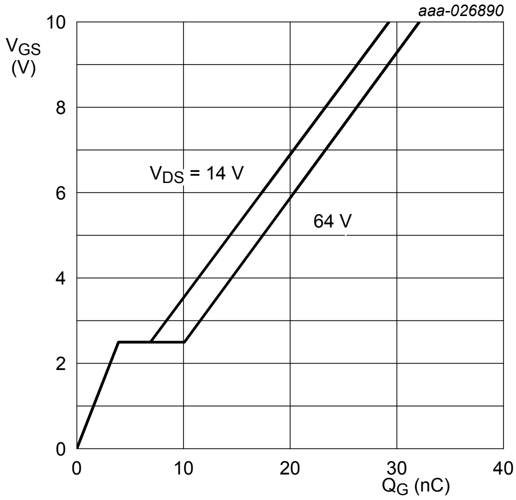
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



$$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2



T_j = 25 °C; I_D = 5 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

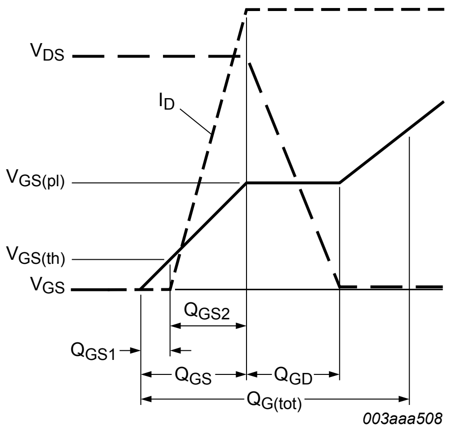
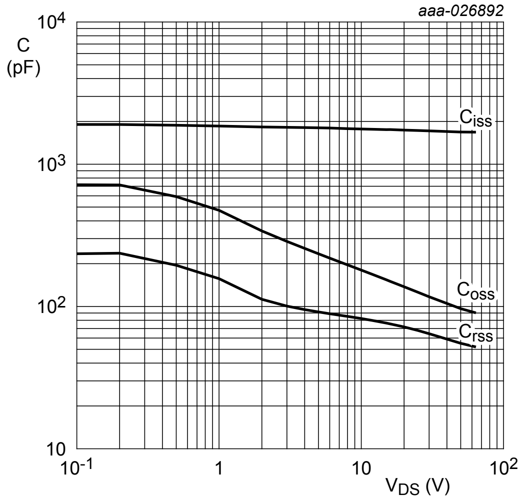
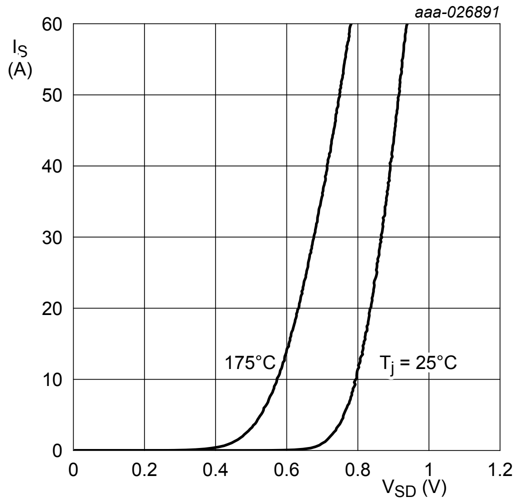


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

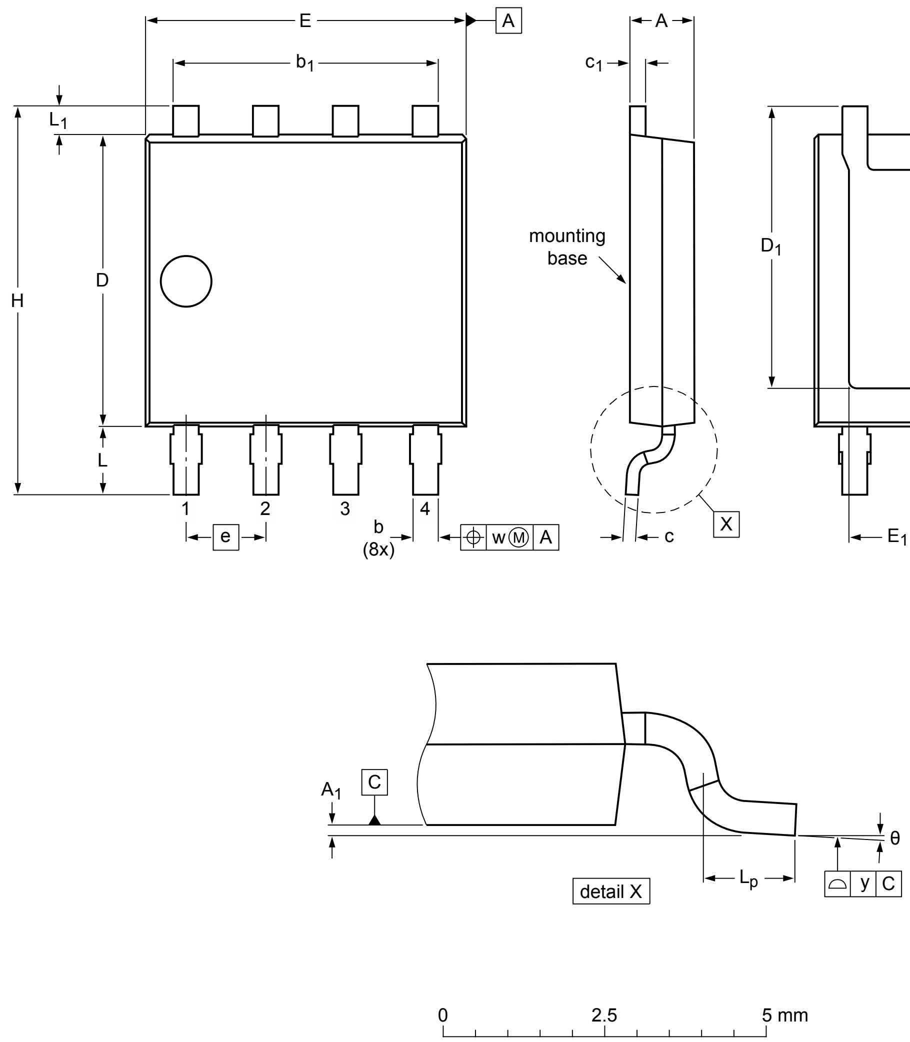


V_{GS} = 0 V

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

11. Package outline

Plastic single ended surface mounted package LFPAK56D; 8 leads **SOT1205**



Dimensions

Unit		A	A_1	b	b_1	c	c_1	$D^{(1)}$	$D_1^{(1)}$	D_2 (ref)	$E^{(1)}$	$E_1^{(1)}$	E_2	e	H	L	L_1	L_p	w	y	θ
mm	max	1.05	0.1	0.50	4.4	0.25	0.30	4.70	4.55	3.5	5.30	1.8	0.85		6.2	1.3	0.55	0.85			8°
	nom													1.27					0.25	0.1	
	min	1.02	0.0	0.35	4.1	0.19	0.24	4.45	4.35	3.4	4.95	1.6	0.60		5.9	0.8	0.30	0.40			0°

Note
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot1205_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1205						~~14-08-21~~ 14-10-28

Fig. 17. Package outline LFPAK56D (SOT1205)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 12 May 2018