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# BUK9K32-100E

Dual N-channel 100 V, 33 mΩ logic level MOSFET

10 December 2013

Product data sheet

## 1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)}$  rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

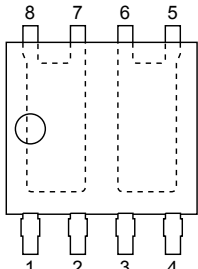
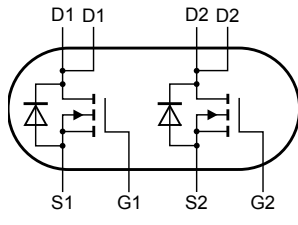
## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	26	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	64	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	26.6	33	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5\text{ A}$ ; $V_{DS} = 80\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	11	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K32-100E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K32-100E	93210E

## 8. Limiting values

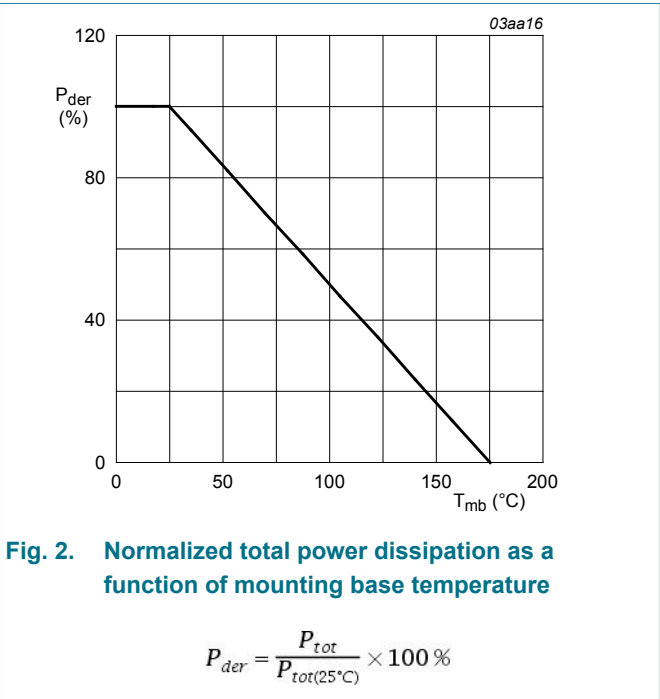
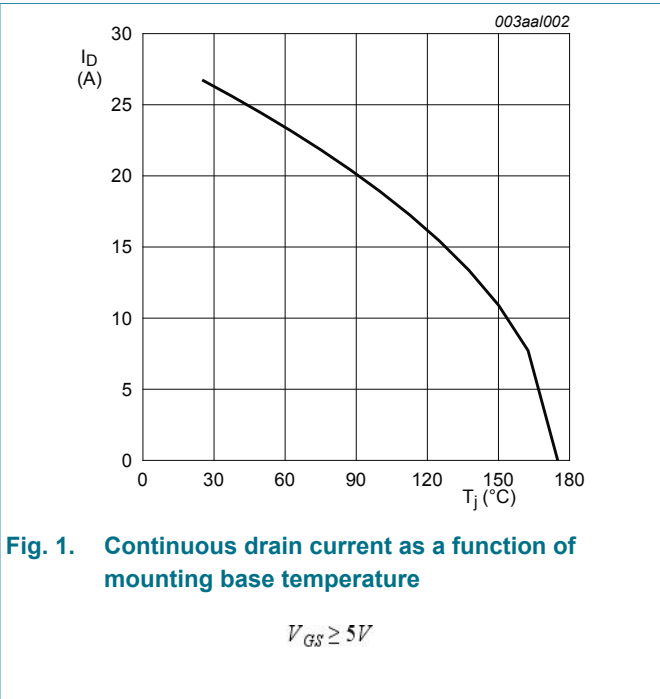
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$ ; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ }^{\circ}\text{C}$ ; DC	-10	10	V
		$T_j \leq 175\text{ }^{\circ}\text{C}$ ; Pulsed	[1][2] -15	15	V
$I_D$	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	26	A
		$T_{mb} = 100\text{ }^{\circ}\text{C}$ ; $V_{GS} = 5\text{ V}$ ; Fig. 1	-	19	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	106	A

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	64	W
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drain diode FET1 and FET2						
I <sub>S</sub>	source current			-	26	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	106	A
Avalanche Ruggedness FET1 and FET2						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 26 A; V <sub>sup</sub> ≤ 100 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; <a href="#">Fig. 3</a>	<a href="#">[3][4]</a>	-	74	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T<sub>j</sub> and or V<sub>GS</sub>.
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C





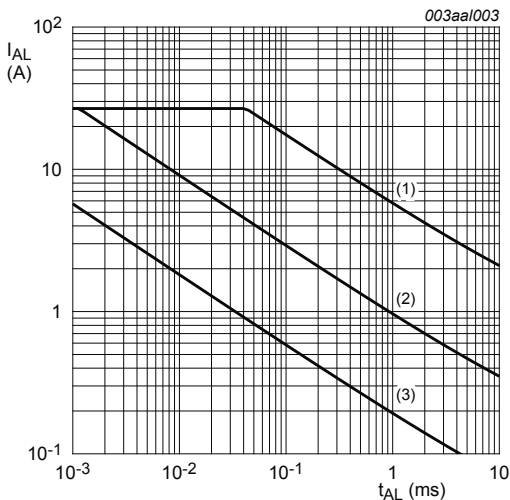


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j\ (init)} = 25^{\circ}C$ ; (2)  $T_{j\ (init)} = 150^{\circ}C$ ; (3) Repetitive Avalanche

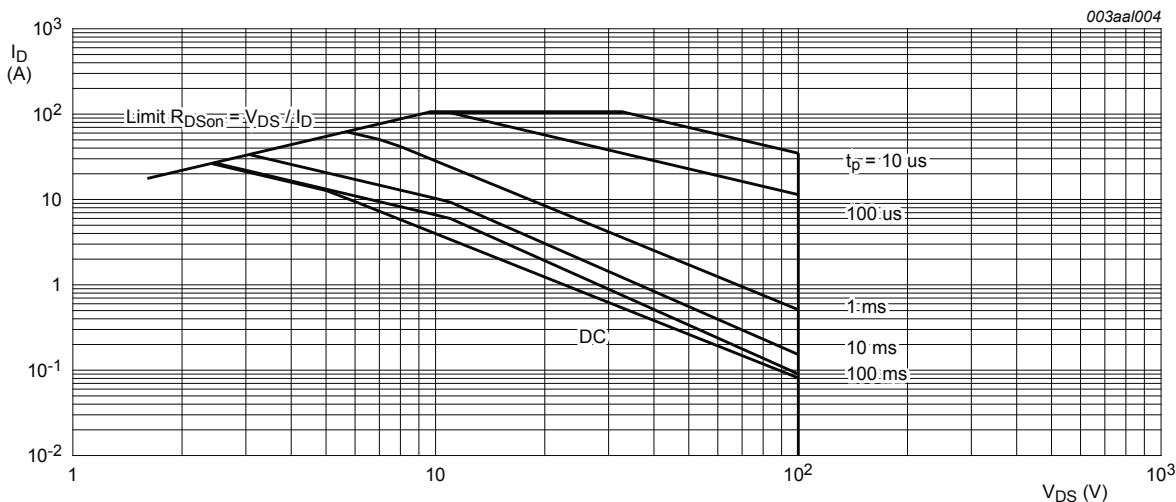


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.36	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

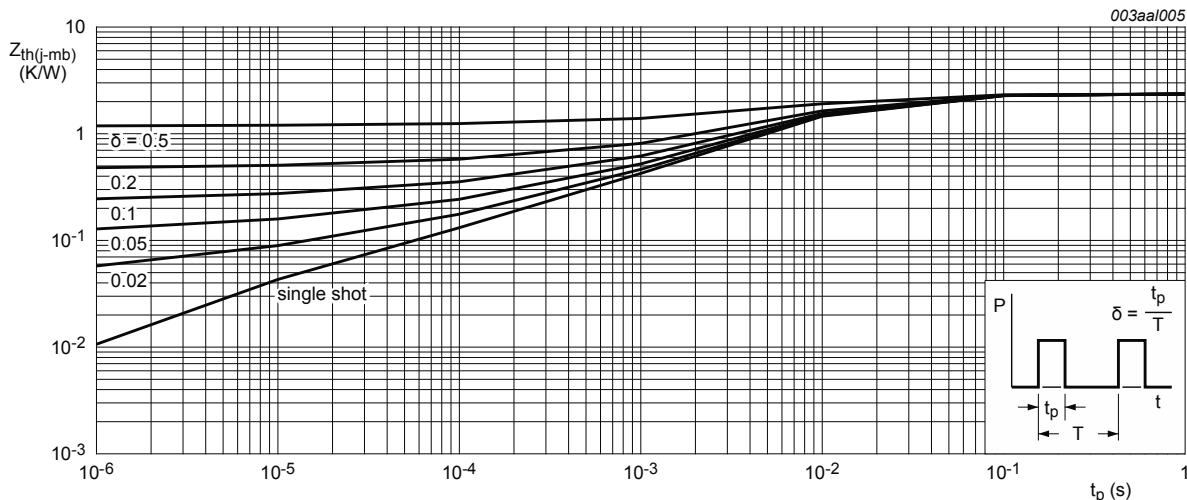


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = -55 ^\circ C$	90	-	-	V
		$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 ^\circ C$ ; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = 175 ^\circ C$ ; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	0.5	-	-	V
		$I_D = 1 mA$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 ^\circ C$ ; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	-	-	2.45	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 ^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 100 V$ ; $V_{GS} = 0 V$ ; $T_j = 175 ^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -10 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = 10 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 V$ ; $I_D = 5 A$ ; $T_j = 175 ^\circ C$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	73.4	91	mΩ
		$V_{GS} = 10 V$ ; $I_D = 5 A$ ; $T_j = 25 ^\circ C$ ; <a href="#">Fig. 11</a>	-	25.6	31	mΩ
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 V$ ; $I_D = 5 A$ ; $T_j = 25 ^\circ C$ ; <a href="#">Fig. 11</a>	-	26.6	33	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5 A$ ; $V_{DS} = 80 V$ ; $V_{GS} = 5 V$ ; $T_j = 25 ^\circ C$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	27.3	-	nC
$Q_{GS}$	gate-source charge		-	4.7	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q <sub>GD</sub>	gate-drain charge			-	11	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>		-	2377	3168	pF
C <sub>oss</sub>	output capacitance			-	153	184	pF
C <sub>rss</sub>	reverse transfer capacitance			-	101	139	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 80 V; R <sub>L</sub> = 15 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 5 Ω; I <sub>D</sub> = 5 A; T <sub>j</sub> = 25 °C		-	12.6	-	ns
t <sub>r</sub>	rise time			-	22	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	39.5	-	ns
t <sub>f</sub>	fall time			-	23.1	-	ns
Source-drain diode FET1 and FET2							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 5 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>		-	0.78	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C		-	35.6	-	ns
Q <sub>r</sub>	recovered charge			-	47.3	-	nC

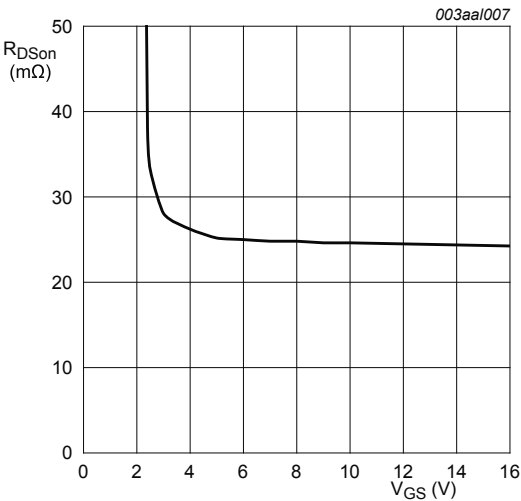
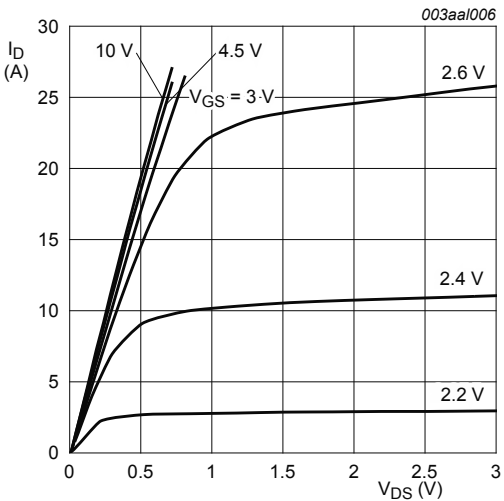


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^{\circ}\text{C}; I_D = 5\text{ A}$



$T_j = 25\text{ }^{\circ}\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

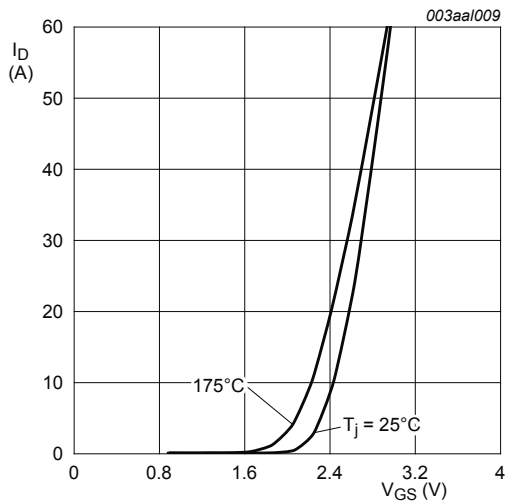


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

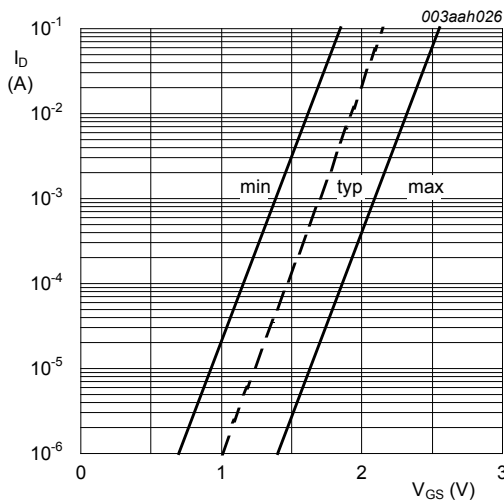


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{ V}$

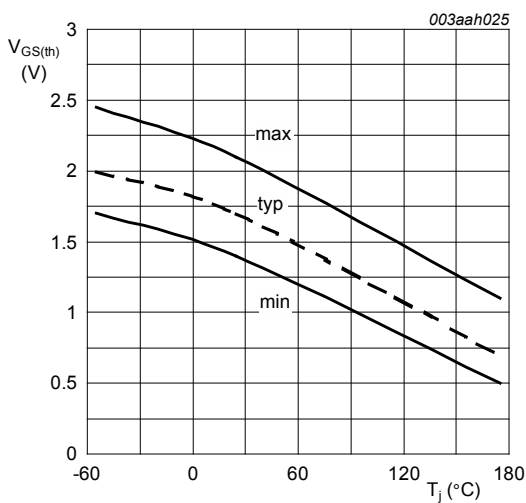


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

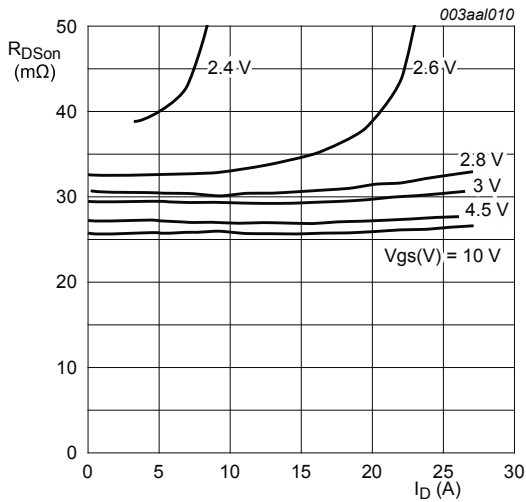


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$



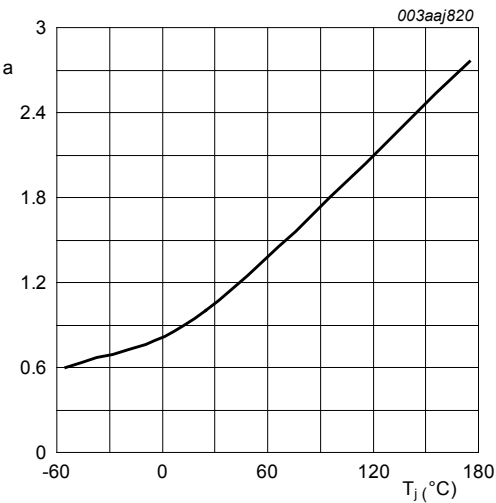


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^{\circ}\text{C})}$$

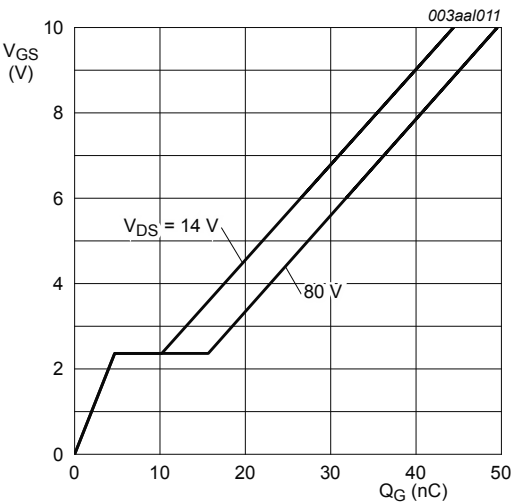


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}\text{C}; I_D = 5\text{ A}$$

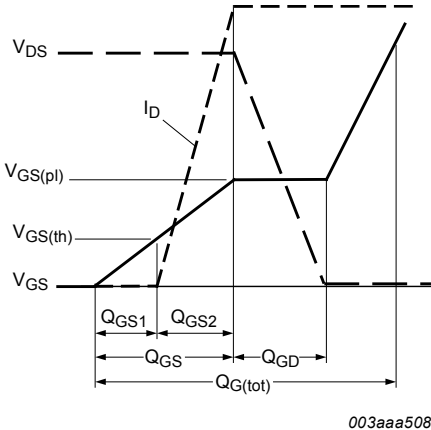


Fig. 13. Gate charge waveform definitions

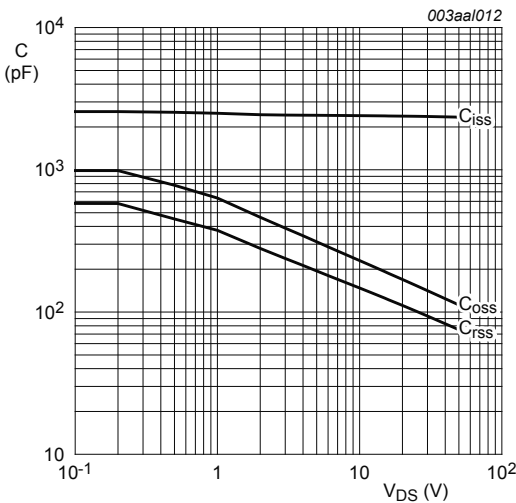


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

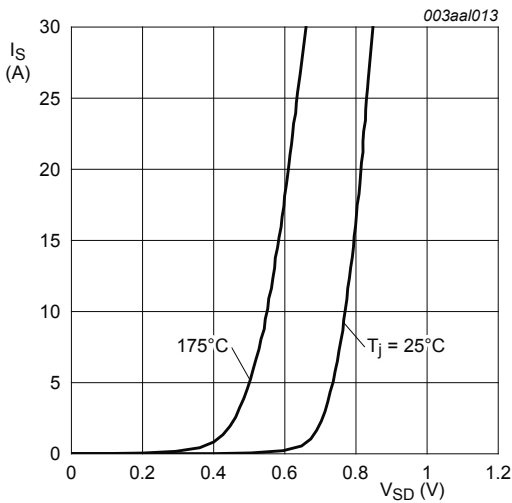


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

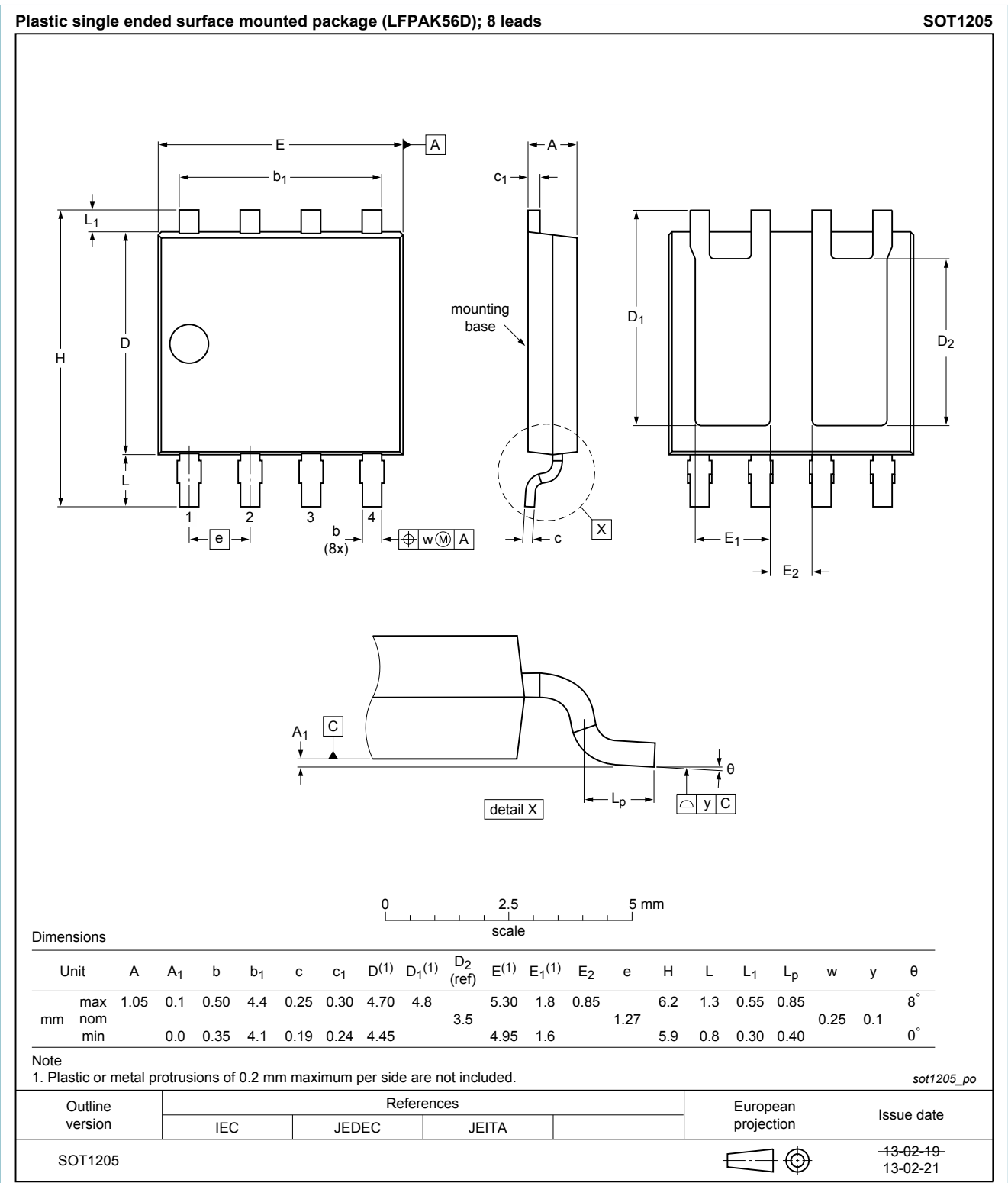


Fig. 17. Package outline LPAK56D (SOT1205)

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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13. Contents

1 General description ..... 1

2 Features and benefits ..... 1

3 Applications ..... 1

4 Quick reference data ..... 1

5 Pinning information ..... 2

6 Ordering information ..... 2

7 Marking ..... 2

8 Limiting values ..... 2

9 Thermal characteristics ..... 4

10 Characteristics ..... 5

11 Package outline ..... 10

12 Legal information ..... 11

12.1 Data sheet status ..... 11

12.2 Definitions ..... 11

12.3 Disclaimers ..... 11

12.4 Trademarks ..... 12

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