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[MG2420] Datasheet

(No. ADS0701)

V1.2

REVISION HISTORY

Version	Date	Description
V1.0	2013.10.24	▪ First version release.
V1.1	2014.04.21	▪ Sec 4.1 - Temperature updated. ▪ Sec 5 - Application circuit is updated.
V1.2	2014.09.01	▪ Sec 4.8 - Crystal Oscillator parameters (TYP and MAX value for ESR, C_O and C_L) are updated. ▪ Sec 5 - Table 3. Bill of Materials is updated. C_{11} and C_{12} is changed from 30pF to 13pF.

CONTENTS

FIGURES

TABLES

1. INTRODUCTION

MG2420 is a low-power 2.4GHz IEEE 802.15.4 and ZigBee compliant radio transceiver. Operation frequency of MG2420 covers an ISM band of 2.4~2.48GHz. In addition to the standard data-rate specified in IEEE802.15.4, MG2420 provides enhanced multiple data rates with channel coding (1M~3Mbps).

MG2420 can be controlled by an external microcontroller, and its operations can be configured through a high speed Serial Peripheral Interface (SPI).

Ultra Low Power Consumption:
The current consumption of MG2420 is very low; which is 15.4 mA in Rx mode and 16.1 mA in Tx mode with output Power of 0 dBm. Utilization of higher data rate (~3Mbps) helps minimizing the time for transmission and reception, which leads to further reduction of power consumption.

Low Cost Solution:
MG2420 is a single chip RF transceiver, which includes RF front-end, VCO, PLL, and digital block including baseband modem, MAC, power management, and a high-speed SPI. It's packaged in compact 4x4mm package. Only small numbers of external components - RF matching network, crystal, bias resistor and antenna - are required as application circuit; this leads to the low cost solution.

Improved Interference Rejection and Longer Range:
MG2420 shows excellent interference rejection performance; it can receive wanted signal with the presence of interference from ZigBee or other communication devices (i.e. Wi-Fi or Bluetooth). It has a longer communication range based on high transmit power up to +9 dBm and high sensitivity of -97dBm at 250Kbps mode.

1.1. APPLICATIONS

- Home Automation and Security
- Automatic Meter Reading
- Factory Automation and Motor Control
- Energy Management
- Remote Keyless Entry with Acknowledgement
- Low Power Telemetry
- Health-care equipment
- PC peripherals
- Toys and Gaming peripherals
- Remote Controller for Consumer Electronics
- Audio and Video Applications

2. KEY FEATURES

2.1. RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Low-power consumption
  - 15.4mA at RX mode
  - 16.1mA at TX mode with 0 dBm output
  - 28.4mA at TX mode with +9 dBm output
- High RX Sensitivity
  - -97dBm @ 250kbps (2Mcps Mode)
  - -93dBm @ 1Mbps (2Mcps Mode)
  - -90dBm @ 2Mbps (4Mcps Mode)
  - -86dBm @ 3Mbps (4Mcps Mode)
- No External T/R Switch and Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9 dBm
- Excellent TX EVM: 6% for 2Mcps mode, 8% for 4Mcps mode
- Direct Sequence Spread Spectrum
- MSK(O-QPSK) Modulation
- Channel coding with various rates of 1/2, 3/4
- Scalable Data Rate
  - 250kbps for IEEE 802.15.4 and ZigBee applications
  - 1Mbps for applications beyond IEEE 802.15.4 with RF bandwidth of 2MHz
  - 2~3Mbps for applications beyond IEEE 802.15.4 with RF bandwidth of 4MHz
- Digital RSSI Output
- Compliant to IEEE802.15.4

2.2. Integrated MAC

- Two 256-byte FIFOs
- FIFO management
- AES-128 Engine
- CRC-16 Computation and Check
- Automatic ACK transmission

2.3. Clock Inputs

- 32MHz Crystal for System Clock

2.4. Power

- 1.2V(Core)/1.8~3.6V(I/O) Operation
- Several On-chip Voltage Regulator for Analog part and Digital part separately.
- Power Supply Range for Internal Regulator(1.8V(Min) ~ 3.6V(Max))
- Power Management Scheme with Deep Sleep Mode Support; Current consumption under 1μA

2.5. Package

- Lead-Free/RoHS 28-pin QFN Package (4mm x4mm x 0.85mm)

3. PIN DESCRIPTION

MG2420 pin-out diagram and description are shown in [**Figure 1**] and [**Table 1**], respectively.

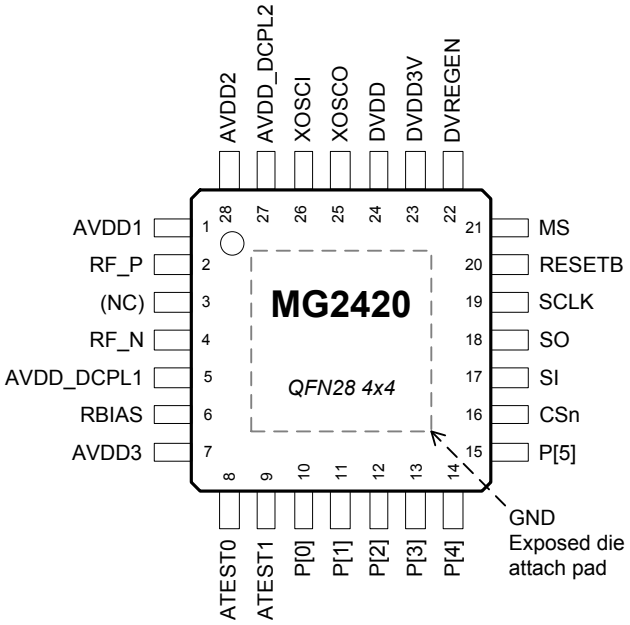


Figure 1. MG2420 Pin-out Diagram

Note: *The exposed die pad is located at the bottom of a chip and electrically connected to the die ground inside the package. It shall be soldered to ground on the board.*

Table 1. MG2420 Pin Description

Radio, Synthesizer, and Oscillator			
Pin	**Pin Name**	**Pin type**	**Pin Description**
2	RF_P	RF I/O	Positive RF input signal to LNA in RX mode. Positive RF output signal from PA in TX mode. It should be biased by AVDD_DCPL1. Refer to Figure 2 (Sec.5).
4	RF_N	RF I/O	Negative RF input signal to LNA in RX mode. Negative RF output signal from PA in TX mode. It should be biased by AVDD_DCPL1. Refer to Figure 2 (Sec.5).
6	RBIAS	Analog I/O	External precision bias resistor (510K) to generate the reference current.
25	XOSCO	Analog I/O	X-tal osc. buffer output or Crystal-unit pin-2
26	XOSCI	Analog I/O	X-tal osc. buffer input or Crystal-unit pin-1
1	AVDD1	Power I	1.8V to 3.6V RF/analog power supply connection
28	AVDD2	Power I	1.8V to 3.6V RF/analog power supply connection
7	AVDD3	Power I	1.8V to 3.6V RF/analog power supply connection
5	AVDD_DCPL1	Power O	Regulated Output of AVDD1 for PA bias
27	AVDD_DCPL2	Power O	Regulated Output of AVDD2 for decoupling
8	ATEST0	Analog O	Analog Temperature sensor output Analog test signal output
9	ATEST1	Analog O	Analog test signal output
Digital			

Pin	Pin Name	Pin type	Pin Description
19	SCLK	Digital I	SPI Interface: Serial Clock.
18	SO	Digital O	SPI Interface: Serial Out
17	SI	Digital I	SPI Interface: Serial In
16	CSn	Digital I	SPI Interface: Chip Select. Active low.
20	RESETB	Digital I	External reset. Active low.
10	P[0]	Digital I/O	General purpose digital I/O. Typical usage is setting to output mode to interface with MCU. When the SIGNAL_OUT (0x2F6[6:4]) sets to 0x2, P[0]~P[5] are assigned to TRSW, nTRSW, IRQ, CRCOK, PLL_LOCK and EXTCLK, respectively; for details, refer to Sec.7.4 and Sec.9.3.
11	P[1]	Digital I/O	
12	P[2]	Digital I/O	
13	P[3]	Digital I/O	
14	P[4]	Digital I/O	
15	P[5]	Digital I/O	
22	DVREGEN	Digital I	Digital VREG enable input. When high, digital voltage regulator is active.
24	DVDD	Power O	Regulated Output of DVDD3V for decoupling
23	DVDD3V	Power I	1.8V to 3.6V digital power supply connection
21	MS	Digital I	NC(Not Connected)
Ground and NC			
Pin	**Pin Name**	**Pin type**	**Pin Description**
Exposed bottom	GND	Ground	Ground for RF, analog, digital core, and IO
3	NC		NC It can be connected to GND.

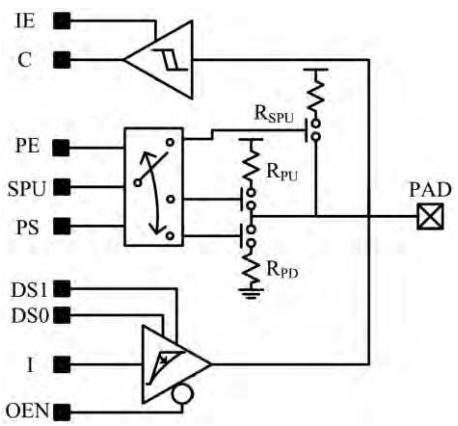
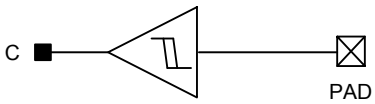
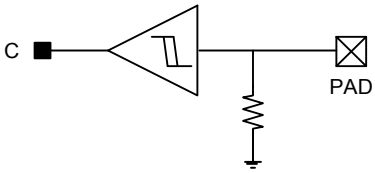
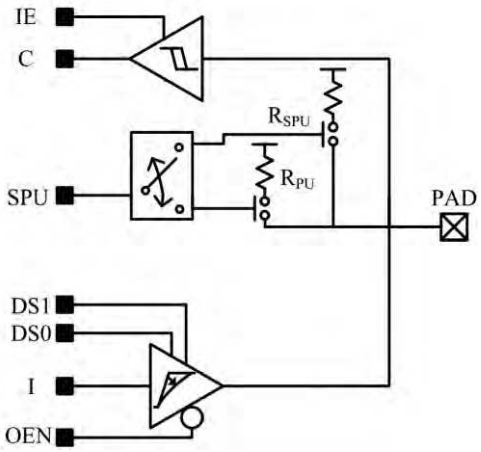
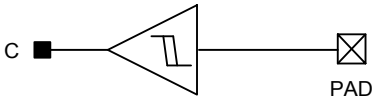
RF_P and RF_N are the differential RF input/output ports. The balun and impedance matching circuits are required to interface a single-ended 50-Ohm antenna.

There are 4 pins connected to 3.0V supply, which is applied to internal voltage regulators. And there are 3 output pins of the regulated 1.2V voltages for decoupling. These regulated outputs should not be used to supply power to external circuits. DVDD is the output of the internal digital regulator which is controlled by the DVREGEN pin. Other analog voltage regulators are controlled by the power management block and activated by the power mode.

SCLK, SO, SI, and CSn are used in slave SPI interface. RESETB is an external reset input with active low.

The exposed die pad is located at the bottom of the chip and electrically connected to the die ground inside the package. It shall be soldered to the board ground.

Table 2. I/O Equivalent Circuit Summary

Equivalent Circuit Schematic	Reset Status	Note
GPIO (P[5:0])		
	Input with pull-up	Refer to Sec.7.4. In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
SCLK, SI, CSn, RESETB		
	Input with HiZ	In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
MS		
	Input with pull-down	In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
SO		
	Input with pull-up	Output @ CSn=low Otherwise, input with pull-up In Deep Sleep Mode(DVREGEN = Low), PAD Status is Strong Pull-Up
DVREGEN		
	Input	

4. ELECTRICAL CHARACTERISTICS

4.1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DDIO}	Digital I/O supply voltage	-0.3 to 3.6	V
V_{DDA}	Analog supply voltage	-0.3 to 3.6	V
V_{DD12}	Regulated output voltage on pins 5, 24, 27	-0.3 to 1.32	V
T_{STG}	Storage Temperature	-40 to 150	°C
ESD	HBM MM CDM	2000 200 750	V

Stress exceeding one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only. And functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL CHARACTERISTICS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE1: All voltage values are based on V_{SS} and V_{SSIO}.
NOTE2: These values were obtained under worst-case test conditions specially prepared for MG2420 and these conditions are not sustained in normal operation environment.

CAUTION: *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

4.2. Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DDIO}	Digital I/O supply voltage (DVDD3V)	1.8	3.0	3.6	V
V_{DDA}	Analog supply voltage on pins 1, 7, 28	1.8	3.0	3.6	V
T_{OP}	Operating temperature range	-40		85	°C

4.3. Digital I/O DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	Unit
V_{DDIO}	I/O supply voltage(DVDD3V)	1.8	3.0	3.6	V
AGND	Chip ground		0		V
V_{IH}	Input high voltage	2.0		3.6	V
V_{IL}	Input low voltage	-0.3		0.8	V
V_{OH}	Output high voltage	2.4			V
V_{OL}	Output low voltage			0.4	V
R_{PU}	Pull-up Resistance		66		kΩ
R_{PD}	Pull-down Resistance		66		kΩ
R_{SPU}	Strong Pull-up Resistance DVDD3V=3.3V	1.42	1.62	1.92	kΩ

4.4. Current Consumption

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz, Data rate=250Kbps

Parameter	MIN	TYP	MAX	UNIT	Note
TX Mode @+9dBm Output Power @+8dBm Output Power @+7dBm Output Power @+6dBm Output Power @+5dBm Output Power @+4dBm Output Power @+3dBm Output Power @+2dBm Output Power @+1dBm Output Power @ 0dBm Output Power		 28.4 24.7 22.1 21.1 20.5 19.1 18.5 17.4 16.4 16.1		mA	Measured at 2450MHz Channel AES, Peripheral, and Temp. Sensor Disabled
RX Mode		15.4		mA	AES, Peripheral, and Temp. Sensor Disabled
Deep Sleep Mode			1	μA	DVREGEN=0
Analog Temperature Sensor		0.06		mA	Current consumption increases at using this

4.5. RF Receive Section

4.5.1. Chip Rate of 2Mcps (RF Bandwidth: 2MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
RF Frequency Range (Center Frequency)	2405		2480	MHz	
Maximum Input Level 1000 kbps 250 kbps		 -3.7 -2		dBm	PER≤1% Packet length of 20-byte
Spurious Radiation 30-1000 MHz 1-12.75 GHz		 -60 -60		dBm	Compiles with EN 300 328, EN 300 400, FCC, and ARIB STD-T66.
Received RF Bandwidth (Chip Rate)		2		MHz	
Channel Spacing		5		MHz	Compiles with IEEE 802.15.4
Receiver Sensitivity 1000 kbps 250 kbps		 -93 -97		dBm	PER≤1% Packet length of 20-byte
Adjacent Channel Rejection +5MHz -5MHz		 30 31		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Adjacent Channel Rejection +5MHz -5MHz		 48 49		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Filtered IEEE 802.15.4 interferer signal
Alternate Channel Rejection +10MHz -10MHz		 53 56		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Alternate Channel Rejection +10MHz -10MHz		 58 59		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Filtered IEEE 802.15.4 interferer signal
Others Channel Rejection ≥ +15MHz ≥ -15MHz		 65 65		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Co-channel Rejection		-6.6		dB	250kbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Wi-Fi IEEE 802.11n Rejection		47		dB	250Kbps, 40-byte WANTED Signal -82dBm, Interference 802.11n (BW40MHz) +27/-27Mhz

Blocking/desensitization -250MHz -100MHz -50MHz +50MHz +100MHz +250MHz		 -20 -23 -23 -25 -23 -23		dBm	250kbps, 20-byte P_{RF} = sensitivity+3 ETSI EN 300 440-1 V1.6.1 (2010-04)-37[2] blocking/desensitization

4.5.2. Chip Rate of 4Mcps (RF Bandwidth: 4MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
RF Frequency Range (Center Frequency)	2405		2480	MHz	
Maximum Input Level 3000 kbps 2000 kbps		 2.3 -0.2		dBm	PER≤1% Packet length of 20-byte
Spurious Radiation 30-1000 MHz 1-12.75 GHz		 -60 -60		dBm	Compiles with EN 300 328, EN 300 400, FCC, and ARIB STD-T66.
Received RF Bandwidth (Chip Rate)		4		MHz	
Channel Spacing		10		MHz	Recommended.
Receiver Sensitivity 3000 kbps 2000 kbps		 -86 -90		dBm	PER≤1% Packet length of 20-byte
Adjacent Channel Rejection +10MHz -10MHz		 41 41		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Alternate Channel Rejection +20MHz -20MHz		 60 61		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Others Channel Rejection ≥ +30MHz ≥ -30MHz		 61 62		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal
Co-channel Rejection		-6		dB	2Mbps, 20-byte P_{RF} = sensitivity+3 Non-Filtered IEEE 802.15.4 interferer signal

Blocking/desensitization -250MHz -100MHz -50MHz +50MHz +100MHz +250MHz		 -24 -28 -28 -29 -28 -27		dBm	2Mbps, 20-byte [2] P_{RF} = sensitivity+3

4.6. RF Transmit Section

4.6.1. Chip Rate of 2Mcps (RF Bandwidth: 2MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
Transmit Chip Rate		2		Mcps	
TX Output Power		9		dBm	Using the recommended matching circuit
Error Vector Magnitude (EVM)		6		%	
Harmonics 2nd harmonic 3rd harmonic		 -45 -45		dBm	Using the recommended matching circuit
Spurious Emission 30Hz~1GHz 1GHz~2.5GHz 2.5GHz~12.7GHz 5.15~5.3GHz		 -60 -60 -60 -60		dBm	Complies with EN 300 440, FCC, and ARIB STD-T66.

4.6.2. Chip Rate of 4Mcps (RF Bandwidth: 4MHz)

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
Transmit Chip Rate		4		Mcps	
TX Output Power		9		dBm	Using the recommended matching circuit
Error Vector Magnitude (EVM)		8		%	
Harmonics 2nd harmonic 3rd harmonic		 -45 -45		dBm	Using the recommended matching circuit
Spurious Emission 30Hz~1GHz 1GHz~2.5GHz 2.5GHz~12.7GHz 5.15~5.3GHz		 -60 -60 -60 -60		dBm	Complies with EN 300 440, FCC, and ARIB STD-T66.

4.7. Frequency Synthesizer Characteristics

Test Conditions: T_{OP}=25C, V_{DDA}=V_{DDIO}=3.0V, f_{RF}=2.45GHz

Parameter	MIN	TYP	MAX	UNIT	Note
Phase Noise @ 100KHz offset @ 1MHz offset @ 2MHz offset @ 3MHz offset @ 5MHz offset @ 10MHz offset @ 50MHz offset		 -82.2 -110.3 -117.0 -119.5 -123.3 -134.0 -149.0		dBc/Hz	
PLL Lock Time			80	μsec	

4.8. Crystal Oscillator

Parameter	MIN	TYP	MAX	UNIT	Note
Crystal Oscillator Frequency		32		MHz	
Crystal Frequency Accuracy Requirement	-40		+40	ppm	
Equivalent series resistance (ESR)		30[1]	60[2]	Ω	
Crystal shunt capacitance (C_O)		3	5	pF	
Crystal load capacitance (C_L)		9[1]	13[2]	pF	
Start-up time			0.8	ms	

4.9. Analog Temperature Sensor

Test Conditions: V_{DDA}=V_{DDIO}=3.0V

Parameter	MIN	TYP	MAX	UNIT	Note
Output voltage at -40°C		0.8276		V	
Output voltage at 0°C		0.7709		V	
Output voltage at +27°C		0.7322		V	
Output voltage at +85°C		0.6463		V	
Temperature coefficient		-1.4526		mV/°C	Linear fitted from -40°C to 85°C
Current consumption		0.06		mA	

[1] The negative resistance of driving circuit is five times larger than the ESR of crystal oscillator with crystal satisfying above TYP conditions.
[2] The negative resistance of driving circuit is two times larger than the ESR of crystal oscillator with crystal satisfying above MAX conditions.

5. APPLICATION

A typical application diagram of MG2420 is shown in [Figure 2]. A few external components are required as shown in the figure. [Table 3] describes the external components and lists their typical values.

The inductor, L1 is used as an RF matching and as an output load of the PA(power amplifier) simultaneously. The components near the RF_P/RF_N pins, L2, L3, C2, and C3 form a balun which converts the differential RF signals to a single-ended RF signal. L4, C4, and C5 form an LC harmonic filter to suppress the TX output harmonics. In addition, C4 is used for DC blocking. All together with adequate values, they also transform the impedance to match a 50-Ohm antenna.

As shown in [Figure 2], RF_P and RF_N are biased by AVDD_DCPL1 through L1 and L3.

The 32MHz crystal with loading capacitors is connected to MG2420. It provides the reference frequency source for MG2420.

CD1, CD2, and CD3 are supply decoupling capacitors, whose values depend on PCB artwork and stack-up information.

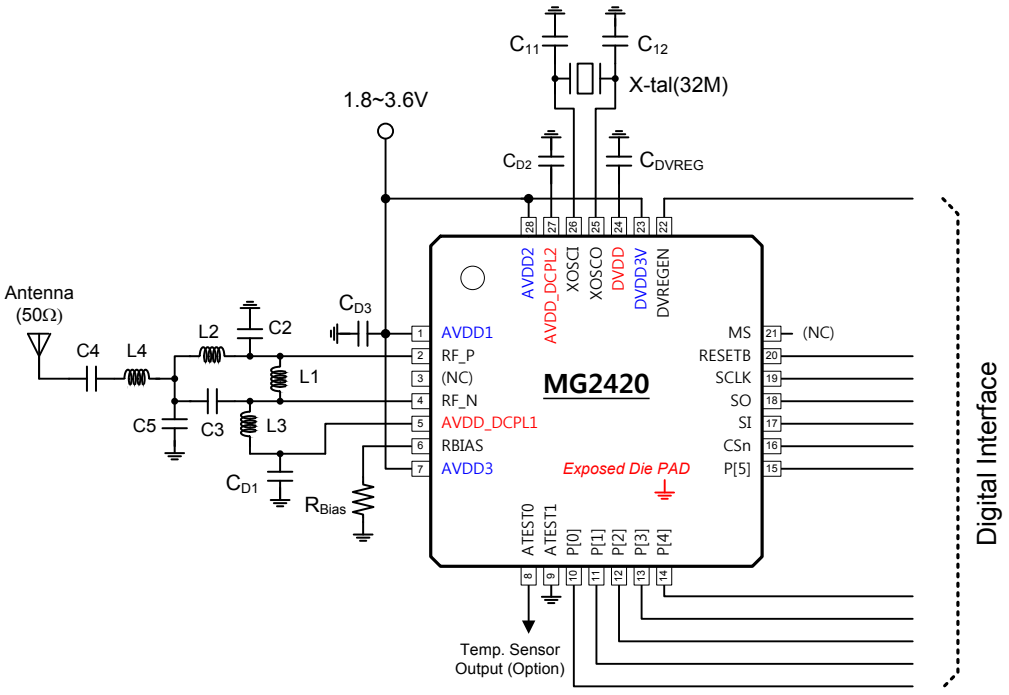


Figure 2. MG2420 Application Circuit

Table 3. Bill of Materials for Figure 2

No	Component	Description	Value
1	L1	RF matching inductor	5.1nH
2	L2, L3	RF balun inductors	2.4nH
3	C2	RF balun capacitor	1.2pF
4	C3	RF balun capacitor	1.0pF
5	L4	RF LC filter/matching inductor	3.9nH
6	C5	RF LC filter/matching capacitor	1.5pF
7	C4	DC blocking capacitor	1.0pF
8	Rbias	Resistor for internal bias current reference	510KΩ
9	X-tal	32MHz crystal unit	32M (±40ppm, 16pF)
10	C11, C12	Crystal loading capacitors	13pF[3]
11	C_{DVREG}	Decoupling capacitor for DVDD (digital voltage regulator output)	1uF
12	C_{D1}	Decoupling capacitor for AVDD_DCPL1	1nF
13	C_{D2}	Decoupling capacitor for AVDD_DCPL2	1uF
14	C_{D3}	Decoupling capacitor for AVDD1	1uF

[3] The value of crystal loading capacitance depends on crystal oscillator.

6. FUNCTIONAL DESCRIPTION

6.1. Block Diagram

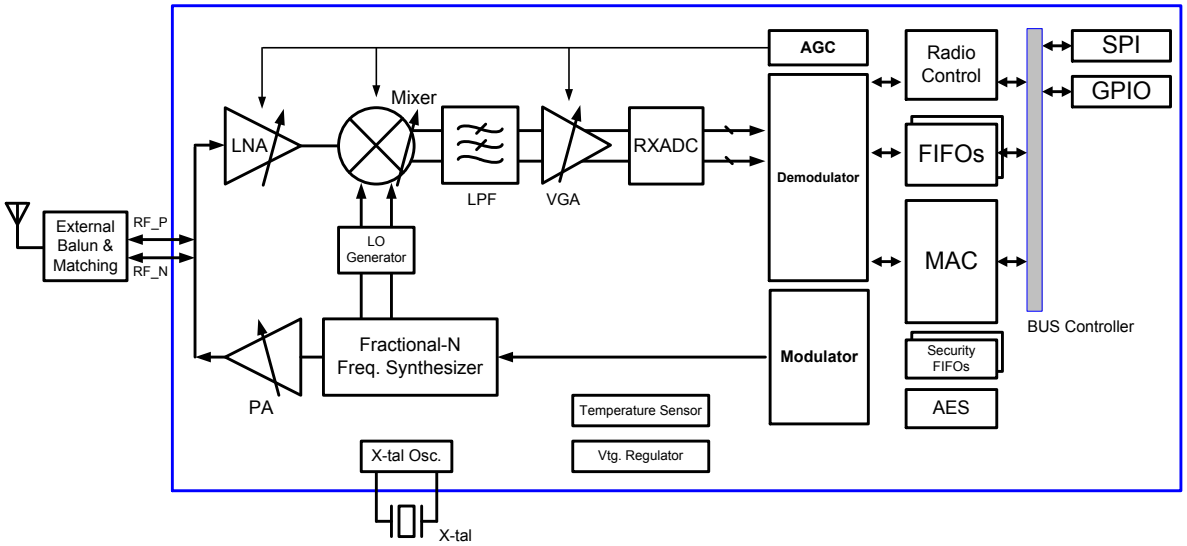


Figure 3. MG2420 block diagram.

A simplified block diagram of MG2420 is shown in [Figure 3]. Since the bidirectional differential RF pins are used for RX and TX, no external T/R switch is required. The receiver is designed with direct-conversion architecture, and it operates in the 2.4GHz band with excellent receiver sensitivity and robustness to interfererence. Transmitter architecture is based on direct-modulation technique using direct RF frequency synthesis.

The LNA amplifies the received RF signal at RF_P and RF_N pins, and the RX Mixer converts the RF signal to the baseband frequency in quadrature(I and Q). Gains of LNA and mixer are controlled coarsely by AGC block.

Channel filtering occurs in the LPF(low-pass filter). The VGA(variable-gain amplifier) provides sufficient gain, controlled by the AGC, to drive the RXADC(analog-to-digital converter). And, the RX ADC converts the VGA output signals to the signed binary digital signals.

The frequency synthesizer (PLL) generates the carrier signals for channel frequency.

The LO generator transforms the differential outputs of the PLL into the quadrature(I, Q) signals required for local signals in the RX Mixer.

The PA(power amplifier) amplifies the modulated RF signal from the PLL. TX output power level is controlled in the PA by register setting.

The modulator transforms the raw data came from TX FIFO into the modulated signals. It consists of the bit-to-symbol mapping block, the spreading block, the convolution encoder, the interleaver, and the mapping circuit for direct-modulation.

The demodulator processes the digitized RX signals of the ADC outputs, which store the RX

FIFO after processing correlation, frequency offset control, timing synchronization, deinterleaver, and viterbi decoder.

The AGC(automatic gain controller) controls gains of RF circuits to maintain the input level of the RXADC.

The functions of the MAC are to transfer the data from higher layer to PHY block, to send the received data from PHY to higher layer, and to encrypt/decrypt the data in the AES.

The Radio Controller module controls the operation state, the FIFOs, power up/down of RF/Analog blocks, and clock on/off of modem sub blocks. It provides operating sequences for both transmit and receive. Also it controls the sleep mode.

The X-tal oscillator generates a reference clock for RF and digital blocks.

Several voltage regulators are integrated to provide the operating voltage for analog and digital blocks.

An SPI serial interface is used for radio configuration and packet handling. GPIO pins are typically used for microcontroller interface.

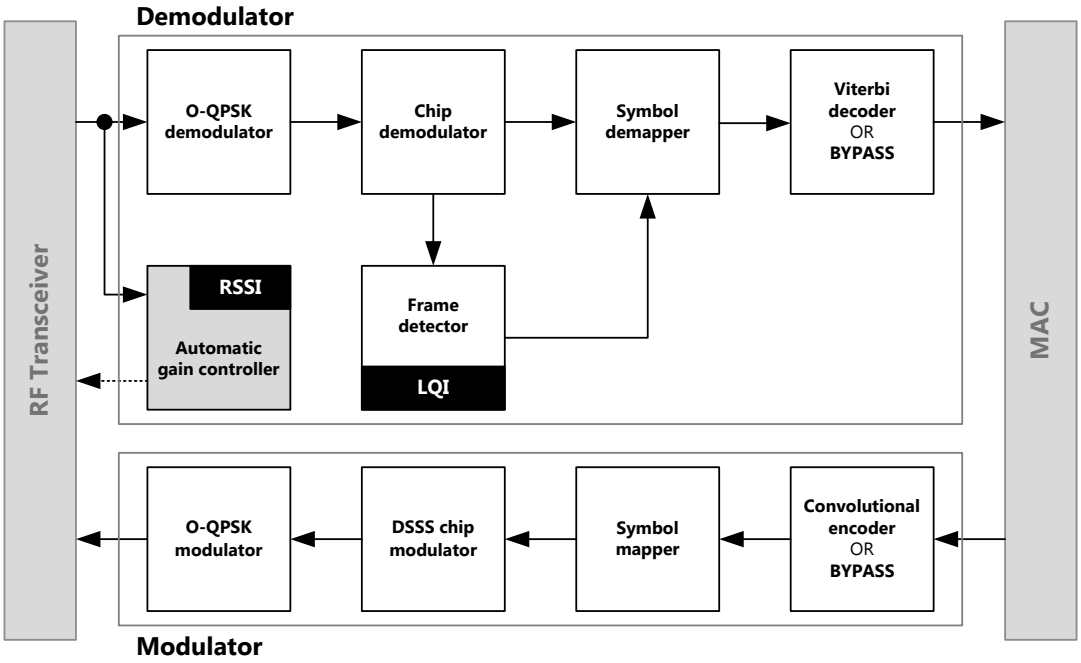


Figure 4. Baseband PHY block diagram

The baseband PHY (i.e. modem) is composed of the O-QPSK modulator and demodulator with simple convolutional channel coder. [Figure 4] shows the baseband PHY block diagram.

The modulation starts from fetching the data in the TX MAC FIFO. The PHY payload (PHY service data unit; PSDU) is optionally encoded with the convolutional channel encoder. After appending the preamble, SFD and length field to the PHY payload, a constructed frame (PHY protocol data unit; PPDU) is mapped to designated symbols according to the data-rate

control of the PHY controller. Each symbol is spread accordingly by the DSSS chip modulator. The spread PHY bit stream in the chip-level is then modulated to the O-QPSK signal and transmitted by the RF transmitter. Especially for the 250Kbps data-rate packet, its structure is fully compliant to the IEEE802.15.4 O-QPSK PHY specification.

With the RF receiver, the received O-QPSK signal is demodulated to the chip sequences. The gain amplifying blocks in the RF receiver are controlled by the automatic gain controller (AGC). The chip sequence is appropriately de-spread by the chip demodulator, and then the start of the designated frame is determined by detecting the synchronization header (preamble and SFD). When the SFD is detected, the baseband PHY generates the interrupt which indicates the start of a packet.

The length and the PHY payload followed by the synchronization header are decoded by the symbol demapper and Viterbi decoder (if the convolutional encoding is applied), and stored in the RX MAC FIFO. When the last data of the PHY payload is stored, the interrupt is generated to indicate the end of the packet reception. After a packet reception interrupt occurs, the RX MAC procedure is performed.

When a packet is received, the baseband PHY provides both of the received signal strength Indicator (RSSI) and the link quality indicator (LQI) automatically. They are used to decide the quality of the communication channel.

While a packet does not exist, the baseband PHY continuously provides the RSSI of the RF signal at antenna. The measured RSSI is used to decide the communication channel state. Clear channel assessment (CCA) operation is based on this information. The CCA operation is used to prevent a collision when multiple users try to use a channel simultaneously. When a channel is determined as busy, packet transmission is deferred until the channel state changes to idle.

6.2. Data Rate

MG2420 supports various data rates of 1~3Mbps for applications beyond IEEE 802.15.4 compliances.

The 1Mbps modes, which is listed in [Table 4], occupy 2MHz RF channel bandwidth which is same as the IEEE 802.15.4-2.4GHz 250Kbps standard mode.

The 2M~3Mbps modes, which are listed in [Table 5], occupy an RF channel bandwidth of 4MHz.

The high data rate modes of 1M~3Mbps use decreased spreading factor with the same preamble structure as 250Kbps. Also, they can use the FEC. The data rate is selected by writing to the registers: SEL_TXDR (0x211[3:0]) and CLK_SEL(0x2C6[1]).