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MG245X
Datasheet

(No. ADS0101)

V2.55

REVISION HISTORY

Version	Date	Description
VER.1.0	2008.1.19	▪ First Official Version Release
VER.1.1	2008.1.24	▪ Section 5 -Delete the followings in the Table 1. P0[0]:SCKO of SPI master P0[5]:SSB of SPI slave P0[6]:SDO of SPI slave P0[2]:MISO of SPI master P0[3]:SPICSNI P0[7]:SDI of SPI slave P0[1]:MOSI of SPI master P0[4]:SCKI of SPI slave ▪ Section 7.6.7 -Modify SPER(SPI E REGISTER) -> SPER(SPI EXTENDED REGISTER) ▪ Section 7.6.12 -Modify SADCREF of SADCCON register
VER.1.2	2008.2.28	▪ Section 3 -Correct Typing Error(-99dBm -> -98dBm: High RF RX Sensitivity) ▪ Section 6 - Add 'NOTE' ▪ Section 7.2 - Add 'NOTE' ▪ Section 7.5 -PM3: Change from 1μA to 0.3μA. ▪ Section 10 -Add Blocking/Desensitization -PM3: Change from 1μA to 0.3μA.
VER.1.3	2008.4.10	▪ Section 4 - Modify Power ▪ [Figure 2] - AVDD_XOSC -> DVDD_XOSC ▪ [Table 1] -PIN H4: Modify Pin Description -PIN B5/B6 (AVDD_XOSC -> DVDD_XOSC)

		▪ Section 6 -Modify entire contents ▪ Section 7.3 -Modify contents(Add CLKDIV0) ▪ Section 7.6.14 / 7.6.15 -Modify [Figure 18] / [Figure 19] and contents ▪ Section 7.8.2 -Entire contents of PLL0/1/2/3 (PLL CONTROL 0/1/2/3 REGISTER, 0x2286, 0x2287, 0x2288, 0x228B)
VER.1.31	2008.6.19	▪ Section 7.6.3 -Modify WDTCON. WDTWE: Modify Description. WDTEN: Modify Reset Value(0->1) WDTPRE: Modify Reset Value(0->11) ▪ Section 7.7.3 -Modify MTFCSTS. Full: Modify R/W part(R/W ->R/O) Empty: Modify R/W part(R/W ->R/O)
VER.1.4	2008.7.20	▪ Section 7.1.1 -Add the address table of code banking including common area. ▪ Section 7.5 -Modify entire contents. ▪ Section 7.6.4 -Modify entire contents. - Add ‘Note’. ▪ Section 7.6.8 -Add ‘Note’ for ADPCM. ▪ Section 7.6.10 -Add ‘Note’ in the bit field 0(mode) of QCTL. ▪ Section 7.6.14 -Add ‘Note’.

		▪ Section 7.6.15 -Add 'Note'.
VER.1.41	2008.12.8	▪ Section 9 - Change V_{DD} to V_{DDIO} on V_{IH} , V_{IL} , V_{OH} ▪ Section 7.2 -Add NOTE ▪ Section 8,9 - Change MAX value 2.0 to 1.65 on VDD - Change MAX value 3.6 to 3.3 on VDDIO ▪ Section 7.6.4 - Modify NOTE
VER.1.42	2009.2.13	▪ Section 7.1.4 - Change 'P3OEN, P0OEN' initial/reset value to 0xFF, 'P1OEN' initial/reset value to 0xEF. ▪ Section 7.8.1 - RX End Interrupt (RXEND_INT) Correct 'TX FIFO' to 'RX FIFO' ▪ Section 7.8.2 -PCMD0 (PHY COMMAND0 REGISTER, 0x2200) Name RXON : Contents corrected - PCMD1 (PHY COMMAND1 REGISTER,0x2201) Name RXOFF : Contents corrected -RXRFPU (RF RX PATH POWER-UP REGISTER, 0x2205) Name LNAPU : Contents corrected -TXRFPD (RF TX PATH POWER-DOWN REGISTER, 0x2206) Name TXUMBUFPD : Contents corrected -PHYSTS1 (PHY STATUS1 REGISTER, 0x2271) Name TXSTSF, MDSTSF : Contents corrected
VER.1.5	2009.2.27	▪ Section 6 -Modify 'application circuit' ▪ Section 7.2 -Delete Reset Errata.

		▪ Section 7.5 -Add PDM Register, PDCON Register ▪ Section 7.6.4 -Change RTEN to STEN bit in PDCON ▪ Section 7.6.5 -Add RCOSC1 Register
VER.1.51	2009.6.22	▪ Section 7.5 - Modify reset value of PDM, PDCON register. ▪ Section 7.6.5 -Modify reset value of RCOSC1 register. ▪ Section 7.8.2 -Change 'TDCNF0' to 'TDCNF3', 'TDCNF1' to 'TDCNF0'.
VER.2.0	2009.12.10	▪ Section 7.1.4 - P1OEN/P0REN/P1REN/P3REN reset value modified. ▪ Section 7.6.11 - Contents modified. ▪ Section 7.6.12 - Modify '8kHz' to '16kHz'. - SADCCON - SADCDONE, SADCREF contents modified. - SADCVALH - contents modified. - SADCVALL - contents modified. - SADCBIASH, SADCBIASL delete. ▪ Section 7.6.14 - contents and note modified. ▪ Section 7.6.15 - contents and note modified. ▪ Section 10. - Add PM1 max value. ▪ All section - Datasheet of MG2450 and of MG2455 are combined.
VER.2.01	2010.4.1	▪ Section 7.6.4. - RTDLY description and reset value are changed.
VER.2.02	2010.9.15	▪ Section 7.1.1. - The address of code banking is corrected(BANK 3). ▪Section 10. - Receiver Sensitivity is modified in the table.
VER.2.1	2010.10.8	▪ The contents corresponding to MG2450A and MG2455A are added to all sections.

		▪ Section 6 - Table 5-the differential impedances of each chip is added. ▪ Section 7.5 - The content for changing the operation mode is updated. - The description for PDCON[2] is modified. ▪ Section 7.6.4 - The content of sleep timer interrupt interval is updated. ▪ Section 7.6.8 - The description of VSPCTL is updated. - ENC_PREDICT0/1, DEC_PREDICT0/1, ENC_INDEX and DEC_INDEX registers are added for MG2450A and MG2455A. - The description of ENCCTL[5] and DECCTL[5] is updated. ▪ Section 8 - ESD item is added to the table. ▪ Section 10 - The table about differential impedances is added.
VER.2.2	2010.12.6	▪ Section 4/7.6/7.6.12/7.6.14/7.6.15/ - Contents corrected to 4-channel 12-bit ADC (ENOB > 8-bit) ▪ Section 10 - PM1 in table is changed.
VER2.3	2011.3.2	▪ Section 5 - Table 1 is corrected.(H1,2/J1,2)
VER2.31	2011.5.12	▪ Section 5 - D1 and E1 in Table 1 are modified. - 3 and 4 in Table 2 are modified. - MS[0], MS[1], and MS[2] are modified in [Table 1 and 2].
VER2.4	2011.7.30	▪ Section 10 - Input range of Sensor ADC is added. - Adjacent/Alternate/Others channel rejection and co-channel rejection values are updated.
VER2.5	2012.2.2	▪ The contents related with the 32kHz clock are updated in Sec 4/Sec 5/Sec 7.1.4/Sec 7.3/Sec 7.5/Sec 7.6.4/Sec 7.6.5/Sec 11.
VER2.51	2012.2.28.	▪ Sec 10 - The electrical characteristics for the flash memory are added .

VER2.52	2012.5.22.	Sec 7.6.11 - The description of the internal voltage regulator is updated. Sec 10 - The crystal frequency accuracy requirement is updated (±10ppm → ±40ppm).
VER2.53	2012.6.7.	Sec 7.6.8.1 - contents modified. - Add 'Note'.
VER2.54	2014.4.9.	Sec 6 - Updated Figure 4, Figure 5
VER2.55	2014.4.21.	Sec 8 - Storage Temperature updated.

CONTENTS

FIGURES

TABLES

1. INTRODUCTION

This guide is a datasheet for MG2450, MG2450A, MG2455 and MG2455A(hereinafter "MG245X") of RadioPulse. The specification applied only to specific model is described with MG2450, MG2450A, MG2455 or MG2455A mark. The characteristics without marking specific model are common.

MG245X is a true single-chip solution, compliant to ZigBee specifications and IEEE802.15.4, a complete wireless solution for ZigBee applications such as home control and sensor network.

MG245X consists of an RF transceiver with baseband modem, a hardwired MAC and an embedded 8051 microcontroller with internal flash memory for application program. It also includes numerous general-purpose I/O pins and peripheral devices such as timer and UART and is one of the first devices to provide an embedded Voice CODEC. This chip is ideal for very low power applications.

RadioPulse provides its customer with ZigBee stack software in compiled library. User application software can be compiled using a popular C-language compiler such as Keil.

2. APPLICATIONS

- Home Automation and Security
- Automatic Meter Reading
- Factory Automation and Motor Control
- Replacement for legacy wired UART
- Voice Applications
- Energy Management
- Remote Keyless Entry with Acknowledgement
- Low Power Telemetry
- Health-care equipments
- PC peripherals
- Toys

3. ENHANCED FEATURES

- Scalable Data Rate; 250kbps for ZigBee, 500kbps and 1Mbps for custom applications.
- Voice Codec Support; μ-law/a-law/ADPCM
- High RF RX Sensitivity; -98dBm @1.5V
- High RF TX Power of +8dBm @1.5V
- Embedded 8051 Compatible Microprocessor with 96KB Embedded Flash Memory for Program Space
- 8KB of Data Memory
- Power Management Scheme with Deep Sleep Mode(under 1μA)
- Single Voltage operation; 1.9 to 3.3V using an internal regulator(1.5V core)

4. FEATURES

RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Low Power Consumption
- Low Operating Voltage of 1.5V
- High Sensitivity of –98dBm@1.5V
- No External T/R Switch and Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +8dBm@1.5V
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- Scalable Data Rate: 250Kbps for ZigBee, 500Kbps and 1Mbps for private application
- RSSI Measurement
- Compliant to IEEE802.15.4

Hardwired MAC

- Two 256-byte circular FIFOs
- FIFO management
- AES-128 Engine
- CRC-16 Computation and Check

8051-Compatible Microcontroller

- 8051 Compatible(single cycle execution)
- 96KB Embedded Flash Memory

- 8KB Data Memory
- 128-byte CPU dedicated Memory
- 1KB Boot ROM
- Dual DPTR Support
- Multi-Bank Support for 96KB Program Memory(3Banks)
- I2S/PCM Interface with two128-byte FIFOs
- μ-law/a-law/ADPCM Voice Codec
- Two High-Speed UARTs with Two 16-byte FIFOs (up to 1Mbps)
- 4 Timers/2 PWMs
- Watchdog Timer
- Sleep Timer
- Quadrature Signal Decoder
- 24 General Purpose I/Os(MG2450 / MG2450A) / 22 General Purpose I/Os(MG2455 / MG2455A)
- Internal RC oscillator for Sleep Timer
- On-chip Power-on-Reset
- 4-channel 12-bit ADC (ENOB > 8-bit)
- SPI Master/Slave Interface
- ISP (In System Programming)
- Internal Temperature Sensor

Clock Inputs

- 16MHz Crystal for System Clock(optional 19.2MHz)
- 32.768kHz Oscillator for Sleep Timer(optional)

Power

- When using Internal Regulator of MG245X
  1.5V(Core)/1.9~3.3V(I/O) Operation
- When NOT using Internal Regulator of MG245X
  1.5V(Core)/1.5V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode Support
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Power Supply Range for Internal Regulator(1.9V(Min) ~ 3.6V(Max))
- Battery Monitoring Support

Package

- MG2450/MG2450A: Lead-Free 72-ball VFBGA Package (5mm × 5mm x 0.9mm)
- MG2455/MG2455A: Lead-Free 48-pin QFN Package (7mm x 7mm x 0.9mm)

5. PIN DESCRIPTION

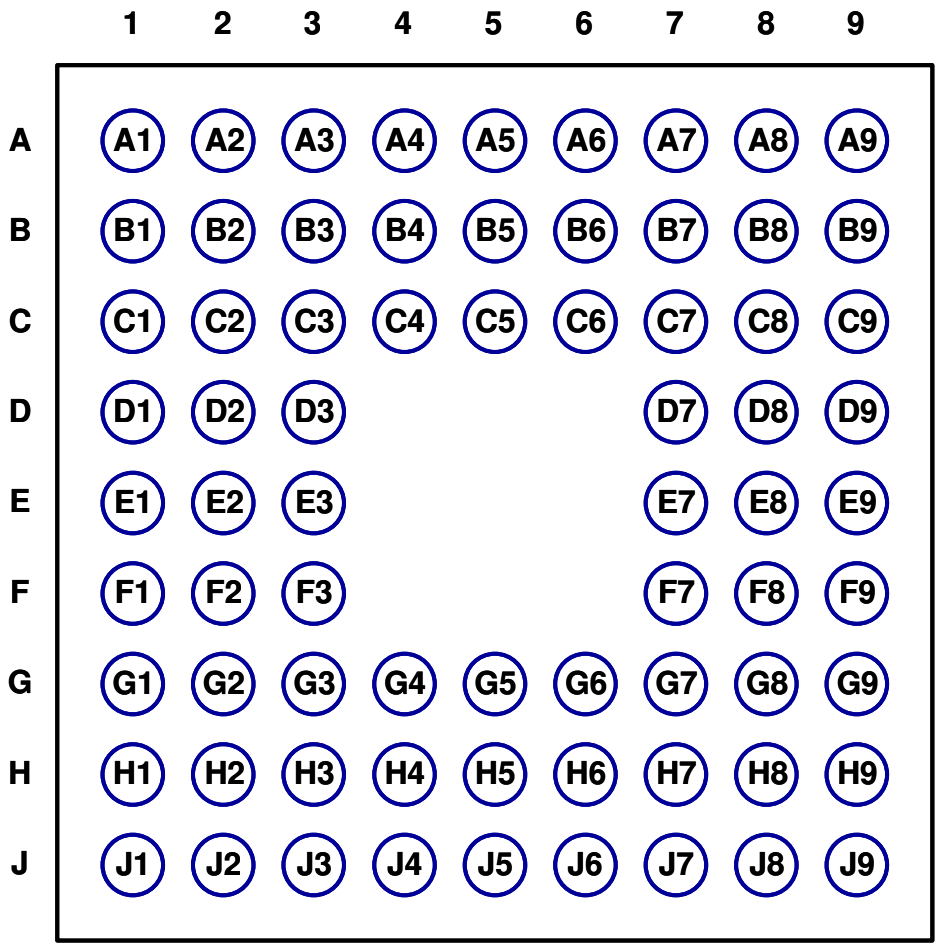

Figure 1. Pinout top view(1) of MG2450-B72 and MG2450-B72A(72-ball VFBGA Package)

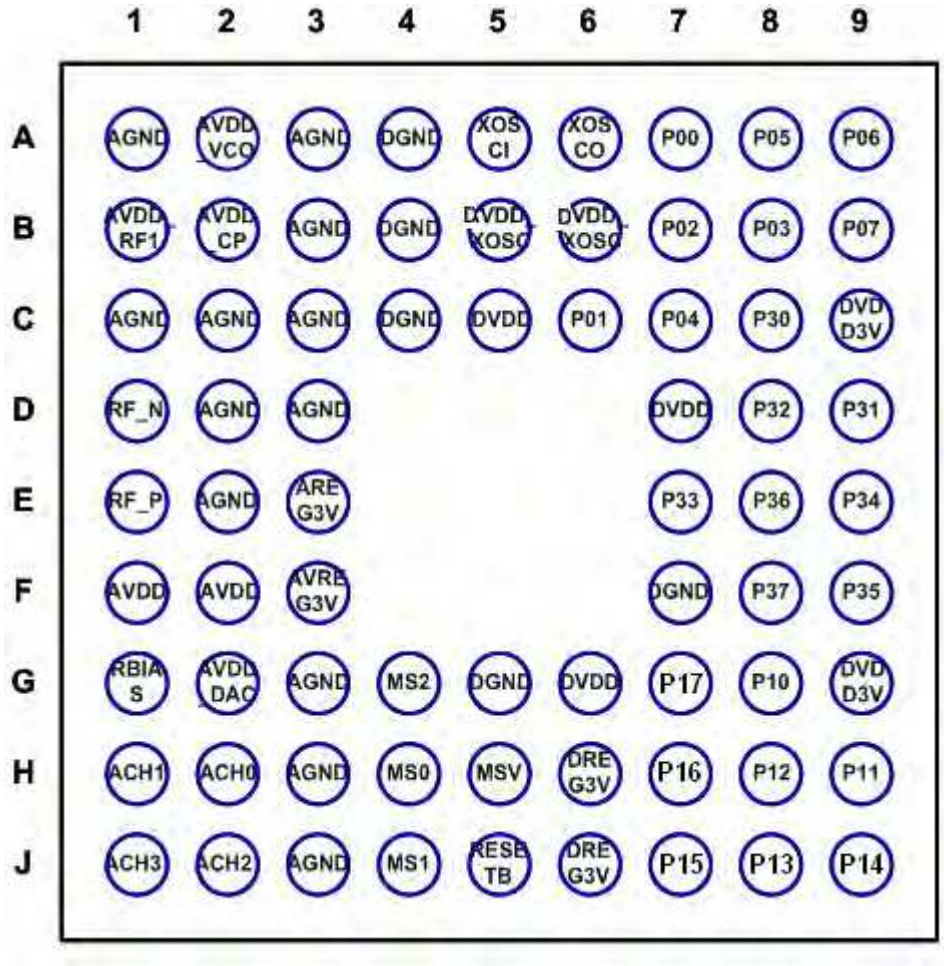

Figure 2. Pinout top view(2) of MG2450-B72 and MG2450-B72A(72-ball VFBGA Package)

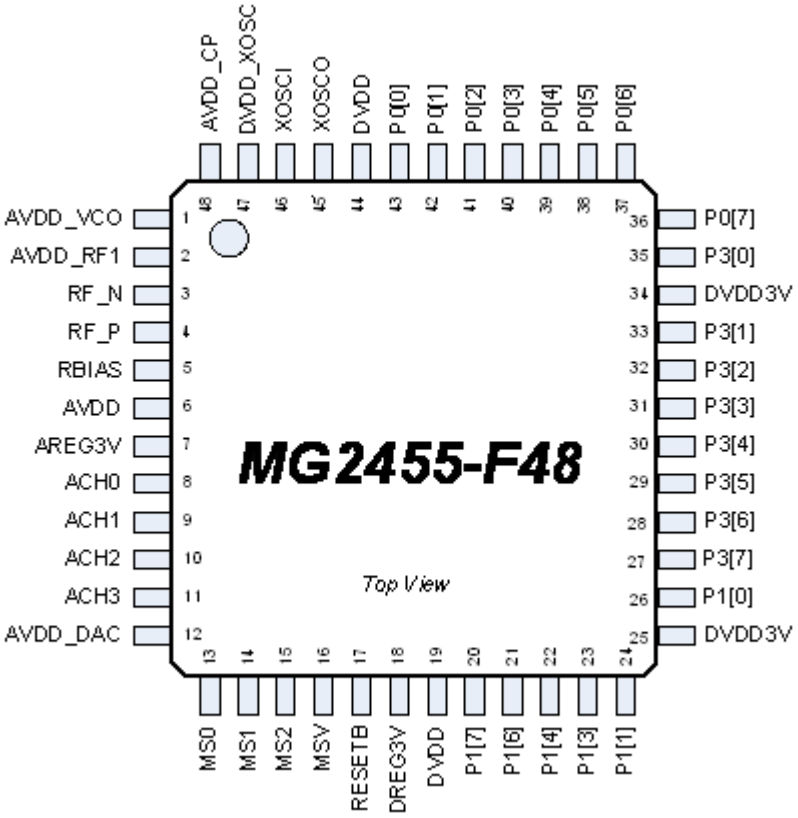

Figure 3. Pinout top view of MG2455-F48 and MG2455-F48A

(Exposed Pad 48-pin QFN Package)

** Chip Ground(GND) is located at the bottom of a chip*

The Pinout overview of MG2450 and MG2450A is shown in [Table 1].

Table 1. Pinout overview of MG2450/MG2450A

Ball	Ball Name	Ball Type	Ball Description
A1	AGND	Ground	Ground for RF and Analog blocks.
A2	AVDD_VCO	Power	1.5V Power supply for VCO and Divider
A3	AGND	Ground	Ground for RF and Analog blocks.
A4	DGND	Ground	Ground for digital core and IO.
A5	XOSCI	Analog	Crystal Oscillator Input.
A6	XOSCO	Analog	Crystal Oscillator Output.
A7	P0[0]	B (digital)	Port P0.0 / I2SRX_DI.
A8	P0[5]	B (digital)	Port P0.5 / I2STX_LRCLK.
A9	P0[6]	B (digital)	Port P0.6 / I2STX_BCLK.
B1	AVDD_RF1	Power	1.5V Power supply for LNA and PA.
B2	AVDD_CP	Power	1.5V Power supply for Charge Pump and PFD.
B3	AGND	Ground	Ground for RF and Analog blocks.
B4	DGND	Ground	Ground for digital core and IO.
B5	DVDD_XOSC	Power	1.5V Power supply for Crystal oscillator.
B6			
B7	P0[2]	B (digital)	Port P0.2 / I2SRX_BCLK.
B8	P0[3]	B (digital)	Port P0.3 / I2SRX_MCLK.
B9	P0[7]	B (digital)	Port P0.7 / I2STX_MCLK.
C1	AGND	Ground	Ground for RF and Analog blocks.
C2	AGND	Ground	Ground for RF and Analog blocks.
C3	AGND	Ground	Ground for RF and Analog blocks.
C4	DGND	Ground	Ground for digital core and IO.
C5	DVDD	Power	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V

		(In/Out)	Power supply for Digital Core(input mode @ No REG).
C6	P0[1]	B (digital)	Port P0.1 / I2SRX_LRCK.
C7	P0[4]	B (digital)	Port P0.4 / I2STX_DO.
C8	P3[0]	B (digital)	Port P3.0 / RXD0 / QUADXA.
C9	DVDD3V	Power	3.0V Power supply for Digital IO.
D1	RF_N	RF	Negative RF input/output signal to LNA / from PA in receive / transmit mode. It should be biased by AVDD_15. Refer to Sec.6.
D2	AGND	Ground	Ground for RF and Analog blocks.
D3	AGND	Ground	Ground for RF and Analog blocks.
D7	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG).
D8	P3[2]	B (digital)	Port P3.2 / INT0 (active low).
D9	P3[1]	B (digital)	Port P3.1 / TXD0 / QUADXB.
E1	RF_P	RF	Positive RF input/output signal to LNA / from PA in receive / transmit mode. It should be biased by AVDD_15. Refer to Sec.6.
E2	AGND	Ground	Ground for RF and Analog blocks.
E3	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator.
E7	P3[3]	B (digital)	Port P3.3 / INT1 (active low).
E8	P3[6]	B (digital)	Port P3.6 / 12mA Drive capability /PWM2/RTS1/SPICLK.
E9	P3[4]	B (digital)	Port P3.4 /T0/RTS0/QUADYA/SPIDI.
F1	AVDD	Power (In/Out)	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V Power supply for Mixer, VGA and LPF (input mode @ No REG).
F2	AVDD	Power	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V

		(In/Out)	Power supply for Mixer, VGA and LPF (input mode @ No REG).
F3	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator.
F7	DGND	Ground	Ground for digital core and IO.
F8	P3[7]	B (digital)	Port P3.7 / 12mA Drive capability /PWM3 /CTS1/SPICSN(slave only).
F9	P3[5]	B (digital)	Port P3.5 /T1/CTS0/QUADYB/SPIDO.
G1	RBIAS	Analog	External bias resistor.
G2	AVDD_DAC	Power	1.5V Power supply for ADC and DAC.
G3	AGND	Ground	Ground for RF and Analog blocks.
G4	MS[2]	I (digital)	MS[2:0](Mode Select) 000:Normal Mode 100:ISP Mode
G5	DGND	Ground	Ground for digital core and IO.
G6	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG).
G7	P1[7]	O (digital)	Port P1.7 GPO / P0AND/ TRSW / Fold / Clocks / BIST Fail Indicator.
G8	P1[0]	B (digital)	Port P1.0 / RXD1.
G9	DVDD3V	Power	3.0V Power supply for Digital IO.
H1	ACH1	Analog	Sensor ADC input
H2	ACH0	Analog	Sensor ADC input.
H3	AGND	Ground	Ground for RF and Analog blocks.
H4	MS[0]	I (digital)	MS[2:0](Mode Select) 000:Normal Mode 100:ISP Mode
H5	MSV	I (digital)	Mode Select of Voltage.
H6	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator.
H7	P1[6]	B	Port P1.6 / TRSWB.

		(digital)	
H8	P1[2]	B (digital)	Port P1.2 / RTCLKOUT.
H9	P1[1]	B (digital)	Port P1.1 / TXD1.
J1	ACH3	Analog	Sensor ADC input
J2	ACH2	Analog	Sensor ADC input.
J3	AGND	Ground	Ground for RF and Analog blocks.
J4	MS[1]	I (digital)	MS[2:0](Mode Select) 000:Normal Mode 100:ISP Mode
J5	RESETB	I (digital)	Reset (Active Low).
J6	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator.
J7	P1[5]	B (digital)	Port P1.5.
J8	P1[3]	B (digital)	Port P1.3 / QUADZA.
J9	P1[4]	B (digital)	Port P1.4 / QUADZB / Sleep Timer OSC Input.

The Pinout overview of MG2455 and MG2455A is shown in [Table 2].

Table 2. Pinout overview of MG2455/MG2455A

Pin NO.	Pin Name	Pin Type	Pin Description
Exposed bottom	GND	Ground	Ground for RF, Analog, digital core, and IO
1	AVDD_VCO	Power	1.5V Power supply for VCO and Divider
2	AVDD_RF1	Power	1.5V Power supply for LNA and PA
3	RF_N	RF	Negative RF input/output signal to LNA / from PA in receive / transmit mode. It should be biased by AVDD_15. Refer to Sec.6.
4	RF_P	RF	Positive RF input/output signal to LNA / from PA in receive /

			transmit mode. It should be biased by AVDD_15. Refer to Sec.6.
5	RBIAS	Analog	External bias resistor
6	AVDD	Power (In/Out)	Output of Analog Internal Voltage Regulator (1.5V) / 1.5V Power supply for Mixer, VGA, and LPF (input mode @ No REG)
7	AVREG3V	Power	3.0V Power supply for Analog Internal Voltage Regulator
8	ACH0	Analog	Sensor ADC input
9	ACH1	Analog	Sensor ADC input
10	ACH2	Analog	Sensor ADC input
11	ACH3	Analog	Sensor ADC input
12	AVDD_DAC	Power	1.5V Power supply for ADC and DAC
13	MS[0]	I (digital)	MS[2:0] (Mode Select) ▪ When using Internal Regulator of MG2455/MG2455A 000: Normal mode 100: ISP mode ▪ When NOT using Internal Regulator of MG2455/MG2455A 010: Normal mode 110: ISP mode
14	MS[1]	I (digital)	
15	MS[2]	I (digital)	
16	MSV	I (digital)	Mode Select of Voltage 0 – 1.5V
17	RESETB	I (digital)	Reset (Active Low)
18	DVREG3V	Power	3.0V Power supply for Internal Voltage Regulator
19	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG)
20	P1[7]	O (digital)	Port P1.7 GPO / P0AND / TRSW
21	P1[6]	B (digital)	Port P1.6 / TRSWB
22	P1[4]	B (digital)	Port P1.4 / QUADZB / Sleep Timer OSC Input
23	P1[3]	B (digital)	Port P1.3 / QUADZA
24	P1[1]	B	Port P1.1 / TXD1

		(digital)	
25	DVDD3V	Power	3.0V Power supply for Digital IO
26	P1[0]	B (digital)	Port P1.0 / RXD1
27	P3[7]	B (digital)	Port P3.7 / 12mA Drive capability / PWM3 / CTS1 / SPICSN
28	P3[6]	B (digital)	Port P3.6 / 12mA Drive capability /PWM2 / RTS1 / SPICLK
29	P3[5]	B (digital)	Port P3.5 / T1 / CTS0 / QUADYB / SPIDO
30	P3[4]	B (digital)	Port P3.4 / T0 / RTS0 / QUADYA / SPIDI
31	P3[3]	B (digital)	Port P3.3 / INT1 (active low)
32	P3[2]	B (digital)	Port P3.2 / INT0 (active low)
33	P3[1]	B (digital)	Port P3.1 / TXD0 / QUADXB
34	DVDD3V	Power	3.0V Power supply for Digital IO
35	P3[0]	B (digital)	Port P3.0 / RXD0 / QUADXA
36	P0[7]	B (digital)	Port P0.7 / I2STX_MCLK
37	P0[6]	B (digital)	Port P0.6 / I2STX_BCLK
38	P0[5]	B (digital)	Port P0.5 / I2STX_LRCLK
39	P0[4]	B (digital)	Port P0.4 / I2STX_DO
40	P0[3]	B (digital)	Port P0.3 / I2SRX_MCLK
41	P0[2]	B (digital)	Port P0.2 / I2SRX_BCLK
42	P0[1]	B	Port P0.1 / I2SRX_LRCK

		(digital)	
43	P0[0]	B (digital)	Port P0.0 / I2SRX_DI
44	DVDD	Power (In/Out)	Output of Digital Internal Voltage Regulator (1.5V) / 1.5V Power supply for Digital Core(input mode @ No REG)
45	XOSCO	Analog	Crystal Oscillator Output
46	XOSCI	Analog	Crystal Oscillator Input
47	DVDD_XOSC	Power	1.5V Power supply for Crystal oscillator.
48	AVDD_CP	Power	1.5V Power supply for Charge Pump and PFD

6. APPLICATION CIRCUITS

The MG245X operates from a single supply voltage. The core must run at 1.5V, so, if 1.5V is available, both the core and the I/O can run from 1.5V. If a higher voltage I/O is required (or higher voltage is available on the board) the MG245X contains an on-chip voltage regulator that can step down a 1.9V~3.3V supply to 1.5V for the core. In this case the I/O can be run from a 1.9V to 3.3V supply.

A typical application circuit for the MG245X using 1.9V~3.3V as the I/O power through the internal regulator is shown in [Figure 4, 5].

Typical value and description of external components are shown in [Table 3, 4] below.

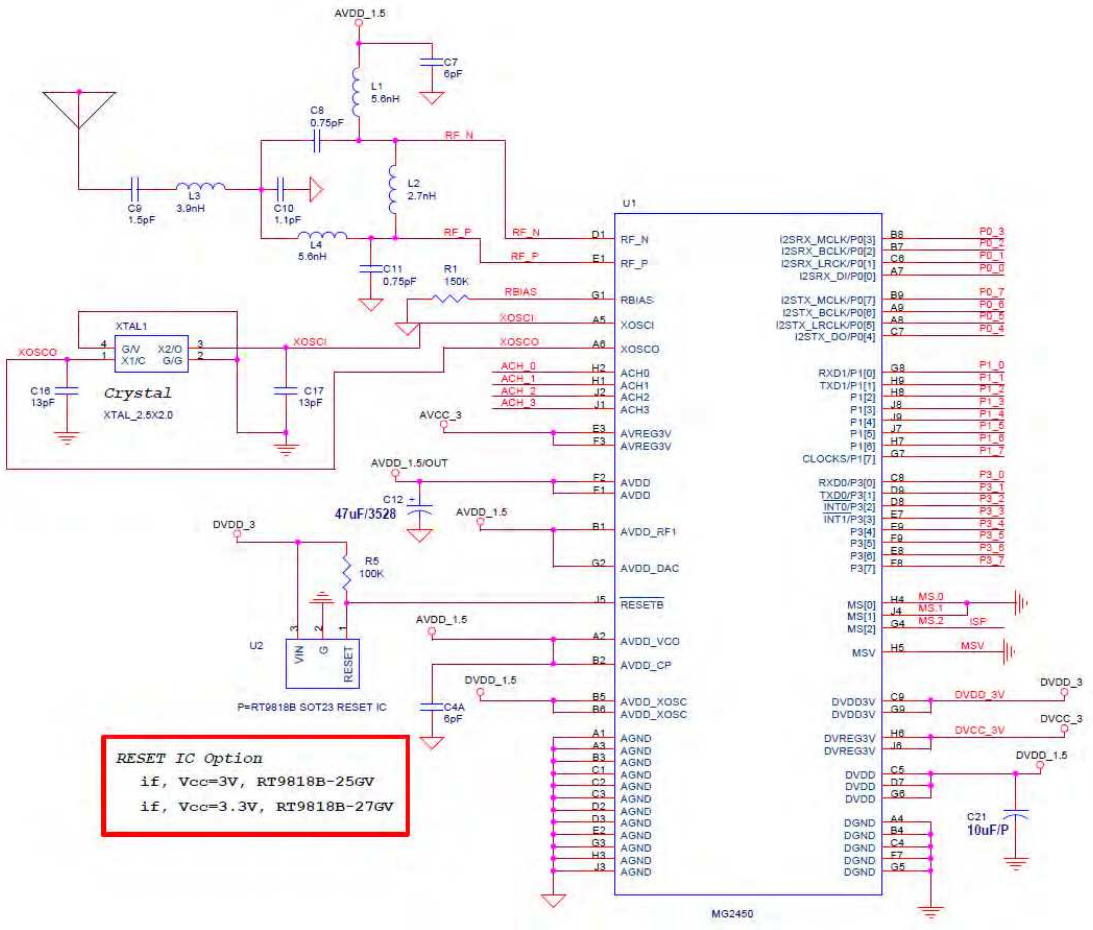

Figure 4. MG2450/MG2450A Application Circuit (I/O Power: 1.9V~3.3V , MS[1]=0)