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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

[MG2460] Datasheet

(No. ADS0601)

V1.1

REVISION HISTORY

Version	Date	Description
V1.0	2014.12.31	▪ First version release.
V1.1	2015.03.12	▪ Section 9.21 always-on register addresses are changed.

CONTENTS

FIGURES

TABLES

1. INTRODUCTION

The MG2460 is a 2.4GHz system-on-chip (SoC) compliant to IEEE 802.15.4 and ZigBee. The MG2460 integrates a high performance transceiver, a hardwired MAC with AES-128 engine, an accelerated 80251 MCU with internal 128-KB flash memory and 16-KB SRAM, and application-specific peripherals.

The transceiver operates in the 2.4~2.4835 GHz ISM band, with Tx output power up to +9 dBm, Rx sensitivity of -98 dBm and excellent coexistence with 802.11 WLAN. It supports high data rates, 1 Mbps and 2 Mbps, besides standard specific data rate of 250 kbps. In addition, it can also support channel coding for robust data communications.

The internal 80251 is an enhanced version of the standard 8051 with 16-bit and 32-bit capability. With 16KB SRAM data memory, numerous general-purpose I/O pins and peripheral devices such as timer and UART, the MG2460 can provide best programmability for wide-range of applications.

In addition, for special applications including sensor network, voice, LED lighting control, and remote controller, the MG2460 integrates application specific functions; a 12-bit four channel ADC is for sensor network application, voice encoder/decoder of ADPCM and μ/a-law are embedded for voice application, a 5 channel PWM (pulse width modulator) is for LED lighting control, and programmable IR (infrared) modulator is for remote controller application.

1.1. APPLICATIONS

- 2.4 GHz IEEE 802.15.4 Applications
- RF4CE Remote Control Systems
- Lighting Systems
- Voice Applications
- Home/Building Automation
- Industrial Control and Monitoring
- Energy Management
- Low Power Wireless Sensor Networks
- Consumer Electronics
- Health-care equipment
- Toys

2. KEY FEATURES

RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Low Power Consumption
- High Sensitivity of –98 dBm at 250kbps
- No External T/R Switch or Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9 dBm
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- Supports High Data Rates, 1 Mbps and 2 Mbps, besides 250Kbps specified in IEEE802.15.4
- RSSI Measurement
- Compliant to IEEE802.15.4

Hardwired MAC

- Two 256-byte circular FIFOs
- FIFO management
- AES Encryption/Decryption Engine(128 bit)
- CRC-16 Computation and Check

80251-Compatible MCU

- Accelerated 80251 core
- 128KB Embedded Flash Memory
- 16KB Data Memory
- 256-byte CPU dedicated Memory
- 1KB Boot ROM
- I2S/PCM Interface with two 256-byte FIFOs
- µ-law/a-law/ADPCM Voice Encoder/Decoder
- Two High-Speed UARTs with Two 256-byte FIFOs(up to 1Mbps)
- Four Timer/Counters
- 5 PWM channels
- Watchdog Timer
- Sleep Timer using the 32kHz RC-OSC clock
- Quadrature Signal Decoder
- 29 General Purpose I/Os for MG2460
- Internal 32kHz RC oscillator for Sleep Timer
- 16 MHz High Speed RC oscillator for the fast start-up from reset & power-down mode
- On-chip Power-on-Reset and Brown-out detector
- 4-channel 12-bit ADC(ENOB > 10-bit)
- SPI Master/Slave Interface with two 128-byte FIFOs
- I2C Master/Slave with 16-byte FIFO
- Programmable IR(Infra-Red) Modulator
- ISP (In System Programming)
- External clock output function(500KHz, 1/2/4/8/16/32 MHz selectable)

Clock Inputs

- 32MHz Crystal for System Clock

Power

- Power Supply Range for Internal Regulator(2.0V(Min) ~ 3.6V(Max))
- 2.0~3.6V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode
- Separate On-chip Regulators for Analog and Digital Circuitry.

Package

- Lead-Free 56-pin QFN Package (7mm x 7mm)

3. BLOCK DIAGRAM

[Figure 1] shows the block diagram of MG2460. The MG2460 consists of a 2.4GHz RF, a baseband PHY, a MAC hardware engine, an industry-standard enhanced 80251 MCU, an in-system programmable flash memory 128KB, a 16KB data RAM, and rich peripherals such as a voice encoder/decoder block, I2C, 5-channel PWM.

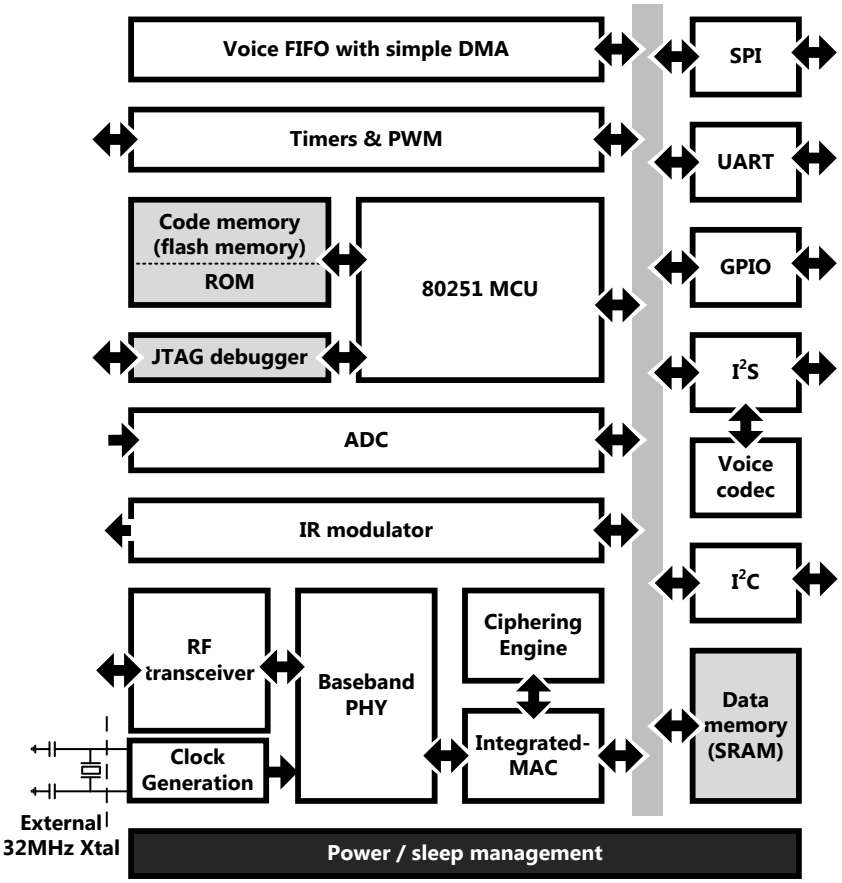


Figure 1. Functional Block Diagram of MG2460

MG2460 integrates an RF transceiver compliant to IEEE802.15.4 RF. The RF transceiver operates in an ISM band of 2.4 ~ 2.48GHz with excellent receiver sensitivity and programmable output power up to +9 dBm.

The MAC block supports IEEE802.15.4 compliant functions and it is located between the microprocessor and the baseband modem. MAC block includes FIFOs for transmitting/receiving packets, an AES engine for security operation, a CRC and related control circuit. In addition, it supports automatic CRC check and address decoding.

MG2460 integrates a high performance embedded microcontroller, compatible to an Intel 80251 microcontroller in an instruction level. Its enhanced pipeline architecture provides a rise of processing speed an average of 2.0 X running at the same clock frequency as a standard 80251 and up to 30 times faster than a standard 8051.

The memory part of the embedded microcontroller consists of program memory and data memory. The data memory has 2 memory areas. For more detailed explanations, refer to Sec 7.3.3.Data Memory.

MG2460 includes 29 GPIOs and various peripheral circuits to aid in the development of the application circuit with an interrupt handler to control the peripherals. MG2460 uses 32MHz crystal oscillator for RF PLL and 8MHz clock generated from 32MHz in clock generator is used as the default clock of 80251 MCU subsystem. The clocks for MAC and a baseband modem are separately controlled by the internal clock and reset block.

MG2460 supports a voice function as follows; The data generated by an external ADC is inputted to the voice block via I2S interface. After the data is received via I2S, it is compressed by the voice encoder and stored in the Voice TXFIFO. Then the data in the Voice TXFIFO is transferred to the MAC TXFIFO and transmitted via PHY. On the other hand, the received data in the MAC RXFIFO is transferred to voice RXFIFO via DMA operation. Then the data in the Voice RXFIFO is decompressed in the internal voice decoder. After that, the decompressed data is transferred to the external DAC via I2S interface.

4. PIN DESCRIPTION

The pin-out diagram of MG2460 is shown in [Figure 2] below. The description for that is summarized in [Table 1].

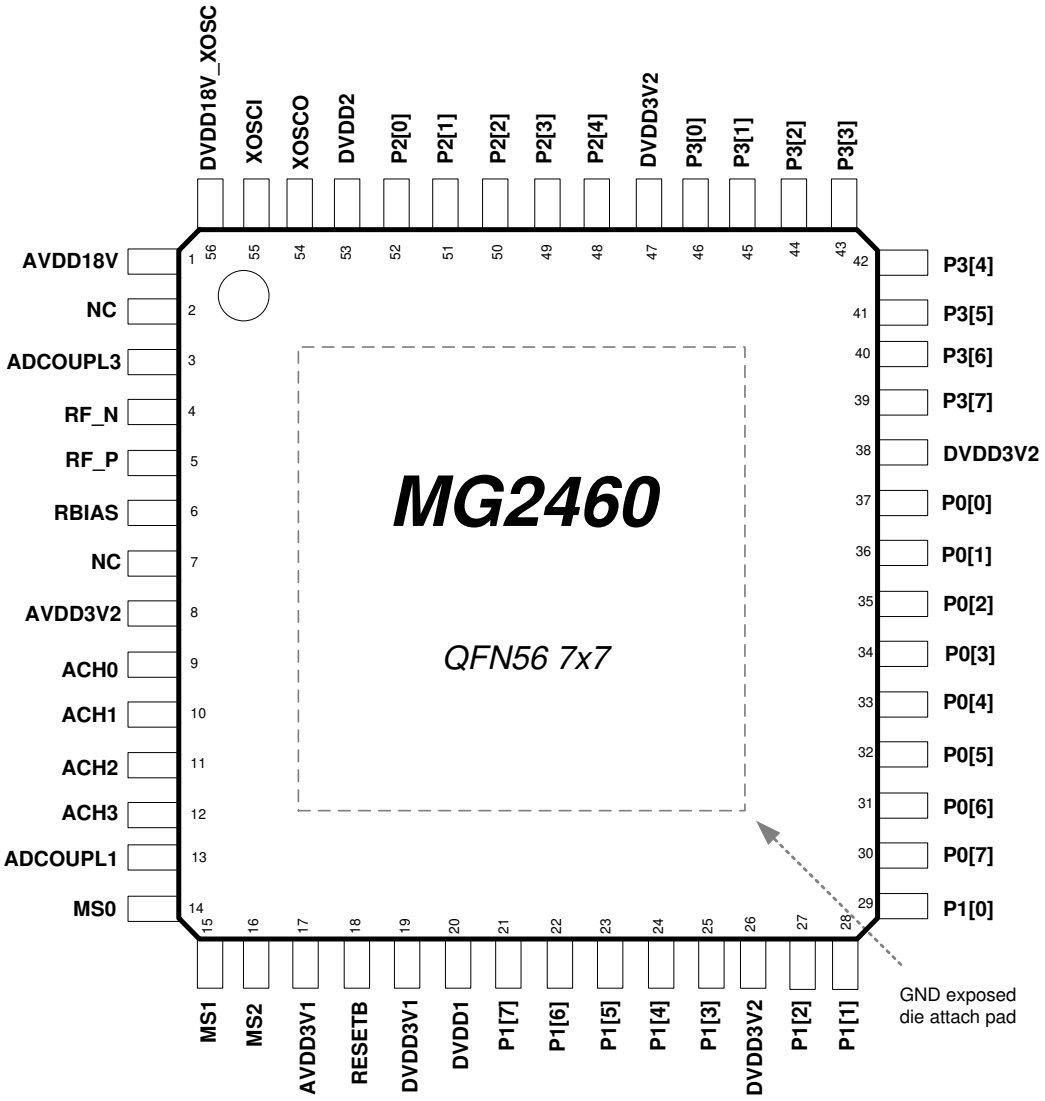


Figure 2. Pinout Top View of MG2460

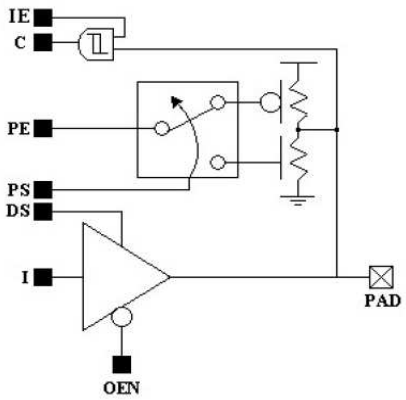
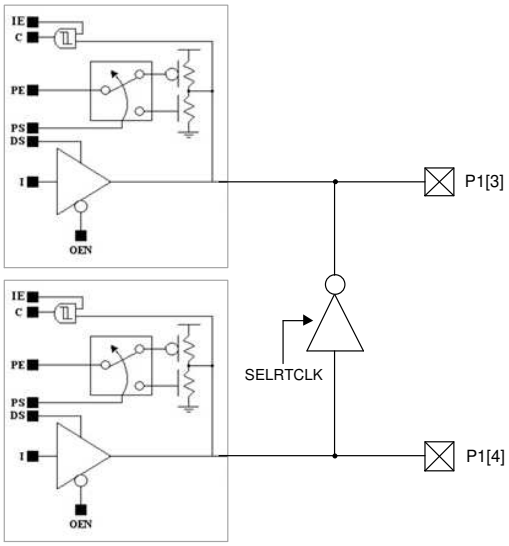
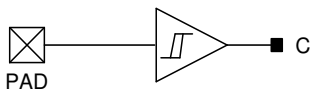
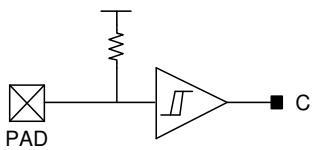
Note: *The exposed ground pad is located at the bottom of the chip and electrically connected to the die ground inside the package. It must be connected to a solid ground plane.*

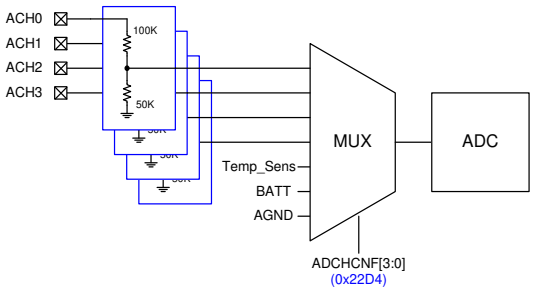
Table 1. Pin Description

Radio, Synthesizer, and Oscillator			
Pin	**Pin Name**	**Pin type**	**Pin Description**
17	AVDD3V1	Power	2.0V to 3.6V RF/Analog power supply connection
8	AVDD3V2	Power	2.0V to 3.6V RF/Analog power supply connection
13	ADCOUPL1	Power	1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits.
3	ADCOUPL3	Power	1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits.
1	AVDD18V	Power	1.8V RF/Analog power supply connection
5	RF_P	RF I/O	Positive RF input signal to LNA in RX mode Positive RF output signal from PA in TX mode It should be biased by ADCOUPL3. Refer to Figure 3(Sec. 6)
4	RF_N	RF I/O	Negative RF input signal to LNA in RX mode Negative RF output signal from PA in TX mode It should be biased by ADCOUPL3. Refer to Figure 3(Sec. 6)
6	RBIAS	Analog I/O	External precision bias resistor(510kohm) to generate the reference current
9	ACH0	Analog I/O	ADC input
10	ACH1	Analog I/O	ADC input
11	ACH2	Analog I/O	ADC input
12	ACH3	Analog I/O	ADC input
Digital and Oscillator			
Pin	**Pin Name**	**Pin type**	**Pin Description**
19	DVDD3V1	Power	2.0V to 3.6V Digital power supply connection
26,38,47	DVDD3V2	Power	2.0V to 3.6V Digital power supply connection
20	DVDD1	Power	1.8V Digital power supply decoupling. * Note: Do not use for supplying external circuits. *Note: It should not be connected together with DVDD2 (pin 53).
53	DVDD2	Power	1.8V Digital power supply decoupling. * Note: Do not use for supplying external circuits. *Note: It should not be connected together with DVDD1 (pin 20).
56	DVDD18V_XOSC	Power	1.8V digital power supply connection
14	MS[0]	I(digital)	MS[2:0] (Mode Select) **Value** / **Mode Configuration** 000 – Normal mode with internal digital regulator 100 – ISP mode with internal digital regulator Others – Reserved
15	MS[1]	I(digital)	
16	MS[2]	I(digital)	
18	RESETB	I(digital)	Reset(active low)
30	P0[7]	B (digital)	Port P0.7/I2STX_MCLK/PTC_GATE2

31	P0[6]	B (digital)	Port P0.6/I2STX_BCLK/PTC_GATE1
32	P0[5]	B (digital)	Port P0.5/I2STX_LRCLK/PTC_GATE0
33	P0[4]	B (digital)	Port P0.4/I2STX_DO/PWM4, 16mA drive capability
34	P0[3]	B (digital)	Port P0.3/I2SRX_MCLK/PWM3, 16mA drive capability
35	P0[2]	B (digital)	Port P0.2/I2SRX_BCLK/PWM2, 16mA drive capability
36	P0[1]	B (digital)	Port P0.1/I2SRX_LRCLK/PWM1, 16mA drive capability
37	P0[0]	B (digital)	Port P0.0/I2SRX_DI/PWM0, 16mA drive capability
21	P1[7]	B (digital)	Port P1.7 / I2C_SDA/TRSW
22	P1[6]	B (digital)	Port P1.6 / I2C_SCL/TRSWB
23	P1[5]	B (digital)	Port P1.5
24	P1[4]	B (digital)	Port P1.4/QUADZB/EXT_RTC_CLK/PTC_GATE4/XOSC32K_IN
25	P1[3]	B (digital)	Port P1.3/QUADZA/PTC_GATE3/IR_TX/CLK_OUT/XOSC32K_OUT
27	P1[2]	B (digital)	Port P1.2
28	P1[1]	B (digital)	Port P1.1/TXD1
29	P1[0]	B (digital)	Port P1.0/RXD1
39	P3[7]	B (digital)	Port P3.7/CTS1/SPICSN
40	P3[6]	B (digital)	Port P3.6/RTS1/SPICLK
41	P3[5]	B (digital)	Port P3.5/CTS0/QUADYB/SPIDO/T1
42	P3[4]	B (digital)	Port P3.4/RTS0/QUADYA/SPIDI/T0
43	P3[3]	B (digital)	Port P3.3/nINT1
44	P3[2]	B (digital)	Port P3.2/nINT0
45	P3[1]	B (digital)	Port P3.1/TXD0/QUADXB
46	P3[0]	B (digital)	Port P3.0/RXD0/QUADXA
48	P2[4]	I(digital)	JTAG Reset, active low, Port P2.4
49	P2[3]	I(digital)	JTAG clock, Port P2.3
50	P2[2]	I(digital)	JTAG mode select, Port P2.2
51	P2[1]	I(digital)	JTAG Data Input, Port P2.1
52	P2[0]	O(digital)	JTAG Data Output, Port P2.0
54	XOSCO	Analog I/O	32MHz crystal oscillator pin or external clock input
55	XOSCI	Analog I/O	32MHz crystal oscillator pin
Ground			
Pin	**Pin Name**	**Pin type**	**Pin Description**
Exposed bottom	GND	Ground	Ground for RF, Analog, digital core, and IO

Table 2. I/O Pins Equivalent Circuit Summary

Equivalent Circuit Schematic	Reset Status	Note
GPIO (P0[7:0], P1[7:0], P3[7:0], P2[4:0])		
	Input with pull-up	I/O with the programmable pull-up/pull-down function
GPIO with 32.768kHz crystal oscillator buffer (P1[4:3])		
	input with pull-up, crystal buffer disabled	Refer to Sec.8.18 (32.768kHz Crystal Oscillator).
MS[2],MS[1],MS[0]		
	Input	
RESETB		
	Input	
ACH0, ACH1, ACH2, ACH3		

	Analog Input	

5. ELECTRICAL CHARACTERISTICS

5.1. Absolute Maximum Ratings

Parameter		Min.	Max	Unit	
Supply Voltage (AVDD3V1,AVDD3V2,DVDD3V1,DVDD3V2)		-0.3	3.6	V	All supply pins must have the same voltage.
Voltage on any Digital Pin					
Storage Temperature		-40	150	℃	
ESD	HBM		2	kV	All pads, according to human-body model(JEDEC STD 22)
	CDM		500	V	According to charged-device model(JEDEC STD 22)

Exceeding one or more of these ratings may cause permanent damage to the device.
These are stress ratings only, and the functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL SPECIFICATIONS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: These values were obtained under worst-case test conditions specially prepared for the MG2460 and these conditions are not sustained in normal operation environment.

CAUTION: *ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.*

5.2. Recommended Operating Conditions

Parameter	MIN	MAX	UNIT
Operating ambient temperature range, T_{OP}	-40	85	℃
Operating supply voltage, VDD (AVDD3V1,AVDD3V2,DVDD3V1,DVDD3V2)	2.0	3.6	V
Voltage on any digital pin	-0.3	VDD	V

5.3. DC Characteristics

All voltage values are based on Ground.

Parameter		MIN	TYP	MAX	UNIT
VDD Operating Supply Voltage	VDD=3.30V VDD=3.00V VDD=2.56V VDD=2.20V	3.00 2.70 2.30 2.00		3.60 3.30 2.82 2.42	V
V_{IH} Logic-high Input Voltage	VDD=3.30V	2.10 1.90		3.60 3.30	V

	VDD=3.00V VDD=2.56V VDD=2.20V	1.70 1.50		2.82 2.42	
V_{IL}	Logic-low Input Voltage VDD=3.30V VDD=3.00V VDD=2.56V VDD=2.20V	 -0.3 -0.3 -0.3 -0.3		 0.8 0.7 0.6 0.5	V
R_{PU}	Pull-up Resistor VDD=3.30V VDD=3.00V VDD=2.56V VDD=2.20V	 34K 37K 44K 53K	48K 54K 66K 81K	72K 82K 101K 125K	Ω
R_{PD}	Pull-down Resistor VDD=3.30V VDD=3.00V VDD=2.56V VDD=2.20V	 28K 30K 33K 39K	47K 51K 62K 76K	90K 102K 128K 161K	Ω
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	VDD*0.73			V
I_{OL}	Low-level Output Current @V_{OL}(max)[1] VDD=3.30V (DS=0) VDD=3.00V (DS=0) VDD=2.56V (DS=0) VDD=2.20V (DS=0) VDD=3.30V (DS=1) VDD=3.00V (DS=1) VDD=2.56V (DS=1) VDD=2.20V (DS=1)	 6.3 5.7 4.8 3.9 9.5 8.6 7.2 5.9			mA
I_{OH}	High-level Output Current @V_{OH}(min)[2] VDD=3.30V (DS=0) VDD=3.00V (DS=0) VDD=2.56V (DS=0) VDD=2.20V (DS=0) VDD=3.30V (DS=1) VDD=3.00V (DS=1) VDD=2.56V (DS=1) VDD=2.20V (DS=1)	 7.4 5.9 4.3 3.3 11.2 8.9 6.5 5.0			mA

[1] For P0[7:5], P1[7:0], P2[4:0] and P3[7:0] pins
[2] For P0[7:5], P1[7:0], P2[4:0] and P3[7:0] pins

5.4. Current Consumption and timing characteristics

Measured on 2-layer reference design with T_{OP} = 25°C, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
MCU active. No radio and peripherals (UART1&RNG) active. @ MCU clock = 8MHz		5.8		mA
RX mode , MCU active and peripherals (UART1&RNG) active		26.3		mA
TX mode , MCU active and peripherals (UART1&RNG) active @maximum output power @+0dBm		40.5 24		mA
Power mode1. Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off, 32kHz RCOSC, POR, BOD, and sleep timer active.		42.8		µA
Power mode2. Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32kHz RCOSC and sleep timer active.		1.0		µA
Power mode3. Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32kHz RCOSC and sleep timer off.		0.1		µA
Wake-up and timing				
Power mode1 → MCU Active Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of 16MHz RCOSC		110		µs
Power mode2 → MCU Active Digital regulator off, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of regulator and 16MHz RCOSC		280		µs
MCU Active → TX or RX (PM1) Initially running on 16MHz RCOSC, added start-up time of 32MHz crystal oscillator and PLL lock time.		922		µs
MCU Active → TX or RX (PM2) Initially running on 16MHz RCOSC, added modem initialization, dc calibration, PLL lock and MAC setting time.[3]		3000		us
TX/RX and RX/TX turnaround			192	µs

5.5. RF Receive Section

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range (channel center frequency)[4]	2405		2480	MHz
Maximum input level (PER=1%) @ 250kbps		1		dBm

[3] In PM2 digital regulator is off, so all settings needed for chip operation is cleared. Thus, additional chip initialization time is needed.

[4] Extended range: 2394~2507MHz

Spurious radiation @30MHz-1000MHz @1GHz-12.75GHz		 -65 -65		dBm
Received RF bandwidth		2		MHz
Channel spacing[5]		5		MHz
Receiver sensitivity (PER≤1%, packet length of 20-byte) @ 250kbps		-98		dBm
Adjacent channel rejection (-82dB,adjacent modulated channel at ±5MHz, PER=1%, 250kbps) +5MHz -5MHz		 31 32		dB
Alternate channel rejection (-82dB, adjacent modulated channel at ±10MHz, PER=1%, 250kbps) +10MHz -10MHz		 51 51		dB
Others channel rejection (-82dB, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps) ≥+15MHz ≥-15MHz		 55 55		dB
Co-channel rejection (-82dB. Undesired IEEE 802.15.4 modulated signal at the same frequency. Signal level for PER=1%, 250kbps)		-6		dB
Blocking/desensitization +250MHz +100MHz +50MHz -50MHz -100MHz -250MHz		 -27 -31 -34 -32 -28 -22		dBm
RSSI dynamic range			90	dB
RSSI accuracy		± 3		dB

5.6. RF Transmit Section

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range(channel center frequency)[6]	2405		2480	MHz
TX output power (using the recommended matching circuit)		9		dBm

[5]Specified in IEEE Standard 802.15.4™

[6]Extended range: 2394~2507MHz

Transmit chip rate		2		Mcps
Error vector magnitude(EVM)		7		%
Harmonics 2nd harmonic 3rd harmonic		 -45 -45		dBm
Spurious emission (complies with EN 300-440, FCC and ARIB STD-T66) 30Hz ~ 1GHz 1GHz ~ 12.75GHz 5.15GHZ ~ 5.3GHZ		 -60 -50 -50		dBm

5.7. Frequency Synthesizer

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier @ ±100kHz offset @ ±1MHz offset @ ±2MHz offset @ ±3MHz offset @ ±5MHz offset		 -77.5 -98.7 -110.3 -113.2 -115.6		dBc/Hz
Lock time		100	192	μs

5.8. 32MHz Crystal Oscillator

Measured on 2-layer reference design with T_{OP}=25℃, DXOSC18V=1.8V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Crystal frequency		32		MHz
Crystal frequency accuracy requirement	-40		40	ppm
Equivalent series resistance(ESR)		30[7]	60[8]	Ω
Crystal shunt capacitance(C_O)		3	5	pF
Crystal load capacitance(C_L)		9[6]	13[7]	pF
Start-up time			0.8	ms

[7] The negative resistance of driving circuit is five times larger than the ESR of crystal oscillator with crystal satisfying above TYP conditions.
[8] The negative resistance of driving circuit is two times larger than the ESR of crystal oscillator with crystal satisfying above MAX conditions.

5.9. 16MHz RC Oscillator

Measured on 2-layer reference design with T_{OP}=25℃, DXOSC18V=1.8V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Frequency		16		MHz
Frequency accuracy before calibration	-25		25	%
Frequency accuracy after calibration	-3		3	%
Initial calibration time		50		μs
Start-up time			1	μs

5.10. 32kHz RC Oscillator

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Calibrated frequency		32.787		kHz
frequency accuracy after calibration		0.3		%
Initial calibration time		1		ms
Start-up time			100	μs

5.11. 32.768kHz Crystal Oscillator

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Frequency		32.768		kHz
Crystal frequency accuracy requirement	-40		40	ppm
Equivalent series resistance(ESR)		50	100	kΩ
Crystal shunt capacitance(C_O)		0.9		pF
Crystal load capacitance(C_L)		12.5		pF
Start-up time		1.2		s

5.12. Temperature Sensor

Measured on 2-layer reference design with VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
output voltage at -40℃		-295		
output voltage at 25℃		76		
output voltage at 85℃		418		
temperature coefficient		5.703		/℃

All measurement results are obtained using the 12-bit ADC.

5.13. ADC

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Input voltage	0		VDD	V
Input resistance		150		kΩ
Full-scale signal			3	V
Effective number of bits(ENOB) Single-ended input, 12bit setting		10.8		bits
Signal to noise and distortion(SINAD) Single-ended input, 12bit setting		66.78		dB
Internal reference voltage		1.25		V
Current consumption		0.46		mA

5.14. Flash Memory

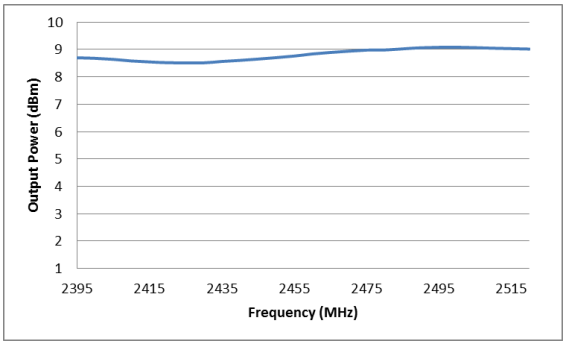
5.14.1. Flash memory characteristics

Characteristic	Symbol	Conditions	MIN	TYP	MAX	UNIT
Endurance	Nendu	20ms erase and 20 us program time at 1.8V	20,000			cycles
Data retention	Tret	25 °C	100			years

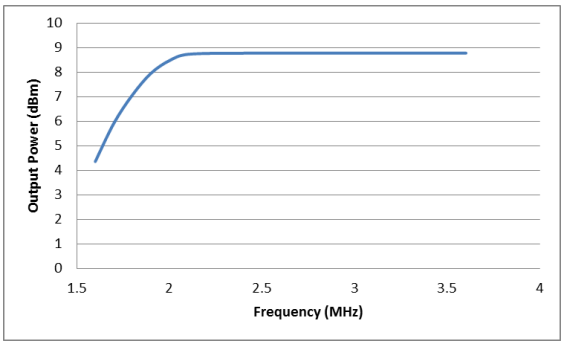
5.14.2. Flash memory and page size

Name	Size	Unit
Flash main memory block	131,072	bytes
Flash information block	1,024	bytes
Flash page size	512	bytes

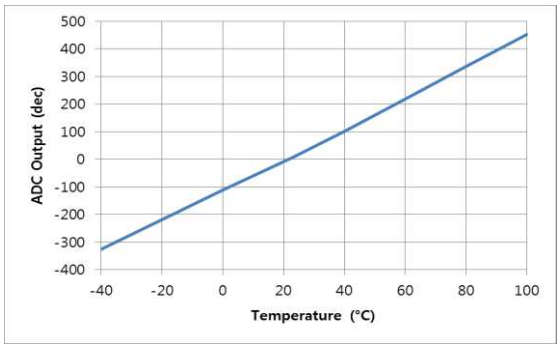
5.15. Typical Performance Curves



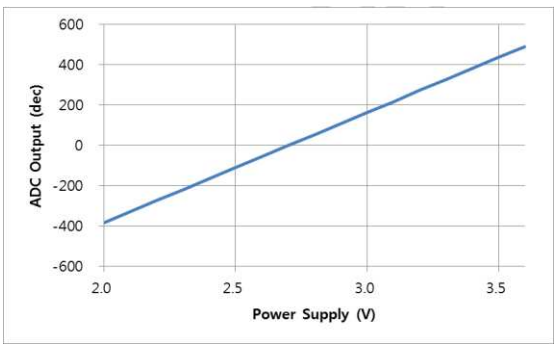
Output Power vs. Frequency



Power Supply vs. Output Power@2450 MHz



Temperature Sensor



Battery Monitor