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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

[MG2471] Datasheet

(No. ADS0901)

V1.2

REVISION HISTORY

Version	Date	Description
V1.0	2014.3.27	▪ The first version release.
V1.1	2014.5.9	▪ Updated Sec 8.15 ▪ Unified the abbreviations for Write-Only and Read-Only (WO: Write-Only, RO: Read-Only)
V1.2	2014.9.1	▪ Updated Sec 5.8, Crystal Oscillator parameters (TYP and MAX value for ESR, C_O and C_L) are updated. ▪ Table 3. Bill of Materials in Sec. 6 is updated. C_{11} and C_{12} is changed from 30pF to 13pF.

CONTENTS

FIGURES

TABLES

1. INTRODUCTION

MG2471 is a true 2.4 GHz system-on-chip (SOC) designed for low-power and low-cost applications based on IEEE802.15.4 and RF4CE. The MG2471 uses the ISM band of 2.4 ~ 2.48 GHz. In addition to the standard data-rate specified in IEEE802.15.4, enhanced multiple data-rate modes (31.25Kbps ~ 1Mbps) with channel coding are supported.

MG2471 combines an advanced RF transceiver with an industry-standard enhanced 8051 MCU, a baseband PHY, a MAC with AES-128 HW engine, an in-system programmable 64KB flash memory, a 6-KB RAM, and many other application-specific peripherals.
This chip is best for very low-power RF4CE remote control applications.

1.1. APPLICATIONS

- 2.4 GHz IEEE 802.15.4 Applications
- RF4CE Remote Control Systems
- Lighting Systems
- Home/Building Automation
- Industrial Control and Monitoring
- Energy Management
- Low Power Wireless Sensor Networks
- Consumer Electronics
- Health-care equipment
- Toys

2. KEY FEATURES

RF Transceiver

- Single-chip 2.4GHz RF Transceiver
- Low Power Consumption
- High Sensitivity of –98dBm at 250kbps
- No External T/R Switch or Filter needed
- On-chip VCO, LNA, and PA
- Programmable Output Power up to +9.0dBm
- Direct Sequence Spread Spectrum
- O-QPSK Modulation
- Scalable Data Rate including 250Kbps specified in IEEE802.15.4: 31.25Kbps ~ 1Mbps
- RSSI Measurement
- Compliant to IEEE802.15.4

Hardwired MAC

- Two 256-byte circular FIFOs
- FIFO management
- AES Encryption/Decryption Engine(128 bit)
- CRC-16 Computation and Check

8051-Compatible MCU

- 8051 Compatible (single cycle execution)
- 64KB Embedded Flash Memory
- 6KB Data Memory
- 128-byte CPU dedicated Memory
- 1KB Boot ROM
- Dual DPTR Support
- I2S/PCM Interface with two 256-byte FIFOs
- Two High-Speed UARTs with Two 16-byte FIFOs(up to 1Mbps)
- Four Timer/Counters
- 5 PWM channels
- Watchdog Timer
- Sleep Timer using the 32kHz RC-OSC clock
- Quadrature Signal Decoder
- 22 General Purpose I/Os
- Internal 32kHz RC oscillator for Sleep Timer
- 16 MHz RC oscillator for the fast start-up from reset & power-down mode
- On-chip Power-on-Reset and Brown-out detector
- 4-channel 12-bit ADC(ENOB > 10-bit)
- SPI Master/Slave Interface with two 16-byte FIFOs
- I2C Master/Slave with 16-byte FIFO
- Programmable IR(Infra-Red) Modulator
- ISP (In System Programming)
- External clock output function(500KHz, 1/2/4/8/16/32 MHz selectable)

Clock Inputs

- 32MHz Crystal for System Clock

Power

- 1.8V(Core)/2.0~3.6V(I/O) Operation
- Power Management Scheme with Deep Sleep Mode
- Separate On-chip Regulators for Analog and Digital Circuitry.
- Power Supply Range for Internal Regulator(2.0V(Min) ~ 3.6V(Max))

Package

- Lead-Free 48-pin QFN Package (7mm x 7mm)

3. BLOCK DIAGRAM

[Figure 1] shows the block diagram of MG2471. The MG2471 consists of a 2.4GHz RF, a baseband PHY, a MAC hardware engine, an industry-standard enhanced 8051 MCU, an in-system programmable flash memory 64KB, a 6KB data RAM, and rich peripherals such as I2C, 5-channel PWM.

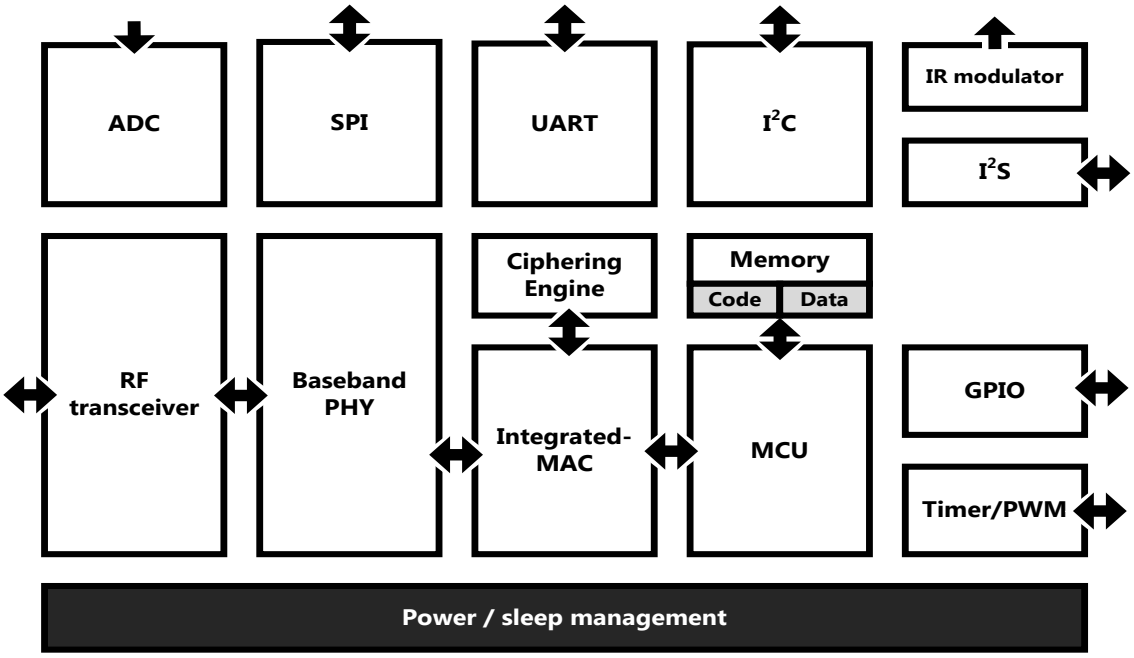


Figure 1. Functional Block Diagram of MG2471

MG2471 integrates an RF transceiver compliant to IEEE802.15.4 RF. The RF transceiver operates on an ISM band of 2.4 ~ 2.48GHz with excellent receiver sensitivity and programmable output power up to +8.8dBm.

The MAC block supports IEEE802.15.4 compliant functions and it is located between the microprocessor and the baseband modem. MAC block includes FIFOs for transmitting/receiving packets, an AES engine for security operation, a CRC and related control circuit. In addition, it supports automatic CRC check and address decoding.

MG2471 integrates a high performance embedded microcontroller, compatible to industry standard 8051 microcontroller in an instruction level. This embedded microcontroller has 8-bit operation architecture sufficient for controller applications. The embedded microcontroller has 4-stage pipeline architecture to improve the performance over previous compatible chips making it capable of executing simple instructions during a single cycle.

The memory part of the embedded microcontroller consists of program memory and data memory. The data memory has 2 memory areas. For more detailed explanations, refer to Sec 7.1.2. Data Memory.

MG2471 includes 22 GPIOs and various peripheral circuits to aid in the development of the application circuit with an interrupt handler to control the peripherals. MG2471 uses 32MHz

crystal oscillator for RF PLL and 8MHz clock generated from 32MHz in clock generator is used as the default clock of 8051 MCU subsystem. The clocks for MAC, a baseband modem are separately controlled by the internal clock and reset block.

4. PIN DESCRIPTION

The pin-out diagram of MG2471 is shown in [Figure 2] and the detailed description is in [Table 1].

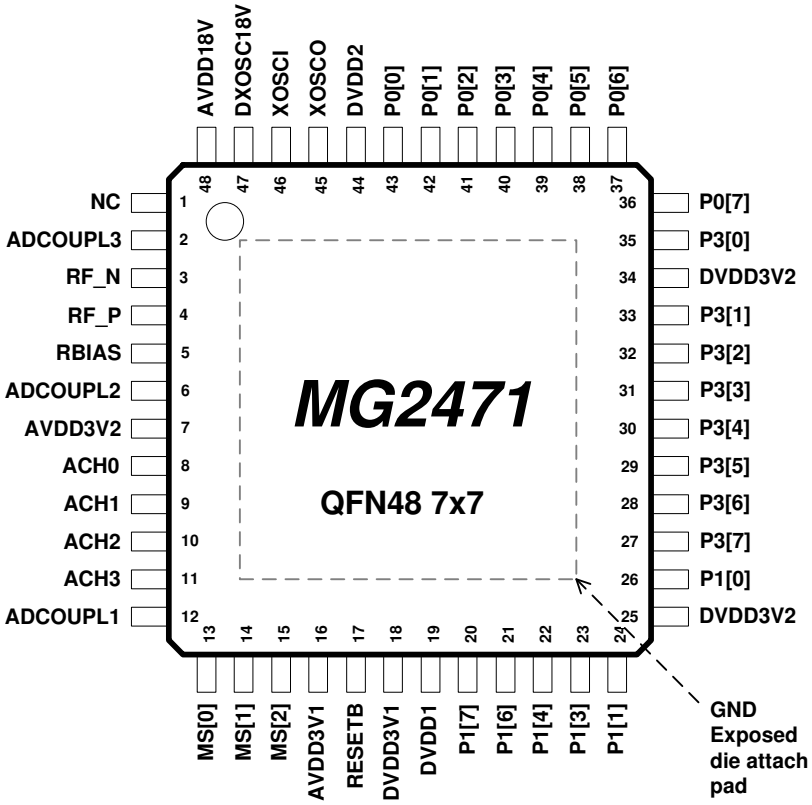


Figure 2. Pinout Top View of MG2471

Note: The exposed ground pad is located at the bottom of the chip and electrically connected to the die ground inside the package. It must be connected to a solid ground plane.

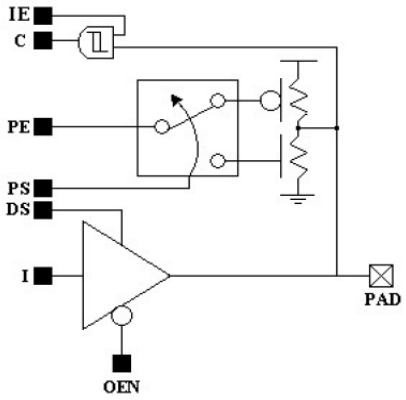
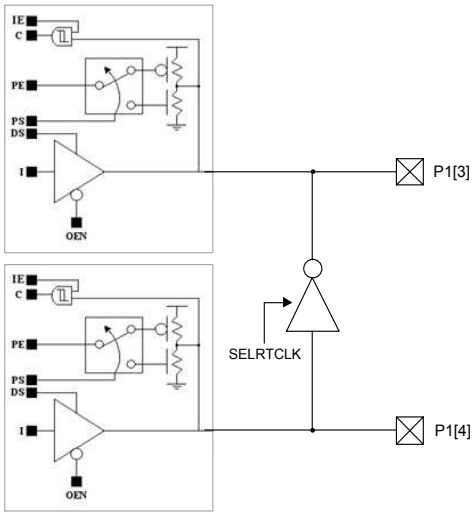
Table 1. Pin Description

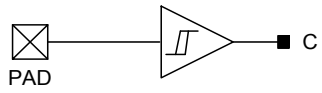
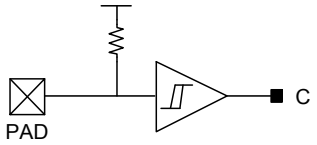
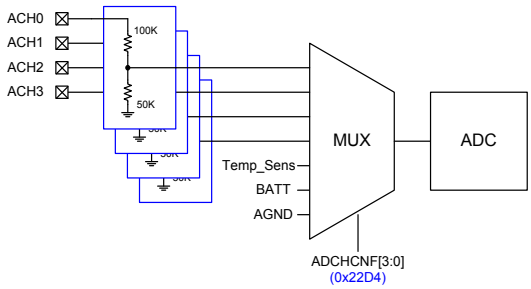
Radio, Synthesizer, and Oscillator			
Name	**Pin**	**Type**	**Description**
AVDD3V1	16	Power	2.0V to 3.6V RF/Analog power supply connection
AVDD3V2	7	Power	2.0V to 3.6V RF/Analog power supply connection
ADCOUPL1	12	Power	1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits.
ADCOUPL2	6	Power	1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits.
ADCOUPL3	2	Power	1.8V RF/Analog power supply decoupling. Do not use for supplying external circuits.
AVDD18V	48	Power	1.8V RF/Analog power supply connection
RF_P	4	RF I/O	Positive RF input signal to LNA in RX mode Positive RF output signal from PA in TX mode

			It should be biased by ADCOUPL3. Refer to [Figure 3] in Sec.6.
RF_N	3	RF I/O	Negative RF input signal to LNA in RX mode Negative RF output signal from PA in TX mode It should be biased by ADCOUPL3. Refer to [Figure 3] in Sec.6.
RBIAS	5	Analog I/O	External precision bias resistor(510kohm) to generate the reference current
ACH0	8	Analog I/O	ADC input
ACH1	9	Analog I/O	ADC input
ACH2	10	Analog I/O	ADC input
ACH3	11	Analog I/O	ADC input
Digital and Oscillator			
Name	**Pin**	**Type**	**Description**
DVDD3V1	18	Power	2.0V to 3.6V Digital power supply connection
DVDD3V2	25,34	Power	2.0V to 3.6V Digital power supply connection
DVDD1	19	Power	1.8V Digital power supply decoupling. *Note: Do not use for supplying external circuits. *Note: It should not be connected together with DVDD2 (pin 44).
DVDD2	44	Power	1.8V Digital power supply decoupling. *Note: Do not use for supplying external circuits. *Note: It should not be connected together with DVDD1 (pin 19).
DXOSC18V	47	Power	1.8V Digital power supply connection
RESETB	17	Digital input	Reset, active low
MS[0]	13	Digital input	Mode Selection Value / Mode Configuration 000 / Normal mode with internal digital regulator 100 / ISP mode with internal digital regulator others / Reserved
MS[1]	14	Digital input	
MS[2]	15	Digital input	
P0[0]	43	Digital I/O	Port P0.0/I2SRX_DI/PWM0, 16mA drive capability
P0[1]	42	Digital I/O	Port P0.1/I2SRX_LRCLK/PWM1, 16mA drive capability
P0[2]	41	Digital I/O	Port P0.2/I2SRX_BCLK/PWM2, 16mA drive capability
P0[3]	40	Digital I/O	Port P0.3/I2SRX_MCLK/PWM3, 16mA drive capability
P0[4]	39	Digital I/O	Port P0.4/I2STX_DO/PWM4, 16mA drive capability
P0[5]	38	Digital I/O	Port P0.5/I2STX_LRCLK/PTC_GATE0
P0[6]	37	Digital I/O	Port P0.6/I2STX_BCLK/PTC_GATE1
P0[7]	36	Digital I/O	Port P0.7/I2STX_MCLK/PTC_GATE2
P1[0]	26	Digital I/O	Port P1.0/RXD1
P1[1]	24	Digital I/O	Port P1.1/TXD1
P1[3]	23	Digital I/O	Port P1.3/QUADZA/PTC_GATE3/IR_TX/CLK_OUT /XOSC32K_OUT
P1[4]	22	Digital I/O	Port P1.4/QUADZB/EXT_RTC_CLK/PTC_GATE4 /XOSC32K_IN
P1[6]	21	Digital I/O	Port P1.6/I2C_SCL/TRSWB
P1[7]	20	Digital I/O	Port P1.7/I2C_SDA/TRSW

P3[0]	35	Digital I/O	Port P3.0/RXD0/QUADXA
P3[1]	33	Digital I/O	Port P3.1/TXD0/QUADXB
P3[2]	32	Digital I/O	Port P3.2/nINT0
P3[3]	31	Digital I/O	Port P3.3/nINT1
P3[4]	30	Digital I/O	Port P3.4/RTS0/QUADYA/SPIDI/T0
P3[5]	29	Digital I/O	Port P3.5/CTS0/QUADYB/SPIDO/T1
P3[6]	28	Digital I/O	Port P3.6/RTS1/SPICLK
P3[7]	27	Digital I/O	Port P3.7/CTS1/SPICSN
XOSCI	46	Analog I/O	32MHz crystal oscillator pin
XOSCO	45	Analog I/O	32MHz crystal oscillator pin or external clock input
NC	1		Do not connect.
Ground			
Exposed bottom		Ground	Ground for RF, Analog, digital core, and I/O

Table 2. I/O Pins Equivalent Circuit Summary

Equivalent Circuit Schematic	Reset Status	Note
GPIO (P0[7:0], P1[1:0], P1[7:6], P3[7:0])		
	Input with pull-up	I/O with the programmable pull-up/pull-down function
GPIO with 32.768kHz crystal oscillator buffer (P1[4:3])		
	input with pull-up, crystal buffer disabled	Refer to Sec.8.18 (32.768kHz Crystal Oscillator).
MS[2],MS[1],MS[0]		

	Input	
RESETB		
	Input	
ACH0, ACH1, ACH2, ACH3		
	Analog Input	

5. ELECTRICAL CHARACTERISTICS

5.1. Absolute Maximum Ratings

Parameter		Min.	Max	Unit	
Supply voltage(AVDD3V1,AVDD3V2, DVDD3V1,DVDD3V2)		-0.3	3.6	V	The voltage of all supply pins must be same.
Core voltage(ADCOUPL1,ADCOUPL2,ADCOUPL3,AVDD18V,DVDD1,DVDD2,DXOSC18V)		-0.3	2	V	
Storage Temperature		-40	150	°C	
ESD	HBM		2	kV	All pads, according to human-body model(JEDEC STD 22)
	CDM		500	V	According to charged-device model(JEDEC STD 22)

Exceeding one or more of these ratings may cause permanent damage to the device.
These are stress ratings only, and the functional operation of the device at these or any other conditions beyond those indicated under “ELECTRICAL SPECIFICATIONS” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: These values were obtained under worst-case test conditions specially prepared for the MG2471 and these conditions are not sustained in normal operation environment.

CAUTION: *ESD sensitive device. Precaution should be used when handling the device to prevent permanent damage.*

5.2. Recommended Operating Conditions

Parameter	MIN	MAX	UNIT
Operating ambient temperature range, T_{OP}	-40	85	℃
Operating supply voltage, VDD (AVDD3V1,AVDD3V2,DVDD3V1,DVDD3V2)	2	3.6	V
Voltage on any digital pin	-0.3	VDD	V

5.3. DC Characteristics

All voltage values are based on Ground.

Parameter		MIN	TYP	MAX	UNIT
VDD Operating Supply Voltage					
	VDD=3.30V	3.00		3.60	V
	VDD=3.00V	2.70		3.30	
	VDD=2.56V	2.30		2.82	
	VDD=2.20V	2.00		2.42	

V_{IH}	Logic-high Input Voltage				
	VDD=3.30V	2.10		3.60	V
	VDD=3.00V	1.90		3.30	
	VDD=2.56V	1.70		2.82	
	VDD=2.20V	1.50		2.42	
V_{IL}	Logic-low Input Voltage				
	VDD=3.30V	-0.3		0.8	V
	VDD=3.00V	-0.3		0.7	
	VDD=2.56V	-0.3		0.6	
	VDD=2.20V	-0.3		0.5	
R_{PU}	Pull-up Resistor				
	VDD=3.30V	34K	48K	72K	Ω
	VDD=3.00V	37K	54K	82K	
	VDD=2.56V	44K	66K	101K	
	VDD=2.20V	53K	81K	125K	
R_{PD}	Pull-down Resistor				
	VDD=3.30V	28K	47K	90K	Ω
	VDD=3.00V	30K	51K	102K	
	VDD=2.56V	33K	62K	128K	
	VDD=2.20V	39K	76K	161K	
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	VDD*0.73			V
I_{OL}	Low-level Output Current @V_{OL}(max)[1]				
	VDD=3.30V (DS=0)	6.3			mA
	VDD=3.00V (DS=0)	5.7			
	VDD=2.56V (DS=0)	4.8			
	VDD=2.20V (DS=0)	3.9			
	VDD=3.30V (DS=1)	9.5			
	VDD=3.00V (DS=1)	8.6			
	VDD=2.56V (DS=1)	7.2			
	VDD=2.20V (DS=1)	5.9			
I_{OH}	High-level Output Current @V_{OH}(min)[2]				
	VDD=3.30V (DS=0)	7.4			mA
	VDD=3.00V (DS=0)	5.9			
	VDD=2.56V (DS=0)	4.3			
	VDD=2.20V (DS=0)	3.3			
	VDD=3.30V (DS=1)	11.2			
	VDD=3.00V (DS=1)	8.9			
	VDD=2.56V (DS=1)	6.5			
	VDD=2.20V (DS=1)	5.0			

[1] For P0[7:5], P1[1:0], P1[4:3], P1[7:6], and P3[7:0] pins
[2] For P0[7:5], P1[1:0], P1[4:3], P1[7:6], and P3[7:0] pins

5.4. Current Consumption and Timing Characteristics

T_{OP} = 25˚C, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
MCU active. No radio and peripherals (UART1&RNG) active. @ MCU clock = 8MHz @ MCU clock = 16MHz		 4.2 5.2		mA
RX mode. MCU active @ MCU clock = 8MHz		24.9		mA
TX mode. MCU active @ MCU clock = 8MHz @ maximum transmit output power @ 0dBm		 36.5 22.5		mA
Power mode1. Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off, 32kHz RCOSC, POR, BOD, and sleep timer active.		35.3	44.4	µA
Power mode1. Digital regulator on, 16MHz RCOSC, 32MHz crystal oscillator off, 32.768kHz crystal oscillator, POR, BOD, and sleep timer active.		45.3	54.4	µA
Power mode2. Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32kHz RCOSC and sleep timer active.		1.8	4.1	µA
Power mode2. Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32.768kHz crystal oscillator and sleep timer active.		11.8	14.1	µA
Power mode3. Digital regulator off, 16MHz RCOSC, 32MHz crystal oscillator off, 32kHz RCOSC(32.768kHz crystal oscillator) and sleep timer off.			1	µA
Wake-up and timing				
Power mode1 → MCU Active Digital regulator on, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of 16MHz RCOSC		5		µs
Power mode2 → MCU Active Digital regulator off, 16MHz RCOSC and 32MHz crystal oscillator off. Start-up of regulator and 16MHz RCOSC		100		µs
MCU Active → TX or RX Initially running on 16MHz RCOSC, Added start-up time of 32MHz crystal oscillator.		992		µs
TX/RX and RX/TX turnaround			192	µs

5.5. RF Receive Section

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range[3](center frequency)	2405		2480	MHz
Maximum input level (PER=1%) @ 1000kbps @ 500kbps @ 250kbps @ 125kbps @ 62.5kbps @ 31.25kbps		 -6 -9 -2 -4 5 5		dBm
Spurious radiation @ 30MHz – 1000MHz		 -73.7		dBm

[3] Extended range: 2394~2507MHz

@ 1GHz – 12.75GHz		-73.7		
Received RF bandwidth		2		MHz
Channel spacing[4]		5		MHz
Receiver sensitivity (PER≤1%, PSDU length of 20-byte) @ 1000kbps @ 500kbps @ 250kbps @ 125kbps @ 62.5kbps @ 31.25kbps		 -93 -91 -98 -99 -103 -105		dBm
Adjacent channel rejection (Sensitivity+3, adjacent modulated channel at ±5MHz, PER=1%, 250kbps) +5MHz -5MHz		 27 27		dB
Alternate channel rejection (Sensitivity+3, adjacent modulated channel at ±10MHz, PER=1%, 250kbps) +10MHz -10MHz		 48 47		dB
Others channel rejection (Sensitivity+3, adjacent modulated channel at over ±15MHz, PER=1%, 250kbps) ≥+15MHz ≥-15MHz		 53 52		dB
Co-channel rejection (Sensitivity+3. Undesired IEEE 802.15.4 modulated signal at the same frequency. Signal level for PER=1%, 250kbps)		-8.9		dB
Blocking/desensitization -250MHz -100MHz -50MHz +50MHz +100MHz +250MHz		 -25 -35 -38 -37 -35 -31		dBm
RSSI dynamic range			80	dB
RSSI accuracy		± 3		dB

5.6. RF Transmit Section

Measured on 2-layer reference design with T_{OP}=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
RF frequency range[5](center frequency)	2405		2480	MHz
TX output power (using the recommended matching circuit)		+9.0		dBm
Transmit chip rate		2		Mcps
Error vector magnitude (EVM)		7		%
Harmonics 2nd harmonic 3rd harmonic		 -43.9 -51.0		dBm
Spurious emission (complies with EN 300-440, FCC and ARIB STD-T66) 30Hz ~ 1GHz 1GHz ~ 12.75GHz		 < -75 < -43.9		dBm

[4] Specified in IEEE Standard 802.15.4™
[5] Extended range: 2394~2507MHz

1.8 ~ 1.9GHz 5.15 ~ 5.3GHz		< -75 < -75		

5.7. Frequency Synthesizer

T_{OP}=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier @ ±100kHz offset @ ±1MHz offset @ ±2MHz offset @ ±3MHz offset @ ±5MHz offset @ ±10MHz offset @ ±50MHz offset		 -76.5 -99.6 -108.6 -112.7 -115.2 -121.2 -140.9		dBc/Hz
Lock time		97		μs

5.8. 32MHz Crystal Oscillator

T_{OP}=25℃, DXOSC18V=1.8V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Crystal frequency		32		MHz
Crystal frequency accuracy requirement	-40		40	ppm
Equivalent series resistance(ESR)		30[6]	60[7]	Ω
Crystal shunt capacitance(C_O)		3	5	pF
Crystal load capacitance(C_L)		13[6]	16[7]	pF
Start-up time			0.8	ms

5.9. 16MHz RC Oscillator

T_{OP}=25℃, DXOSC18V=1.8V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Frequency		16		MHz
Frequency accuracy before calibration	-25		25	%
Frequency accuracy after calibration	-3		3	%
Initial calibration time		50		μs
Start-up time			1	μs

[6] The negative resistance of driving circuit is five times larger than the ESR of crystal oscillator with crystal satisfying above TYP conditions.
[7] The negative resistance of driving circuit is two times larger than the ESR of crystal oscillator with crystal satisfying above MAX conditions.

5.10. 32kHz RC Oscillator

T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Calibrated frequency		32.787		kHz
frequency accuracy after calibration	-0.3		0.3	%
Initial calibration time		1		ms
Start-up time			100	μs

5.11. 32.768kHz Crystal Oscillator

T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Frequency		32.768		kHz
Crystal frequency accuracy requirement	-40		40	ppm
Equivalent series resistance(ESR)		50	100	kΩ
Crystal shunt capacitance(C_O)		0.9		pF
Crystal load capacitance(C_L)		12.5		pF
Start-up time		1.2		s

5.12. Temperature Sensor

VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Output at -40℃		-295		
Output at 25℃		76		
Output at 85℃		418		
Temperature coefficient		5.703		/℃

All measurement results are obtained using the 12-bit ADC.

5.13. ADC

T_{OP}=25℃, VDD=3.0V, unless otherwise noted.

Parameter(Condition)	MIN	TYP	MAX	UNIT
Input voltage	0		VDD	V
Input resistance		150		kΩ
Full-scale signal			3	V
Effective number of bits(ENOB) Single-ended input, 12bit setting		10.8		bits
Signal to noise and distortion(SINAD) Single-ended input, 12bit setting		66.78		dB
Current consumption		0.46		mA
Internal reference voltage		1.25		V

5.14. Flash Memory

5.14.1. Flash memory characteristics

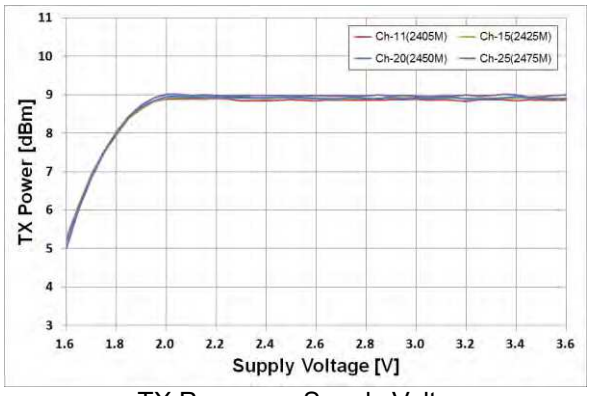
Characteristic	Symbol	Conditions	MIN	TYP	MAX	UNIT
Endurance	Nendu	20ms erase and 20 us program time at 1.8V	20,000			cycles
Data retention	Tret	25 °C	100			years

5.14.2. Flash memory and page size

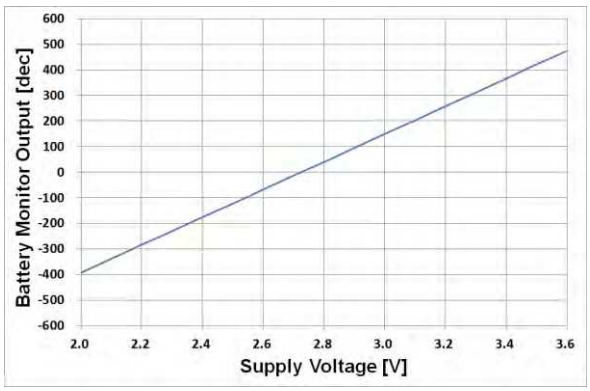
Name	Size	Unit
Flash main memory block	65,536	bytes
Flash information block	1,024	bytes
Flash page size	512	bytes

5.15. Typical Performance Curves

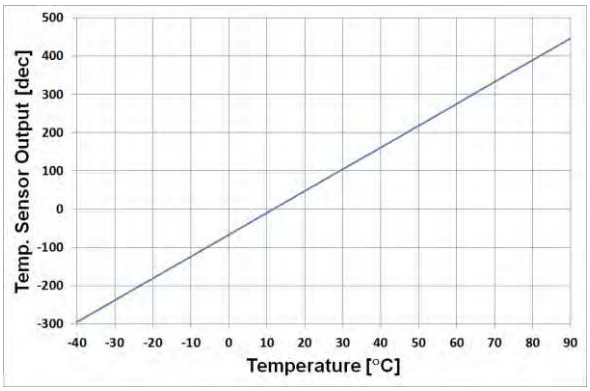
T_{OP}=25℃, VDD=3.0V, and fc=2450MHz, unless otherwise noted. All parameters measured on 2-layer reference design.



TX Power vs. Supply Voltage



ADC – Battery monitoring output



ADC – Temperature sensor output

6. REFERENCE APPLICATION CIRCUITS

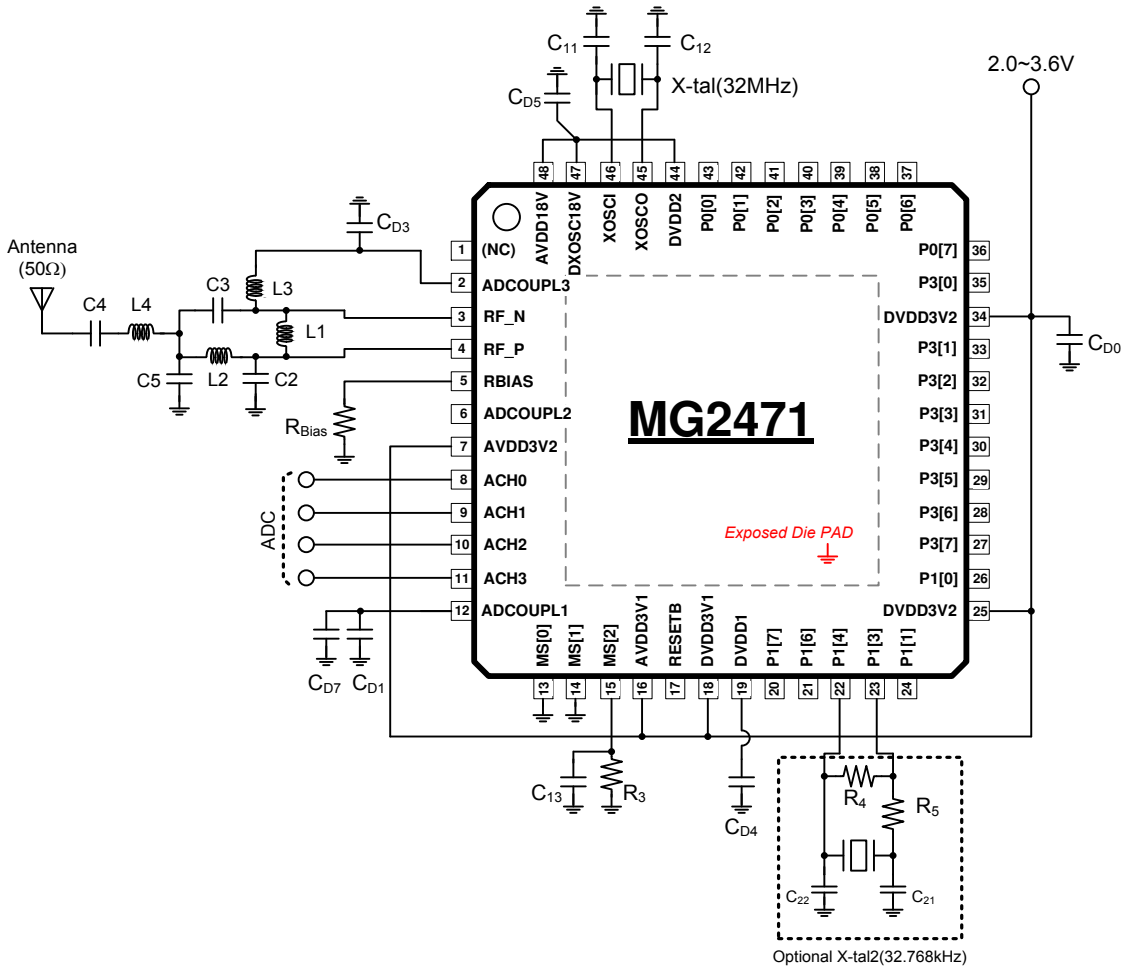
A typical application diagram of the MG2471 is shown in [Figure 3]. Only a few external components are required for the operation of the MG2471. [Table 3] describes the external components including decoupling capacitors.

The inductor, L1 is used as a matching component for the LNA and as an output load for the PA, respectively. The components near the RF_P/RF_N pins, L2, L3, C2, and C3 form a balun which converts the differential RF signals to a single-ended RF signal. And, L4, C4, and C5 form a LC harmonic filter to suppress the TX output harmonics. In addition, C4 is needed for DC blocking. All together with adequate values, they also transform the impedance to match a 50-Ohm antenna.

As shown in [Figure 3], RF_P and RF_N are biased by ADCOUPL3 through L1 and L3.

The 32MHz crystal provides the reference frequency source for MG2471. C11 and C12 are loading capacitors of it. C_{D0}, C_{D1}, C_{D3}, C_{D4}, C_{D5}, C_{D7}, and C_7 are supply decoupling capacitors, whose values depend on PCB artwork and stack-up information.

The components' values listed in Table 3 are selected for 2-layer reference PCB design.



**** GND is bottom pad (down-bonding pad) in the above schematic*

Figure 3. MG2471 Typical Application Circuit

In applications, some GPIO pins (among P0, P1 and P3) and ADC input pins may be unused. Then, the unused GPIO pins are recommended to be floating and configured as the input pull-up state: the input pull-up is the default state of the GPIOs. For the detail register configuration on the GPIOs, please refer to the Sec 8.2. Similarly, the unused ADC input pins are recommended to be connected to the ground.

Table 3. Bill of Materials for Figure 3

No	Component	Description	Value
1	L1	RF matching inductor	2.4nH
2	L2, L3	RF balun inductors	4.7nH
3	C2, C3	RF balun capacitors	0.75pF
4	L4	RF LC filter/matching inductor	5.1nH
5	C5	RF LC filter/matching capacitor	0.5pF
6	C4	RF matching/DC blocking capacitor	1.0pF
7	Rbias	Resistor for internal bias current reference	510kohm
8	X-tal	32MHz crystal unit	32MHz
9	C11, C12	Crystal loading capacitors	13pF[8]
10	C_{D0}	Decoupling capacitor for DVDD3V	10uF
11	C_{D1}	Decoupling capacitor for ADCOUPL1	1uF
12	C_{D7}	Decoupling capacitor for ADCOUPL1	1uF
13	C_{D3}	Decoupling capacitor for ADCOUPL3	1uF
14	C_{D4}	Decoupling capacitor for DVDD1	1uF
15	C_{D5}	Decoupling capacitor for DVDD2 and DXOSC18V	100pF
16	R_3	Pull-down resistor for MS[2] input	10kohm
18	C_{13}	Capacitor for MS[2] input	1uF
19	C_{21}	(option) Capacitor for 32.768kHz crystal oscillator	33pF
20	C_{22}	(option) Capacitor for 32.768kHz crystal oscillator	15pF
21	R_4	(option) Resistor for 32.768kHz crystal oscillator	22Mohm
22	R_5	(option) Resistor for 32.768kHz crystal oscillator	330kohm

[8] The value of crystal loading capacitance depends on crystal oscillator.