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Data Sheet, V3.0, Jan. 2001

C161CS-32R/-L
C161JC-32R/-L
C161JI-32R/-L

16-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

Edition 2001-01

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Data Sheet, V3.0, Jan. 2001

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Revision History: **2001-01** V3.0

Previous Version: 2000-08 V2.0 (intermediate version)
1999-03 (Advance Information)

Page	Subjects (major changes since last revision)[1)]
All	Converted to Infineon layout
2	Derivative Synopsis Table updated
4, 6, 10, 18	Programmable Interface Routing introduced
27, 28	GPT block diagrams updated
29	RTC description improved
35	OWD description improved
39ff	RSTCON and SDLM registers added
51	Description of input/output voltage and hysteresis improved
53	Separate table for power consumption
57	Clock generation mode table updated
60	External clock drive specification improved
62	Reset calibration time specified, definition of V_{AREF} improved
63	Programmable sample time introduced
65ff	Timing tables updated to 25 MHz

1) Changes refer to version 1999-03.

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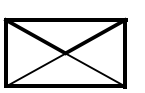

C161CS/JC/JI

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
  - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 59 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
  - Additional 32 kHz Oscillator
- On-Chip Memory Modules
  - 2 KBytes On-Chip Internal RAM (IRAM)
  - 8 KBytes On-Chip Extension RAM (XRAM)
  - 256 KBytes On-Chip Mask ROM
- On-Chip Peripheral Modules
  - 12-Channel 10-bit A/D Converter with Programmable Conversion Time down to 7.8 µs
  - Two 16-Channel Capture/Compare Units (eight IO lines each)
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Asynchronous/Synchronous Serial Channels
  - High-Speed Synchronous Serial Channel (SPI)
  - On-Chip CAN Interface (Rev. 2.0B active, Full CAN / Basic CAN) with 15 Message Objects (**C161CS 2x, C161JC 1x**)
  - Serial Data Link Module (SDLM), compliant with J1850, supporting Class 2 (**C161JC/JI**)
  - IIC Bus Interface (10-bit Addressing, 400 kHz) with 2 Channels (multiplexed)
  - On-Chip Real Time Clock
- Up to 16 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support

- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 93 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- Supported by a Large Range of Development Tools like C-Compilers,
  Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers,
  Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 128-Pin TQFP Package

This document describes several derivatives of the C161 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C161CS/JC/JI Derivative Synopsis

Derivative	On-Chip Program Memory	Serial Bus Interface(s)	Maximum CPU Frequency
SAK-C161CS-32RF SAB-C161CS-32RF	256 KByte ROM	CAN1, CAN2	25 MHz
SAK-C161CS-LF SAB-C161CS-LF	---	CAN1, CAN2	25 MHz
SAK-C161JC-32RF SAB-C161JC-32RF	256 KByte ROM	CAN1, SDLM	25 MHz
SAK-C161JC-LF SAB-C161JC-LF	---	CAN1, SDLM	25 MHz
SAK-C161JI-32RF SAB-C161JI-32RF	256 KByte ROM	SDLM	25 MHz
SAK-C161JI-LF SAB-C161JI-LF	---	SDLM	25 MHz

For simplicity all versions are referred to by the term **C161CS/JC/JI** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C161CS/JC/JI please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Introduction

The C161CS/JC/JI derivatives are high performance derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM, internal RAM, and extension RAM.

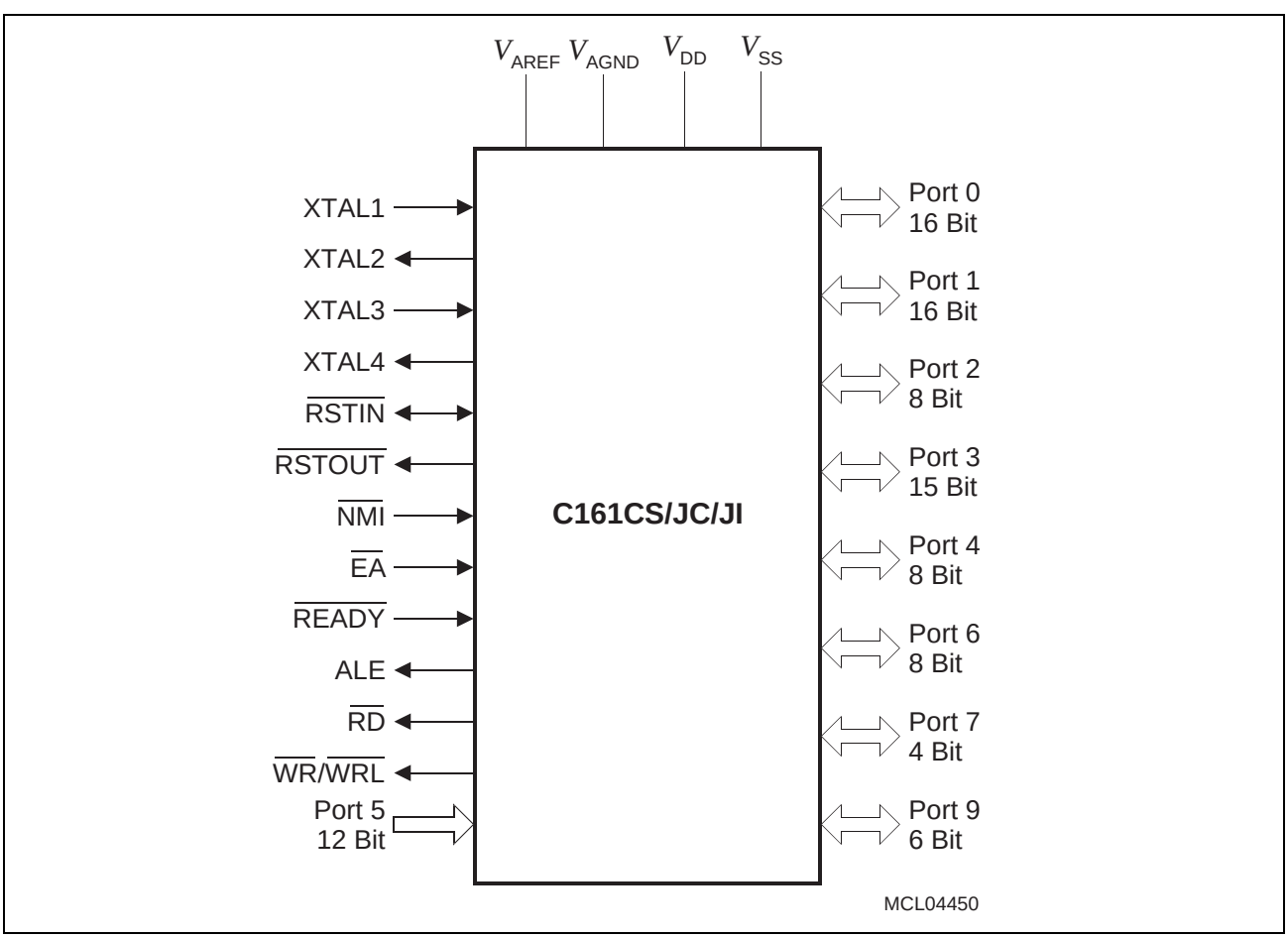

Figure 1 Logic Symbol

Pin Configuration
(top view)

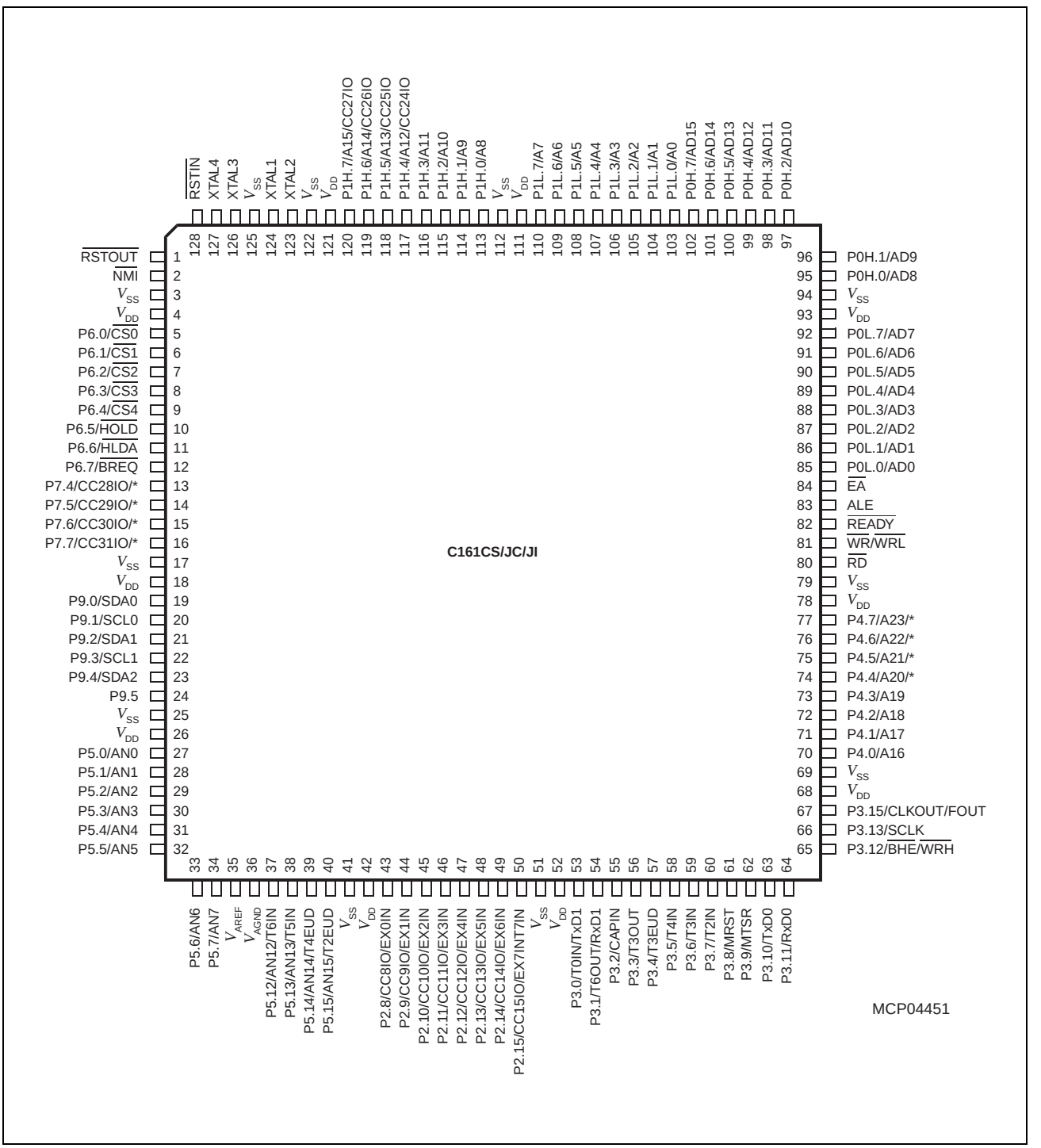

Figure 2

***)** The marked pins of Port 4 and Port 7 can have interface lines assigned to them (CAN interface in the **C161CS** and **C161JC**, SDLM interface in the **C161JC** and **C161JI**). **Table 2** on the pages below lists the possible assignments.

Table 2 Pin Definitions and Functions

Symbol	Pin No.	Input Outp.	Function
$\overline{\text{RSTOUT}}$	1	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	2	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C161CS/JC/JI to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	5	O	$\overline{\text{CS0}}$ Chip Select 0 Output
P6.1	6	O	$\overline{\text{CS1}}$ Chip Select 1 Output
P6.2	7	O	$\overline{\text{CS2}}$ Chip Select 2 Output
P6.3	8	O	$\overline{\text{CS3}}$ Chip Select 3 Output
P6.4	9	O	$\overline{\text{CS4}}$ Chip Select 4 Output
P6.5	10	I	$\overline{\text{HOLD}}$ External Master Hold Request Input
P6.6	11	I/O	$\overline{\text{HLDA}}$ Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	12	O	$\overline{\text{BREQ}}$ Bus Request Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P7		IO	Port 7 is a 4-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). Port 7 pins provide inputs/outputs for CAPCOM2 and serial interface lines.[1)]
P7.4	13	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.,
		I	CAN1_RxD CAN 1 Receive Data Input, (**C161CS/JC**)
		I	CAN2_RxD CAN 2 Receive Data Input, (**C161CS**)
		O	SDL_TxD SDLM Transmit Data Output (**C161JC/JI**)
P7.5	14	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.,
		O	CAN1_TxD CAN 1 Transmit Data Output, (**C161CS/JC**)
		O	CAN2_TxD CAN 2 Transmit Data Output, (**C161CS**)
		I	SDL_RxD SDLM Receive Data Input (**C161JC/JI**)
P7.6	15	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.,
		I	CAN1_RxD CAN 1 Receive Data Input, (**C161CS/JC**)
		I	CAN2_RxD CAN 2 Receive Data Input, (**C161CS**)
		O	SDL_TxD SDLM Transmit Data Output (**C161JC/JI**)
P7.7	16	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.,
		O	CAN1_TxD CAN 1 Transmit Data Output, (**C161CS/JC**)
		O	CAN2_TxD CAN 2 Transmit Data Output, (**C161CS**)
		I	SDL_RxD SDLM Receive Data Input (**C161JC/JI**)
P9		IO	Port 9 is a 6-bit bidirectional open drain I/O port (provide external pullup resistors if required). It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The following Port 9 pins also serve for alternate functions:
P9.0	19	I/O	SDA0 IIC Bus Data Line 0
P9.1	20	I/O	SCL0 IIC Bus Clock Line 0
P9.2	21	I/O	SDA1 IIC Bus Data Line 1
P9.3	22	I/O	SCL1 IIC Bus Clock Line 1
P9.4	23	I/O	SDA2 IIC Bus Data Line 2
P9.5	24	–	–
			*Note: Port 9 pins can only tolerate positive overload currents (see **Table 9**).*

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function		
P5		I	Port 5 is a 12-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:		
P5.0	27	I	AN0		
P5.1	28	I	AN1		
P5.2	29	I	AN2		
P5.3	30	I	AN3		
P5.4	31	I	AN4		
P5.5	32	I	AN5		
P5.6	33	I	AN6		
P5.7	34	I	AN7		
P5.12	37	I	AN12,	T6IN	GPT2 Timer T6 Count Inp.
P5.13	38	I	AN13,	T5IN	GPT2 Timer T5 Count Inp.
P5.14	39	I	AN14,	T4EUD	GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	40	I	AN15,	T2EUD	GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P2		IO	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:
P2.8	43	I/O I	CC8IO CAPCOM1: CC8 Capture Inp./Compare Output, EX0IN Fast External Interrupt 0 Input
P2.9	44	I/O I	CC9IO CAPCOM1: CC9 Capture Inp./Compare Output, EX1IN Fast External Interrupt 1 Input
P2.10	45	I/O I	CC10IO CAPCOM1: CC10 Capture Inp./Compare Outp., EX2IN Fast External Interrupt 2 Input
P2.11	46	I/O I	CC11IO CAPCOM1: CC11 Capture Inp./Compare Outp., EX3IN Fast External Interrupt 3 Input
P2.12	47	I/O I	CC12IO CAPCOM1: CC12 Capture Inp./Compare Outp., EX4IN Fast External Interrupt 4 Input
P2.13	48	I/O I	CC13IO CAPCOM1: CC13 Capture Inp./Compare Outp., EX5IN Fast External Interrupt 5 Input
P2.14	49	I/O I	CC14IO CAPCOM1: CC14 Capture Inp./Compare Outp., EX6IN Fast External Interrupt 6 Input
P2.15	50	I/O I I	CC15IO CAPCOM1: CC15 Capture Inp./Compare Outp., EX7IN Fast External Interrupt 7 Input, T7IN CAPCOM2: Timer T7 Count Input *Note: During Sleep Mode a spike filter on the EXnIN interrupt inputs suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter.*

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	53	I	T0IN	CAPCOM1 Timer T0 Count Input,
		O	TxD1	ASC1 Clock/Data Output (Async./Sync)
P3.1	54	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Output (Sync.)
P3.2	55	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	56	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	57	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	58	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	59	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	60	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	61	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	62	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	63	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	64	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	65	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	66	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	67	O	CLKOUT	System Clock Output (= CPU Clock)
		O	FOUT	Programmable Frequency Output

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. The Port 4 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 4 is selectable (TTL or special). Port 4 can be used to output the segment address lines and for serial interface lines:[1)]
P4.0	70	O	A16 Least Significant Segment Address Line
P4.1	71	O	A17 Segment Address Line
P4.2	72	O	A18 Segment Address Line
P4.3	73	O	A19 Segment Address Line
P4.4	74	O	A20 Segment Address Line,
		I	CAN2_RxD CAN 2 Receive Data Input, (**C161CS**)
		I	SDL_RxD SDLM Receive Data Input (**C161JC/JI**)
P4.5	75	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input, (**C161CS/JC**)
P4.6	76	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output, (**C161CS/JC**)
		O	CAN2_TxD CAN 2 Transmit Data Output, (**C161CS**)
		I	SDL_RxD SDLM Receive Data Input (**C161JC/JI**)
P4.7	77	O	A23 Most Significant Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input, (**C161CS/JC**)
		O	CAN2_TxD CAN 2 Transmit Data Output, (**C161CS**)
		I	CAN2_RxD CAN 2 Receive Data Input, (**C161CS**)
		O	SDL_TxD SDLM Transmit Data Output (**C161JC/JI**)
$\overline{RD}$	80	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	81	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
$\overline{\text{READY}}$	82	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pullup device will hold this pin high when nothing is driving it.
ALE	83	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{\text{EA}}$	84	I	External Access Enable pin. A low level at this pin during and after Reset forces the C161CS/JC/JI to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
PORT0 P0L.0-7 P0H.0-7	 85-92 95-102	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 - A15 AD8 - AD15 *Note: At the end of an external reset (EA = '0') PORT0 also inputs the configuration values.*

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
P1L.0-7	103-110		
P1H.0-7	113-120		
			The following PORT1 pins also serve for alternate functions:
P1H.4	117	I/O	CC24IO CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	118	I/O	CC25IO CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	119	I/O	CC26IO CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	120	I/O	CC27IO CAPCOM2: CC27 Capture Inp./Compare Outp.
XTAL2	123	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	124	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
XTAL3	126	I	XTAL3: Input to the 32-kHz oscillator amplifier and input to the internal clock generator
XTAL4	127	O	XTAL4: Output of the oscillator amplifier circuit. To clock the device from an external source, drive XTAL3, while leaving XTAL4 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin No.	Input Outp.	Function
$\overline{\text{RSTIN}}$	128	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C161CS/JC/JI. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*
V_{AREF}	35	–	Reference voltage for the A/D converter.
V_{AGND}	36	–	Reference ground for the A/D converter.
V_{DD}	4, 18, 26[2], 42, 52, 68, 78, 93, 111, 121	–	Digital Supply Voltage: +5 V during normal operation and idle mode. ≥ 2.5 V during power down mode if RTC is off ≥ 2.7 V during power down mode if RTC is running
V_{SS}	3, 17, 25[2], 41, 51, 69, 79, 94, 112, 122, 125	–	Digital Ground.

1) The CAN and/or SDLM interface lines are assigned to ports P4 and P7 under software control. Within the CAN module or SDLM several assignments can be selected.

2) Supply pins 25 and 26 feed the Analog/Digital Converter and should be decoupled separately.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Functional Description

The architecture of the C161CS/JC/JI combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.
The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C161CS/JC/JI.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

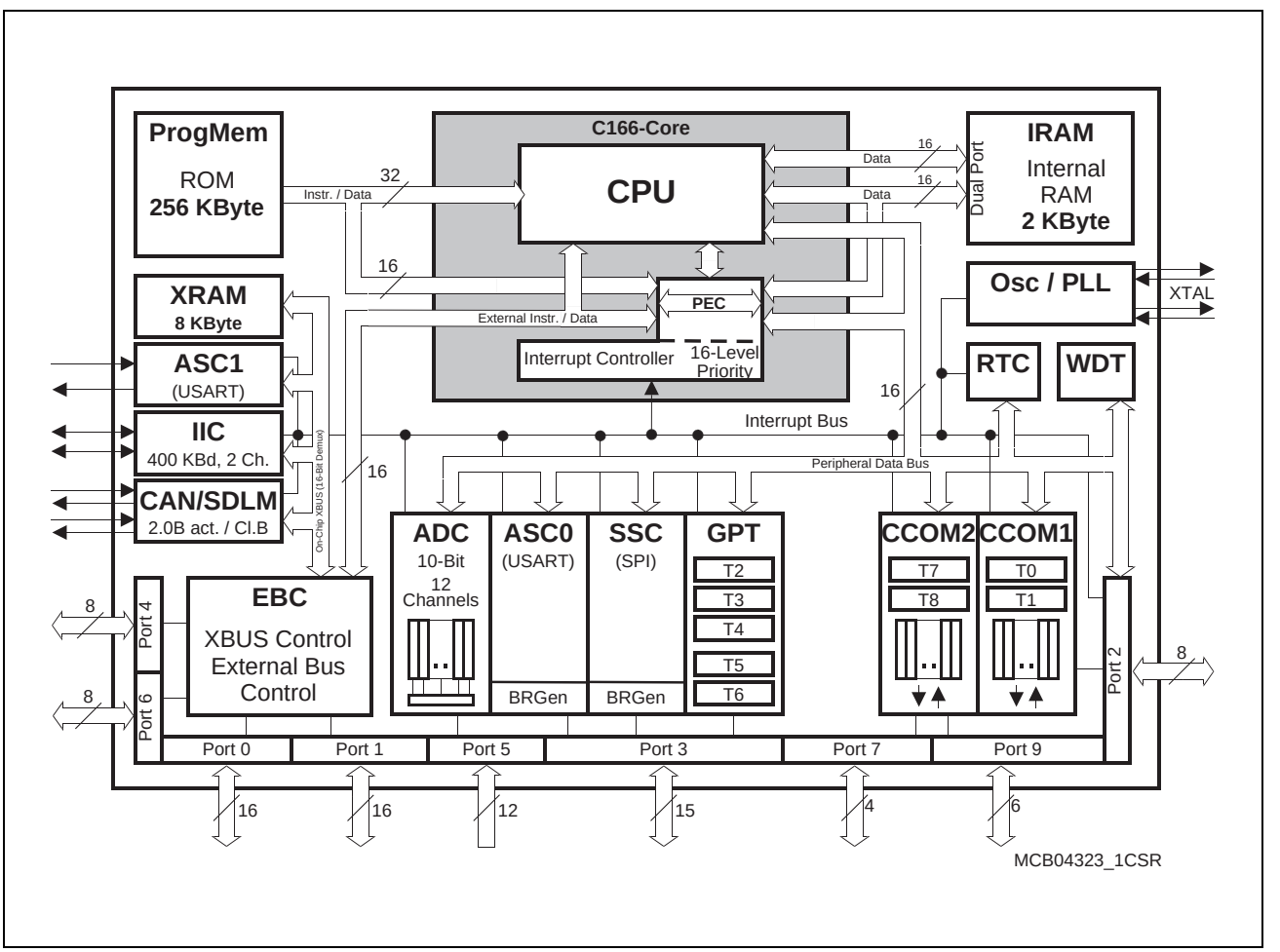

Figure 3 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resoures, the X-Peripherals (see **Figure 3**).

The XBUS resources (XRAM, CAN, SDLM, IIC, ASC1) of the C161CS/JC/JI can be enabled during initialization by setting the general X-Peripheral enable bit XPEN (SYSCON.2).
If the X-Peripherals remain disabled they consume neither address space nor port pins.

Memory Organization

The memory space of the C161CS/JC/JI is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C161CS/JC/JI incorporates 256 KBytes of on-chip mask-programmable ROM for code or constant data. The lower 32 KBytes of the on-chip ROM can be mapped either to segment 0 or segment 1.

2 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2 $\times$ 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

8 KBytes of on-chip Extension RAM (XRAM) are provided to store user data, user stacks, or code. The XRAM is accessed like external memory and therefore cannot be used for the system stack or for register banks and is not bitaddressable. The XRAM permits 16-bit accesses with maximum speed.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/ output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{CS}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C161CS/JC/JI offers the possibility to switch the $\overline{CS}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{CS}$ signals are directly generated from the address. The unlatched $\overline{CS}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular ‘Ready’ function.

A $\overline{HOLD}$/$\overline{HLDA}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to ‘1’ the Slave Mode is selected where pin $\overline{HLDA}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Note: When one or both of the on-chip CAN Modules or the SDLM are used with the interface lines assigned to Port 4, the interface lines override the segment address lines and the segment address output on Port 4 is therefore limited to 6/4 bits i.e. address lines A21/A19 … A16. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C161CS/JC/JI's instructions can be executed in just one machine cycle which requires 80 ns at 25 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16-bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

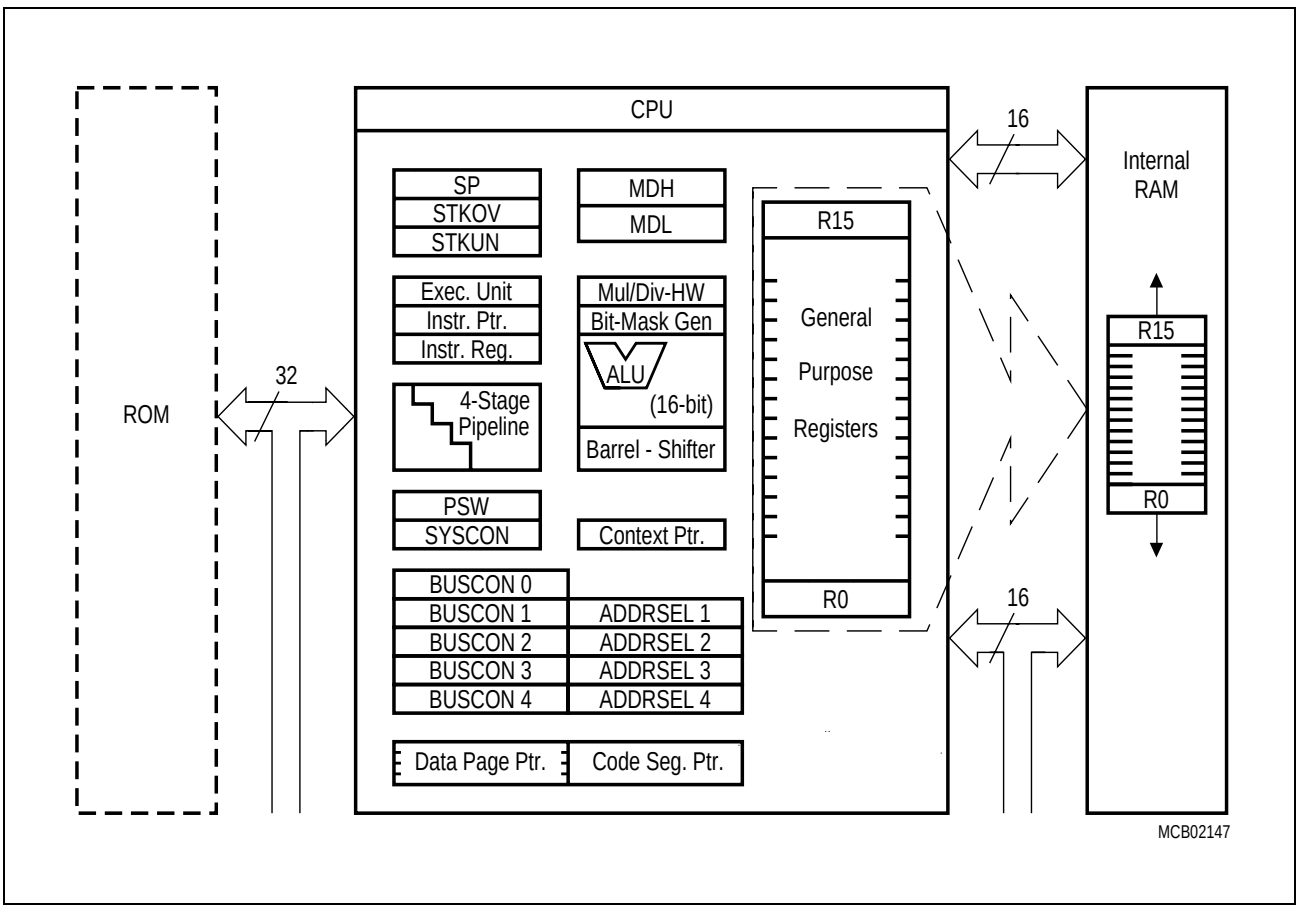

Figure 4 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C161CS/JC/JI instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C161CS/JC/JI is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C161CS/JC/JI supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is ‘stolen’ from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C161CS/JC/JI has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the ‘TRAP’ instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C161CS/JC/JI interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 3 C161CS/JC/JI Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM Register 0	CC0IR	CC0IE	CC0INT	$00'0040_H$	10_H
CAPCOM Register 1	CC1IR	CC1IE	CC1INT	$00'0044_H$	11_H
CAPCOM Register 2	CC2IR	CC2IE	CC2INT	$00'0048_H$	12_H
CAPCOM Register 3	CC3IR	CC3IE	CC3INT	$00'004C_H$	13_H
CAPCOM Register 4	CC4IR	CC4IE	CC4INT	$00'0050_H$	14_H
CAPCOM Register 5	CC5IR	CC5IE	CC5INT	$00'0054_H$	15_H
CAPCOM Register 6	CC6IR	CC6IE	CC6INT	$00'0058_H$	16_H
CAPCOM Register 7	CC7IR	CC7IE	CC7INT	$00'005C_H$	17_H
CAPCOM Register 8	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
CAPCOM Register 9	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
CAPCOM Register 10	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
CAPCOM Register 11	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
CAPCOM Register 12	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
CAPCOM Register 13	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
CAPCOM Register 14	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
CAPCOM Register 15	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
CAPCOM Register 16	CC16IR	CC16IE	CC16INT	$00'00C0_H$	30_H
CAPCOM Register 17	CC17IR	CC17IE	CC17INT	$00'00C4_H$	31_H
CAPCOM Register 18	CC18IR	CC18IE	CC18INT	$00'00C8_H$	32_H
CAPCOM Register 19	CC19IR	CC19IE	CC19INT	$00'00CC_H$	33_H
CAPCOM Register 20	CC20IR	CC20IE	CC20INT	$00'00D0_H$	34_H
CAPCOM Register 21	CC21IR	CC21IE	CC21INT	$00'00D4_H$	35_H
CAPCOM Register 22	CC22IR	CC22IE	CC22INT	$00'00D8_H$	36_H
CAPCOM Register 23	CC23IR	CC23IE	CC23INT	$00'00DC_H$	37_H
CAPCOM Register 24	CC24IR	CC24IE	CC24INT	$00'00E0_H$	38_H
CAPCOM Register 25	CC25IR	CC25IE	CC25INT	$00'00E4_H$	39_H
CAPCOM Register 26	CC26IR	CC26IE	CC26INT	$00'00E8_H$	$3A_H$
CAPCOM Register 27	CC27IR	CC27IE	CC27INT	$00'00EC_H$	$3B_H$
CAPCOM Register 28	CC28IR	CC28IE	CC28INT	$00'00E0_H$	$3C_H$
CAPCOM Register 29	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H