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Data Sheet, V2.0, Dec. 2000

C165

16-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

Edition 2000-12

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Data Sheet, V2.0, Dec. 2000

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Revision History:	**2000-12**		V2.0
Previous Version:	1998-12	Update 0.5µ technology	
	01.96	3 Volt Addendum	
	07.95	25 MHz Addendum	
	09.94	Data Sheet	

Page	Subjects (major changes since last revision)
All	Converted to Infineon layout
2	ROM derivatives removed, 25-MHz derivatives and 3 V derivatives included
6ff	Pin numbers for TQFP added
14	Address window arbitration and master/slave mode introduced
32	New standard layout for section “Absolute Maximum Ratings”
33	Section “Operating Conditions” added
34f	Parameter “$\overline{\text{RSTIN}}$ pullup” replaced by “$\overline{\text{RSTIN}}$ current”
36f	DC Characteristics for reduced supply voltage added
38f	Separate specification for power consumption with greatly improved values
40ff	Description of clock generation improved
45, 55, 65	Timing adapted to 25 MHz
48, 58, 66	Timing for reduced supply voltage added

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16-Bit Single-Chip Microcontroller **C165**
C166 Family

C165

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80 ns Instruction Cycle Time at 25 MHz CPU Clock
  - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 28 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via prescaler or via direct clock input
- On-Chip Memory Modules
  - 2 KBytes On-Chip Internal RAM (IRAM)
- On-Chip Peripheral Modules
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
- Up to 16 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle and Power Down Modes
- Programmable Watchdog Timer
- Up to 77 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis
- Power Supply: the C165 can operate from a 5 V or a 3 V power supply
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 100-Pin MQFP Package (0.65 mm pitch)
- 100-Pin TQFP Package (0.5 mm pitch)

This document describes several derivatives of the C165 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

Table 1 C165 Derivative Synopsis

Derivative[1]	Max. Operating Frequency	Operating Voltage	Package
SAF-C165-LM	20 MHz	4.5 to 5.5 V	MQFP-100
SAB-C165-LM	20 MHz	4.5 to 5.5 V	MQFP-100
SAF-C165-L25M	25 MHz	4.5 to 5.5 V	MQFP-100
SAB-C165-L25M	25 MHz	4.5 to 5.5 V	MQFP-100
SAF-C165-LF	20 MHz	4.5 to 5.5 V	TQFP-100
SAB-C165-LF	20 MHz	4.5 to 5.5 V	TQFP-100
SAF-C165-L25F	25 MHz	4.5 to 5.5 V	TQFP-100
SAB-C165-L25F	25 MHz	4.5 to 5.5 V	TQFP-100
SAF-C165-LM3V	20 MHz	3.0 to 3.6 V	MQFP-100
SAB-C165-LM3V	20 MHz	3.0 to 3.6 V	MQFP-100
SAF-C165-LF3V	20 MHz	3.0 to 3.6 V	TQFP-100
SAB-C165-LF3V	20 MHz	3.0 to 3.6 V	TQFP-100

[1] This Data Sheet is valid for devices starting with and including design step HA.

For simplicity all versions are referred to by the term **C165** throughout this document.

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C165 please refer to the "**Product Catalog Microcontrollers**", which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

Introduction

The C165 is a derivative of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. It combines high CPU performance (up to 12.5 million instructions per second) with peripheral functionality and enhanced IO-capabilities. The C165 is especially suited for cost sensitive applications.

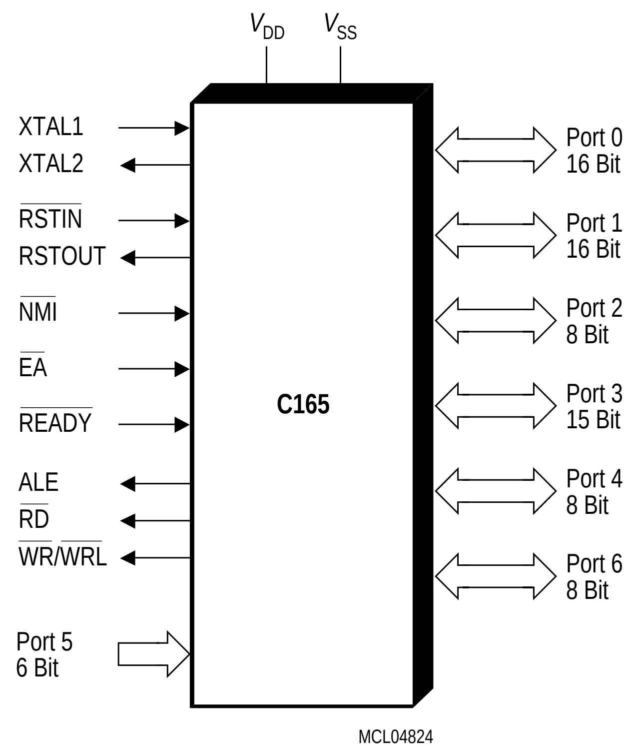

Figure 1 Logic Symbol

Pin Configuration TQFP Package
(top view)

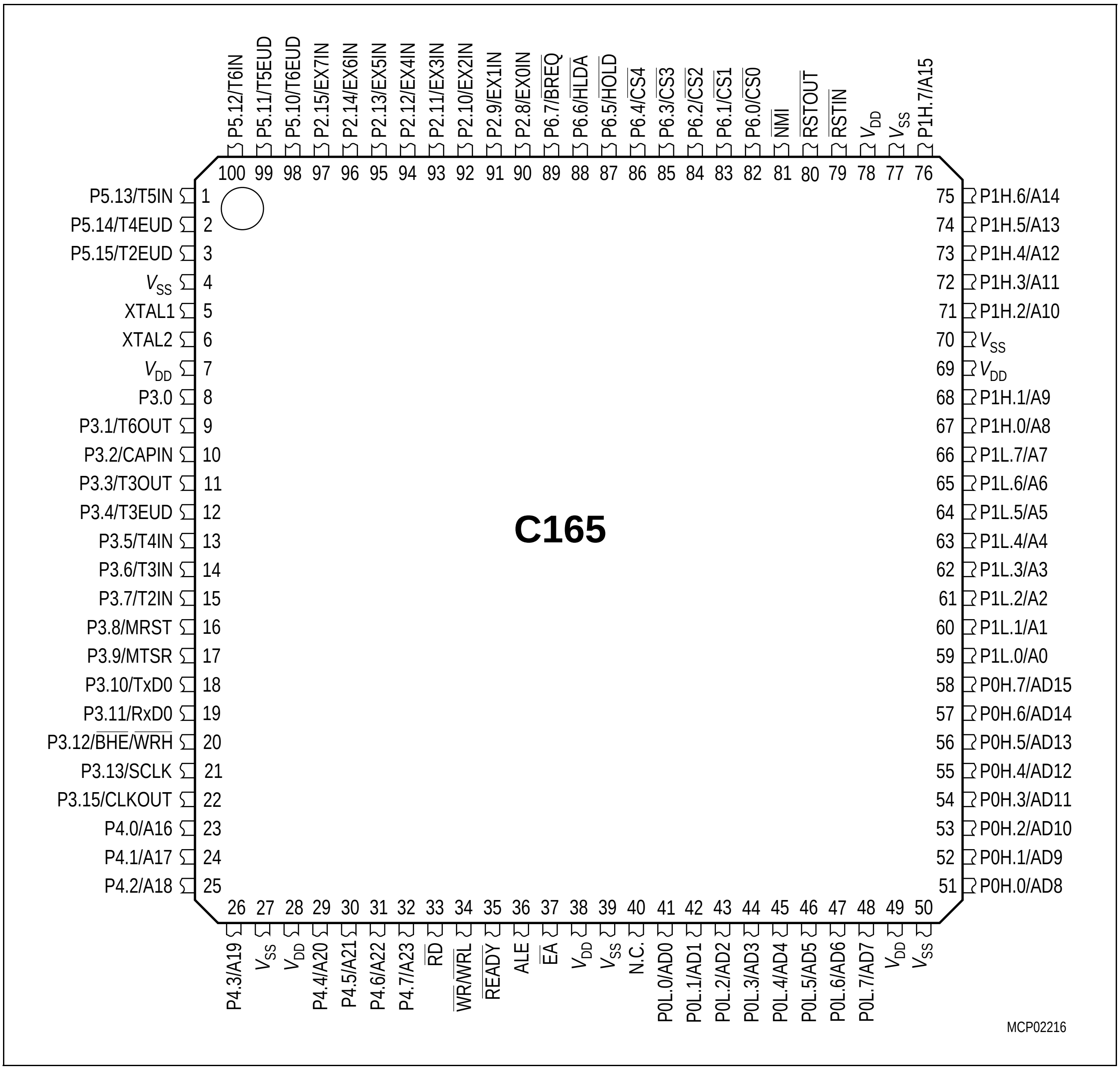

Figure 2

Pin Configuration MQFP Package
(top view)

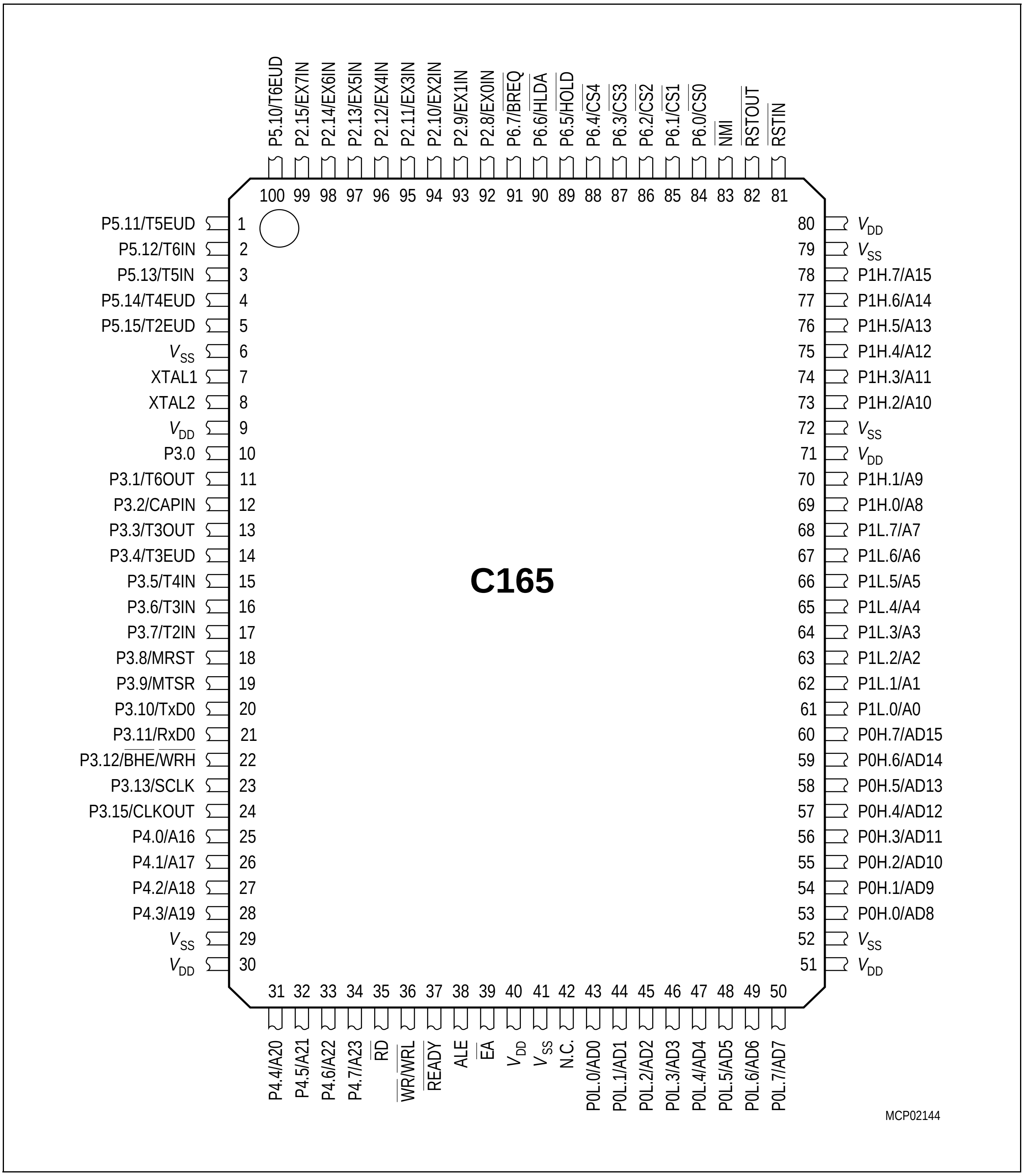

Figure 3

Table 2 Pin Definitions and Functions

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function	
XTAL1	5	7	I	XTAL1:	Input to the oscillator amplifier and input to the internal clock generator
XTAL2	6	8	O	XTAL2:	Output of the oscillator amplifier circuit.
				To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.	
P3			IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The Port 3 pins serve for following alternate functions:	
P3.0	8	10			
P3.1	9	11	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	10	12	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	11	13	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	12	14	I	T3EUD	GPT1 Timer T3 Ext. Up/Down Ctrl Input
P3.5	13	15	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Input
P3.6	14	16	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	15	17	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Input
P3.8	16	18	I/O	MRST	SSC Master-Receive/Slave-Transmit Input/Output
P3.9	17	19	I/O	MTSR	SSC Master-Transmit/Slave-Receive Output/Input
P3.10	18	20	O	TxD0	ASC0 Clock/Data Output (Asyn./Sync.)
P3.11	19	21	I/O	RxD0	ASC0 Data Inp. (Asyn.) or In/Out (Sync)
P3.12	20	22	O	$\overline{\text{BHE}}$	Ext. Memory High Byte Enable Signal,
			O	$\overline{\text{WRH}}$	Ext. Memory High Byte Write Strobe
P3.13	21	23	I/O	SCLK	SSC Master Cl. Output / Slave Cl. Input
P3.15	22	24	O	CLKOUT	System Clock Output (= CPU Clock)

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P4			IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines:
P4.0	23	25	O	A16 Least Significant Segment Address Line
P4.1	24	26	O	A17 Segment Address Line
P4.2	25	27	O	A18 Segment Address Line
P4.3	26	28	O	A19 Segment Address Line
P4.4	29	31	O	A20 Segment Address Line
P4.5	30	32	O	A21 Segment Address Line
P4.6	31	33	O	A22 Segment Address Line
P4.7	32	34	O	A23 Most Significant Segment Address Line
$\overline{\text{RD}}$	33	35	O	External Memory Read Strobe. $\overline{\text{RD}}$ is activated for every external instruction or data read access.
$\overline{\text{WR}}$/ $\overline{\text{WRL}}$	34	36	O	External Memory Write Strobe. In $\overline{\text{WR}}$-mode this pin is activated for every external data write access. In $\overline{\text{WRL}}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{\text{READY}}$	35	37	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle waitstates until the pin returns to a low level. An internal pullup device holds this pin high when nothing is driving it.
ALE	36	38	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{\text{EA}}$	37	39	I	External Access Enable pin. A low level at this pin during and after Reset forces the C165 to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
NC	40	42	–	This pin is not connected in the C165. No connection to the PCB is required.
PORT0 P0L.0-7 P0H.0-7	 41-48 51-58	 43-50 53-60	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: D0 – D7 D0 – D7 P0H.0 – P0H.7: I/O D8 – D15 **Multiplexed bus modes:** Data Path Width: 8-bit 16-bit P0L.0 – P0L.7: AD0 – AD7 AD0 – AD7 P0H.0 – P0H.7: A8 – A15 AD8 – AD15
PORT1 P1L.0-7 P1H.0-7	 59-66 67,68, 71-76	 61-68 69-70, 73-78	IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
$\overline{\text{RSTIN}}$	79	81	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C165. An internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle a reset duration of ca. 1 ms is recommended.*
$\overline{\text{RST OUT}}$	80	82	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	81	83	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C165 to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
P6			IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The Port 6 pins also serve for alternate functions:
P6.0	82	84	O	$\overline{\text{CS0}}$ Chip Select 0 Output
P6.1	83	85	O	$\overline{\text{CS1}}$ Chip Select 1 Output
P6.2	84	86	O	$\overline{\text{CS2}}$ Chip Select 2 Output
P6.3	85	87	O	$\overline{\text{CS3}}$ Chip Select 3 Output
P6.4	86	88	O	$\overline{\text{CS4}}$ Chip Select 4 Output
P6.5	87	89	I	$\overline{\text{HOLD}}$ External Master Hold Request Input
P6.6	88	90	I/O	HLDA Hold Acknowledge Outp.(master mode) or Input (slave mode)
P6.7	89	91	O	$\overline{\text{BREQ}}$ Bus Request Output
P2			IO	Port 2 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The following Port 2 pins serve for alternate functions:
P2.8	90	92	I	EX0IN Fast External Interrupt 0 Input
P2.9	91	93	I	EX1IN Fast External Interrupt 1 Input
P2.10	92	94	I	EX2IN Fast External Interrupt 2 Input
P2.11	93	95	I	EX3IN Fast External Interrupt 3 Input
P2.12	94	96	I	EX4IN Fast External Interrupt 4 Input
P2.13	95	97	I	EX5IN Fast External Interrupt 5 Input
P2.14	96	98	I	EX6IN Fast External Interrupt 6 Input
P2.15	97	99	I	EX7IN Fast External Interrupt 7 Input
P5			I	Port 5 is a 6-bit input-only port with Schmitt-Trigger char. The pins of Port 5 also serve as timer inputs:
P5.10	98	100	I	T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl Input
P5.11	99	1	I	T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl Input
P5.12	100	2	I	T6IN GPT2 Timer T6 Count Input
P5.13	1	3	I	T5IN GPT2 Timer T5 Count Input
P5.14	2	4	I	T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl Input
P5.15	3	5	I	T2EUD GPT1 Timer T2 Ext. Up/Down Ctrl Input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Nr TQFP	Pin Nr MQFP	Input Outp.	Function
V_{DD}	7, 28, 38, 49, 69, 78	9, 30, 40, 51, 71, 80	–	Digital Supply Voltage: + 5 V or + 3 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	4, 27, 39, 50, 70, 77	6, 29, 41, 52, 72, 79	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated like on a hardware reset. Especially the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

Functional Description

The architecture of the C165 combines advantages of both RISC and CISC processors and of advanced peripheral subsystems in a very well-balanced way. In addition the on-chip memory blocks allow the design of compact systems with maximum performance.
The following block diagram gives an overview of the different on-chip components and of the advanced, high bandwidth internal bus structure of the C165.

Note: All time specifications refer to a CPU clock of 25 MHz (see definition in the AC Characteristics section).

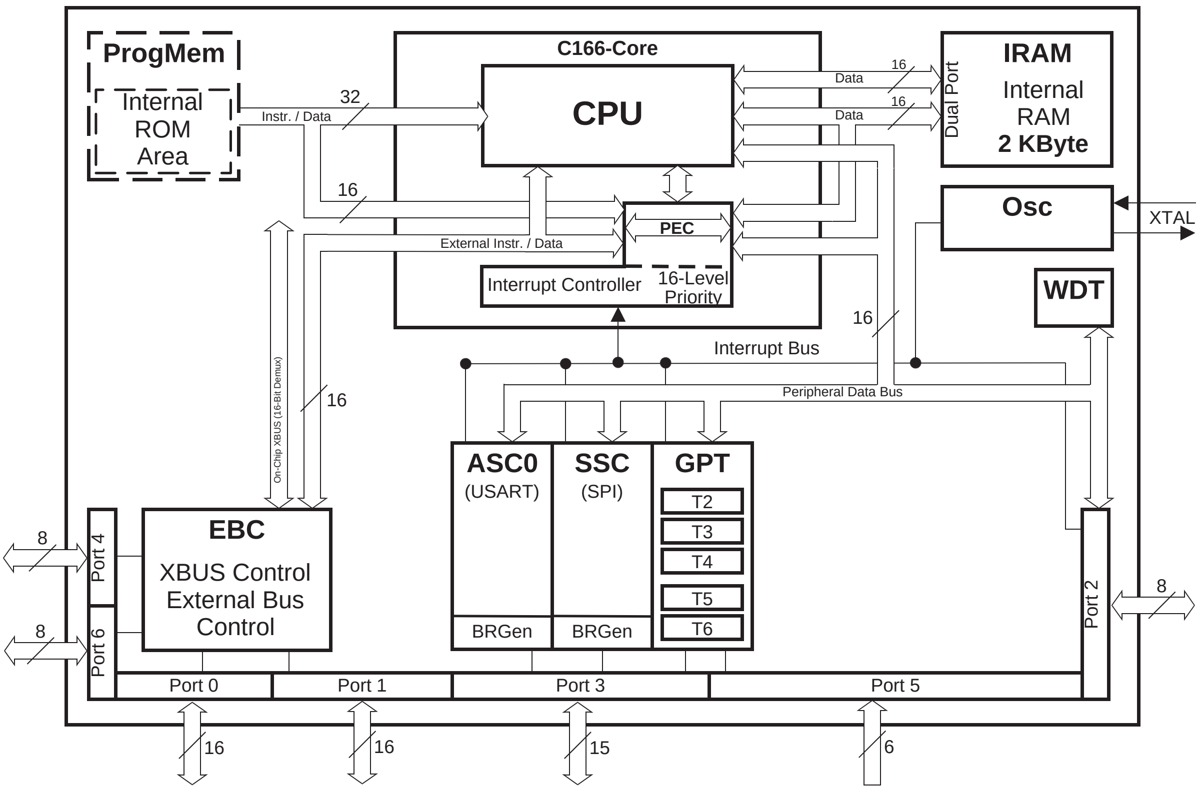

Figure 4 Block Diagram

The program memory, the internal RAM (IRAM) and the set of generic peripherals are connected to the CPU via separate buses. A fourth bus, the XBUS, connects external resources as well as additional on-chip resoures, the X-Peripherals (see **Figure 4**).

Memory Organization

The memory space of the C165 is configured in a Von Neumann architecture which means that code memory, data memory, registers and I/O ports are organized within the same linear address space which includes 16 MBytes. The entire memory space can be accessed bytewise or wordwise. Particular portions of the on-chip memory have additionally been made directly bitaddressable.

The C165 is prepared to incorporate on-chip program memory (not in the ROM-less derivatives, of course) for code or constant data. The internal ROM area can be mapped either to segment 0 or segment 1.

2 KBytes of on-chip Internal RAM (IRAM) are provided as a storage for user defined variables, for the system stack, general purpose register banks and even for code. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7, RH7) so-called General Purpose Registers (GPRs).

1024 bytes (2 × 512 bytes) of the address space are reserved for the Special Function Register areas (SFR space and ESFR space). SFRs are wordwide registers which are used for controlling and monitoring functions of the different on-chip units. Unused SFR addresses are reserved for future members of the C166 Family.

In order to meet the needs of designs where more memory is required than is provided on chip, up to 16 MBytes of external RAM and/or ROM can be connected to the microcontroller.

External Bus Controller

All of the external memory accesses are performed by a particular on-chip External Bus Controller (EBC). It can be programmed either to Single Chip Mode when no external memory is required, or to one of four different external memory access modes, which are as follows:

– 16-/18-/20-/24-bit Addresses, 16-bit Data, Demultiplexed
– 16-/18-/20-/24-bit Addresses, 16-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Multiplexed
– 16-/18-/20-/24-bit Addresses, 8-bit Data, Demultiplexed

In the demultiplexed bus modes, addresses are output on PORT1 and data is input/output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input/output.

Important timing characteristics of the external bus interface (Memory Cycle Time, Memory Tri-State Time, Length of ALE and Read Write Delay) have been made programmable to allow the user the adaption of a wide range of different types of memories and external peripherals.
In addition, up to 4 independent address windows may be defined (via register pairs ADDRSELx / BUSCONx) which control the access to different resources with different bus characteristics. These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1. All accesses to locations not covered by these 4 address windows are controlled by BUSCON0.

Up to 5 external $\overline{\text{CS}}$ signals (4 windows plus default) can be generated in order to save external glue logic. The C165 offers the possibility to switch the $\overline{\text{CS}}$ outputs to an unlatched mode. In this mode the internal filter logic is switched off and the $\overline{\text{CS}}$ signals are directly generated from the address. The unlatched $\overline{\text{CS}}$ mode is enabled by setting CSCFG (SYSCON.6).

Access to very slow memories or memories with varying access times is supported via a particular 'Ready' function.

A $\overline{\text{HOLD}}$/$\overline{\text{HLDA}}$ protocol is available for bus arbitration and allows to share external resources with other bus masters. The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7 … P6.5 ($\overline{\text{BREQ}}$, $\overline{\text{HLDA}}$, $\overline{\text{HOLD}}$) are automatically controlled by the EBC. In Master Mode (default after reset) the $\overline{\text{HLDA}}$ pin is an output. By setting bit DP6.7 to '1' the Slave Mode is selected where pin $\overline{\text{HLDA}}$ is switched to input. This allows to directly connect the slave controller to another master controller without glue logic.

For applications which require less than 16 MBytes of external memory space, this address space can be restricted to 1 MByte, 256 KByte, or to 64 KByte. In this case Port 4 outputs four, two, or no address lines at all. It outputs all 8 address lines, if an address space of 16 MBytes is used.

Central Processing Unit (CPU)

The main core of the CPU consists of a 4-stage instruction pipeline, a 16-bit arithmetic and logic unit (ALU) and dedicated SFRs. Additional hardware has been spent for a separate multiply and divide unit, a bit-mask generator and a barrel shifter.

Based on these hardware provisions, most of the C165's instructions can be executed in just one machine cycle which requires 80 ns at 25 MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle independent of the number of bits to be shifted. All multiple-cycle instructions have been optimized so that they can be executed very fast as well: branches in 2 cycles, a 16 × 16 bit multiplication in 5 cycles and a 32-/16 bit division in 10 cycles. Another pipeline optimization, the so-called 'Jump Cache', allows reducing the execution time of repeatedly performed jumps in a loop from 2 cycles to 1 cycle.

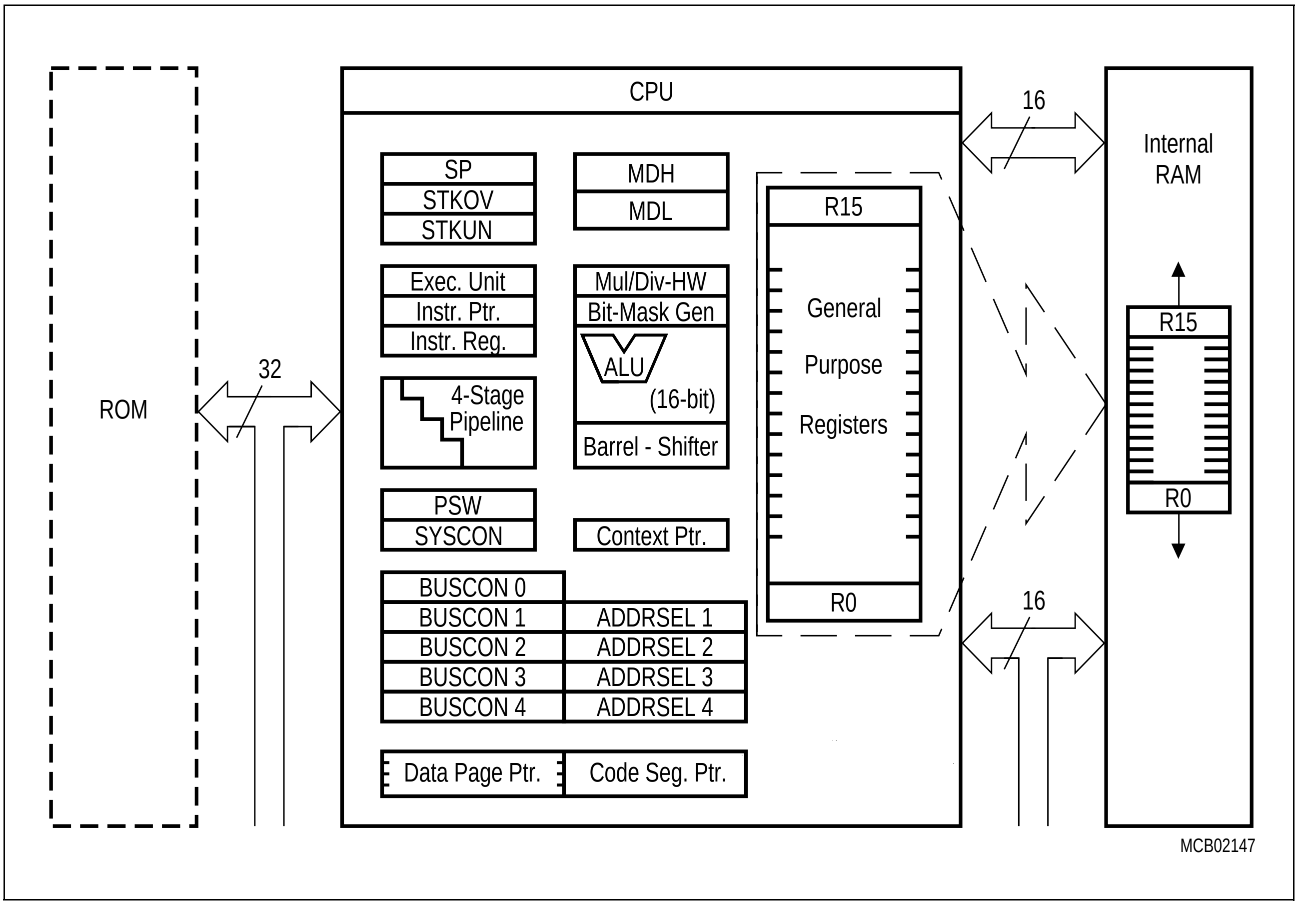

Figure 5 CPU Block Diagram

The CPU has a register context consisting of up to 16 wordwide GPRs at its disposal. These 16 GPRs are physically allocated within the on-chip RAM area. A Context Pointer (CP) register determines the base address of the active register bank to be accessed by the CPU at any time. The number of register banks is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 1024 words is provided as a storage for temporary data. The system stack is allocated in the on-chip RAM area, and it is accessed by the CPU via the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared against the stack pointer value upon each stack access for the detection of a stack overflow or underflow.

The high performance offered by the hardware implementation of the CPU can efficiently be utilized by a programmer via the highly efficient C165 instruction set which includes the following instruction classes:

– Arithmetic Instructions
– Logical Instructions
– Boolean Bit Manipulation Instructions
– Compare and Loop Control Instructions
– Shift and Rotate Instructions
– Prioritize Instruction
– Data Movement Instructions
– System Stack Instructions
– Jump and Call Instructions
– Return Instructions
– System Control Instructions
– Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

Interrupt System

With an interrupt response time within a range from just 5 to 12 CPU clocks (in case of internal program execution), the C165 is capable of reacting very fast to the occurrence of non-deterministic events.

The architecture of the C165 supports several mechanisms for fast and flexible response to service requests that can be generated from various sources internal or external to the microcontroller. Any of these interrupt requests can be programmed to being serviced by the Interrupt Controller or by the Peripheral Event Controller (PEC).

In contrast to a standard interrupt service where the current program execution is suspended and a branch to the interrupt vector table is performed, just one cycle is 'stolen' from the current CPU activity to perform a PEC service. A PEC service implies a single byte or word data transfer between any two memory locations with an additional increment of either the PEC source or the destination pointer. An individual PEC transfer counter is implicity decremented for each PEC service except when performing in the continuous transfer mode. When this counter reaches zero, a standard interrupt is performed to the corresponding source related vector location. PEC services are very well suited, for example, for supporting the transmission or reception of blocks of data. The C165 has 8 PEC channels each of which offers such fast interrupt-driven data transfer capabilities.

A separate control register which contains an interrupt request flag, an interrupt enable flag and an interrupt priority bitfield exists for each of the possible interrupt sources. Via its related register, each source can be programmed to one of sixteen interrupt priority levels. Once having been accepted by the CPU, an interrupt service can only be interrupted by a higher prioritized service request. For the standard interrupt processing, each of the possible interrupt sources has a dedicated vector location.

Fast external interrupt inputs are provided to service external interrupts with high precision requirements. These fast interrupt inputs feature programmable edge detection (rising edge, falling edge or both edges).

Software interrupts are supported by means of the 'TRAP' instruction in combination with an individual trap (interrupt) number.

Table 3 shows all of the possible C165 interrupt sources and the corresponding hardware-related interrupt flags, vectors, vector locations and trap (interrupt) numbers.

Note: Interrupt nodes which are not used by associated peripherals, may be used to generate software controlled interrupt requests by setting the respective interrupt request bit (xIR).

Table 3 C165 Interrupt Nodes

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
External Interrupt 0	CC8IR	CC8IE	CC8INT	$00'0060_H$	18_H
External Interrupt 1	CC9IR	CC9IE	CC9INT	$00'0064_H$	19_H
External Interrupt 2	CC10IR	CC10IE	CC10INT	$00'0068_H$	$1A_H$
External Interrupt 3	CC11IR	CC11IE	CC11INT	$00'006C_H$	$1B_H$
External Interrupt 4	CC12IR	CC12IE	CC12INT	$00'0070_H$	$1C_H$
External Interrupt 5	CC13IR	CC13IE	CC13INT	$00'0074_H$	$1D_H$
External Interrupt 6	CC14IR	CC14IE	CC14INT	$00'0078_H$	$1E_H$
External Interrupt 7	CC15IR	CC15IE	CC15INT	$00'007C_H$	$1F_H$
GPT1 Timer 2	T2IR	T2IE	T2INT	$00'0088_H$	22_H
GPT1 Timer 3	T3IR	T3IE	T3INT	$00'008C_H$	23_H
GPT1 Timer 4	T4IR	T4IE	T4INT	$00'0090_H$	24_H
GPT2 Timer 5	T5IR	T5IE	T5INT	$00'0094_H$	25_H
GPT2 Timer 6	T6IR	T6IE	T6INT	$00'0098_H$	26_H
GPT2 CAPREL Reg.	CRIR	CRIE	CRINT	$00'009C_H$	27_H
ASC0 Transmit	S0TIR	S0TIE	S0TINT	$00'00A8_H$	$2A_H$
ASC0 Transmit Buffer	S0TBIR	S0TBIE	S0TBINT	$00'011C_H$	47_H
ASC0 Receive	S0RIR	S0RIE	S0RINT	$00'00AC_H$	$2B_H$
ASC0 Error	S0EIR	S0EIE	S0EINT	$00'00B0_H$	$2C_H$
SSC Transmit	SCTIR	SCTIE	SCTINT	$00'00B4_H$	$2D_H$
SSC Receive	SCRIR	SCRIE	SCRINT	$00'00B8_H$	$2E_H$
SSC Error	SCEIR	SCEIE	SCEINT	$00'00BC_H$	$2F_H$
Unassigned node	XP0IR	XP0IE	XP0INT	$00'0100_H$	40_H
Unassigned node	XP1IR	XP1IE	XP1INT	$00'0104_H$	41_H
Unassigned node	XP2IR	XP2IE	XP2INT	$00'0108_H$	42_H
Unassigned node	XP3IR	XP3IE	XP3INT	$00'010C_H$	43_H
Unassigned node	CC29IR	CC29IE	CC29INT	$00'0110_H$	44_H
Unassigned node	CC30IR	CC30IE	CC30INT	$00'0114_H$	45_H
Unassigned node	CC31IR	CC31IE	CC31INT	$00'0118_H$	46_H

The C165 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 4 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 4 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location	Trap Number	Trap Priority
Reset Functions:	–				
– Hardware Reset		RESET	$00'0000_H$	00_H	III
– Software Reset		RESET	$00'0000_H$	00_H	III
– W-dog Timer Overflow		RESET	$00'0000_H$	00_H	III
Class A Hardware Traps:					
– Non-Maskable Interrupt	NMI	NMITRAP	$00'0008_H$	02_H	II
– Stack Overflow	STKOF	STOTRAP	$00'0010_H$	04_H	II
– Stack Underflow	STKUF	STUTRAP	$00'0018_H$	06_H	II
Class B Hardware Traps:					
– Undefined Opcode	UNDOPC	BTRAP	$00'0028_H$	$0A_H$	I
– Protected Instruction Fault	PRTFLT	BTRAP	$00'0028_H$	$0A_H$	I
– Illegal Word Operand Access	ILLOPA	BTRAP	$00'0028_H$	$0A_H$	I
– Illegal Instruction Access	ILLINA	BTRAP	$00'0028_H$	$0A_H$	I
– Illegal External Bus Access	ILLBUS	BTRAP	$00'0028_H$	$0A_H$	I
Reserved	–	–	$[2C_H – 3C_H]$	$[0B_H – 0F_H]$	–
Software Traps – TRAP Instruction	–	–	Any $[00'0000_H – 00'01FC_H]$ in steps of 4_H	Any $[00_H – 7F_H]$	Current CPU Priority

General Purpose Timer (GPT) Unit

The GPT unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication.

The GPT unit incorporates five 16-bit timers which are organized in two separate modules, GPT1 and GPT2. Each timer in each module may operate independently in a number of different modes, or may be concatenated with another timer of the same module.

Each of the three timers T2, T3, T4 of **module GPT1** can be configured individually for one of four basic modes of operation, which are Timer, Gated Timer, Counter, and Incremental Interface Mode. In Timer Mode, the input clock for a timer is derived from the CPU clock, divided by a programmable prescaler, while Counter Mode allows a timer to be clocked in reference to external events.
Pulse width or duty cycle measurement is supported in Gated Timer Mode, where the operation of a timer is controlled by the 'gate' level on an external input pin. For these purposes, each timer has one associated port pin (TxIN) which serves as gate or clock input. The maximum resolution of the timers in module GPT1 is 16 TCL.

The count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD) to facilitate e.g. position tracking.

In Incremental Interface Mode the GPT1 timers (T2, T3, T4) can be directly connected to the incremental position sensor signals A and B via their respective inputs TxIN and TxEUD. Direction and count signals are internally derived from these two input signals, so the contents of the respective timer Tx corresponds to the sensor position. The third position sensor signal TOP0 can be connected to an interrupt input.

Timer T3 has an output toggle latch (T3OTL) which changes its state on each timer overflow/underflow. The state of this latch may be output on pin T3OUT e.g. for time out monitoring of external hardware components, or may be used internally to clock timers T2 and T4 for measuring long time periods with high resolution.

In addition to their basic operating modes, timers T2 and T4 may be configured as reload or capture registers for timer T3. When used as capture or reload registers, timers T2 and T4 are stopped. The contents of timer T3 is captured into T2 or T4 in response to a signal at their associated input pins (TxIN). Timer T3 is reloaded with the contents of T2 or T4 triggered either by an external signal or by a selectable state transition of its toggle latch T3OTL. When both T2 and T4 are configured to alternately reload T3 on opposite state transitions of T3OTL with the low and high times of a PWM signal, this signal can be constantly generated without software intervention.

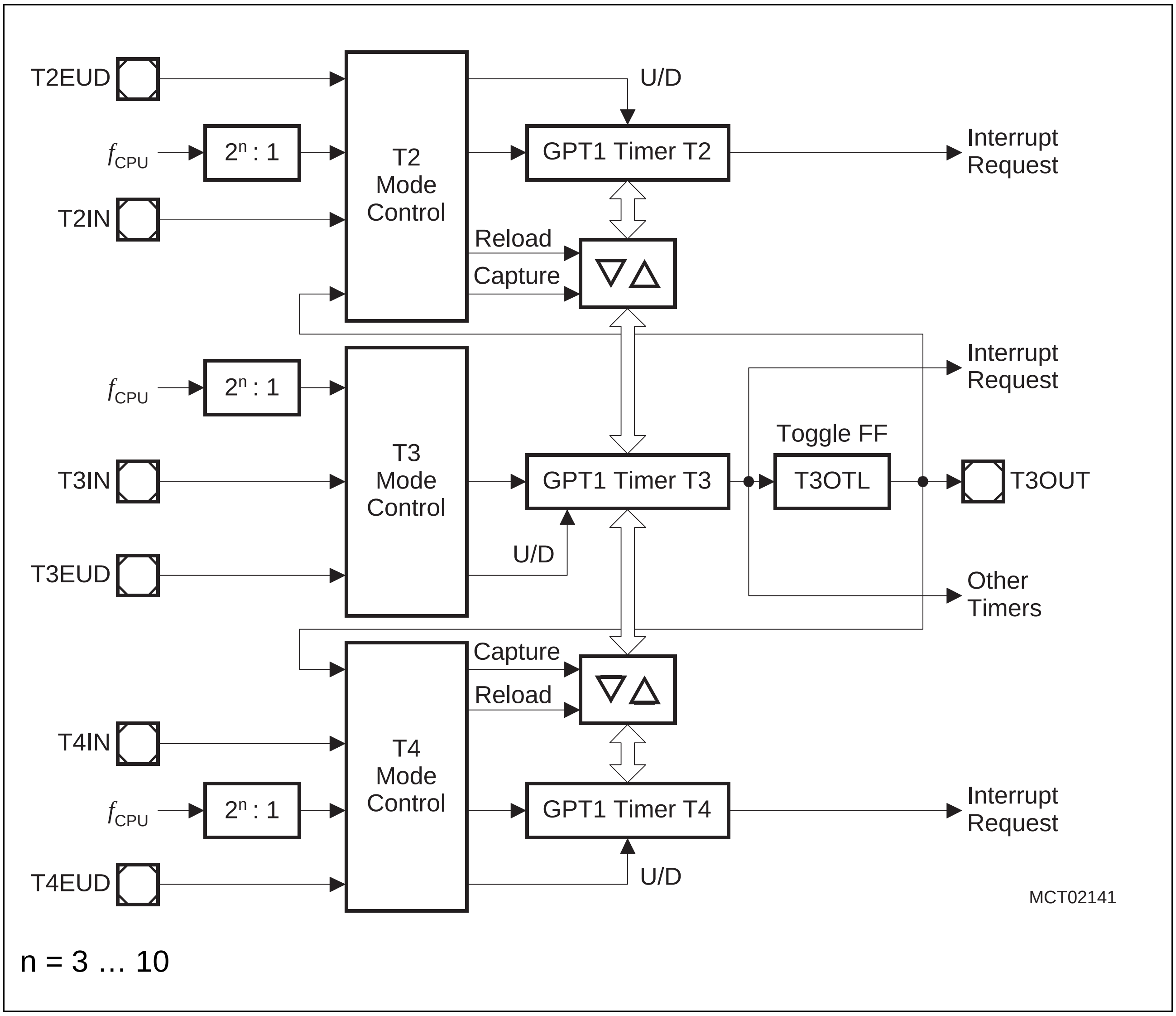

Figure 6　Block Diagram of GPT1

With its maximum resolution of 8 TCL, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock. The count direction (up/down) for each timer is programmable by software. Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5 and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can cause a reload from the CAPREL register. The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the C165 to measure absolute time differences or to perform pulse multiplication without software overhead.