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Data Sheet, V3.3, Feb. 2005

C167CR
C167SR

16-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

Edition 2005-02

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Revision History:	**2005-02**	V3.3
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Page	Subjects (major changes since last revision)
all	The layout of several graphics and text structures has been adapted to company documentation rules, obvious typographical errors have been corrected.
all	The contents of this document have been re-arranged into numbered sections and a table of contents has been added.
6	BGA-type added to product list
8	Pin designation corrected (pin 78)
9	Input threshold control added to Port 6
17 ... 25	Pin diagram and pin description for BGA package added
45	Port 6 added to input-threshold controlled ports
85	Mechanical package drawing corrected (P-MQFP-144-8)
86	Mechanical package drawing added (P-BGA-176-2)

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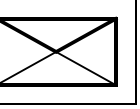

Table of Contents

1 Summary of Features

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80/60 ns Instruction Cycle Time at 25/33 MHz CPU Clock
  - 400/303 ns Multiplication (16 × 16 bits), 800/606 ns Division (32 / 16 bits)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40/30 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clock Generation via on-chip PLL (factors 1:1.5/2/2.5/3/4/5), via prescaler or via direct clock input
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Internal RAM (IRAM)
  - 2 Kbytes On-Chip Extension RAM (XRAM)
  - 128/32 Kbytes On-Chip Mask ROM
- On-Chip Peripheral Modules
  - 16-Channel 10-bit A/D Converter with Programmable Conversion Time down to 7.8 µs
  - Two 16-Channel Capture/Compare Units
  - 4-Channel PWM Unit
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
  - On-Chip CAN Interface (Rev. 2.0B active) with 15 Message Objects (Full CAN / Basic CAN)
- Up to 16 Mbytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle and Power Down Modes
- Programmable Watchdog Timer and Oscillator Watchdog

- Up to 111 General Purpose I/O Lines,
  partly with Selectable Input Thresholds and Hysteresis
- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader
- 144-Pin MQFP Package
- 176-Pin BGA Package[1)]

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set, the temperature range, and the supply voltage
- the package and the type of delivery.

For the available ordering codes for the C167CR please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

This document describes several derivatives of the C167 group. **Table 1** enumerates these derivatives and summarizes the differences. As this document refers to all of these derivatives, some descriptions may not apply to a specific product.

For simplicity all versions are referred to by the term **C167CR** throughout this document.

1) The external connections of the C167CR in P-BGA-176-2 are referred to as pins throughout this document, although they are mechanically realized as solder balls.

Table 1 C167CR Derivative Synopsis

Derivative[1)]	Program ROM Size	XRAM Size	Operating Frequency	Package
SAK-C167SR-LM SAB-C167SR-LM	–	2 Kbytes	25 MHz	P-MQFP-144-8
SAK-C167SR-L33M SAB-C167SR-L33M	–	2 Kbytes	33 MHz	P-MQFP-144-8
SAK-C167CR-LM SAF-C167CR-LM SAB-C167CR-LM	–	2 Kbytes	25 MHz	P-MQFP-144-8
SAK-C167CR-L33M SAB-C167CR-L33M	–	2 Kbytes	33 MHz	P-MQFP-144-8
SAK-C167CR-4RM SAB-C167CR-4RM	32 Kbytes	2 Kbytes	25 MHz	P-MQFP-144-8
SAK-C167CR-4R33M SAB-C167CR-4R33M	32 Kbytes	2 Kbytes	33 MHz	P-MQFP-144-8
SAK-C167CR-16RM	128 Kbytes	2 Kbytes	25 MHz	P-MQFP-144-8
SAK-C167CR-16R33M	128 Kbytes	2 Kbytes	33 MHz	P-MQFP-144-8
SAK-C167CR-LE	–	2 Kbytes	25 MHz	P-BGA-176-2

1) This Data Sheet is valid for devices manufactured in 0.5 µm technology, i.e. devices starting with and including design step GA(-T)6.

2 General Device Information

2.1 Introduction

The C167CR derivatives are high performance derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 16.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules such as program ROM, internal RAM, and extension RAM.

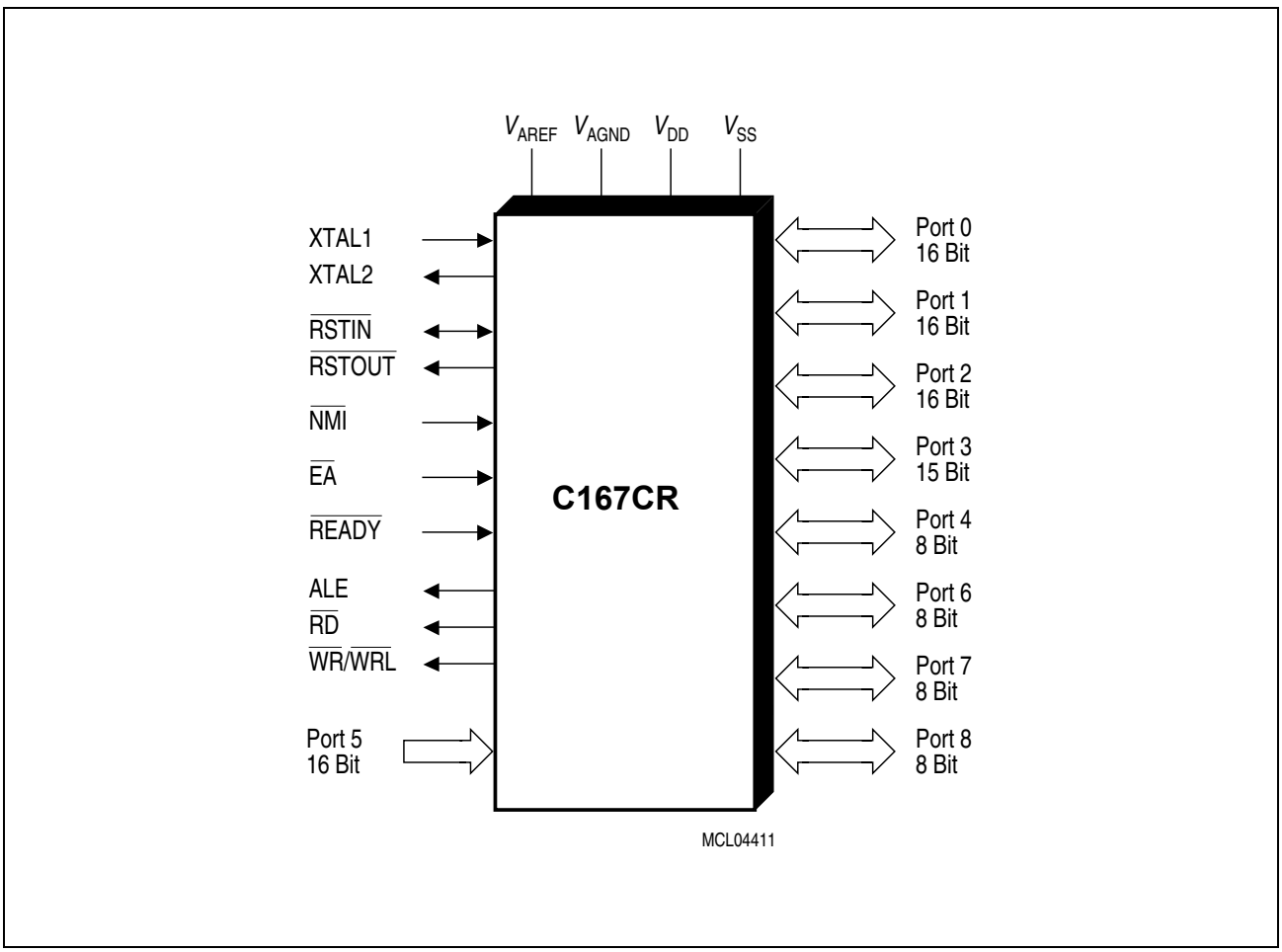

Figure 1 Logic Symbol

2.2 Pin Configuration and Definition for P-MQFP-144-8

The pins of the C167CR are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package.

*Note: The P-BGA-176-2 is described in **Table 3** and **Figure 3**.*

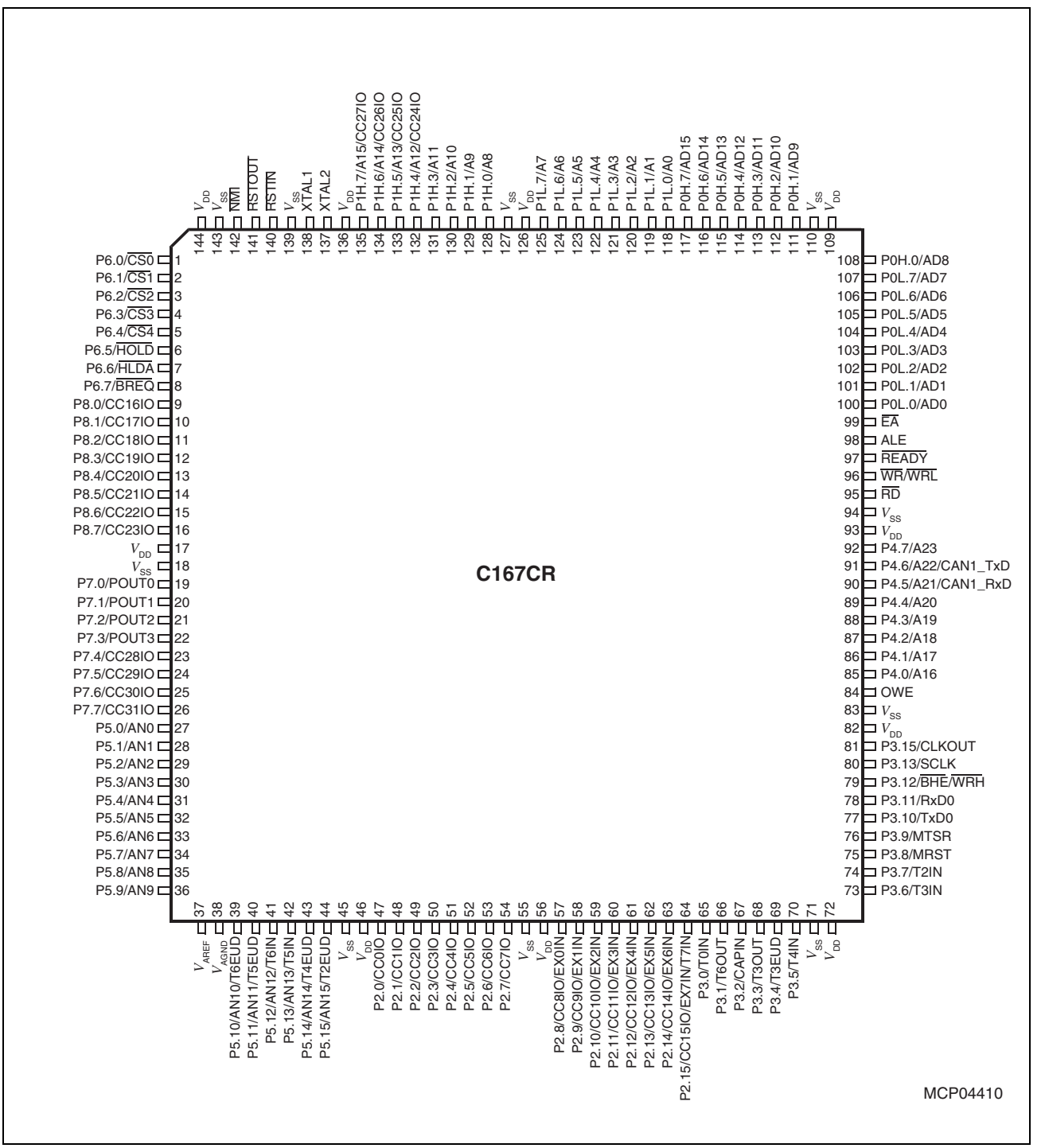

Figure 2 Pin Configuration P-MQFP-144-8 (top view)

Table 2 Pin Definitions and Functions P-MQFP-144-8

Symbol	Pin No.	Input Outp.	Function
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or special). The Port 6 pins also serve for alternate functions:
P6.0	1	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	2	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	3	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	4	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	5	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	6	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	7	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	8	O	$\overline{BREQ}$ Bus Request Output
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	9	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	11	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	12	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	13	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	14	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	15	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	16	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	19	O	POUT0 PWM Channel 0 Output
P7.1	20	O	POUT1 PWM Channel 1 Output
P7.2	21	O	POUT2 PWM Channel 2 Output
P7.3	22	O	POUT3 PWM Channel 3 Output
P7.4	23	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	24	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	25	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	26	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	27	I	AN0
P5.1	28	I	AN1
P5.2	29	I	AN2
P5.3	30	I	AN3
P5.4	31	I	AN4
P5.5	32	I	AN5
P5.6	33	I	AN6
P5.7	34	I	AN7
P5.8	35	I	AN8
P5.9	36	I	AN9
P5.10	39	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	40	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	41	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	42	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	43	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	44	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P2		IO	Port 2 is a 16-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 2 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 2 is selectable (TTL or special). The following Port 2 pins also serve for alternate functions:	
P2.0	47	I/O	CC0IO	CAPCOM1: CC0 Capture Inp./Compare Output
P2.1	48	I/O	CC1IO	CAPCOM1: CC1 Capture Inp./Compare Output
P2.2	49	I/O	CC2IO	CAPCOM1: CC2 Capture Inp./Compare Output
P2.3	50	I/O	CC3IO	CAPCOM1: CC3 Capture Inp./Compare Output
P2.4	51	I/O	CC4IO	CAPCOM1: CC4 Capture Inp./Compare Output
P2.5	52	I/O	CC5IO	CAPCOM1: CC5 Capture Inp./Compare Output
P2.6	53	I/O	CC6IO	CAPCOM1: CC6 Capture Inp./Compare Output
P2.7	54	I/O	CC7IO	CAPCOM1: CC7 Capture Inp./Compare Output
P2.8	57	I/O	CC8IO	CAPCOM1: CC8 Capture Inp./Compare Output,
		I	EX0IN	Fast External Interrupt 0 Input
P2.9	58	I/O	CC9IO	CAPCOM1: CC9 Capture Inp./Compare Output,
		I	EX1IN	Fast External Interrupt 1 Input
P2.10	59	I/O	CC10IO	CAPCOM1: CC10 Capture Inp./Compare Outp.,
		I	EX2IN	Fast External Interrupt 2 Input
P2.11	60	I/O	CC11IO	CAPCOM1: CC11 Capture Inp./Compare Outp.,
		I	EX3IN	Fast External Interrupt 3 Input
P2.12	61	I/O	CC12IO	CAPCOM1: CC12 Capture Inp./Compare Outp.,
		I	EX4IN	Fast External Interrupt 4 Input
P2.13	62	I/O	CC13IO	CAPCOM1: CC13 Capture Inp./Compare Outp.,
		I	EX5IN	Fast External Interrupt 5 Input
P2.14	63	I/O	CC14IO	CAPCOM1: CC14 Capture Inp./Compare Outp.,
		I	EX6IN	Fast External Interrupt 6 Input
P2.15	64	I/O	CC15IO	CAPCOM1: CC15 Capture Inp./Compare Outp.,
		I	EX7IN	Fast External Interrupt 7 Input,
		I	T7IN	CAPCOM2: Timer T7 Count Input

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	65	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	66	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	67	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	68	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	69	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	70	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	73	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	74	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	75	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	76	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	77	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	78	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	79	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe
P3.13	80	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	81	O	CLKOUT	System Clock Output (= CPU Clock)
OWE (V_{PP})	84	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pull-up device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 µA.	

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	85	O	A16 Least Significant Segment Address Line
P4.1	86	O	A17 Segment Address Line
P4.2	87	O	A18 Segment Address Line
P4.3	88	O	A19 Segment Address Line
P4.4	89	O	A20 Segment Address Line
P4.5	90	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	91	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	92	O	A23 Most Significant Segment Address Line
RD	95	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.
$\overline{WR}$/ $\overline{WRL}$	96	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	97	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pull-up device will hold this pin high when nothing is driving it.
ALE	98	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
$\overline{EA}$	99	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
PORT0		IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0
P0L.0-7	100-107		
P0H.0-7	108, 111-117		
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode. The following PORT1 pins also serve for alternate functions:
P1L.0-7	118-125		
P1H.0-7	128-135		
P1H.4	132	I	CC24IO CAPCOM2: CC24 Capture Input
P1H.5	133	I	CC25IO CAPCOM2: CC25 Capture Input
P1H.6	134	I	CC26IO CAPCOM2: CC26 Capture Input
P1H.7	135	I	CC27IO CAPCOM2: CC27 Capture Input
XTAL2	137	O	XTAL2: Output of the oscillator amplifier circuit.
XTAL1	138	I	XTAL1: Input to the oscillator amplifier and input to the internal clock generator To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
$\overline{\text{RSTIN}}$	140	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C167CR. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*
$\overline{\text{RSTOUT}}$	141	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{NMI}}$	142	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{\text{NMI}}$ pin must be low in order to force the C167CR to go into power down mode. If $\overline{\text{NMI}}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{\text{NMI}}$ should be pulled high externally.
V_{AREF}	37	–	Reference voltage for the A/D converter.
V_{AGND}	38	–	Reference ground for the A/D converter.

Table 2 Pin Definitions and Functions P-MQFP-144-8 (cont'd)

Symbol	Pin No.	Input Outp.	Function
V_{DD}	17, 46, 56, 72, 82, 93, 109, 126, 136, 144	–	Digital Supply Voltage: + 5 V during normal operation and idle mode. ≥ 2.5 V during power down mode.
V_{SS}	18, 45, 55, 71, 83, 94, 110, 127, 139, 143	–	Digital Ground.

Note: The following behavioural differences must be observed when the bidirectional reset is active:

- Bit BDRSTEN in register SYSCON cannot be changed after EINIT and is cleared automatically after a reset.
- The reset indication flags always indicate a long hardware reset.
- The PORT0 configuration is treated as if it were a hardware reset. In particular, the bootstrap loader may be activated when P0L.4 is low.
- Pin $\overline{\text{RSTIN}}$ may only be connected to external reset devices with an open drain output driver.
- A short hardware reset is extended to the duration of the internal reset sequence.

2.3 Pin Configuration and Definition for P-BGA-176-2

The pins[1)] of the C167CR are described in detail in **Table 3**, including all their alternate functions. **Figure 3** summarizes all pins in a condensed way, showing their location on the bottom of the package.

*Note: The P-MQFP-144-8 is described in **Table 2** and **Figure 2**.*

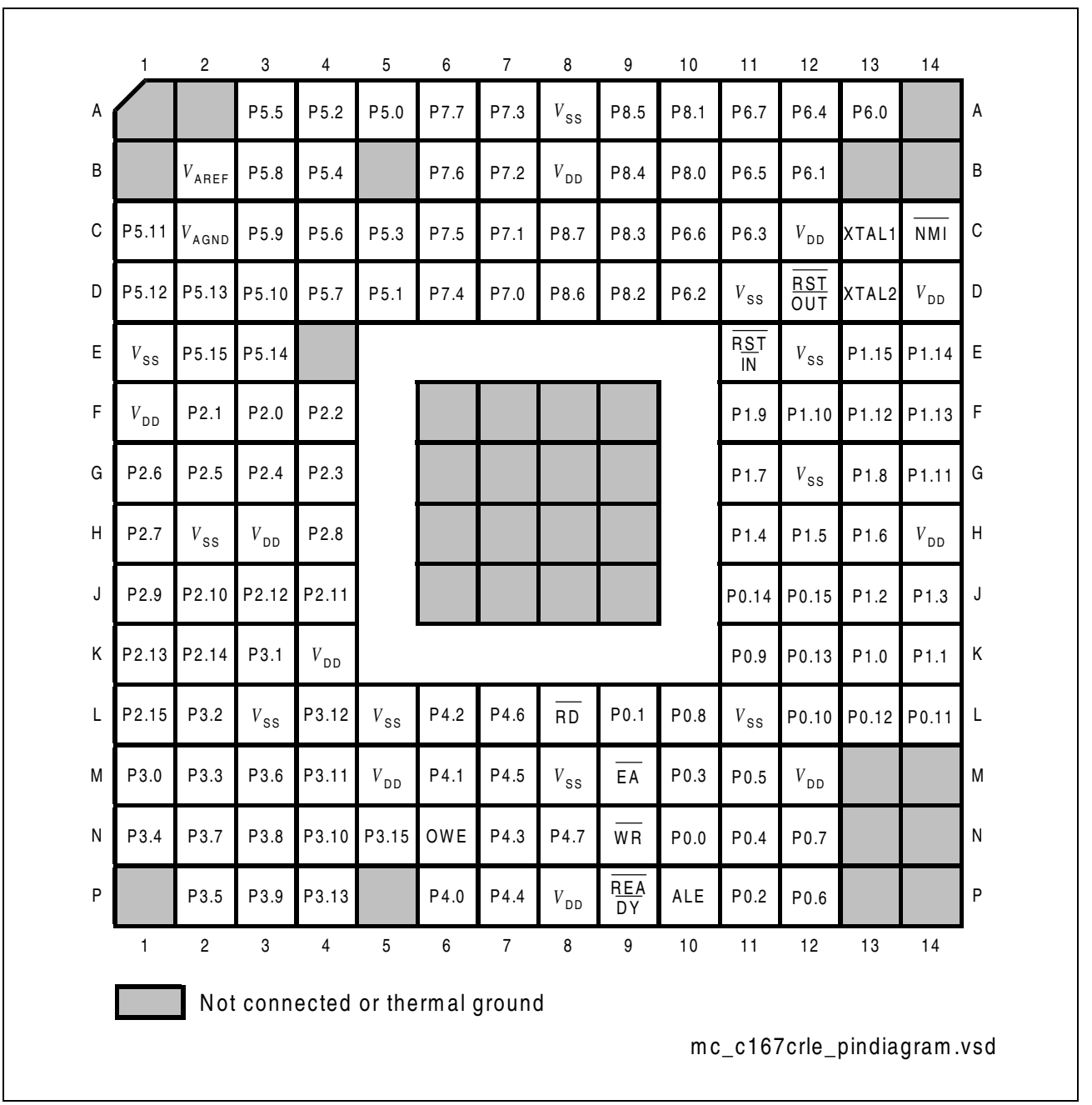

Figure 3 Pin Configuration P-BGA-176-2 (top view)

1) The external connections of the C167CR in P-BGA-176-2 are referred to as pins throughout this document, although they are mechanically realized as solder balls.

Table 3 Pin Definitions and Functions P-BGA-176-2

Symbol	Pin Num.	Input Outp.	Function
P5		I	Port 5 is a 16-bit input-only port with Schmitt-Trigger characteristic. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:
P5.0	A5	I	AN0
P5.1	D5	I	AN1
P5.2	A4	I	AN2
P5.3	C5	I	AN3
P5.4	B4	I	AN4
P5.5	A3	I	AN5
P5.6	C4	I	AN6
P5.7	D4	I	AN7
P5.8	B3	I	AN8
P5.9	C3	I	AN9
P5.10	D3	I	AN10, T6EUD GPT2 Timer T6 Ext. Up/Down Ctrl. Inp.
P5.11	C1	I	AN11, T5EUD GPT2 Timer T5 Ext. Up/Down Ctrl. Inp.
P5.12	D1	I	AN12, T6IN GPT2 Timer T6 Count Inp.
P5.13	D2	I	AN13, T5IN GPT2 Timer T5 Count Inp.
P5.14	E3	I	AN14, T4EUD GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	E2	I	AN15, T2EUD GPT1 Timer T5 Ext. Up/Down Ctrl. Inp.
P7		IO	Port 7 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 7 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 7 is selectable (TTL or special). The following Port 7 pins also serve for alternate functions:
P7.0	D7	O	POUT0 PWM Channel 0 Output
P7.1	C7	O	POUT1 PWM Channel 1 Output
P7.2	B7	O	POUT2 PWM Channel 2 Output
P7.3	A7	O	POUT3 PWM Channel 3 Output
P7.4	D6	I/O	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp.
P7.5	C6	I/O	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp.
P7.6	B6	I/O	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp.
P7.7	A6	I/O	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
P8		IO	Port 8 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 8 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 8 is selectable (TTL or special). The following Port 8 pins also serve for alternate functions:
P8.0	B10	I/O	CC16IO CAPCOM2: CC16 Capture Inp./Compare Outp.
P8.1	A10	I/O	CC17IO CAPCOM2: CC17 Capture Inp./Compare Outp.
P8.2	D9	I/O	CC18IO CAPCOM2: CC18 Capture Inp./Compare Outp.
P8.3	C9	I/O	CC19IO CAPCOM2: CC19 Capture Inp./Compare Outp.
P8.4	B9	I/O	CC20IO CAPCOM2: CC20 Capture Inp./Compare Outp.
P8.5	A9	I/O	CC21IO CAPCOM2: CC21 Capture Inp./Compare Outp.
P8.6	D8	I/O	CC22IO CAPCOM2: CC22 Capture Inp./Compare Outp.
P8.7	C8	I/O	CC23IO CAPCOM2: CC23 Capture Inp./Compare Outp.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 6 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 6 is selectable (TTL or special). The Port 6 pins also serve for alternate functions:
P6.0	A13	O	$\overline{CS0}$ Chip Select 0 Output
P6.1	B12	O	$\overline{CS1}$ Chip Select 1 Output
P6.2	D10	O	$\overline{CS2}$ Chip Select 2 Output
P6.3	C11	O	$\overline{CS3}$ Chip Select 3 Output
P6.4	A12	O	$\overline{CS4}$ Chip Select 4 Output
P6.5	B11	I	$\overline{HOLD}$ External Master Hold Request Input
P6.6	C10	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode)
P6.7	A11	O	$\overline{BREQ}$ Bus Request Output
$\overline{NMI}$	C14	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the $\overline{NMI}$ pin must be low in order to force the C167CR to go into power down mode. If $\overline{NMI}$ is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin $\overline{NMI}$ should be pulled high externally.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
XTAL2 XTAL1	D13 C13	O I	XTAL2: Output of the oscillator amplifier circuit. XTAL1: Input to the oscillator amplifier and input to the internal clock generator. To clock the device from an external source, drive XTAL1, while leaving XTAL2 unconnected. Minimum and maximum high/low and rise/fall times specified in the AC Characteristics must be observed.
$\overline{\text{RSTOUT}}$	D12	O	Internal Reset Indication Output. This pin is set to a low level when the part is executing either a hardware-, a software- or a watchdog timer reset. $\overline{\text{RSTOUT}}$ remains low until the EINIT (end of initialization) instruction is executed.
$\overline{\text{RSTIN}}$	E11	I/O	Reset Input with Schmitt-Trigger characteristics. A low level at this pin while the oscillator is running resets the C167CR. An internal pull-up resistor permits power-on reset using only a capacitor connected to V_{SS}. A spike filter suppresses input pulses < 10 ns. Input pulses > 100 ns safely pass the filter. The minimum duration for a safe recognition should be 100 ns + 2 CPU clock cycles. In bidirectional reset mode (enabled by setting bit BDRSTEN in register SYSCON) the $\overline{\text{RSTIN}}$ line is internally pulled low for the duration of the internal reset sequence upon any reset (HW, SW, WDT). See note below this table. *Note: To let the reset configuration of PORT0 settle and to let the PLL lock a reset duration of ca. 1 ms is recommended.*

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes and also after switching from a demultiplexed bus mode to a multiplexed bus mode.
P1L.0-7	K13, K14, J13, J14, H11, H12, H13, G11		
P1H.0-3	G13, F11, F12, G14		
			The following PORT1 pins also serve for alternate functions:
P1H.4	F13	I	CC24IO CAPCOM2: CC24 Capture Input
P1H.5	F14	I	CC25IO CAPCOM2: CC25 Capture Input
P1H.6	E14	I	CC26IO CAPCOM2: CC26 Capture Input
P1H.7	E13	I	CC27IO CAPCOM2: CC27 Capture Input
PORT0		IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0
P0L.0-7	N10, L9, P11, M10, N11, M11, P12, N12		
P0H.0-7	L10, K11, L12, L14, L13, K12, J11, J12		
$\overline{RD}$	L8	O	External Memory Read Strobe. $\overline{RD}$ is activated for every external instruction or data read access.

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function
$\overline{EA}$	M9	I	External Access Enable pin. A low level at this pin during and after Reset forces the C167CR to begin instruction execution out of external memory. A high level forces execution out of the internal program memory. "ROMless" versions must have this pin tied to '0'.
$\overline{WR}$/ $\overline{WRL}$	N9	O	External Memory Write Strobe. In $\overline{WR}$-mode this pin is activated for every external data write access. In $\overline{WRL}$-mode this pin is activated for low byte data write accesses on a 16-bit bus, and for every data write access on an 8-bit bus. See WRCFG in register SYSCON for mode selection.
$\overline{READY}$	P9	I	Ready Input. When the Ready function is enabled, a high level at this pin during an external memory access will force the insertion of memory cycle time waitstates until the pin returns to a low level. An internal pull-up device will hold this pin high when nothing is driving it.
ALE	P10	O	Address Latch Enable Output. Can be used for latching the address into external memory or an address latch in the multiplexed bus modes.
P4		IO	Port 4 is an 8-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 4 can be used to output the segment address lines and for serial bus interfaces:
P4.0	P6	O	A16 Least Significant Segment Address Line
P4.1	M6	O	A17 Segment Address Line
P4.2	L6	O	A18 Segment Address Line
P4.3	N7	O	A19 Segment Address Line
P4.4	P7	O	A20 Segment Address Line
P4.5	M7	O	A21 Segment Address Line,
		I	CAN1_RxD CAN 1 Receive Data Input
P4.6	L7	O	A22 Segment Address Line,
		O	CAN1_TxD CAN 1 Transmit Data Output
P4.7	N8	O	A23 Most Significant Segment Address Line

Table 3 Pin Definitions and Functions P-BGA-176-2 (cont'd)

Symbol	Pin Num.	Input Outp.	Function	
OWE (V_{PP})	N6	I	Oscillator Watchdog Enable. This input enables the oscillator watchdog when high or disables it when low e.g. for testing purposes. An internal pull-up device holds this input high if nothing is driving it. For normal operation pin OWE should be high or not connected. In order to drive pin OWE low draw a current of at least 200 µA.	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. It is bit-wise programmable for input or output via direction bits. For a pin configured as input, the output driver is put into high-impedance state. Port 3 outputs can be configured as push/pull or open drain drivers. The input threshold of Port 3 is selectable (TTL or special). The following Port 3 pins also serve for alternate functions:	
P3.0	M1	I	T0IN	CAPCOM1 Timer T0 Count Input
P3.1	K3	O	T6OUT	GPT2 Timer T6 Toggle Latch Output
P3.2	L2	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	M2	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	N1	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	P2	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp.
P3.6	M3	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	N2	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp.
P3.8	N3	I/O	MRST	SSC Master-Receive/Slave-Transmit Inp./Outp.
P3.9	P3	I/O	MTSR	SSC Master-Transmit/Slave-Receive Outp./Inp.
P3.10	N4	O	TxD0	ASC0 Clock/Data Output (Async./Sync.)
P3.11	M4	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.)
P3.12	L4	O	$\overline{BHE}$	External Memory High Byte Enable Signal,
		O	$\overline{WRH}$	External Memory High Byte Write Strobe
P3.13	P4	I/O	SCLK	SSC Master Clock Output / Slave Clock Input.
P3.15	N5	O	CLKOUT	System Clock Output (= CPU Clock)