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Data Sheet, Dec. 2000

C505
C505C
C505A
C505CA

8-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

Edition 2000-12

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C505/C505C/C505A/C505CA Data Sheet Revision History : Current Version : 2000-12		
Previous Releases :		08.00, 06.00, 07.99, 12.97
Page (in previous version	Page (in current version)	Subjects (major changes since last revision)
24	24	Version register VR2 for C505A-4R/C505CA-4R BB step is updated.

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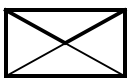


8-Bit Single-Chip Microcontroller
C500 Family

C505/C505C/C505A/
C505CA

Advance Information

- Fully compatible to standard 8051 microcontroller
- Superset of the 8051 architecture with 8 datapointers
- Up to 20 MHz operating frequency
  - 375 ns instruction cycle time @16 MHz
  - 300 ns instruction cycle time @20 MHz (50 % duty cycle)
- On-chip program memory (with optional memory protection)
  - C505(C)(A)-2R : 16K byte on-chip ROM
  - C505A-4R/C505CA-4R: 32K byte on-chip ROM
  - C505A-4E/C505CA-4E: 32K byte on-chip OTP
  - alternatively up to 64k byte external program memory
- 256 byte on-chip RAM
- On-chip XRAM
  - C505/C505C : 256 byte
  - C505A/C505CA : 1K byte

(more features on next page)

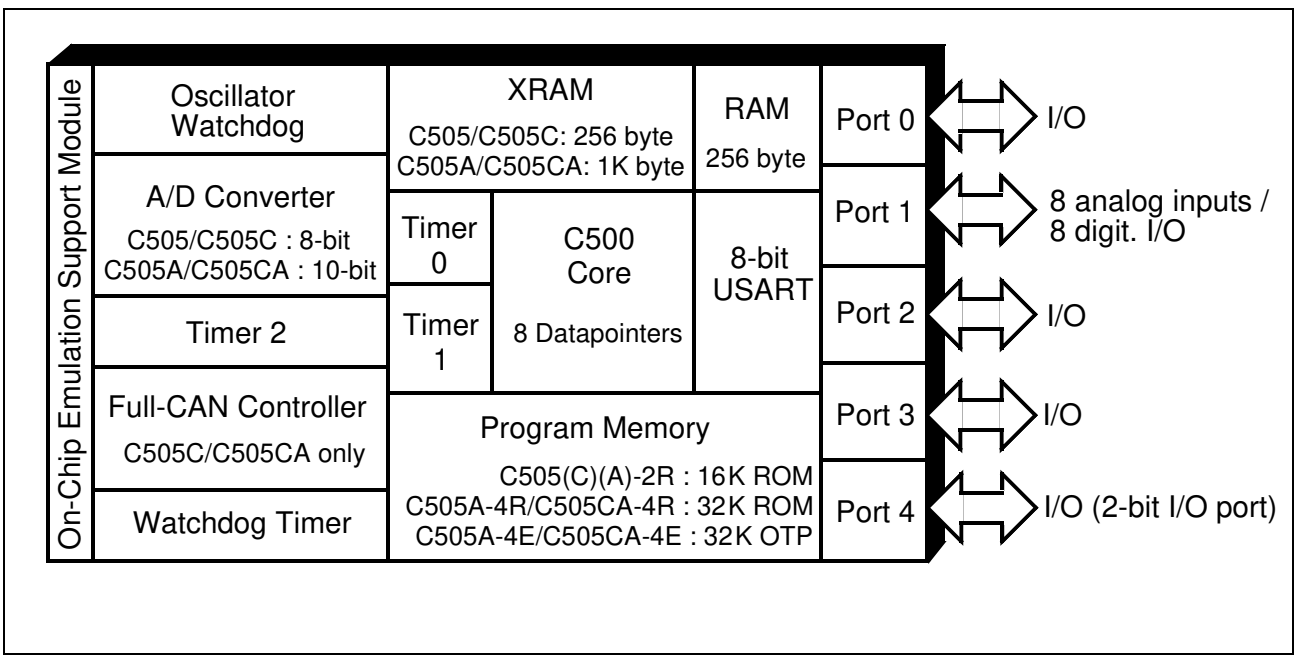


Figure 1
C505 Functional Units

Features (continued) :

- 32 + 2 digital I/O lines
  - Four 8-bit digital I/O ports
  - One 2-bit digital I/O port (port 4)
  - Port 1 with mixed analog/digital I/O capability
- Three 16-bit timers/counters
  - Timer 0 / 1 (C501 compatible)
  - Timer 2 with 4 channels for 16-bit capture/compare operation
- Full duplex serial interface with programmable baudrate generator (USART)
- Full CAN Module, version 2.0 B compliant (C505C and C505CA only)
  - 256 register/data bytes located in external data memory area
  - 1 MBaud CAN baudrate when operating frequency is equal to or above 8 MHz
  - internal CAN clock prescaler when input frequency is over 10 MHz
- On-chip A/D Converter
  - up to 8 analog inputs
  - C505/C505C : 8-bit resolution
  - C505A/C505CA: 10-bit resolution
- Twelve interrupt sources with four priority levels
- On-chip emulation support logic (Enhanced Hooks Technology ™)
- Programmable 15-bit watchdog timer
- Oscillator watchdog
- Fast power on reset
- Power Saving Modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake up capability through P3.2/$\overline{\text{INT0}}$ or P4.1/RXDC pin
- P-MQFP-44 package
- Pin configuration is compatible to C501, C504, C511/C513-family
- Temperature ranges:

SAB-C505 versions	T_A = 0 to 70 °C
SAF-C505 versions	T_A = -40 to 85°C
SAH-C505 versions	T_A = -40 to 110°C
SAK-C505 versions	T_A = -40 to 125°C

Table 1
Differences in Functionality of the C505 MCUs

Device	Internal Program Memory		XRAM Size	A/D Converter Resolution	CAN Controller
	ROM	OTP			
C505-2R	16K byte	–	256 byte	8 Bit	–
C505-L	–	–	256 byte	8 Bit	–
C505C-2R	16K byte	–	256 byte	8 Bit	√
C505C-L	–	–	256 byte	8 Bit	√
C505A-4R	32K byte	–	1K byte	10 Bit	–
C505A-2R	16K byte	–	1K byte	10 Bit	–
C505A-L	–	–	1K byte	10 Bit	–
C505CA-4R	32K byte	–	1K byte	10 Bit	√
C505CA-2R	16K byte	–	1K byte	10 Bit	√
C505CA-L	–	–	1K byte	10 Bit	√
C505A-4E	–	32K byte	1K byte	10 Bit	–
C505CA-4E	–	32K byte	1K byte	10 Bit	√

Note: The term C505 refers to all versions described within this document unless otherwise noted. However the term C505 may also be restricted by the context to refer to only CAN-less derivatives with 8-Bit ADC which are C505-2R and C505-L in this document.

Note: The term C505(C)(A)-2R, for simplicity, is used to stand for C505 16K byte ROM versions within this document which are C505-2R, C505C-2R, C505A-2R and C505CA-2R.

Ordering Information

The ordering code for Infineon Technologies' microcontrollers provides an exact reference to the required product. This ordering code identifies:

- the derivative itself, i.e. its function set
- the specificed temperature rage
- the package and the type of delivery

For the available ordering codes for the C505 please refer to the "**Product information Microcontrollers**", which summarizes all available microcontroller variants.

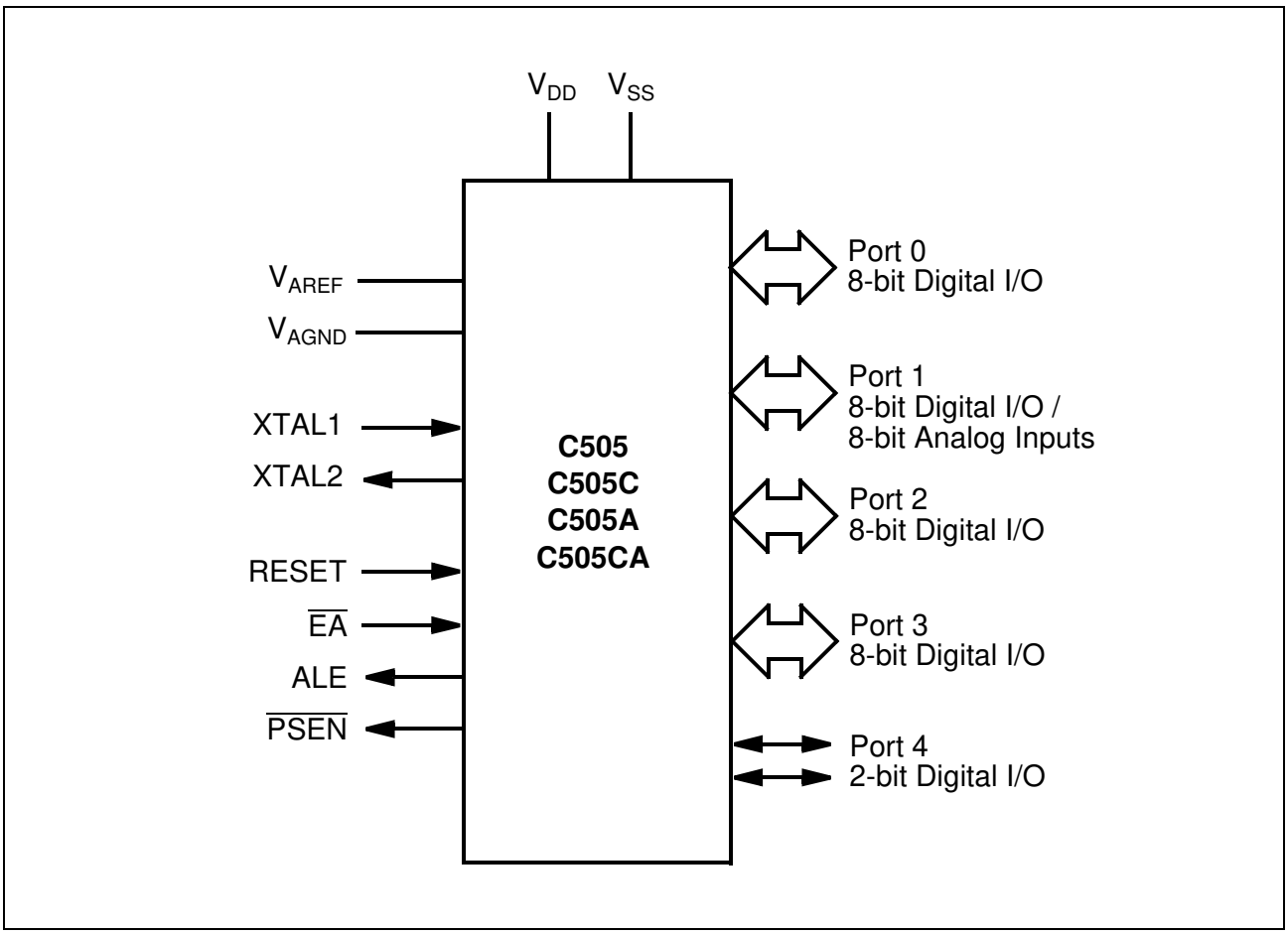


Figure 2
Logic Symbol

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

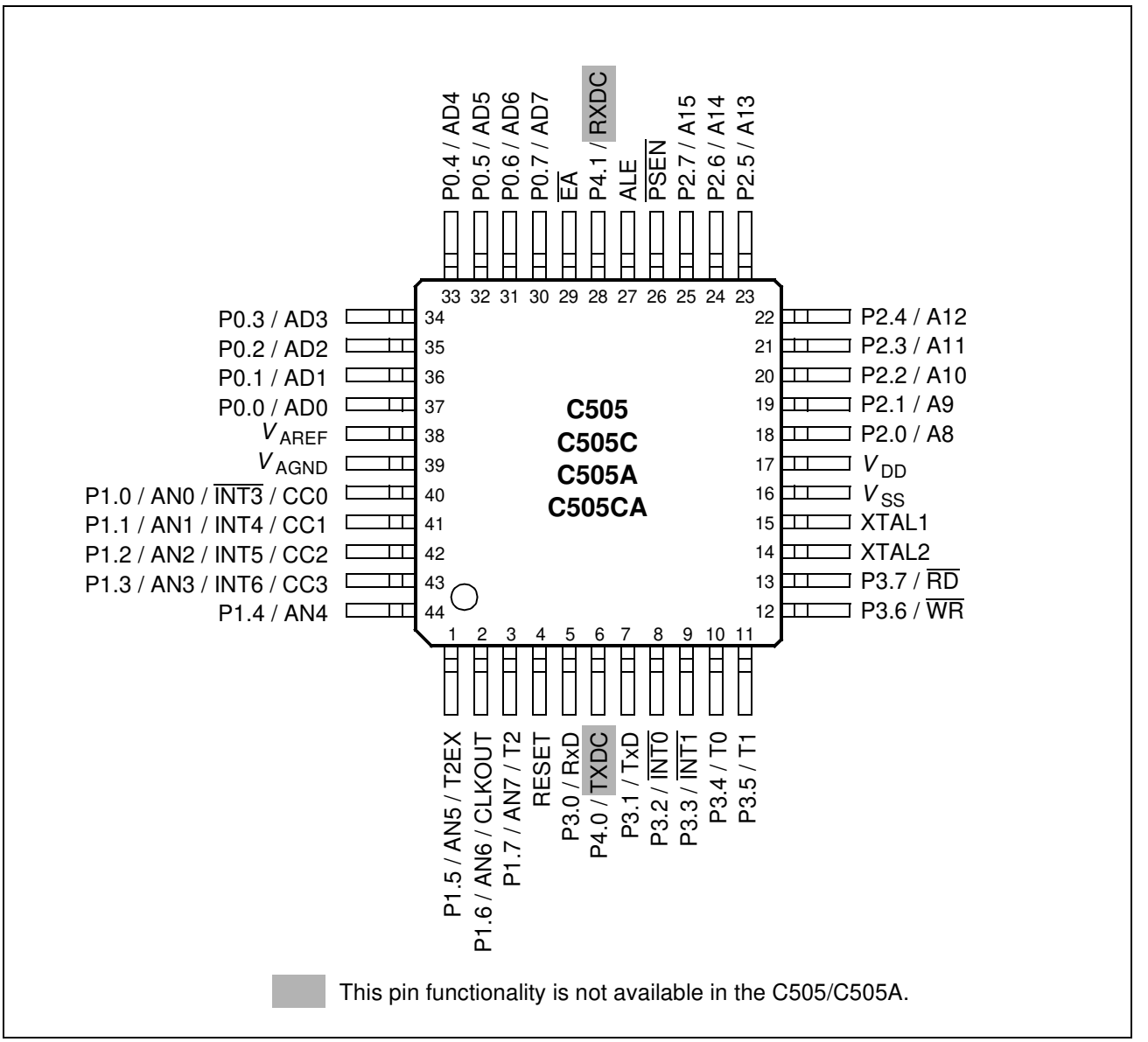


Figure 3
C505 Pin Configuration P-MQFP-44 Package (Top View)

Table 2
Pin Definitions and Functions

Symbol	Pin Number	I/O *)	Function
P1.0-P1.7	40-44,1-3	I/O	**Port 1** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 1 pins can be used for digital input/output or as analog inputs of the A/D converter. Port 1 pins that have 1's written to them are pulled high by internal pull-up transistors and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. As secondary digital functions, port 1 contains the interrupt, timer, clock, capture and compare pins. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for compare functions). The secondary functions are assigned to the pins of port 1 as follows: 40 P1.0 / AN0 / $\overline{\text{INT3}}$ / CC0 — Analog input channel 0 interrupt 3 input / capture/compare channel 0 I/O 41 P1.1 / AN1 / INT4 / CC1 — Analog input channel 1/ interrupt 4 input / capture/compare channel 1 I/O 42 P1.2 / AN2 / INT5 / CC2 — Analog input channel 2 / interrupt 5 input / capture/compare channel 2 I/O 43 P1.3 / AN3 / INT6 / CC3 — Analog input channel 3 interrupt 6 input / capture/compare channel 3 I/O 44 P1.4 / AN4 — Analog input channel 4 1 P1.5 / AN5 / T2EX — Analog input channel 5 / Timer 2 external reload / trigger input 2 P1.6 / AN6 / CLKOUT — Analog input channel 6 / system clock output 3 P1.7 / AN7 / T2 — Analog input channel 7 / counter 2 input Port 1 is used for the low-order address byte during program verification of the C505 ROM versions (i.e. C505(C)(A)-2R/ C505A-4R/C505CA-4R).

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
RESET	4	I	**RESET** A high level on this pin for two machine cycle while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{DD}.
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 3 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for TxD and $\overline{WR}$). The secondary functions are assigned to the pins of port 3 as follows:
	5		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8		P3.2 / $\overline{INT0}$ — External interrupt 0 input / timer 0 gate control input
	9		P3.3 / $\overline{INT1}$ — External interrupt 1 input / timer 1 gate control input
	10		P3.4 / T0 — Timer 0 counter input
	11		P3.5 / T1 — Timer 1 counter input
	12		P3.6 / $\overline{WR}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	13		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P4.0 P4.1	6 28	I/O I/O	**Port 4** is a 2-bit quasi-bidirectional port with internal pull-up arrangement. Port 4 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to the secondary function RXDC must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the two pins of port 4 as follows (C505C and C505CA only) : P4.0 / TXDC Transmitter output of CAN controller P4.1 / RXDC Receiver input of CAN controller
XTAL2	14	O	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of the etxernal clock signal of 50 % should be maintained. Minimum and maximum high and low times as well as rise/ fall times specified in the AC characteristics must be observed.

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-P2.7	18-25	I/O	**Port 2** is a an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register and uses only the internal pullup resistors.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access. When instructions are executed from internal ROM or OTP ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON. ALE should not be driven during reset operation.

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
$\overline{EA}$	29	I	**$\overline{External\ Access\ Enable}$** When held at high level, instructions are fetched from the internal program memory when the PC is less than 4000_H (C505(C)(A)-2R) or 8000_H (C505A-4R/C505CA-4R/C505A-4E/C505CA-4E). When held at low level, the C505 fetches all instructions from external program memory. For the C505 romless versions (i.e. C505-L, C505C-L, C505A-L and C505CA-L) this pin must be tied low. For the ROM protection version $\overline{EA}$ pin is latched during reset.
P0.0-P0.7	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C505 ROM versions. External pullup resistors are required during program verification.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{DD}	17	–	**Power Supply** (+5V)

*) I = Input
O = Output

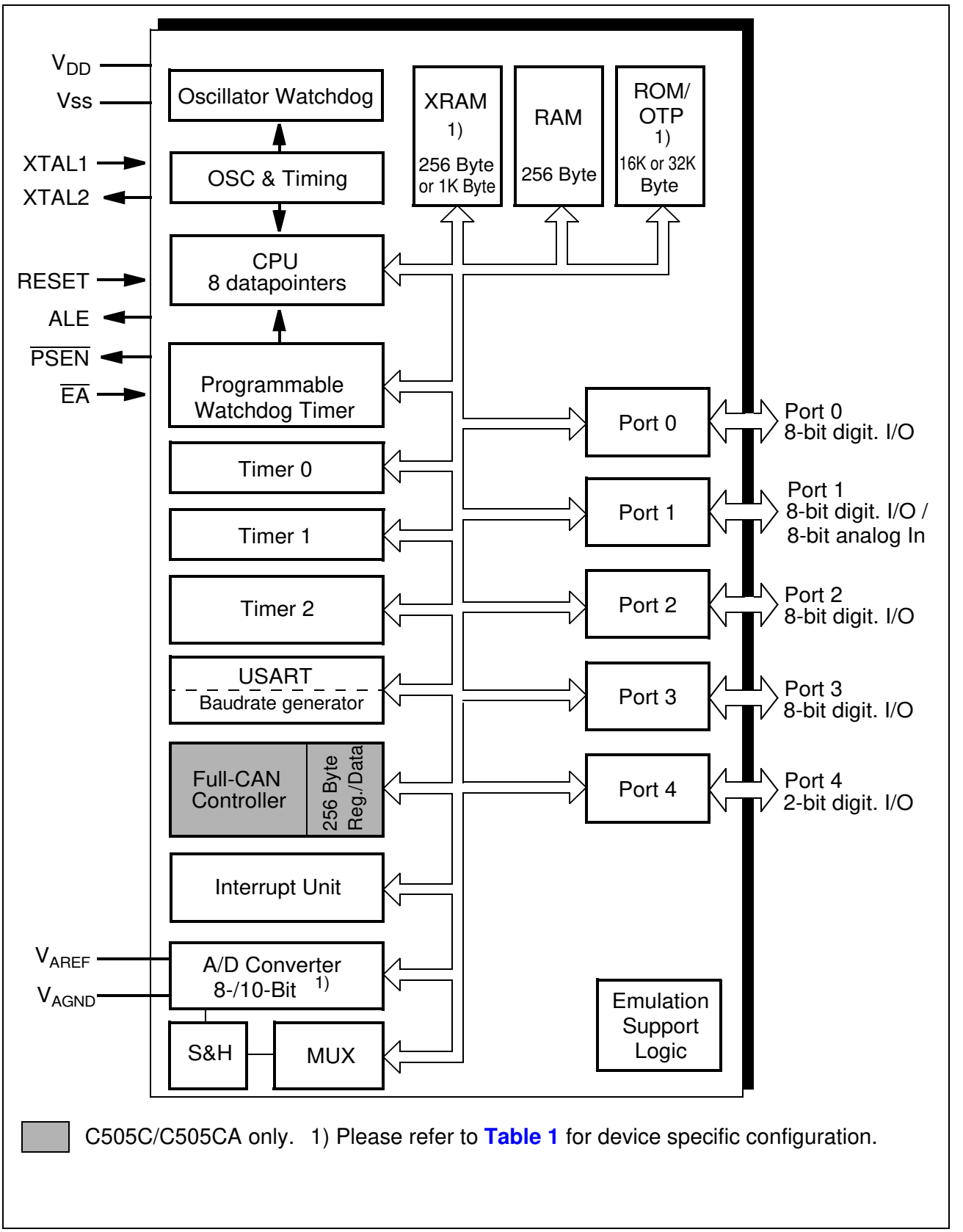


Figure 4
Block Diagram of the C505/C505C/C505A/C505CA

CPU

The C505 is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44 % one-byte, 41 % two-byte, and 15% three-byte instructions. With a 16 MHz crystal, 58% of the instructions are executed in 375 ns (20MHz: 300 ns).

Special Function Register PSW (Address $D0_H$) **Reset Value : 00_H**

Bit No.	MSB							LSB	
	$D7_H$	$D6_H$	$D5_H$	$D4_H$	$D3_H$	$D2_H$	$D1_H$	$D0_H$	
$D0_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	**Carry Flag** Used by arithmetic instruction.
AC	**Auxiliary Carry Flag** Used by instructions which execute BCD operations.
F0	**General Purpose Flag**
RS1 RS0	**Register Bank Select Control Bits** These bits are used to select one of the four register banks.
OV	**Overflow Flag** Used by arithmetic instruction.
F1	**General Purpose Flag**
P	**Parity Flag** Set/cleared by hardware after each instruction to indicate an odd/even number of "one" bits in the accumulator, i.e. even parity.

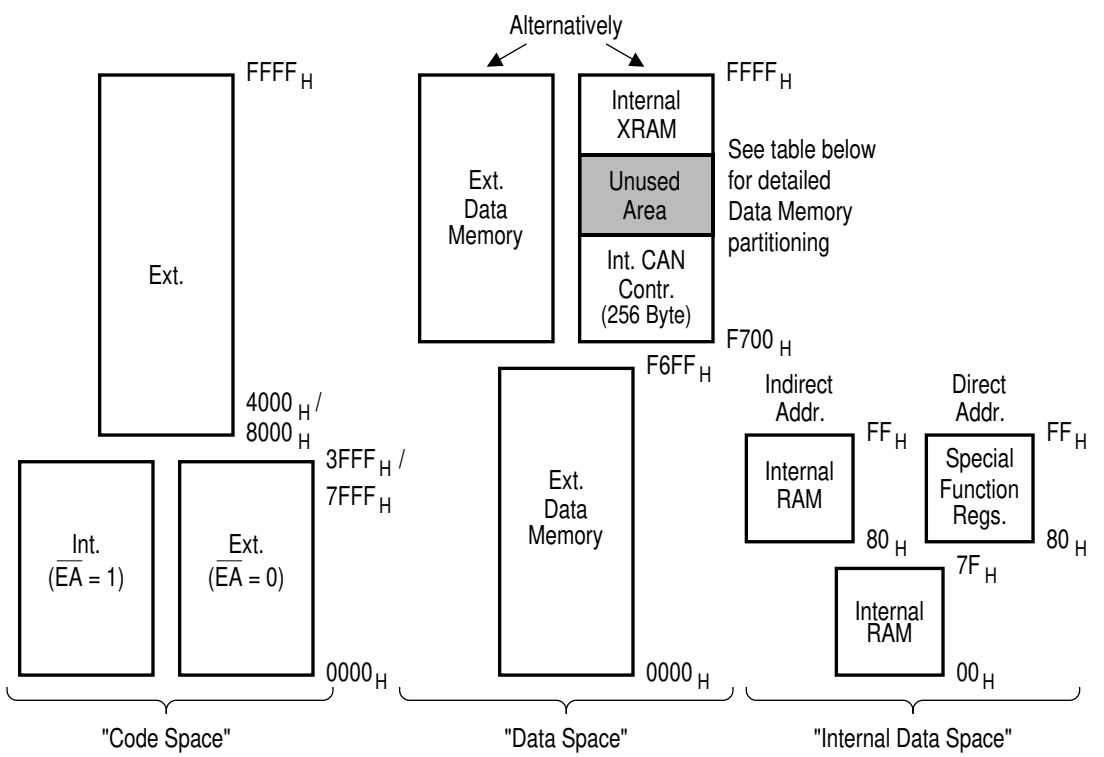
RS1	RS0	Function
0	0	Bank 0 selected, data address 00_H-07_H
0	1	Bank 1 selected, data address 08_H-$0F_H$
1	0	Bank 2 selected, data address 10_H-17_H
1	1	Bank 3 selected, data address 18_H-$1F_H$

Memory Organization

The C505 CPU manipulates operands in the following four address spaces:

- On-chip program memory : 16K byte ROM (C505(C)(A)-2R) or
  32K byte ROM (C505A-4R/C505CA-4R) or
  32K byte OTP (C505A-4E/C505CA-4E)
- Totally up to 64K byte internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- Internal XRAM data memory : 256 byte (C505/C505C)
  1K byte (C505A/C505CA)
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C505 versions.



"Data Space" $F700_H$ to $FFFF_H$:

Device	CAN Area	Unused Area	XRAM Area
C505	–	$F700_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505C	$F700_H$–$F7FF_H$	$F800_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505A	–	$F700_H$–$FBFF_H$	$FC00_H$–$FFFF_H$
C505CA	$F700_H$–$F7FF_H$	$F800_H$–$FBFF_H$	$FC00_H$–$FFFF_H$

Figure 5
C505 Memory Map Memory Map

Reset and System Clock

The reset input is an active high input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pulldown resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the RESET pin to V_{DD} via a capacitor. **Figure 6** shows the possible reset circuitries.

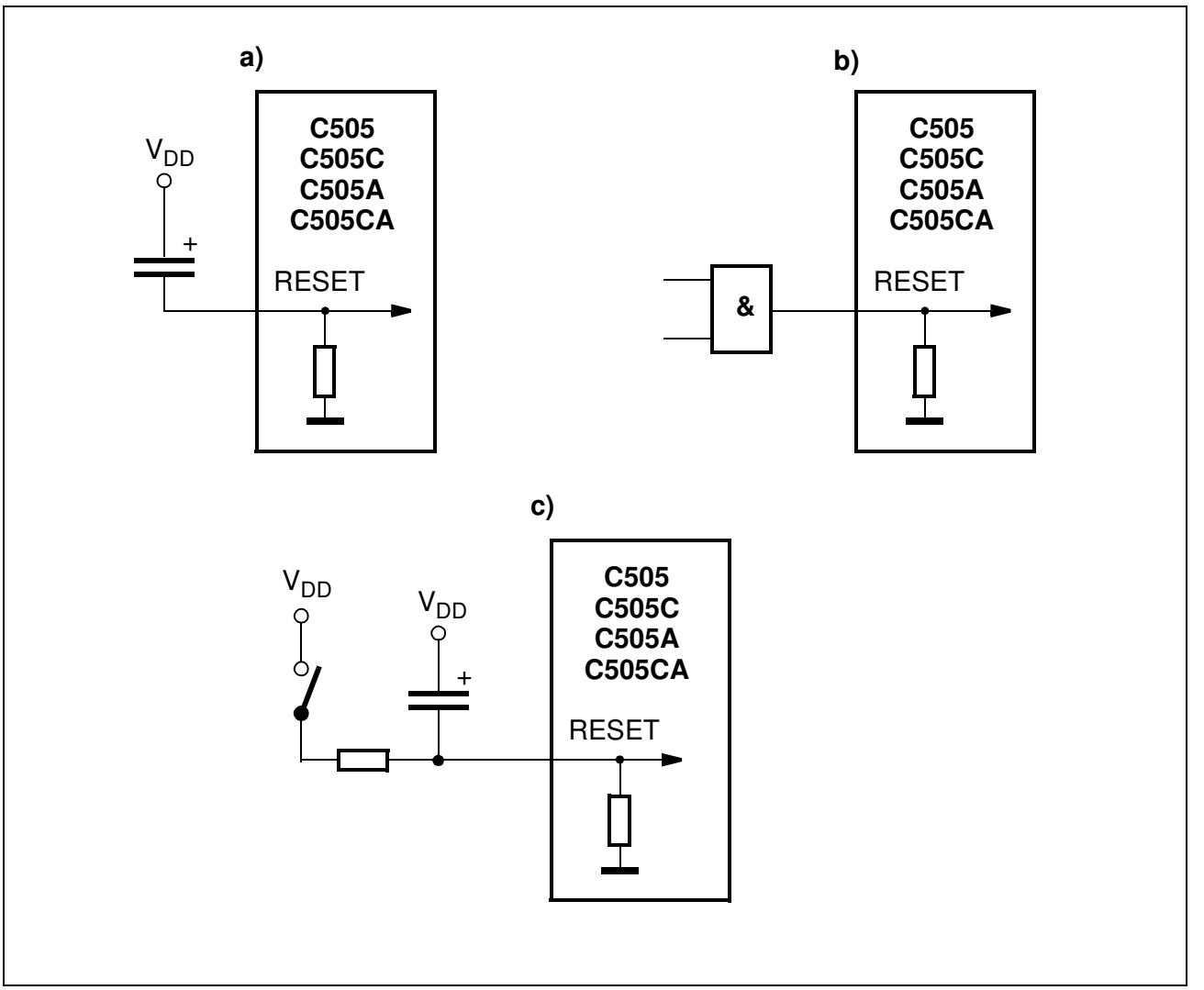


Figure 6
Reset Circuitries

Figure 7 shows the recommended oscillator circuits for crystal and external clock operation.

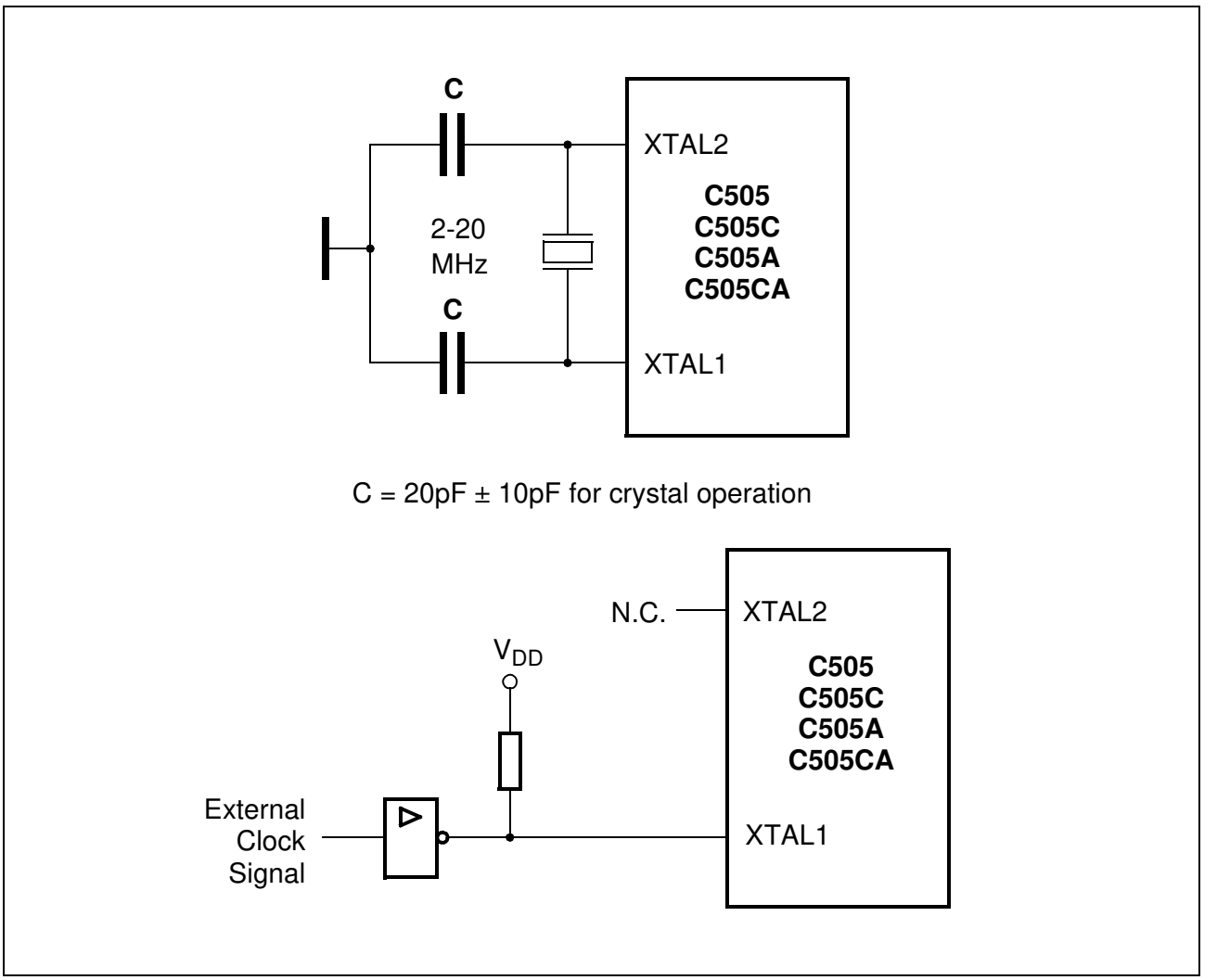


Figure 7
Recommended Oscillator Circuitries

Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C505 contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function regsiter DPSEL. **Figure 8** illustrates the datapointer addressing mechanism.

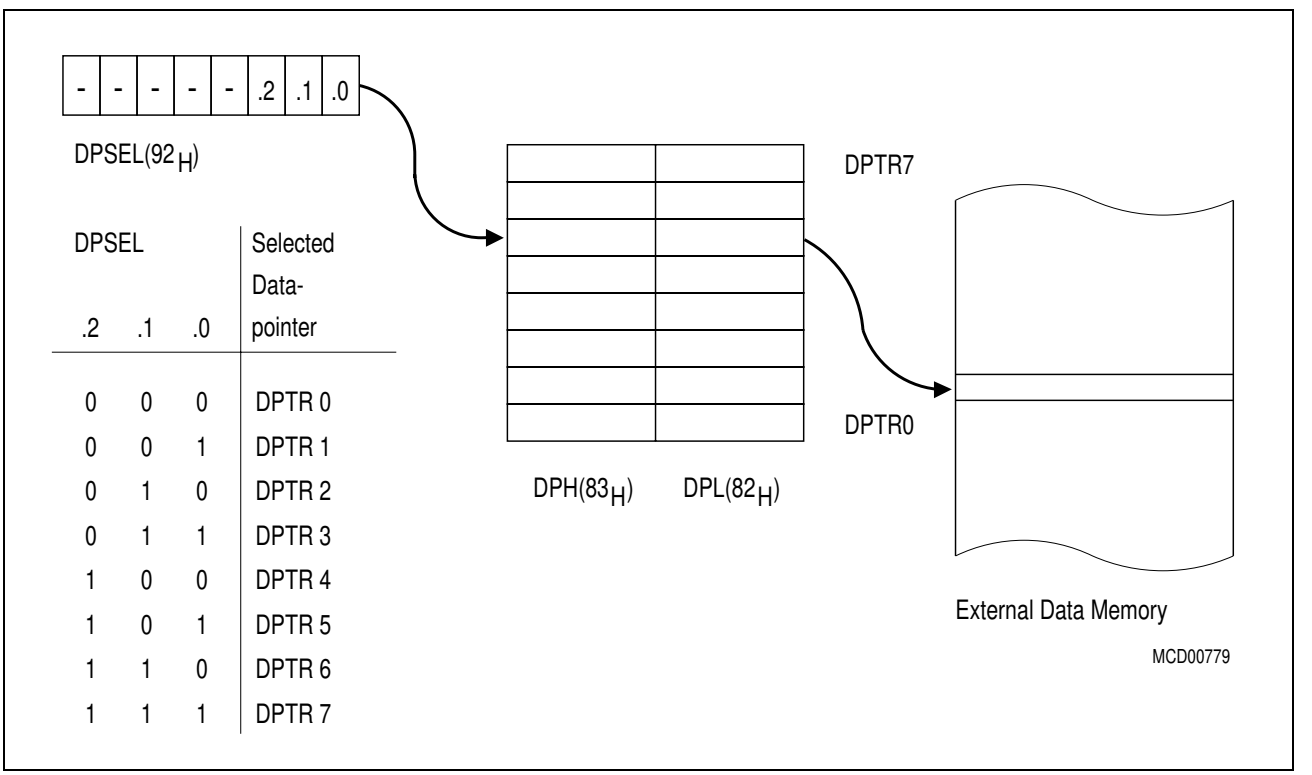


Figure 8
External Data Memory Addressing using Multiple Datapointers

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

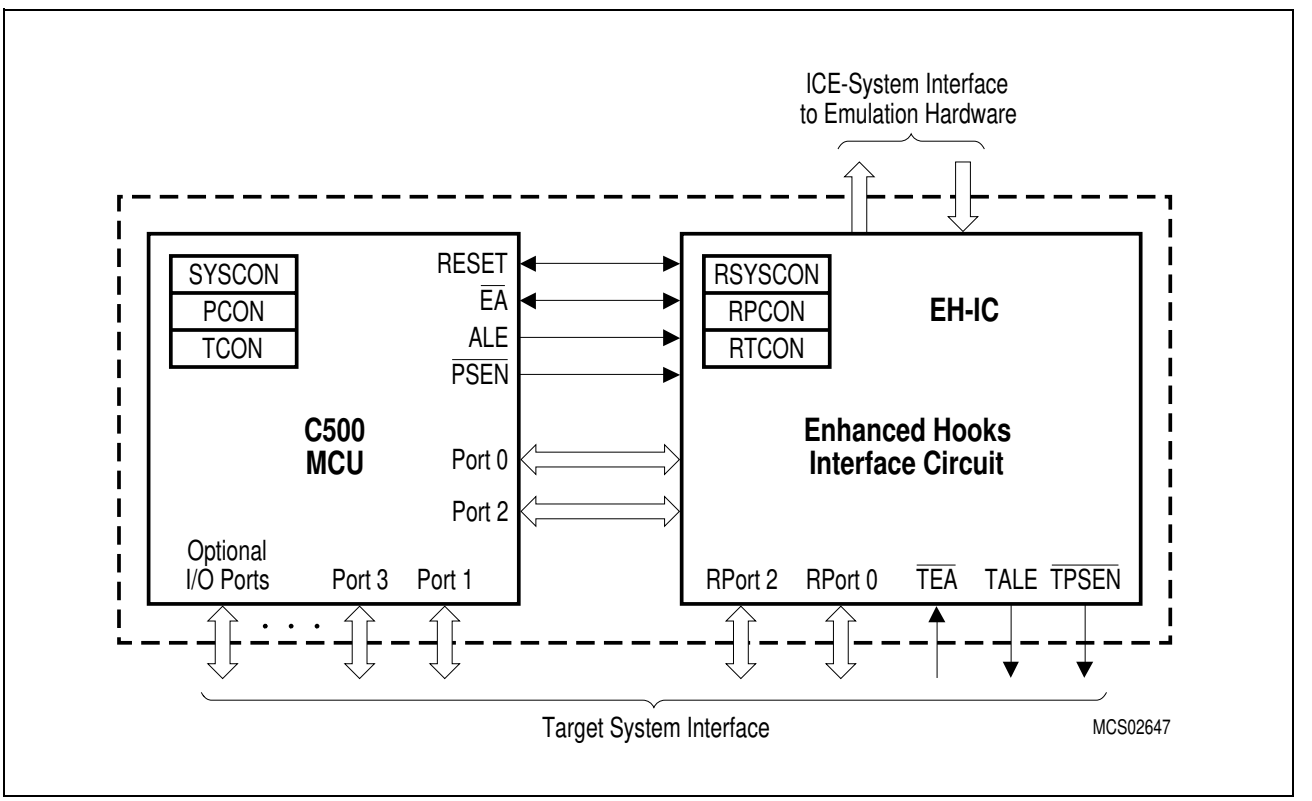


Figure 9
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

[1] "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions : the standard special function register area and the mapped special function register area. Five special function register of the C505 (PCON1,P1ANA, VR0, VR1, VR2) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0“).

The registers and data locations of the CAN controller (CAN-SFRs) are located in the external data memory area at addresses $F700_H$ to $F7FF_H$..

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX100X01_B$**
(C505CA only) **Reset Value : $XX100001_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	CMOD	CSWO 1)	XMAP1	XMAP0	SYSCON

The functions of the shaded bits are not described here.
1) This bit is only available in the C505CA.

Bit	Function
RMAP	Special function register map bit RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area is enabled.
CSWO	CAN Controller switch-off bit CSWO = 0 : CAN Controller is enabled (default after reset). CSWO = 1 : CAN Controller is switched off.

As long as bit RMAP is set, mapped special function register area can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The 52 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C505 are listed in **Table 3** and **Table 4**. In **Table 3** they are organized in groups which refer to the functional blocks of the C505. The CAN-SFRs (applicable for the C505C and C505CA only) are also included in **Table 3**. **Table 4** illustrates the contents of the SFRs in numeric order of their addresses. **Table 5** list the CAN-SFRs in numeric order of their addresses.

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$ [3]
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON[2]	System Control Register	$B1_H$	$XX100X01_B$ [3] [6] $XX100001_B$ [3] [7]
	VR0 [4]	Version Register 0	FC_H	$C5_H$
	VR1 [4]	Version Register 1	FD_H	05_H
	VR2 [4]	Version Register 2	FE_H	[5]
A/D-Converter	ADCON0 [2]	A/D Converter Control Register 0	**$D8_H$** [1]	$00X00000_B$ [3]
	ADCON1	A/D Converter Control Register 1	DC_H	$01XXX000_B$ [3]
	ADDAT	A/D Converter Data Reg. (C505/C505C)	$D9_H$	00_H
	ADST	A/D Converter Start Reg. (C505/C505C)	DA_H	XX_H [3]
	ADDATH	A/D Converter High Byte Data Register (C505A/C505CA)	$D9_H$	00_H
	ADDATL	A/D Converter Low Byte Data Register (C505A/C505CA)	DA_H	$00XXXXXX_B$ [3]
	P1ANA [2] [4]	Port 1 Analog Input Selection Register	90_H	FF_H
Interrupt System	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX000000_B$ [3]
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	$00X00000_B$
	SCON [2]	Serial Channel Control Register	**98_H** [1]	00_H
	IRCON	Interrupt Request Control Register	**$C0_H$** [1]	00_H
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM and CAN Controller	91_H	00_H
	SYSCON[2]	System Control Register	$B1_H$	$XX100X01_B$ [3] [6] $XX100001_B$ [3] [7]

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) “X“ means that the value is undefined and the location is reserved
4) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The content of this SFR varies with the actual step of the C505 (eg. 01_H for the first step)
6) C505 / C505A/C505C only
7) C505CA only

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P1ANA 2) 4)	Port 1 Analog Input Selection Register	**90_H** 1)	FF_H
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P4	Port 4	**E8H** 1)	$XXXXXX11_B$
Serial Channel	ADCON0 2)	A/D Converter Control Register 0	**$D8_H$** 1)	$00X00000_B$ 3)
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H 3)
	SCON	Serial Channel Control Register	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Compare/ Capture Unit / Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H 3)
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CRCH	Reload Register High Byte	CB_H	00_H
	CRCL	Reload Register Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** 1)	$00X00000_B$ 3)
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
Pow. Save Modes	PCON 2)	Power Control Register	87_H	00_H
	PCON1 4)	Power Control Register 1	**88_H** 1)	$0XX0XXXX_B$ 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
CAN Controller (C505C/ C505CA only)	CR	Control Register	$F700_H$	01_H
	SR	Status Register	$F701_H$	XX_H 3)
	IR	Interrupt Register	$F702_H$	XX_H 3)
	BTR0	Bit Timing Register Low	$F704_H$	UU_H 3)
	BTR1	Bit Timing Register High	$F705_H$	$0UUUUUUU_B$ 3)
	GMS0	Global Mask Short Register Low	$F706_H$	UU_H 3)
	GMS1	Global Mask Short Register High	$F707_H$	$UUU11111_B$ 3)
	UGML0	Upper Global Mask Long Register Low	$F708_H$	UU_H 3)
	UGML1	Upper Global Mask Long Register High	$F709_H$	UU_H 3)
	LGML0	Lower Global Mask Long Register Low	$F70A_H$	UU_H 3)
	LGML1	Lower Global Mask Long Register High	$F70B_H$	$UUUUU000_B$ 3)
	UMLM0	Upper Mask of Last Message Register Low	$F70C_H$	UU_H 3)
	UMLM1	Upper Mask of Last Message Register High	$F70D_H$	UU_H 3)
	LMLM0	Lower Mask of Last Message Register Low	$F70E_H$	UU_H 3)
	LMLM1	Lower Mask of Last Message Register High	$F70F_H$	$UUUUU000_B$ 3)
		Message Object Registers :		
	MCR0	Message Control Register Low	$F7n0_H$ 5)	UU_H 3)
	MCR1	Message Control Register High	$F7n1_H$ 5)	UU_H 3)
	UAR0	Upper Arbitration Register Low	$F7n2_H$ 5)	UU_H 3)
	UAR1	Upper Arbitration Register High	$F7n3_H$ 5)	UU_H 3)
	LAR0	Lower Arbitration Register Low	$F7n4_H$ 5)	UU_H 3)
	LAR1	Lower Arbitration Register High	$F7n5_H$ 5)	$UUUUU000_B$ 3)
	MCFG	Message Configuration Register	$F7n6_H$ 5)	$UUUUUU00_B$ 3)
	DB0	Message Data Byte 0	$F7n7_H$ 5)	XX_H 3)
	DB1	Message Data Byte 1	$F7n8_H$ 5)	XX_H 3)
	DB2	Message Data Byte 2	$F7n9_H$ 5)	XX_H 3)
	DB3	Message Data Byte 3	$F7nA_H$ 5)	XX_H 3)
	DB4	Message Data Byte 4	$F7nB_H$ 5)	XX_H 3)
	DB5	Message Data Byte 5	$F7nC_H$ 5)	XX_H 3)
	DB6	Message Data Byte 6	$F7nD_H$ 5)	XX_H 3)
	DB7	Message Data Byte 7	$F7nE_H$ 5)	XX_H 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved. "U" means that the value is unchanged by a reset operation. "U" values are undefined (as "X") after a power-on reset operation
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The notation "n" (n= 1 to F) in the message object address definition defines the number of the related message object.