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Data Sheet, Feb. 2003

C515C

8-Bit Single-Chip Microcontroller

Microcontrollers

Infineon technologies

Never stop thinking.

Edition 2003-02

Published by Infineon Technologies AG,
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Revision History: 2003-02

Previous Version: 2000-08

Page	Subjects (major changes since last revision)

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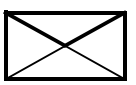

Features

- Full upward compatibility with SAB 80C515A
- On-chip program memory (with optional memory protection)
  - C515C-8R 64 Kbytes on-chip ROM
  - C515C-8E 64 Kbytes on-chip OTP
  - alternatively up to 64 Kbytes external program memory
- 256 bytes on-chip RAM
- 2 Kbytes of on-chip XRAM
- Up to 64 Kbytes external data memory
- Superset of the 8051 architecture with 8 datapointers
- Up to 10 MHz external operating frequency (1 µs instruction cycle time at 6 MHz external clock)
- On-chip emulation support logic (Enhanced Hooks Technology)
- Current optimized oscillator circuit and EMI optimized design

(further features are on next page)

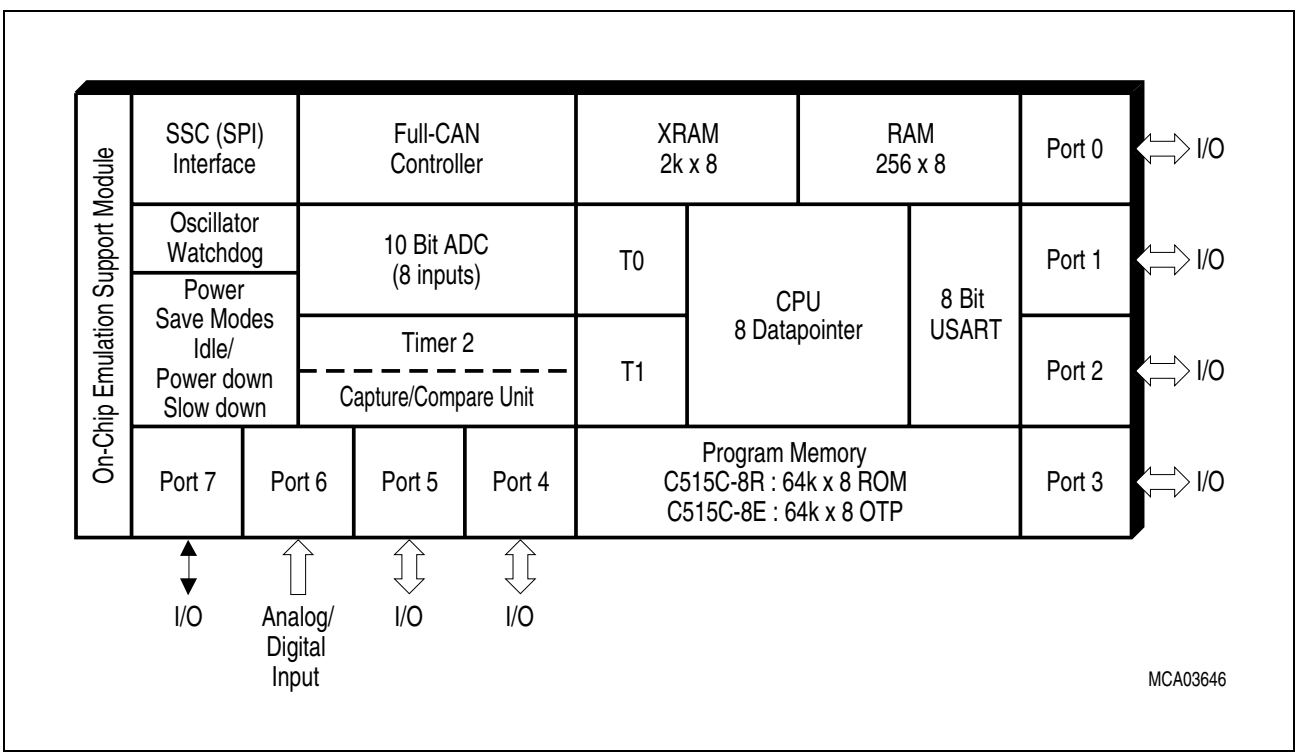

Figure 1 C515C Functional Units

- Eight ports: 48 + 1 digital I/O lines, 8 analog inputs
  - Quasi-bidirectional port structure (8051 compatible)
  - Port 5 selectable for bidirectional port structure (CMOS voltage levels)
- Full-CAN controller on-chip
  - 256 register/data bytes are located in external data memory area
  - max. 1 MBaud at 8 - 10 MHz operating frequency
- Three 16-bit timer/counters
  - Timer 2 can be used for compare/capture functions
- 10-bit A/D converter with multiplexed inputs and built-in self calibration
- Full duplex serial interface with programmable baudrate generator (USART)
- SSC synchronous serial interface (SPI compatible)
  - Master and slave capable
  - Programmable clock polarity/clock-edge to data phase relation
  - LSB/MSB first selectable
  - 2.5 MHz transfer rate at 10 MHz operating frequency
- Seventeen interrupt vectors, at four priority levels selectable
- Extended watchdog facilities
  - 15-bit programmable watchdog timer
  - Oscillator watchdog
- Power saving modes
  - Slow-down mode
  - Idle mode (can be combined with slow-down mode)
  - Software power-down mode with wake-up capability through $\overline{\text{INT0}}$ or RXDC pin
  - Hardware power-down mode
- CPU running condition output pin
- ALE can be switched off
- Multiple separate V_{DD}/V_{SS} pin pairs
- P-MQFP-80-1 package
- Temperature Ranges:
  SAB-C515C versions: T_A = 0 to 70 °C
  SAF-C515C versions: T_A = -40 to 85 °C
  SAH-C515C versions: T_A = -40 to 110 °C

Note: Versions for extended temperature range -40 °C to 110 °C (SAH-C515C) are available on request.

The C515C is an enhanced, upgraded version of the SAB 80C515A 8-bit microcontroller which additionally provides a full CAN interface, a SPI compatible synchronous serial interface, extended power save provisions, additional on-chip RAM, 64K of on-chip program memory, two new external interrupts and RFI related improvements. With a maximum external clock rate of 10 MHz it achieves a 600 ns instruction cycle time (1 µs at 6 MHz).

The C515C-8R contains a non-volatile 64 Kbytes read-only program memory. The C515C-L is identical to the C515C-8R, except that it lacks the on-chip program memory. The C515C-8E is the OTP version in the C515C microcontroller with an on-chip 64 Kbytes one-time programmable (OTP) program memory. The C515C is mounted in a P-MQFP-80-1 package.

If compared to the C515C-8R and C515C-L, the C515C-8E OTP version additionally provides two features:

- The wake-up from software power down mode can, additionally to the external pin P3.2/$\overline{\text{INT0}}$ wake-up capability, also be triggered alternatively by a second pin P4.7/RXDC.
- For power consumption reasons the on-chip CAN controller can be switched off.

Table 1 Differences in Internal Program Memory of the C505 MCUs

Device	Internal Program Memory	
	ROM	**OTP**
C515C-LM	–	–
C515C-8RM	64 Kbytes	–
C515C-8EM	–	64 Kbytes

Note: The term C515C refers to all versions described within this document unless otherwise noted.

Ordering Information

The ordering code for Infineon Technologies' microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set
- The specified temperature rage
- The package and the type of delivery

For the available ordering codes for the C515C please refer to the "**Product information Microcontrollers**", which summarizes all available microcontroller variants.

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

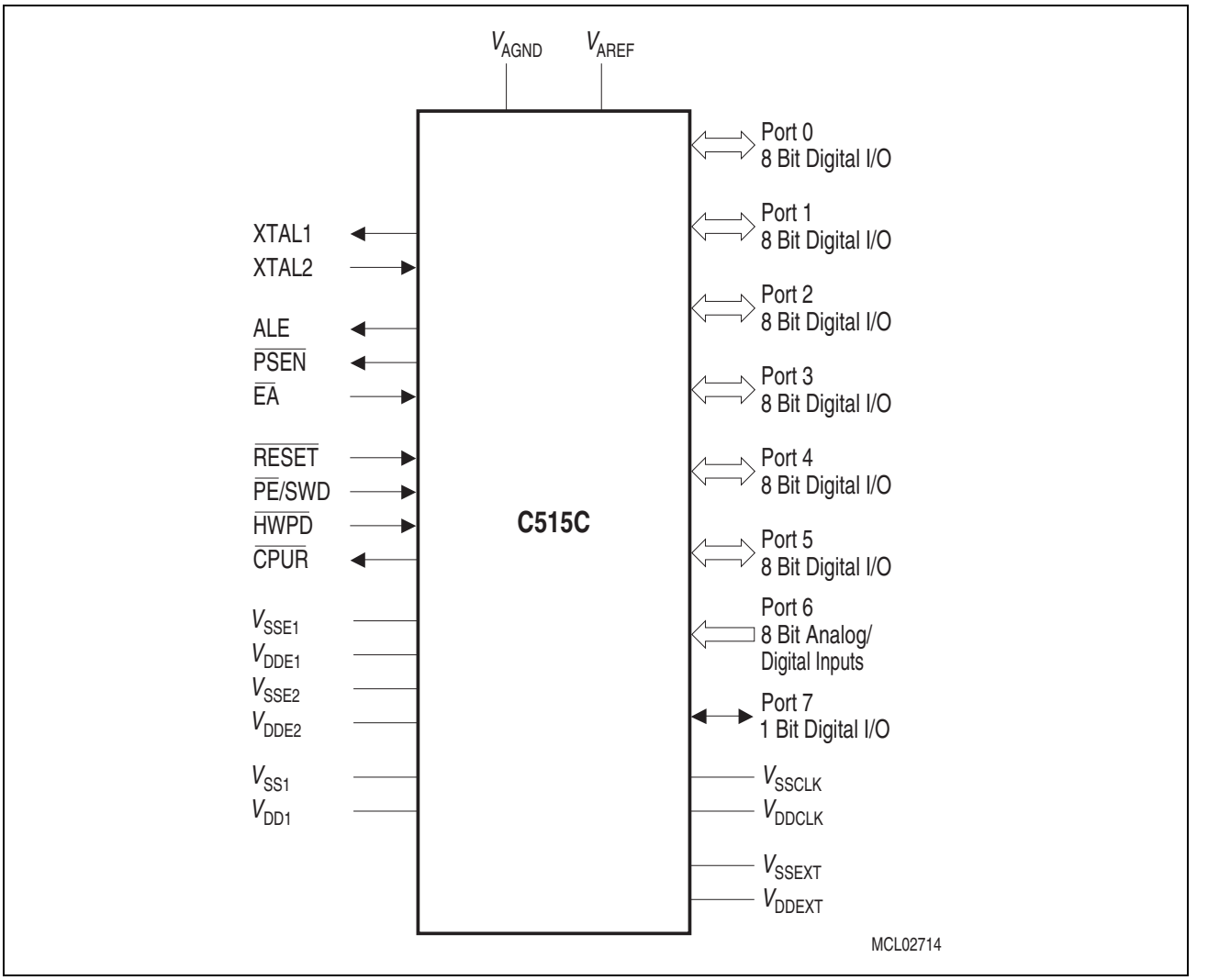

Figure 2 Logic Symbol

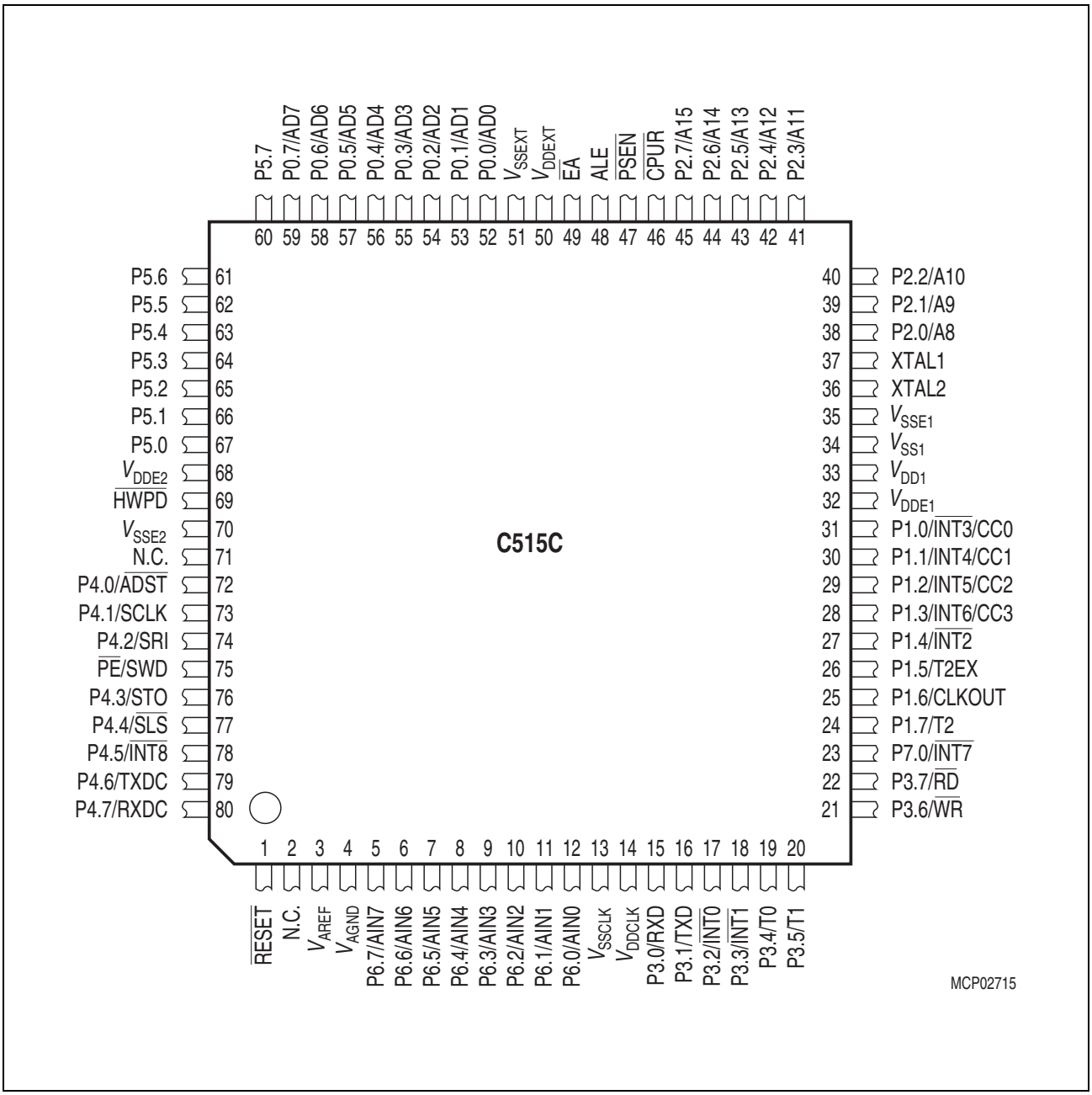

Figure 3 C515C Pin Configuration P-MQFP-80-1 (top view)

Table 2 Pin Definitions and Functions

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{\text{RESET}}$	1	I	**$\overline{\text{RESET}}$** A low level on this pin for the duration of two machine cycles while the oscillator is running resets the C515C. A small internal pullup resistor permits power-on reset using only a capacitor connected to V_{SS}.
V_{AREF}	3	–	**Reference voltage** for the A/D converter
V_{AGND}	4	–	**Reference ground** for the A/D converter
P6.0-P6.7	12-5	I	**Port 6** is an 8-bit unidirectional input port to the A/D converter. Port pins can be used for digital input, if voltage levels simultaneously meet the specifications high/low input voltages and for the eight multiplexed analog inputs.
P7.0 / $\overline{\text{INT7}}$	23	I/O	**Port 7** is an 1-bit quasi-bidirectional I/O port with internal pull-up resistor. When a 1 is written to P7.0 it is pulled high by an internal pull-up resistor, and in that state can be used as input. As input, P7.0 being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistor. If P7.0 is used as interrupt input, its output latch must be programmed to a one (1). The secondary function is assigned to the port 7 pin as follows: P7.0 $\overline{\text{INT7}}$, Interrupt 7 input

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
P3.0-P3.7	15-22	I/O	**Port 3** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 3 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 3 also contains the interrupt, timer, serial port and external memory strobe pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the pins of port 3, as follows:
	15		P3.0 RXD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	16		P3.1 TXD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	17		P3.2 $\overline{INT0}$ — External interrupt 0 input / timer 0 gate control input
	18		P3.3 $\overline{INT1}$ — External interrupt 1 input / timer 1 gate control input
	19		P3.4 T0 — Timer 0 counter input
	20		P3.5 T1 — Timer 1 counter input
	21		P3.6 $\overline{WR}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	22		P3.7 $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
P1.0 - P1.7	31-24	I/O	**Port 1** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 1 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. The port is used for the low-order address byte during program verification. Port 1 also contains the interrupt, timer, clock, capture and compare pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except when used for the compare functions). The secondary functions are assigned to the port 1 pins as follows: 31 P1.0 $\overline{\text{INT3}}$ CC0 Interrupt 3 input / compare 0 output / capture 0 input 30 P1.1 INT4 CC1 Interrupt 4 input / compare 1 output / capture 1 input 29 P1.2 INT5 CC2 Interrupt 5 input / compare 2 output / capture 2 input 28 P1.3 INT6 CC3 Interrupt 6 input / compare 3 output / capture 3 input 27 P1.4 $\overline{\text{INT2}}$ Interrupt 2 input 26 P1.5 T2EX Timer 2 external reload / trigger input 25 P1.6 CLKOUT System clock output 24 P1.7 T2 Counter 2 input
XTAL2	36	I	**XTAL2** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL2 should be driven, while XTAL1 is left unconnected. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
XTAL1	37	O	**XTAL1** Output of the inverting oscillator amplifier.
P2.0-P2.7	38-45	I/O	**Port 2** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup resistors when issuing 1's. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register.
$\overline{\text{CPUR}}$	46	O	**CPU Running Condition** This output pin is at low level when the CPU is running and program fetches or data accesses in the external data memory area are executed. In idle mode, hardware and software power down mode, and with an active $\overline{\text{RESET}}$ signal $\overline{\text{CPUR}}$ is set to high level. $\overline{\text{CPUR}}$ can be typically used for switching external memory devices into power saving modes.
$\overline{\text{PSEN}}$	47	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. The signal remains high during internal program execution.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
ALE	48	O	The **Address Latch Enable** output is used for latching the address into external memory during normal operation. It is activated every six oscillator periods, except during an external data memory access. ALE can be switched off when the program is executed internally.
$\overline{EA}$	49	I	**$\overline{\text{External Access Enable}}$** When held high, the C515C executes instructions always from the internal ROM. When held low, the C515C fetches all instructions from external program memory. *Note: For the ROM protection version $\overline{EA}$ pin is latched during reset.*
P0.0-P0.7	52-59	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application it uses strong internal pullup resistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C515C. External pullup resistors are required during program verification.
P5.0-P5.7	67-60	I/O	**Port 5** is an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 5 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 5 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 5 can also be switched into a bidirectional mode, in which CMOS levels are provided. In this bidirectional mode, each port 5 pin can be programmed individually as input or output.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{\text{HWPD}}$	69	I	**$\overline{\text{Hardware Power Down}}$** A low level on this pin for the duration of one machine cycle while the oscillator is running resets the C515C. A low level for a longer period will force the part to power down mode with the pins floating.
P4.0-P4.7	72-74, 76-80	I/O	**Port 4** is an 8-bit quasi-bidirectional I/O port with internal pull-up resistors. Port 4 pins that have 1's written to them are pulled high by the internal pull-up resistors, and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pull-up resistors. P4 also contains the external A/D converter control pin, the SSC pins, the CAN controller input/output lines, and the external interrupt 8 input. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. The alternate functions are assigned to port 4 as follows: 72 P4.0 $\overline{\text{ADST}}$ External A/D converter start pin 73 P4.1 SCLK SSC Master Clock Output / SSC Slave Clock Input 74 P4.2 SRI SSC Receive Input 76 P4.3 STO SSC Transmit Output 77 P4.4 $\overline{\text{SLS}}$ Slave Select Input 78 P4.5 $\overline{\text{INT8}}$ External interrupt 8 input 79 P4.6 TXDC Transmitter output of the CAN controller 80 P4.7 RXDC Receiver input of the CAN controller

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
$\overline{PE}$/SWD	75	I	**$\overline{Power\ saving\ mode\ enable}$ / Start watchdog timer** A low level on this pin allows the software to enter the power down, idle and slow down mode. In case the low level is also seen during reset, the watchdog timer function is off on default. Use of the software controlled power saving modes is blocked, when this pin is held on high level. A high level during reset performs an automatic start of the watchdog timer immediately after reset. When left unconnected this pin is pulled high by a weak internal pull-up resistor.
V_{SSCLK}	13	–	**Ground (0 V) for on-chip oscillator** This pin is used for ground connection of the on-chip oscillator circuit.
V_{DDCLK}	14	–	**Supply voltage for on-chip oscillator** This pin is used for power supply of the on-chip oscillator circuit.
V_{DDE1} V_{DDE2}	32 68	–	**Supply voltage for I/O ports** These pins are used for power supply of the I/O ports during normal, idle, and power down mode.
V_{SSE1} V_{SSE2}	35 70	–	**Ground (0 V) for I/O ports** These pins are used for ground connections of the I/O ports during normal, idle, and power down mode.
V_{DD1}	33	–	**Supply voltage for internal logic** This pins is used for the power supply of the internal logic circuits during normal, idle, and power down mode.
V_{SS1}	34	–	**Ground (0 V) for internal logic** This pin is used for the ground connection of the internal logic circuits during normal, idle, and power down mode.

Table 2 Pin Definitions and Functions (cont'd)

Symbol	Pin Number P-MQFP-80-1	I/O[1)]	Function
V_{DDEXT}	50	–	**Supply voltage for external access pins** This pin is used for power supply of the I/O ports and control signals which are used during external accesses (for Port 0, Port 2, ALE, $\overline{PSEN}$, P3.6/$\overline{WR}$, and P3.7/$\overline{RD}$).
V_{SSEXT}	51	–	**Ground (0 V) for external access pins** This pin is used for the ground connection of the I/O ports and control signals which are used during external accesses (for Port 0, Port 2, ALE, $\overline{PSEN}$, P3.6/$\overline{WR}$, and P3.7/$\overline{RD}$).
N.C.	2, 71	–	**Not connected** These pins should not be connected.

1) I = Input; O = Output

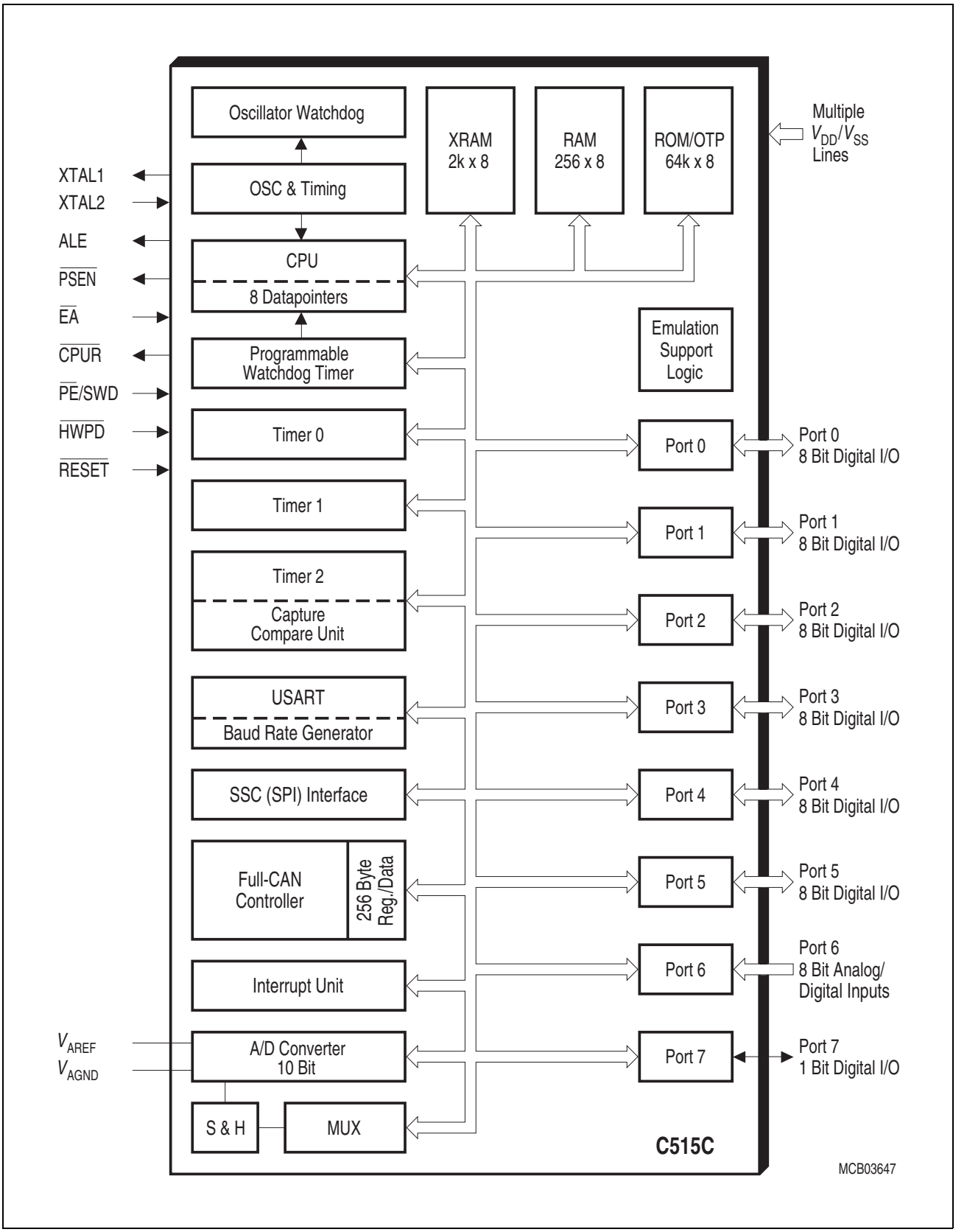

Figure 4 Block Diagram of the C515C

CPU

The C515C is efficient both as a controller and as an arithmetic processor. It has extensive facilities for binary and BCD arithmetic and excels in its bit-handling capabilities. Efficient use of program memory results from an instruction set consisting of 44% one-byte, 41% two-byte, and 15% three-byte instructions. With a 6 MHz crystal, 58% of the instructions are executed in 1 µs (10 MHz: 600 ns).

PSW

Special Function Register (D0$_H$) Reset Value: 00$_H$

Bit No. MSB LSB

	D7$_H$	D6$_H$	D5$_H$	D4$_H$	D3$_H$	D2$_H$	D1$_H$	D0$_H$	
D0$_H$	CY	AC	F0	RS1	RS0	OV	F1	P	PSW

Bit	Function
CY	Carry Flag Used by arithmetic instruction.
AC	Auxiliary Carry Flag Used by instructions which execute BCD operations.
F0	General Purpose Flag
RS1 RS0	Register Bank select control bits These bits are used to select one of the four register banks.
OV	Overflow Flag Used by arithmetic instruction.
F1	General Purpose Flag
P	Parity Flag Set/cleared by hardware after each instruction to indicate an odd/even number of “one” bits in the accumulator, i.e. even parity.

RS1	RS0	Function
0	0	Bank 0 selected, data address 00$_H$-07$_H$
0	1	Bank 1 selected, data address 08$_H$-0F$_H$
1	0	Bank 2 selected, data address 10$_H$-17$_H$
1	1	Bank 3 selected, data address 18$_H$-1F$_H$

Memory Organization

The C515C CPU manipulates data and operands in the following five address spaces:

- up to 64 Kbytes of internal/external program memory
- up to 64 Kbytes of external data memory
- 256 bytes of internal data memory
- 256 bytes CAN controller registers / data memory
- 2 Kbytes of internal XRAM data memory
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C515C.

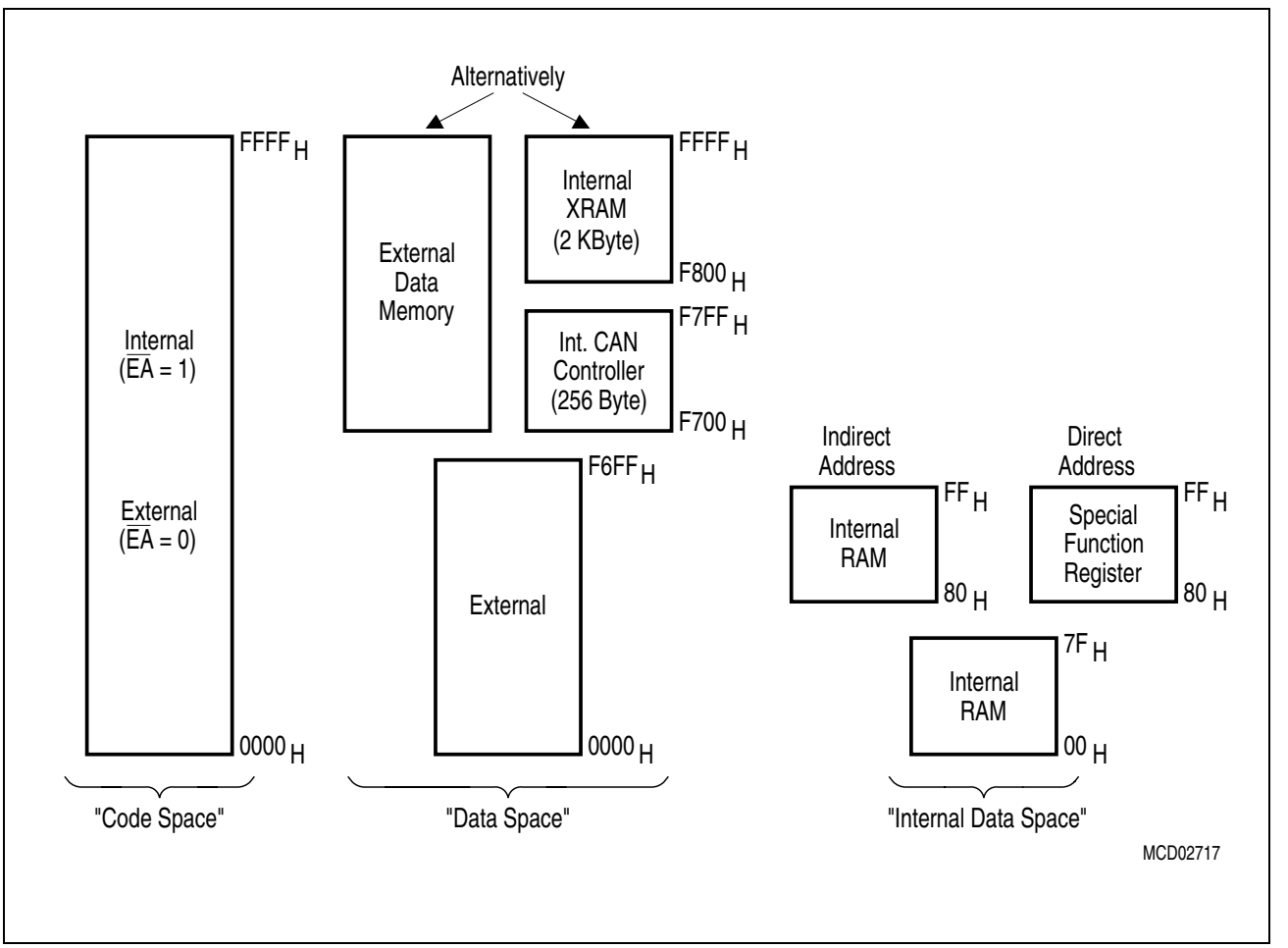

Figure 5 C515C Memory Map

Control of XRAM/CAN Controller Access

The XRAM in the C515C is a memory area that is logically located at the upper end of the external memory space, but is integrated on the chip. Because the XRAM and the CAN controller is used in the same way as external data memory the same instruction types (MOVX) must be used for accessing the XRAM. Two bits in SFR SYSCON, XMAP0 and XMAP1, control the accesses to the XRAM and the CAN controller.

SYSCON
Special Function Register **($B1_H$)** **C515C-8R Reset Value: $X010XX01_B$**
C515C-8E Reset Value: $X010X001_B$

Bit No.	MSB							LSB	
	7	6	5	4	3	2	1	0	
$B1_H$	–	PMOD	EALE	RMAP	–	CSWO	XMAP1	XMAP0	SYSCON

The function of the shaded bits is not described in this section.

Bit	Function
XMAP1	XRAM/CAN controller visible access control Control bit for $\overline{RD}$/$\overline{WR}$ signals during XRAM/CAN Controller accesses. If addresses are outside the XRAM/CAN controller address range or if XRAM is disabled, this bit has no effect. XMAP1 = 0: The signals $\overline{RD}$ and $\overline{WR}$ are not activated during accesses to the XRAM/CAN Controller XMAP1 = 1: Ports 0, 2 and the signals $\overline{RD}$ and $\overline{WR}$ are activated during accesses to XRAM/CAN Controller. In this mode, address and data information during XRAM/CAN Controller accesses are visible externally.
XMAP0	Global XRAM/CAN controller access enable/disable control XMAP0 = 0: The access to XRAM and CAN controller is enabled. XMAP0 = 1: The access to XRAM and CAN controller is disabled (default after reset). All MOVX accesses are performed via the external bus. Further, this bit is hardware protected.

Bit XMAP0 is hardware protected. If it is reset once (XRAM/CAN controller access enabled) it cannot be set by software. Only a reset operation will set the XMAP0 bit again.

The XRAM/CAN controller can be accessed by read/write instructions (MOVX A,DPTR, MOVX @DPTR,A), which use the 16-bit DPTR for indirect addressing. For accessing the XRAM or CAN controller, the effective address stored in DPTR must be in the range of $F700_H$ to $FFFF_H$.

The XRAM can be also accessed by read/write instructions (MOVX A,@Ri, MOVX @Ri,A), which use only an 8-bit address (indirect addressing with registers R0 or R1). Therefore, a special page register XPAGE which provides the upper address information (A8-A15) during 8-bit XRAM accesses. The behaviour of Port 0 and P2 during a MOVX access depends on the control bits XMAP0 and XMAP1 in register SYSCON and on the state of pin $\overline{EA}$. **Table 3** lists the various operating conditions.

Table 3 Behaviour of P0/P2 and $\overline{RD}/\overline{WR}$ During MOVX Accesses

			XMAP1, XMAP0		
			00	**10**	**X1**
$\overline{EA}$ = 0	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data only) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
$\overline{EA}$ = 1	MOVX @DPTR	DPTR < XRAM/CAN address range	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		DPTR ≥ XRAMCAN address range	a) P0/P2→I/0 b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0/P2→Bus ($\overline{RD}/\overline{WR}$-Data) b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0/P2→Bus b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
	MOVX @ Ri	XPAGE < XRAMCAN addr. page range	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used
		XPAGE ≥ XRAMCAN addr. page range	a) P2→I/O P0/P2→I/O b) $\overline{RD}/\overline{WR}$ inactive c) XRAM is used	a) P0→Bus ($\overline{RD}/\overline{WR}$-Data) P2→I/O b) $\overline{RD}/\overline{WR}$ active c) XRAM is used	a) P0→Bus P2→I/O b) $\overline{RD}/\overline{WR}$ active c) ext.memory is used

modes compatible to 8051/C501 family

Reset and System Clock

The reset input is an active low input at pin $\overline{\text{RESET}}$. Since the reset is synchronized internally, the $\overline{\text{RESET}}$ pin must be held low for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pullup resistor is internally connected to V_{DD} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the $\overline{\text{RESET}}$ pin to V_{SS} via a capacitor. **Figure 6** shows the possible reset circuitries.

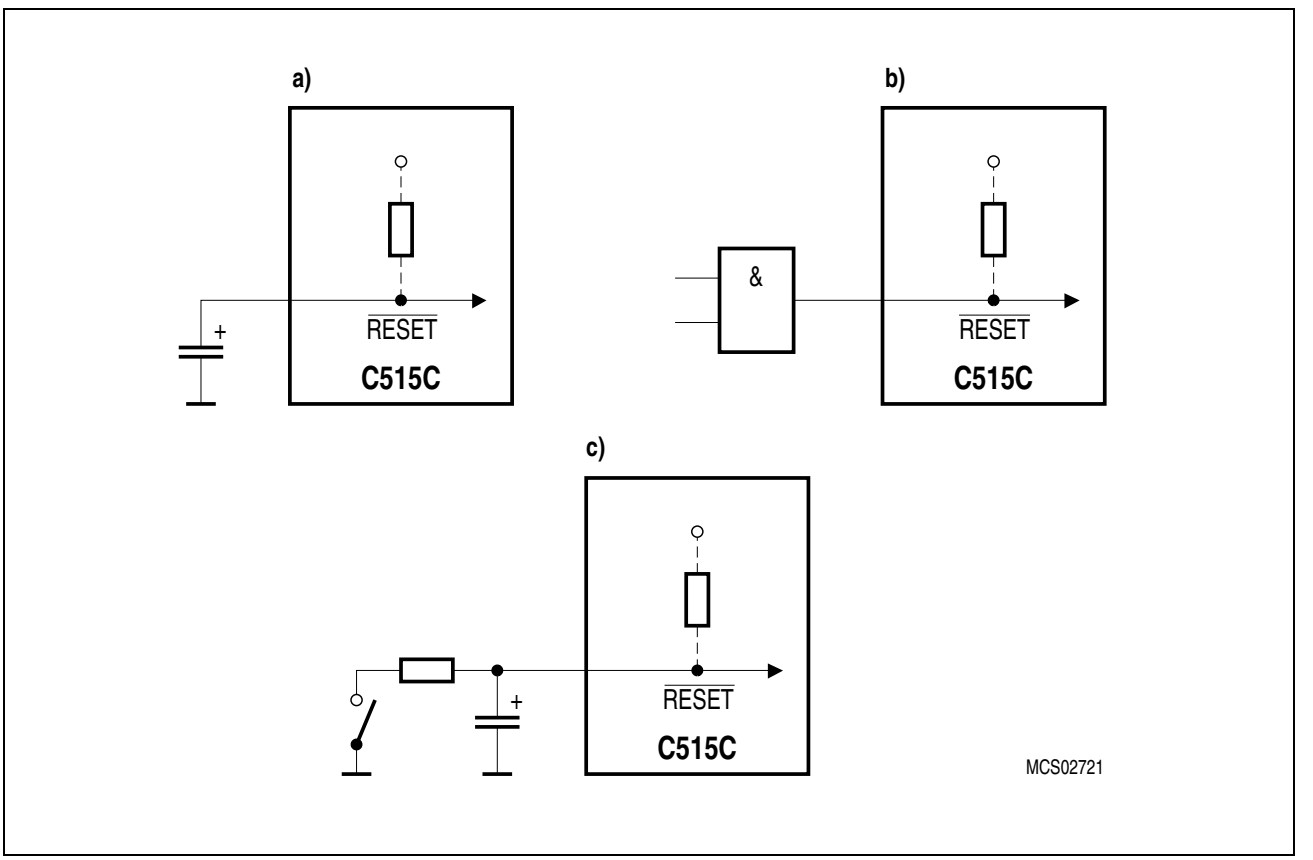

Figure 6 Reset Circuitries

Figure 7 shows the recommended oscillator circiutries for crystal and external clock operation.

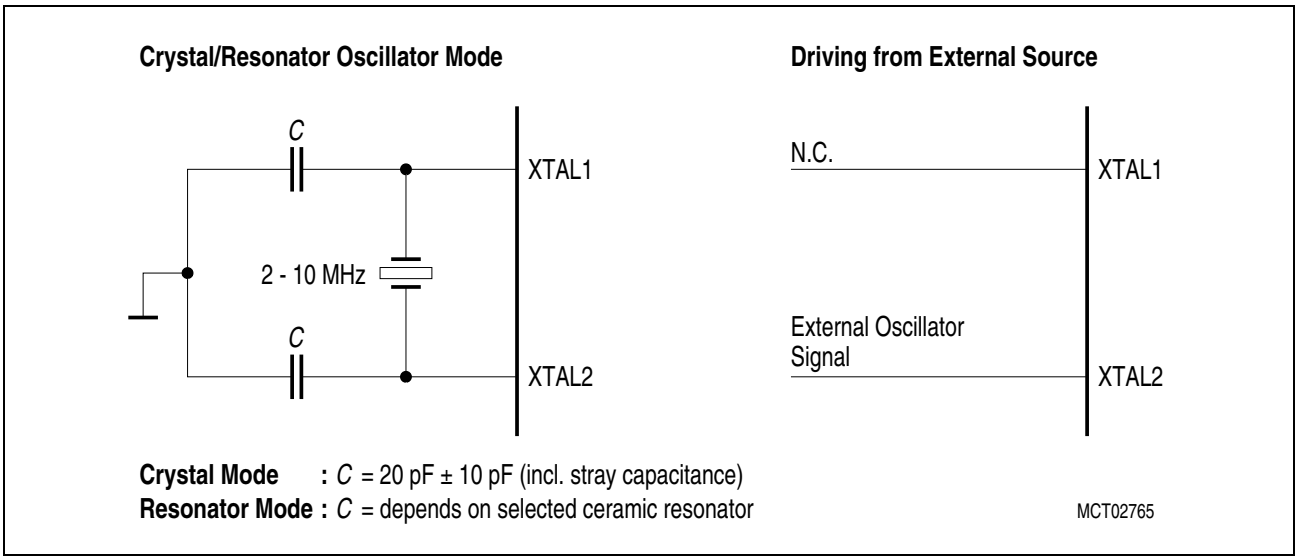

Figure 7 Recommended Oscillator Circuitries

Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C515C contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function register DPSEL. **Figure 8** illustrates the datapointer addressing mechanism.

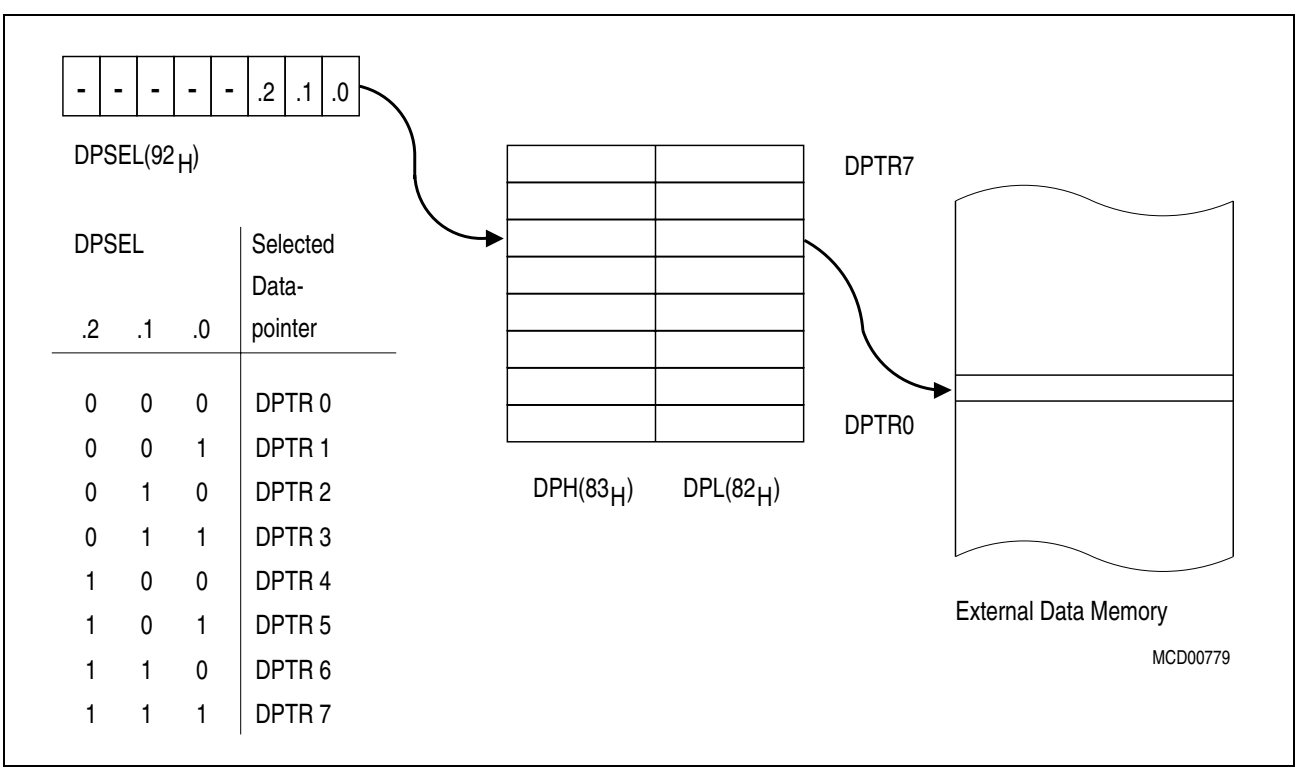

Figure 8 External Data Memory Addressing using Multiple Datapointers