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C8051F000/1/2/5/6/7
C8051F010/1/2/5/6/7

Mixed-Signal 32KB ISP FLASH MCU Family

ANALOG PERIPHERALS
- **SAR ADC**
  - 12-Bit (C8051F000/1/2, C8051F005/6/7)
  - 10-bit (C8051F010/1/2, C8051F015/6/7)
  - ±1LSB INL; No Missing Codes
  - Programmable Throughput up to 100ksps
  - Up to 8 External Inputs; Programmable as Single-Ended or Differential
  - Programmable Amplifier Gain: 16, 8, 4, 2, 1, 0.5
  - Data Dependent Windowed Interrupt Generator
  - Built-in Temperature Sensor (± 3°C)
- **Two 12-bit DACs**
- **Two Analog Comparators**
  - Programmable Hysteresis Values
  - Configurable to Generate Interrupts or Reset
- **Voltage Reference**
  - 2.4V; 15 ppm/°C
  - Available on External Pin
- **Precision VDD Monitor/Brown-out Detector**

ON-CHIP JTAG DEBUG & BOUNDARY SCAN
- On-Chip Debug Circuitry Facilitates Full Speed, Non-Intrusive In-System Debug (No Emulator Required!)
- Provides Breakpoints, Single Stepping, Watchpoints, Stack Monitor
- Inspect/Modify Memory and Registers
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets
- IEEE1149.1 Compliant Boundary Scan
- Low Cost Development Kit

HIGH SPEED 8051 µC CORE
- Pipelined Instruction Architecture; Executes 70% of Instruction Set in 1 or 2 System Clocks
- Up to 25MIPS Throughput with 25MHz Clock
- 21 Vectored Interrupt Sources

MEMORY
- 256 Bytes Internal Data RAM (F000/01/02/10/11/12)
- 2304 Bytes Internal Data RAM (F005/06/07/15/16/17)
- 32k Bytes FLASH; In-System Programmable in 512 byte Sectors

DIGITAL PERIPHERALS
- 4 Byte-Wide Port I/O; All are 5V tolerant
- Hardware SMBus™ (I2C™ Compatible), SPI™, and UART Serial Ports Available Concurrently
- Programmable 16-bit Counter/Timer Array with Five Capture/Compare Modules
- Four General Purpose 16-bit Counter/Timers
- Dedicated Watch-Dog Timer
- Bi-directional Reset

CLOCK SOURCES
- Internal Programmable Oscillator: 2-to-16MHz
- External Oscillator: Crystal, RC,C, or Clock
- Can Switch Between Clock Sources on-the-fly; Useful in Power Saving Modes

SUPPLY VOLTAGE ..... 2.7V to 3.6V
- Typical Operating Current: 12.5mA @ 25MHz
- Multiple Power Saving Sleep and Shutdown Modes

64-Pin TQFP, 48-Pin TQFP, 32-Pin LQFP

Temperature Range: –40°C to +85°C

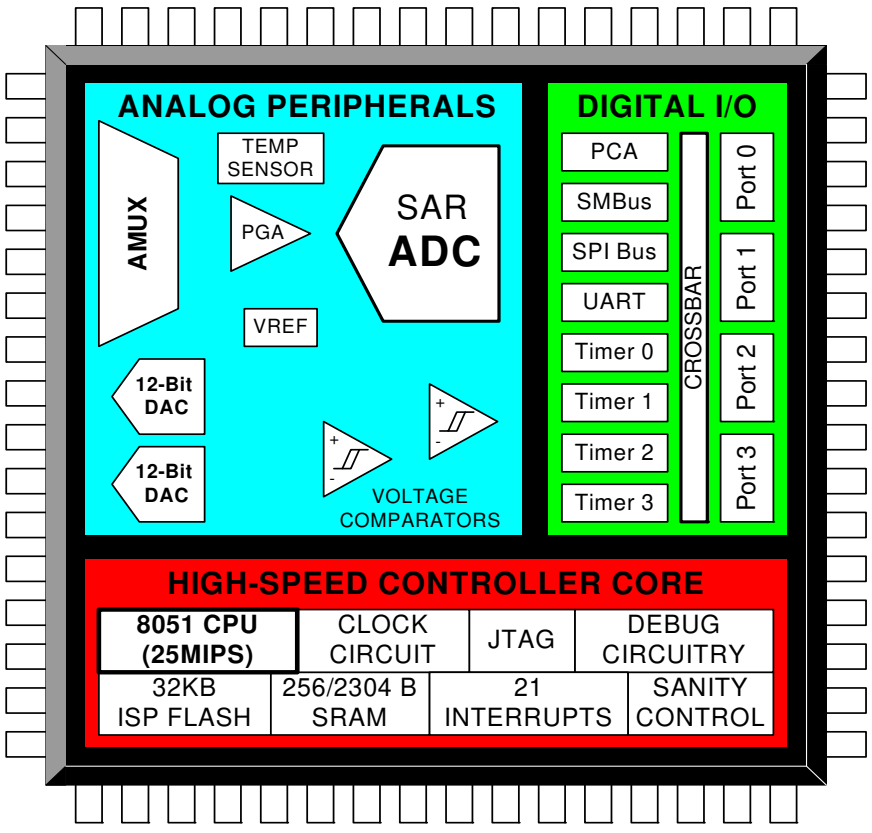


TABLE OF CONTENTS

1. SYSTEM OVERVIEW

The C8051F000 family are fully integrated mixed-signal System on a Chip MCUs with a true 12-bit multi-channel ADC (F000/01/02/05/06/07), or a true 10-bit multi-channel ADC (F010/11/12/15/16/17). See the Product Selection Guide in Table 1.1 for a quick reference of each MCUs' feature set. Each has a programmable gain pre-amplifier, two 12-bit DACs, two voltage comparators (except for the F002/07/12/17, which have one), a voltage reference, and an 8051-compatible microcontroller core with 32kbytes of FLASH memory. There are also I2C/SMBus, UART, and SPI serial interfaces implemented in hardware (not "bit-banged" in user software) as well as a Programmable Counter/Timer Array (PCA) with five capture/compare modules. There are also 4 general-purpose 16-bit timers and 4 byte-wide general-purpose digital Port I/O. The C8051F000/01/02/10/11/12 have 256 bytes of RAM and execute up to 20MIPS, while the C8051F005/06/07/15/16/17 have 2304 bytes of RAM and execute up to 25MIPS.

With an on-board VDD monitor, WDT, and clock oscillator, the MCUs are truly stand-alone System-on-a-Chip solutions. Each MCU effectively configures and manages the analog and digital peripherals. The FLASH memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware. Each MCU can also individually shut down any or all of the peripherals to conserve power.

On-board JTAG debug support allows non-intrusive (uses no on-chip resources), full speed, in-circuit debug using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional when using JTAG debug.

Each MCU is specified for 2.7V-to-3.6V operation over the industrial temperature range (-45C to +85C). The Port I/Os, /RST, and JTAG pins are tolerant for input signals up to 5V. The C8051F000/05/10/15 are available in the 64-pin TQFP (see block diagram in Figure 1.1). The C8051F001/06/11/16 are available in the 48-pin TQFP (see block diagram in Figure 1.2). The C8051F002/07/12/17 are available in the 32-pin LQFP (see block diagram in Figure 1.3).

Table 1.1. Product Selection Guide

	MIPS (Peak)	FLASH Memory	RAM	SMBus/I2C	SPI	UART	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	ADC Resolution (bits)	ADC Max Speed (ksps)	ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution	DAC Outputs	Voltage Comparators	Package
C8051F000	20	32k	256	√	√	√	4	√	32	12	100	8	√	√	12	2	2	64TQFP
C8051F001	20	32k	256	√	√	√	4	√	16	12	100	8	√	√	12	2	2	48TQFP
C8051F002	20	32k	256	√	√	√	4	√	8	12	100	4	√	√	12	2	1	32LQFP
C8051F005	25	32k	2304	√	√	√	4	√	32	12	100	8	√	√	12	2	2	64TQFP
C8051F006	25	32k	2304	√	√	√	4	√	16	12	100	8	√	√	12	2	2	48TQFP
C8051F007	25	32k	2304	√	√	√	4	√	8	12	100	4	√	√	12	2	1	32LQFP
C8051F010	20	32k	256	√	√	√	4	√	32	10	100	8	√	√	12	2	2	64TQFP
C8051F011	20	32k	256	√	√	√	4	√	16	10	100	8	√	√	12	2	2	48TQFP
C8051F012	20	32k	256	√	√	√	4	√	8	10	100	4	√	√	12	2	1	32LQFP
C8051F015	25	32k	2304	√	√	√	4	√	32	10	100	8	√	√	12	2	2	64TQFP
C8051F016	25	32k	2304	√	√	√	4	√	16	10	100	8	√	√	12	2	2	48TQFP
C8051F017	25	32k	2304	√	√	√	4	√	8	10	100	4	√	√	12	2	1	32LQFP

Figure 1.1. C8051F000/05/10/15 Block Diagram

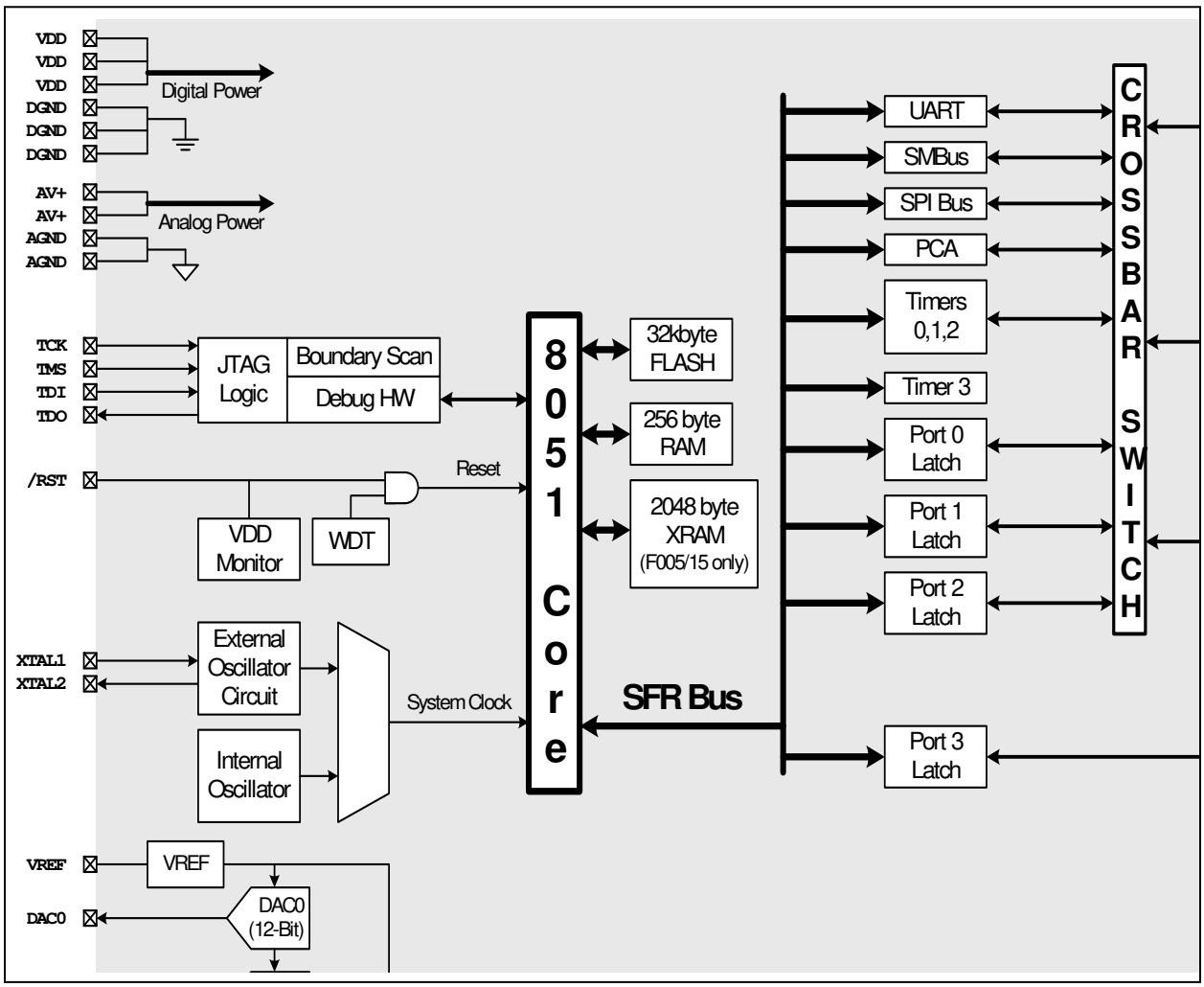


Figure 1.2. C8051F001/06/11/16 Block Diagram

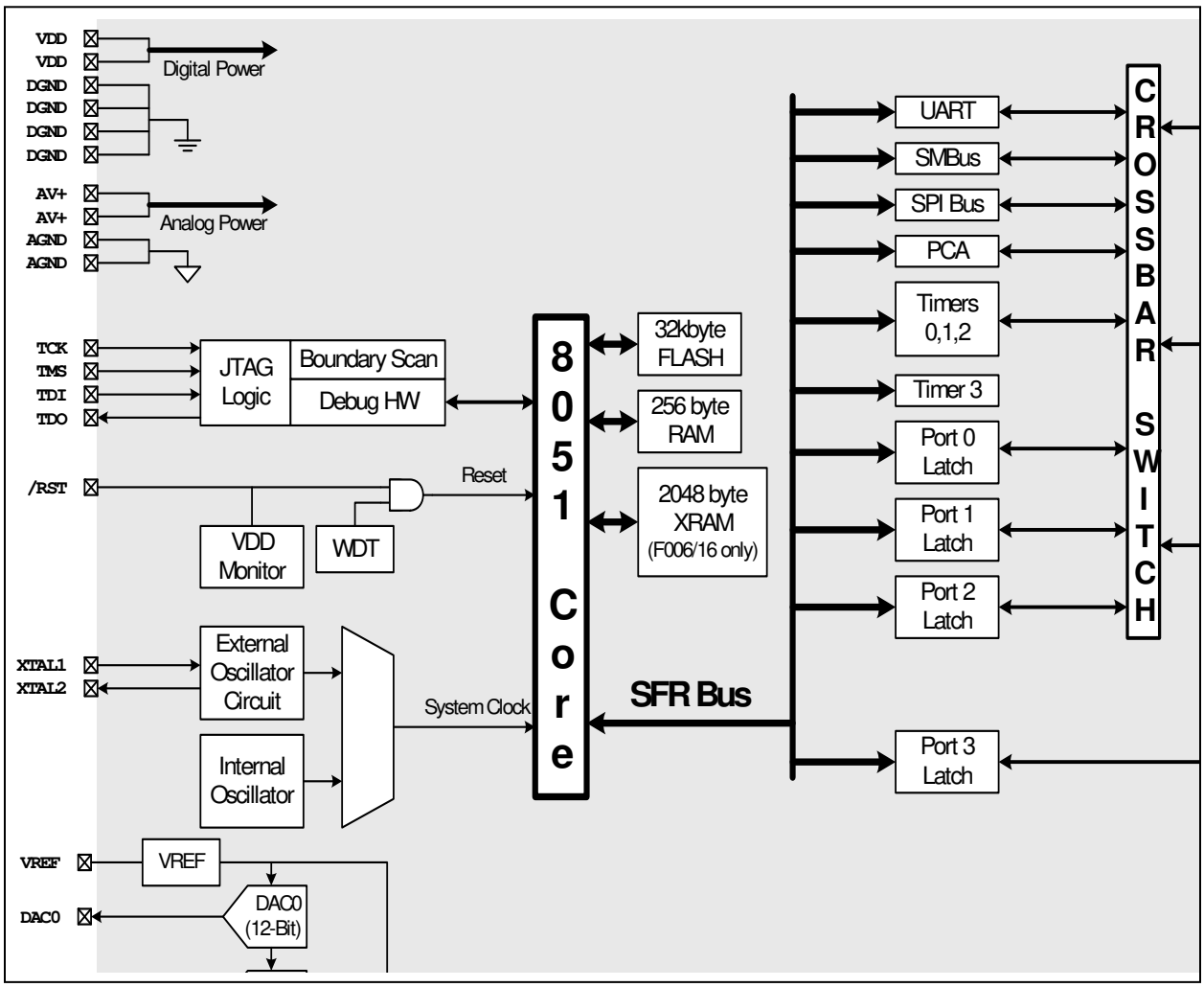
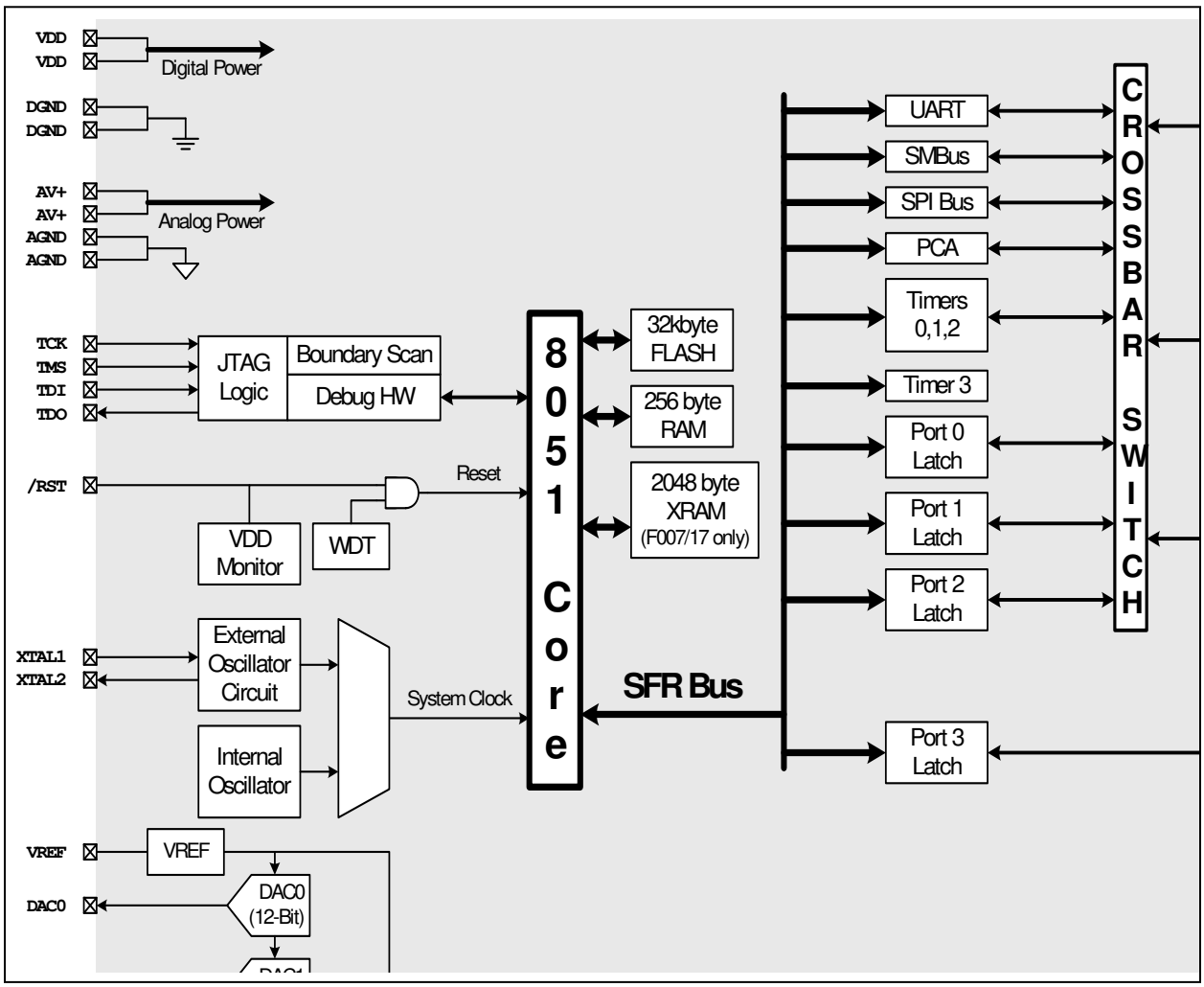


Figure 1.3. C8051F002/07/12/17 Block Diagram



1.1. CIP-51™ CPU

1.1.1. Fully 8051 Compatible

The C8051F000 family utilizes Silicon Laboratories' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The core has all the peripherals included with a standard 8052, including four 16-bit counter/timers, a full-duplex UART, 256 bytes of internal RAM space, 128 byte Special Function Register (SFR) address space, and four byte-wide I/O Ports.

1.1.2. Improved Throughput

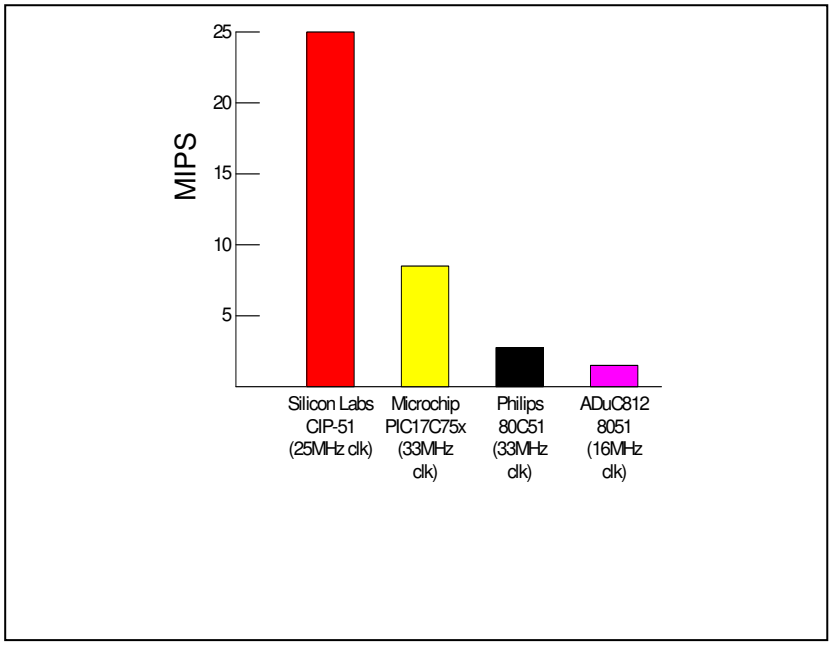
The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The number of instructions versus the system clock cycles to execute them is as follows:

Instructions	26	50	5	14	7	3	1	2	1
Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8

With the CIP-51's maximum system clock at 25MHz, it has a peak throughput of 25MIPS. Figure 1.4 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

Figure 1.4. Comparison of Peak MCU Execution Speeds



1.1.3. Additional Features

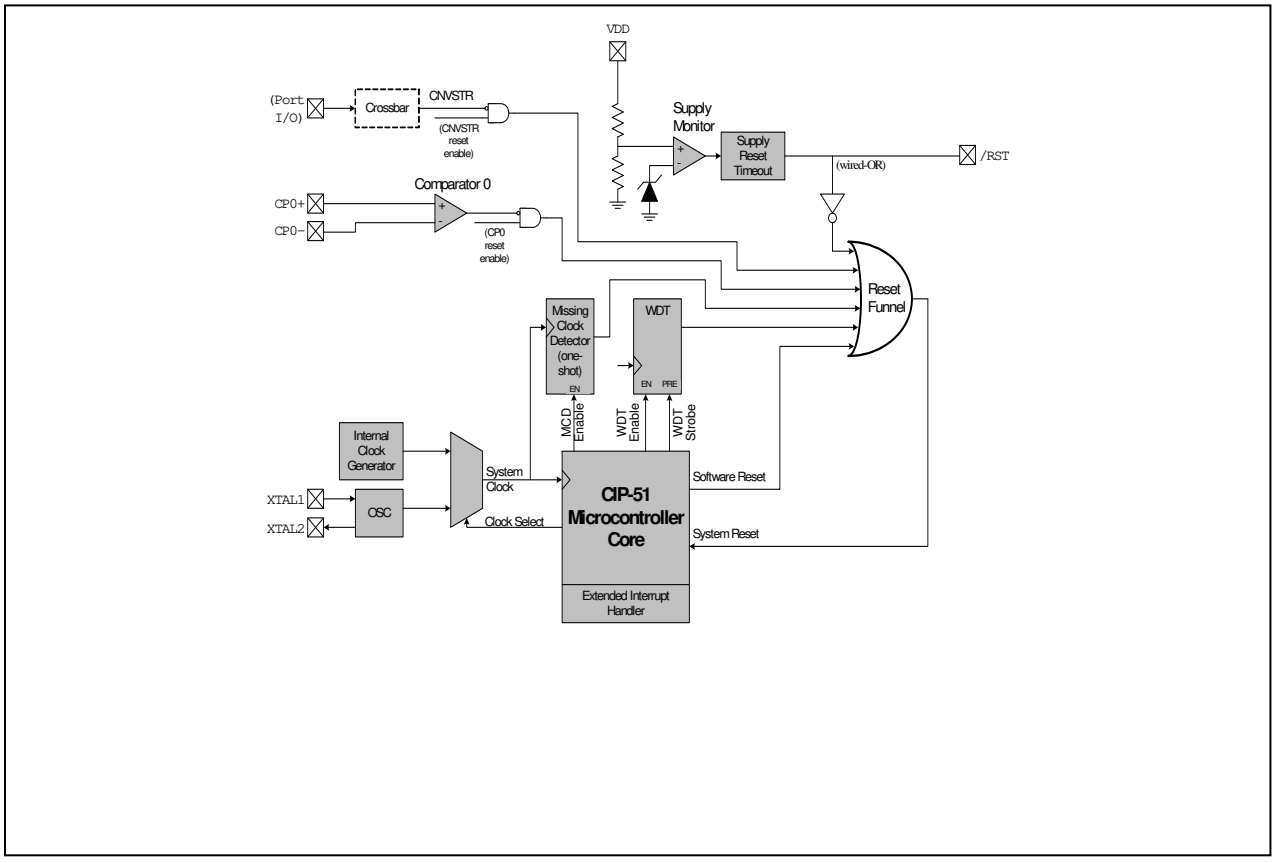
The C8051F000 MCU family has several key enhancements both inside and outside the CIP-51 core to improve its overall performance and ease of use in the end applications.

The extended interrupt handler provides 21 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing the numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

There are up to seven reset sources for the MCU: an on-board VDD monitor, a Watchdog Timer, a missing clock detector, a voltage level detection from Comparator 0, a forced software reset, the CNVSTR pin, and the /RST pin. The /RST pin is bi-directional, accommodating an external reset, or allowing the internally generated POR to be output on the /RST pin. Each reset source except for the VDD monitor and Reset Input Pin may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The MCU has an internal, stand alone clock generator which is used by default as the system clock after any reset. If desired, the clock source may be switched on the fly to the external oscillator, which can use a crystal, ceramic resonator, capacitor, RC, or external clock source to generate the system clock. This can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the fast (up to 16MHz) internal oscillator as needed.

Figure 1.5. On-Board Clock and Reset



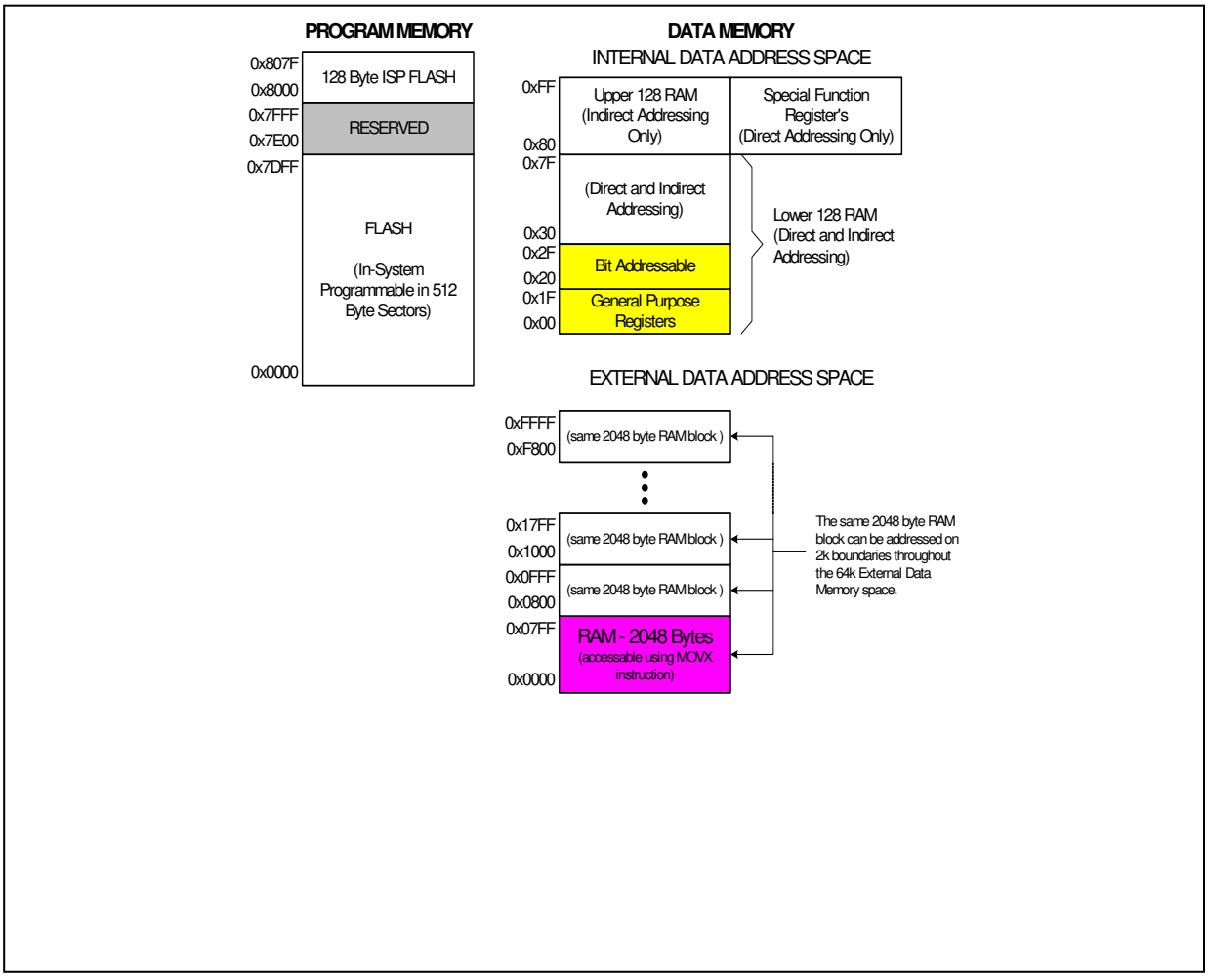
1.2. On-Board Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general-purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The CIP-51 in the C8051F005/06/07/15/16/17 MCUs additionally has a 2048 byte RAM block in the external data memory address space. This 2048 byte block can be addressed over the entire 64k external data memory address range (see Figure 1.6).

The MCU's program memory consists of 32k + 128 bytes of FLASH. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0x7E00 to 0x7FFF are reserved for factory use. There is also a single 128-byte sector at address 0x8000 to 0x807F, which may be useful as a small table for software constants or as additional program space. See Figure 1.6 for the MCU system memory map.

Figure 1.6. On-Board Memory Map



1.3. JTAG Debug and Boundary Scan

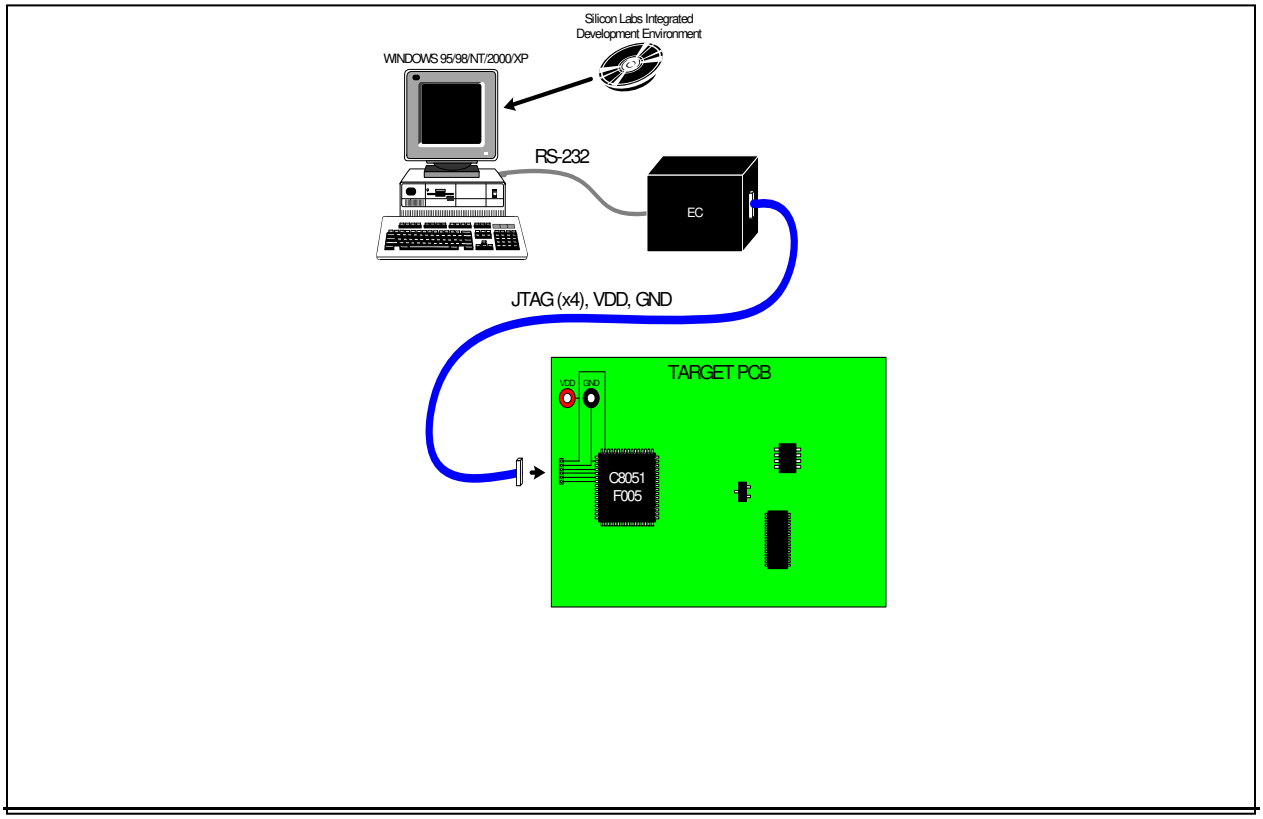
The C8051F000 family has on-chip JTAG and debug circuitry that provide *non-intrusive, full speed, in-circuit debug using the production part installed in the end application* using the four-pin JTAG I/F. The JTAG port is fully compliant to IEEE 1149.1, providing full boundary scan for test and manufacturing purposes.

Silicon Labs' debug system supports inspection and modification of memory and registers, breakpoints, watchpoints, a stack monitor, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them in sync.

The C8051F000DK, C8051F005DK, C8051F010DK, and C8051F015DK are development kits with all the hardware and software necessary to develop application code and perform in-circuit debug with the C8051F000/1/2, F005/6/7, F010/1/2, and F015/6/7 MCUs respectively. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and an RS-232 to JTAG protocol translator module referred to as the EC. It also has a target application board with the associated MCU installed and a large prototyping area, plus the RS-232 and JTAG cables, and wall-mount power supply. The Development Kit requires a Windows 95/98/NT/2000/XP computer with one available RS-232 serial port. As shown in Figure 1.7, the PC is connected via RS-232 to the EC. A six-inch ribbon cable connects the EC to the user's application board, picking up the four JTAG pins and VDD and GND. The EC takes its power from the application board. It requires roughly 20mA at 2.7-3.6V. For applications where there is not sufficient power available from the target board, the provided power supply can be connected directly to the EC.

This is a vastly superior configuration for developing and debugging embedded applications compared to standard MCU Emulators, which use on-board "ICE Chips" and target cables and require the MCU in the application board to be socketed. Silicon Labs' debug environment both increases ease of use and preserves the performance of the precision analog peripherals.

Figure 1.7. Debug Environment Diagram



1.4. Programmable Digital I/O and Crossbar

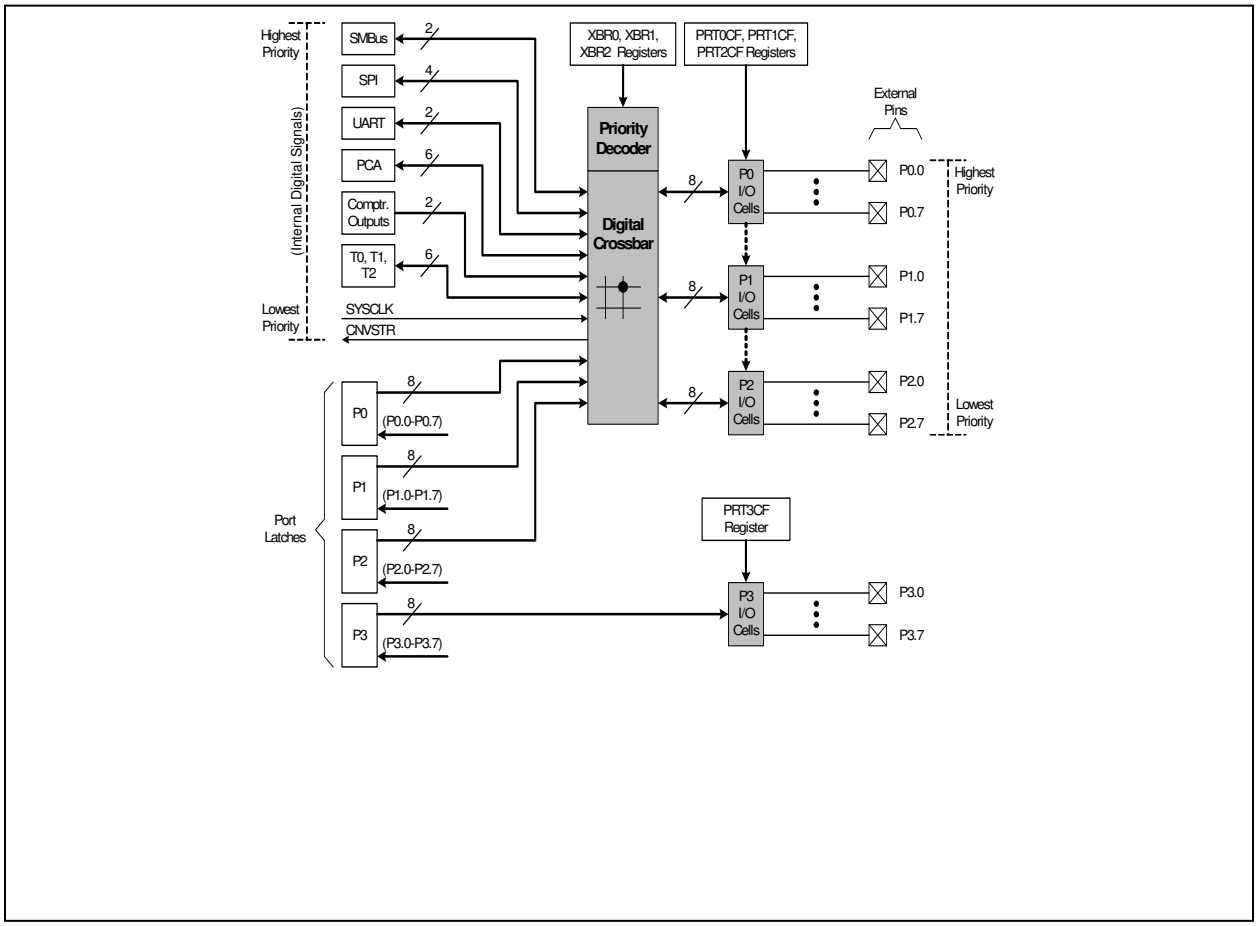
The standard 8051 Ports (0, 1, 2, and 3) are available on the MCUs. All four ports are pinned out on the F000/05/10/15. Ports 0 and 1 are pinned out on the F001/06/11/16, and only Port 0 is pinned out on the F002/07/12/17. The Ports not pinned out are still available for software use as general purpose registers. The Port I/O behave like the standard 8051 with a few enhancements.

Each Port I/O pin can be configured as either a push-pull or open-drain output. Also, the "weak pull-ups" which are normally fixed on an 8051 can be globally disabled, providing additional power saving capabilities for low power applications.

Perhaps the most unique enhancement is the Digital Crossbar. This is essentially a large digital switching network that allows mapping of internal digital system resources to Port I/O pins on P0, P1, and P2. (See Figure 1.8.) Unlike microcontrollers with standard multiplexed digital I/O, all combinations of functions are supported.

The on-board counter/timers, serial buses, HW interrupts, ADC Start of Conversion input, comparator outputs, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for his particular application.

Figure 1.8. Digital Crossbar Diagram

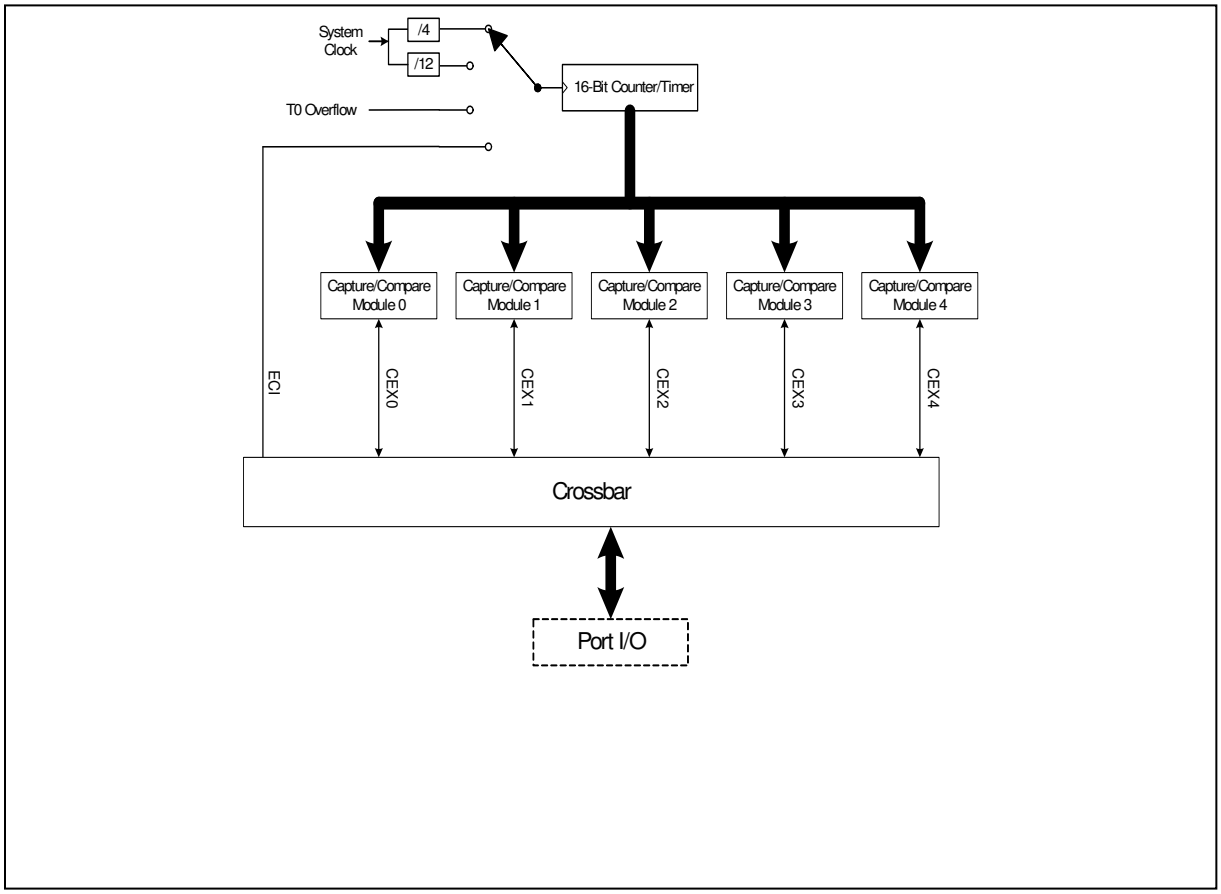


1.5. Programmable Counter Array

The C8051F000 MCU family has an on-board Programmable Counter/Timer Array (PCA) in addition to the four 16-bit general-purpose counter/timers. The PCA consists of a dedicated 16-bit counter/timer timebase with 5 programmable capture/compare modules. The timebase gets its clock from one of four sources: the system clock divided by 12, the system clock divided by 4, Timer 0 overflow, or an External Clock Input (ECI).

Each capture/compare module can be configured to operate in one of four modes: Edge-Triggered Capture, Software Timer, High Speed Output, or Pulse Width Modulator. The PCA Capture/Compare Module I/O and External Clock Input are routed to the MCU Port I/O via the Digital Crossbar.

Figure 1.9. PCA Block Diagram



1.6. Serial Ports

The C8051F000 MCU Family includes a Full-Duplex UART, SPI Bus, and I2C/SMBus. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little intervention by the CPU. The serial buses do not "share" resources such as timers, interrupts, or Port I/O, so any or all of the serial buses may be used together.

1.7. Analog to Digital Converter

The C8051F000/1/2/5/6/7 has an on-chip 12-bit SAR ADC with a 9-channel input multiplexer and programmable gain amplifier. With a maximum throughput of 100ksps, the ADC offers true 12-bit accuracy with an INL of ±1LSB. The ADC in the C8051F010/1/2/5/6/7 is similar, but with 10-bit resolution. Each ADC has a maximum throughput of 100ksps. Each ADC has an INL of ±1LSB, offering true 12-bit accuracy with the C8051F00x, and true 10-bit accuracy with the C8051F01x. There is also an on-board 15ppm voltage reference, or an external reference may be used via the VREF pin.

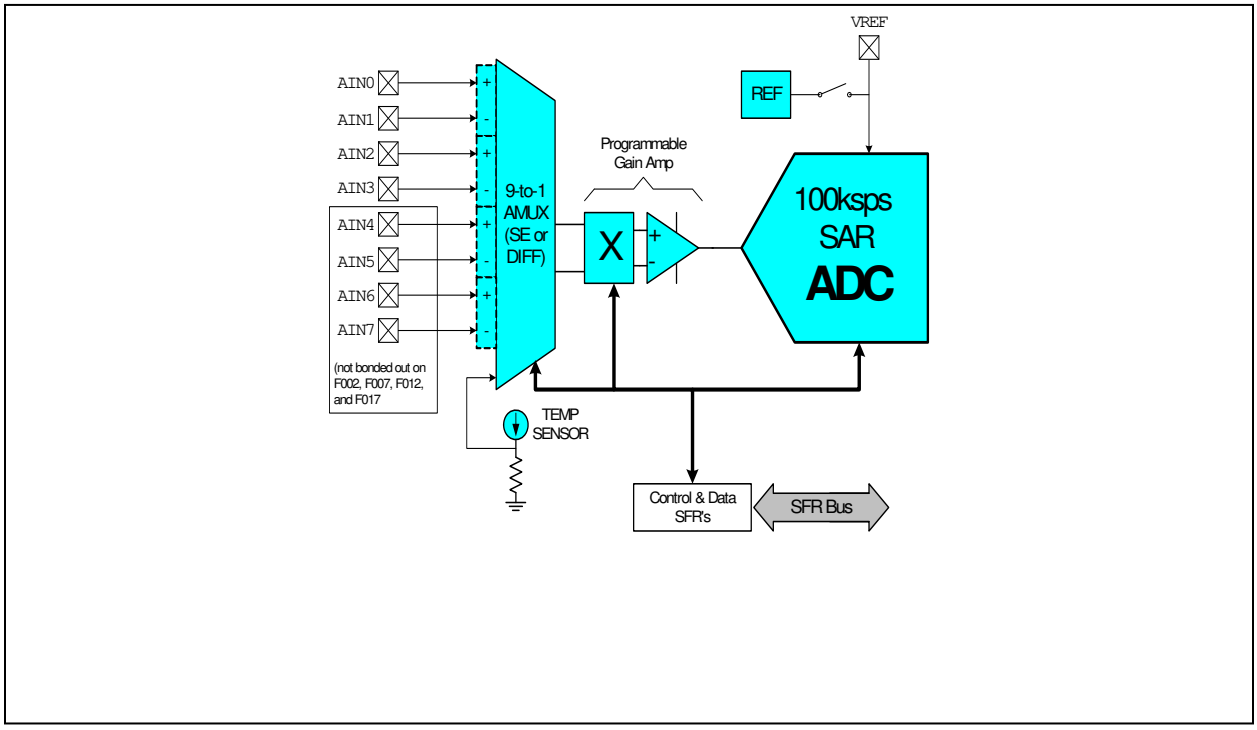
The ADC is under full control of the CIP-51 microcontroller via the Special Function Registers. One input channel is tied to an internal temperature sensor, while the other eight channels are available externally. Each pair of the eight external input channels can be configured as either two single-ended inputs or a single differential input. The system controller can also put the ADC into shutdown to save power.

A programmable gain amplifier follows the analog multiplexer. The gain can be set in software from 0.5 to 16 in powers of 2. The gain stage can be especially useful when different ADC input channels have widely varied input voltage signals, or when it is necessary to "zoom in" on a signal with a large DC offset (in differential mode, a DAC could be used to provide the DC offset).

Conversions can be started in four ways; a software command, an overflow on Timer 2, an overflow on Timer 3, or an external signal input. This flexibility allows the start of conversion to be triggered by software events, external HW signals, or convert continuously. A completed conversion causes an interrupt, or a status bit can be polled in software to determine the end of conversion. The resulting 10 or 12-bit data word is latched into two SFRs upon completion of a conversion. The data can be right or left justified in these registers under software control.

Compare registers for the ADC data can be configured to interrupt the controller when ADC data is within a specified window. The ADC can monitor a key voltage continuously in background mode, but not interrupt the controller unless the converted data is within the specified window.

Figure 1.10. ADC Diagram



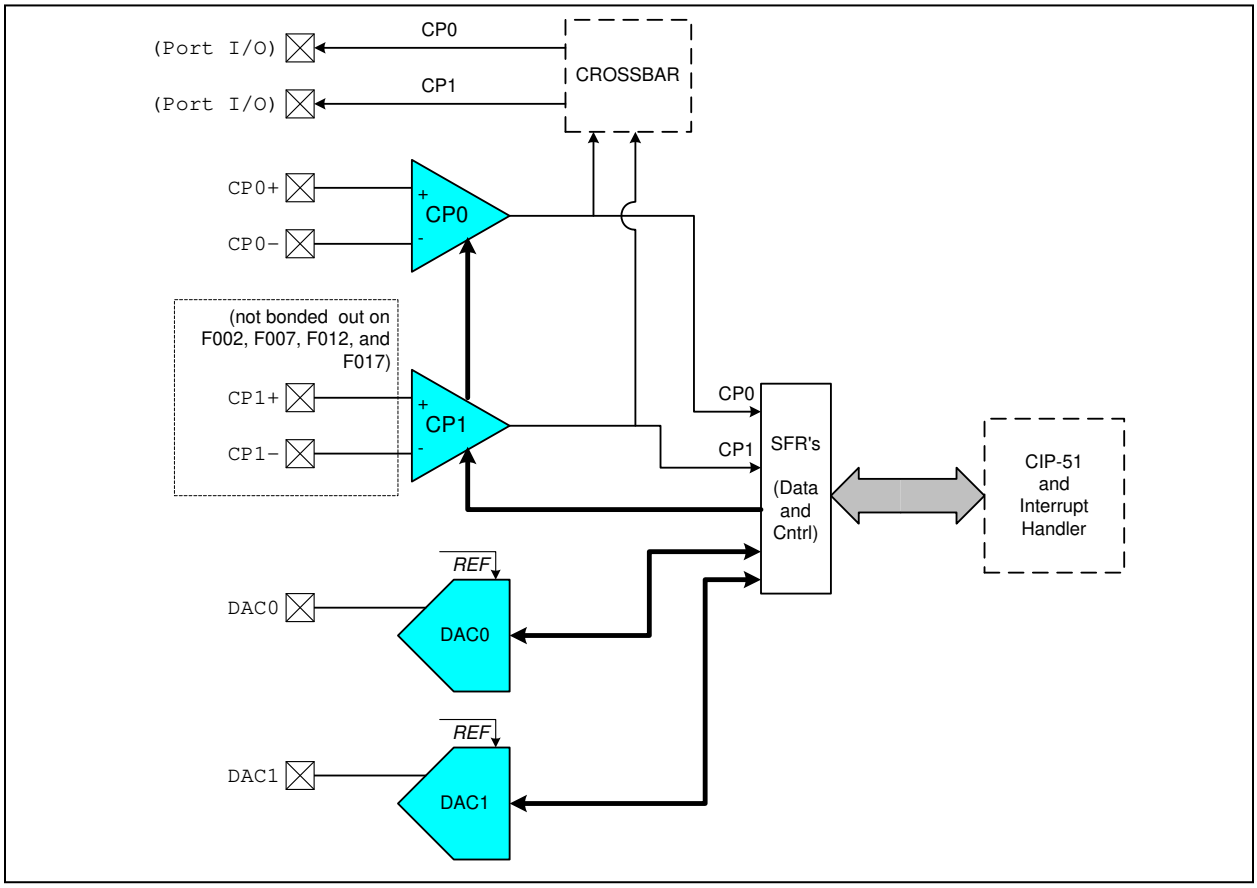
1.8. Comparators and DACs

The C8051F000 MCU Family has two 12-bit DACs and two comparators on chip (the second comparator, CP1, is not bonded out on the F002, F007, F012, and F017). The MCU data and control interface to each comparator and DAC is via the Special Function Registers. The MCU can place any DAC or comparator in low power shutdown mode.

The comparators have software programmable hysteresis. Each comparator can generate an interrupt on its rising edge, falling edge, or both. The comparators' output state can also be polled in software. These interrupts are capable of waking up the MCU from idle mode. The comparator outputs can be programmed to appear on the Port I/O pins via the Crossbar.

The DACs are voltage output mode and use the same voltage reference as the ADC. They are especially useful as references for the comparators or offsets for the differential inputs of the ADC.

Figure 1.11. Comparator and DAC Diagram



2. ABSOLUTE MAXIMUM RATINGS*

Ambient temperature under bias ..... -55 to 125°C
Storage Temperature ..... -65 to 150°C
Voltage on any Pin (except VDD and Port I/O) with respect to DGND ..... -0.3V to (VDD + 0.3V)
Voltage on any Port I/O Pin or /RST with respect to DGND ..... -0.3V to 5.8V
Voltage on VDD with respect to DGND ..... -0.3V to 4.2V
Maximum Total current through VDD, AV+, DGND and AGND 800mA
Maximum output current sunk by any Port pin 100mA
Maximum output current sunk by any other I/O pin 25mA
Maximum output current sourced by any Port pin 100mA
Maximum output current sourced by any other I/O pin 25mA

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. GLOBAL DC ELECTRICAL CHARACTERISTICS

-40°C to +85°C unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Supply Voltage	(Note 1)	2.7	3.0	3.6	V
Analog Supply Current	Internal REF, ADC, DAC, Comparators all active		1	2	mA
Analog Supply Current with analog sub-systems inactive	Internal REF, ADC, DAC, Comparators all disabled, oscillator disabled		5	20	µA
Analog-to-Digital Supply Delta (| VDD – AV+ |)				0.5	V
Digital Supply Voltage		2.7	3.0	3.6	V
Digital Supply Current with CPU active	VDD = 2.7V, Clock=25MHz VDD = 2.7V, Clock=1MHz VDD = 2.7V, Clock=32kHz		12.5 0.5 10		mA mA µA
Digital Supply Current (shutdown)	Oscillator not running		5		µA
Digital Supply RAM Data Retention Voltage			1.5		V
Specified Operating Temperature Range		-40		+85	°C
SYSCLK (System Clock Frequency)	C8051F005/6/7, C8051F015/6/7 (Note 2)	0		25	MHz
SYSCLK (System Clock Frequency)	C8051F000/1/2, C8051F010/1/2 (Note 2)	0		20	MHz
Tsysl (SYSCLK Low Time)		18			ns
Tsysh (SYSCLK High Time)		18			ns

Note 1: Analog Supply AV+ must be greater than 1V for VDD monitor to operate.
Note 2: SYSCLK must be at least 32 kHz to enable debugging.

4. PINOUT AND PACKAGE DEFINITIONS

Table 4.1. Pin Definitions

Name	Pin Numbers			Type	Description
	F000 F005 F010 F015	F001 F006 F011 F016	F002 F007 F012 F017		
VDD	31, 40, 62	23, 32	18, 20		Digital Voltage Supply.
DGND	30, 41, 61	22, 33, 27, 19	17, 21		Digital Ground.
AV+	16, 17	13, 43	9, 29		Positive Analog Voltage Supply.
AGND	5, 15	44, 12	8, 30		Analog Ground.
TCK	22	18	14	D In	JTAG Test Clock with internal pull-up.
TMS	21	17	13	D In	JTAG Test-Mode Select with internal pull-up.
TDI	28	20	15	D In	JTAG Test Data Input with internal pull-up. TDI is latched on a rising edge of TCK.
TDO	29	21	16	D Out	JTAG Test Data Output with internal pull-up. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
XTAL1	18	14	10	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL2	19	15	11	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
/RST	20	16	12	D I/O	Chip Reset. Open-drain output of internal Voltage Supply monitor. Is driven low when VDD is < 2.7V. An external source can force a system reset by driving this pin low.
VREF	6	3	3	A I/O	Voltage Reference. When configured as an input, this pin is the voltage reference for the MCU. Otherwise, the internal reference drives this pin.
CP0+	4	2	2	A In	Comparator 0 Non-Inverting Input.
CP0−	3	1	1	A In	Comparator 0 Inverting Input.
CP1+	2	45		A In	Comparator 1 Non-Inverting Input.
CP1−	1	46		A In	Comparator 1 Inverting Input.
DAC0	64	48	32	A Out	Digital to Analog Converter Output 0. The DAC0 voltage output. (See Section 7 DAC Specification for complete description).
DAC1	63	47	31	A Out	Digital to Analog Converter Output 1. The DAC1 voltage output. (See Section 7 DAC Specification for complete description).
AIN0	7	4	4	A In	Analog Mux Channel Input 0. (See ADC Specification for complete description).
AIN1	8	5	5	A In	Analog Mux Channel Input 1. (See ADC Specification for complete description).
AIN2	9	6	6	A In	Analog Mux Channel Input 2. (See ADC Specification for complete description).
AIN3	10	7	7	A In	Analog Mux Channel Input 3. (See ADC Specification for complete description).
AIN4	11	8		A In	Analog Mux Channel Input 4. (See ADC Specification for complete description).
AIN5	12	9		A In	Analog Mux Channel Input 5. (See ADC Specification for complete description).

Name	Pin Numbers			Type	Description
	F000 F005 F010 F015	F001 F006 F011 F016	F002 F007 F012 F017		
AIN6	13	10		A In	Analog Mux Channel Input 6. (See ADC Specification for complete description).
AIN7	14	11		A In	Analog Mux Channel Input 7. (See ADC Specification for complete description).
P0.0	39	31	19	D I/O	Port0 Bit0. (See the Port I/O Sub-System section for complete description).
P0.1	42	34	22	D I/O	Port0 Bit1. (See the Port I/O Sub-System section for complete description).
P0.2	47	35	23	D I/O	Port0 Bit2. (See the Port I/O Sub-System section for complete description).
P0.3	48	36	24	D I/O	Port0 Bit3. (See the Port I/O Sub-System section for complete description).
P0.4	49	37	25	D I/O	Port0 Bit4. (See the Port I/O Sub-System section for complete description).
P0.5	50	38	26	D I/O	Port0 Bit5. (See the Port I/O Sub-System section for complete description).
P0.6	55	39	27	D I/O	Port0 Bit6. (See the Port I/O Sub-System section for complete description).
P0.7	56	40	28	D I/O	Port0 Bit7. (See the Port I/O Sub-System section for complete description).
P1.0	38	30		D I/O	Port1 Bit0. (See the Port I/O Sub-System section for complete description).
P1.1	37	29		D I/O	Port1 Bit1. (See the Port I/O Sub-System section for complete description).
P1.2	36	28		D I/O	Port1 Bit2. (See the Port I/O Sub-System section for complete description).
P1.3	35	26		D I/O	Port1 Bit3. (See the Port I/O Sub-System section for complete description).
P1.4	34	25		D I/O	Port1 Bit4. (See the Port I/O Sub-System section for complete description).
P1.5	32	24		D I/O	Port1 Bit5. (See the Port I/O Sub-System section for complete description).
P1.6	60	42		D I/O	Port1 Bit6. (See the Port I/O Sub-System section for complete description).
P1.7	59	41		D I/O	Port1 Bit7. (See the Port I/O Sub-System section for complete description).
P2.0	33			D I/O	Port2 Bit0. (See the Port I/O Sub-System section for complete description).
P2.1	27			D I/O	Port2 Bit1. (See the Port I/O Sub-System section for complete description).
P2.2	54			D I/O	Port2 Bit2. (See the Port I/O Sub-System section for complete description).
P2.3	53			D I/O	Port2 Bit3. (See the Port I/O Sub-System section for complete description).
P2.4	52			D I/O	Port2 Bit4. (See the Port I/O Sub-System section for complete description).
P2.5	51			D I/O	Port2 Bit5. (See the Port I/O Sub-System section for complete description).
P2.6	44			D I/O	Port2 Bit6. (See the Port I/O Sub-System section for complete description).
P2.7	43			D I/O	Port2 Bit7. (See the Port I/O Sub-System section for complete description).
P3.0	26			D I/O	Port3 Bit0. (See the Port I/O Sub-System section for complete description).
P3.1	25			D I/O	Port3 Bit1. (See the Port I/O Sub-System section for complete description).
P3.2	24			D I/O	Port3 Bit2. (See the Port I/O Sub-System section for complete description).
P3.3	23			D I/O	Port3 Bit3. (See the Port I/O Sub-System section for complete description).
P3.4	58			D I/O	Port3 Bit4. (See the Port I/O Sub-System section for complete description).
P3.5	57			D I/O	Port3 Bit5. (See the Port I/O Sub-System section for complete description).
P3.6	46			D I/O	Port3 Bit6. (See the Port I/O Sub-System section for complete description).
P3.7	45			D I/O	Port3 Bit7. (See the Port I/O Sub-System section for complete description).

Figure 4.1. TQFP-64 Pinout Diagram

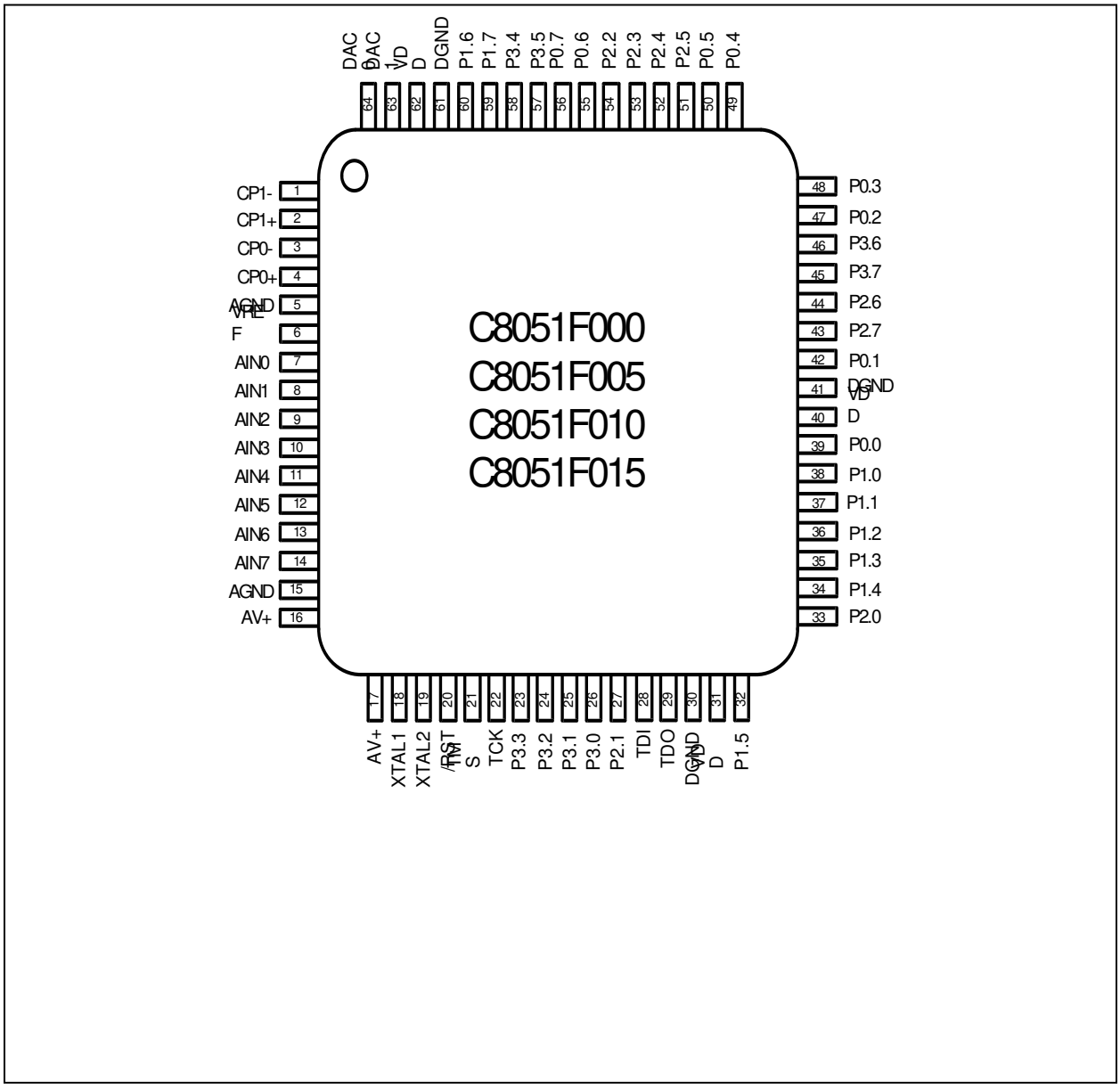
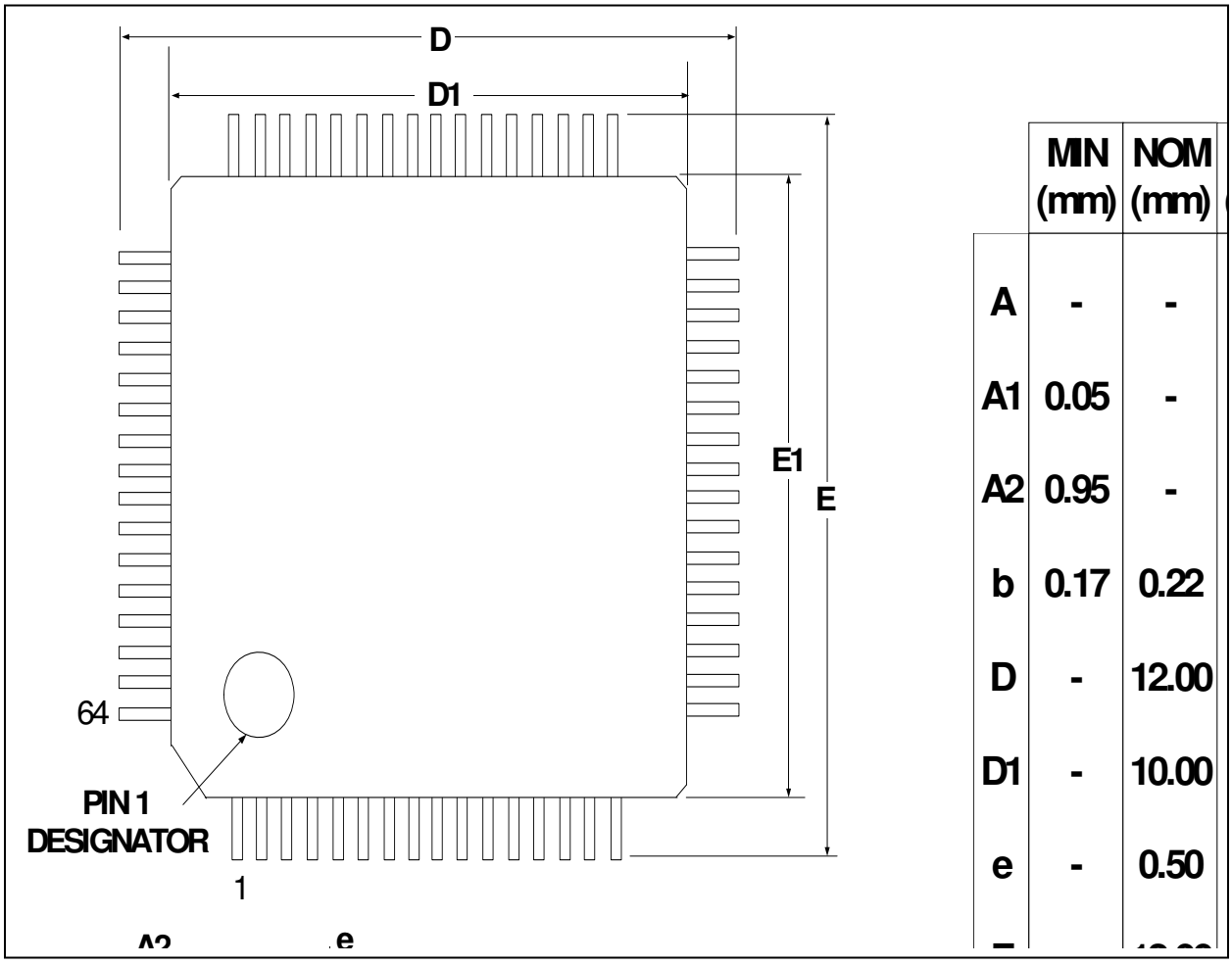


Figure 4.2. TQFP-64 Package Drawing



	MIN (mm)	NOM (mm)
A	-	-
A1	0.05	-
A2	0.95	-
b	0.17	0.22
D	-	12.00
D1	-	10.00
e	-	0.50

Figure 4.3. TQFP-48 Pinout Diagram