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C8051F020/1/2/3

8K ISP FLASH MCU Family

ANALOG PERIPHERALS
- **SAR ADC**
  - 12-Bit (C8051F020/1)
  - 10-Bit (C8051F022/3)
  - ± 1 LSB INL
  - Programmable Throughput up to 100 ksps
  - Up to 8 External Inputs; Programmable as Single-Ended or Differential
  - Programmable Amplifier Gain: 16, 8, 4, 2, 1, 0.5
  - Data-Dependent Windowed Interrupt Generator
  - Built-in Temperature Sensor (± 3°C)
- **8-bit ADC**
  - Programmable Throughput up to 500 ksps
  - 8 External Inputs
  - Programmable Amplifier Gain: 4, 2, 1, 0.5
- **Two 12-bit DACs**
  - Can Synchronize Outputs to Timers for Jitter-Free Waveform Generation
- **Two Analog Comparators**
- **Voltage Reference**
- **Precision VDD Monitor/Brown-Out Detector**

ON-CHIP JTAG DEBUG & BOUNDARY SCAN
- On-Chip Debug Circuitry Facilitates Full- Speed, Non-Intrusive In-Circuit/In-System Debugging
- Provides Breakpoints, Single-Stepping, Watchpoints, Stack Monitor; Inspect/Modify Memory and Registers
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets
- IEEE1149.1 Compliant Boundary Scan
- Low-Cost, **Complete** Development Kit

HIGH SPEED 8051 µC CORE
- Pipelined Instruction Architecture; Executes 70% of Instruction Set in 1 or 2 System Clocks
- Up to 25 MIPS Throughput with 25 MHz Clock
- 22 Vectored Interrupt Sources

MEMORY
- 4352 Bytes Internal Data RAM (4k + 256)
- 64k Bytes FLASH; In-System programmable in 512-byte Sectors
- External 64k Byte Data Memory Interface (programmable multiplexed or non-multiplexed modes)

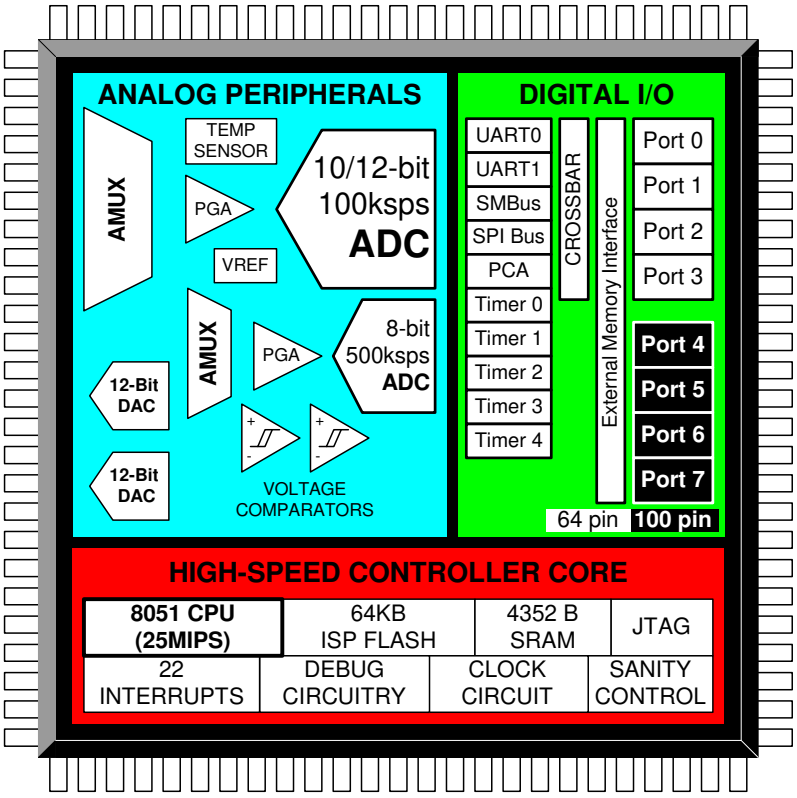
DIGITAL PERIPHERALS
- 8 Byte-Wide Port I/O (C8051F020/2); 5V tolerant
- 4 Byte-Wide Port I/O (C8051F021/3); 5V tolerant
- Hardware SMBus™ (I^2C™ Compatible), SPI™, and Two UART Serial Ports Available Concurrently
- Programmable 16-bit Counter/Timer Array with 5 Capture/Compare Modules
- 5 General Purpose 16-bit Counter/Timers
- Dedicated Watch-Dog Timer; Bi-directional Reset Pin

CLOCK SOURCES
- Internal Programmable Oscillator: 2-to-16 MHz
- External Oscillator: Crystal, RC, C, or Clock
- Real-Time Clock Mode using Timer 3 or PCA

SUPPLY VOLTAGE ..... 2.7V TO 3.6V
- Typical Operating Current: 10 mA @ 20 MHz
- Multiple Power Saving Sleep and Shutdown Modes

100-Pin TQFP and 64-Pin TQFP Packages Available

Temperature Range: -40°C to +85°C



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1. SYSTEM OVERVIEW

The C8051F020/1/2/3 devices are fully integrated mixed-signal System-on-a-Chip MCUs with 64 digital I/O pins (C8051F020/2) or 32 digital I/O pins (C8051F021/3). Highlighted features are listed below; refer to Table 1.1 for specific product feature selection.

- High-Speed pipelined 8051-compatible CIP-51 microcontroller core (up to 25 MIPS)
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit (C8051F020/1) or 10-bit (C8051F022/3) 100 ksps 8-channel ADC with PGA and analog multiplexer
- True 8-bit ADC 500 ksps 8-channel ADC with PGA and analog multiplexer
- Two 12-bit DACs with programmable update scheduling
- 64k bytes of in-system programmable FLASH memory
- 4352 (4096 + 256) bytes of on-chip RAM
- External Data Memory Interface with 64k byte address space
- SPI, SMBus/I^2C, and (2) UART serial interfaces implemented in hardware
- Five general purpose 16-bit Timers
- Programmable Counter/Timer Array with five capture/compare modules
- On-chip Watchdog Timer, VDD Monitor, and Temperature Sensor

With on-chip VDD monitor, Watchdog Timer, and clock oscillator, the C8051F020/1/2/3 devices are truly stand-alone System-on-a-Chip solutions. All analog and digital peripherals are enabled/disabled and configured by user firmware. The FLASH memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware.

On-board JTAG debug circuitry allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional while debugging using JTAG.

Each MCU is specified for 2.7 V-to-3.6 V operation over the industrial temperature range (-45° C to +85° C). The Port I/Os, /RST, and JTAG pins are tolerant for input signals up to 5 V. The C8051F020/2 are available in a 100-pin TQFP package (see block diagrams in Figure 1.1 and Figure 1.3). The C8051F021/3 are available in a 64-pin TQFP package (see block diagrams in Figure 1.2 and Figure 1.4).

Table 1.1. Product Selection Guide

	MIPS (Peak)	FLASH Memory	RAM	External Memory Interface	SMBus/I^2C	SPI	UARTS	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	12-bit 100ksps ADC Inputs	10-bit 100ksps ADC Inputs	8-bit 500ksps ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution (bits)	DAC Outputs	Analog Comparators	Package
C8051F020	25	64k	4352	✓	✓	✓	2	5	✓	64	8	-	8	✓	✓	12	2	2	100TQFP
C8051F021	25	64k	4352	✓	✓	✓	2	5	✓	32	8	-	8	✓	✓	12	2	2	64TQFP
C8051F022	25	64k	4352	✓	✓	✓	2	5	✓	64	-	8	8	✓	✓	12	2	2	100TQFP
C8051F023	25	64k	4352	✓	✓	✓	2	5	✓	32	-	8	8	✓	✓	12	2	2	64TQFP

Figure 1.1. C8051F020 Block Diagram

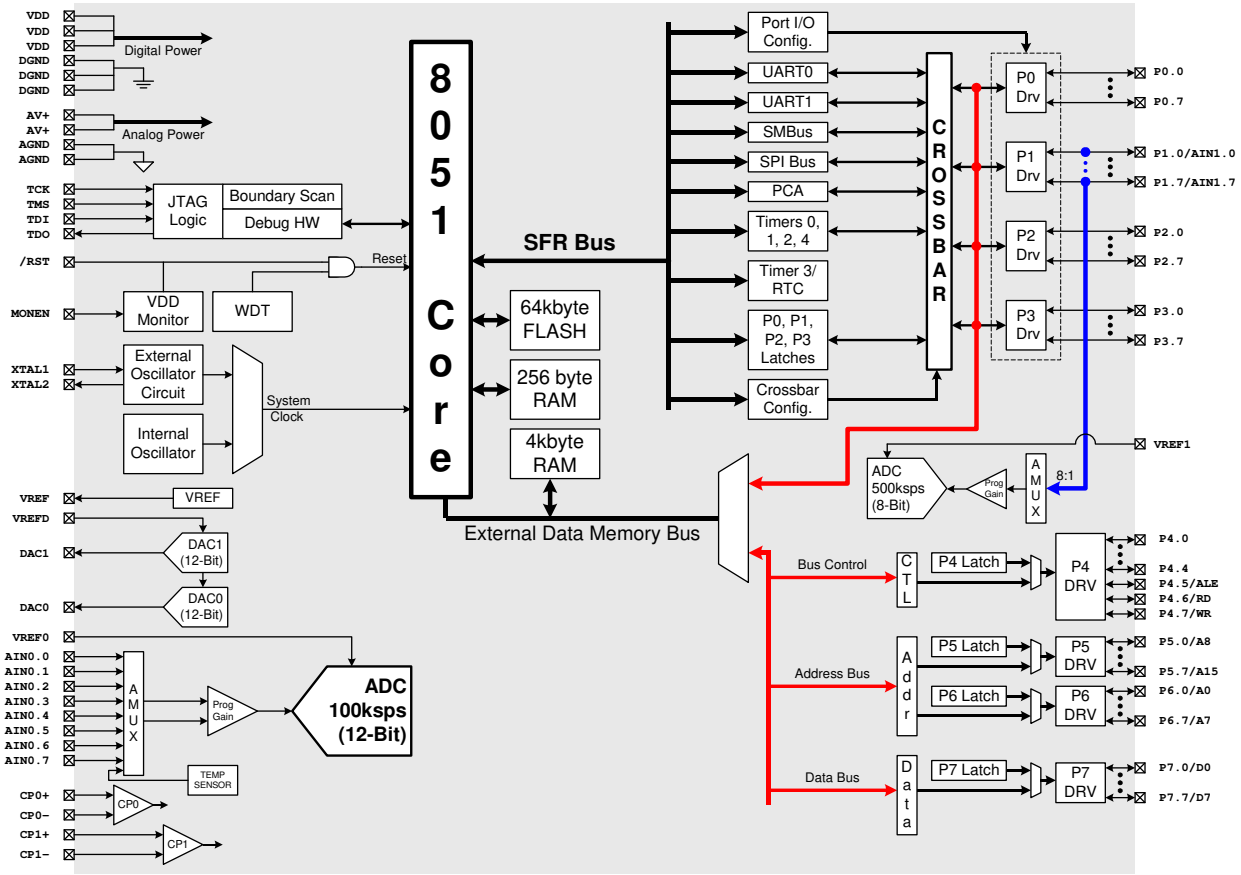


Figure 1.2. C8051F021 Block Diagram

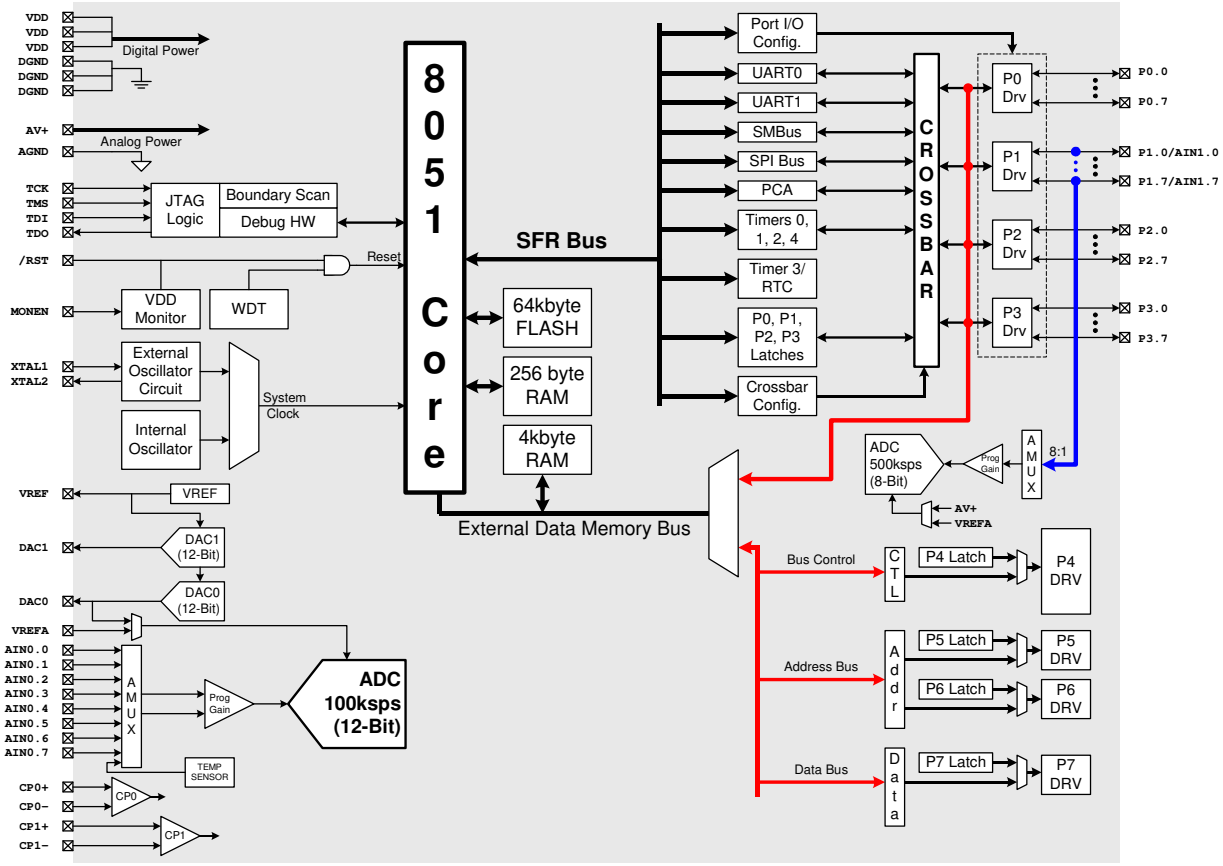


Figure 1.3. C8051F022 Block Diagram

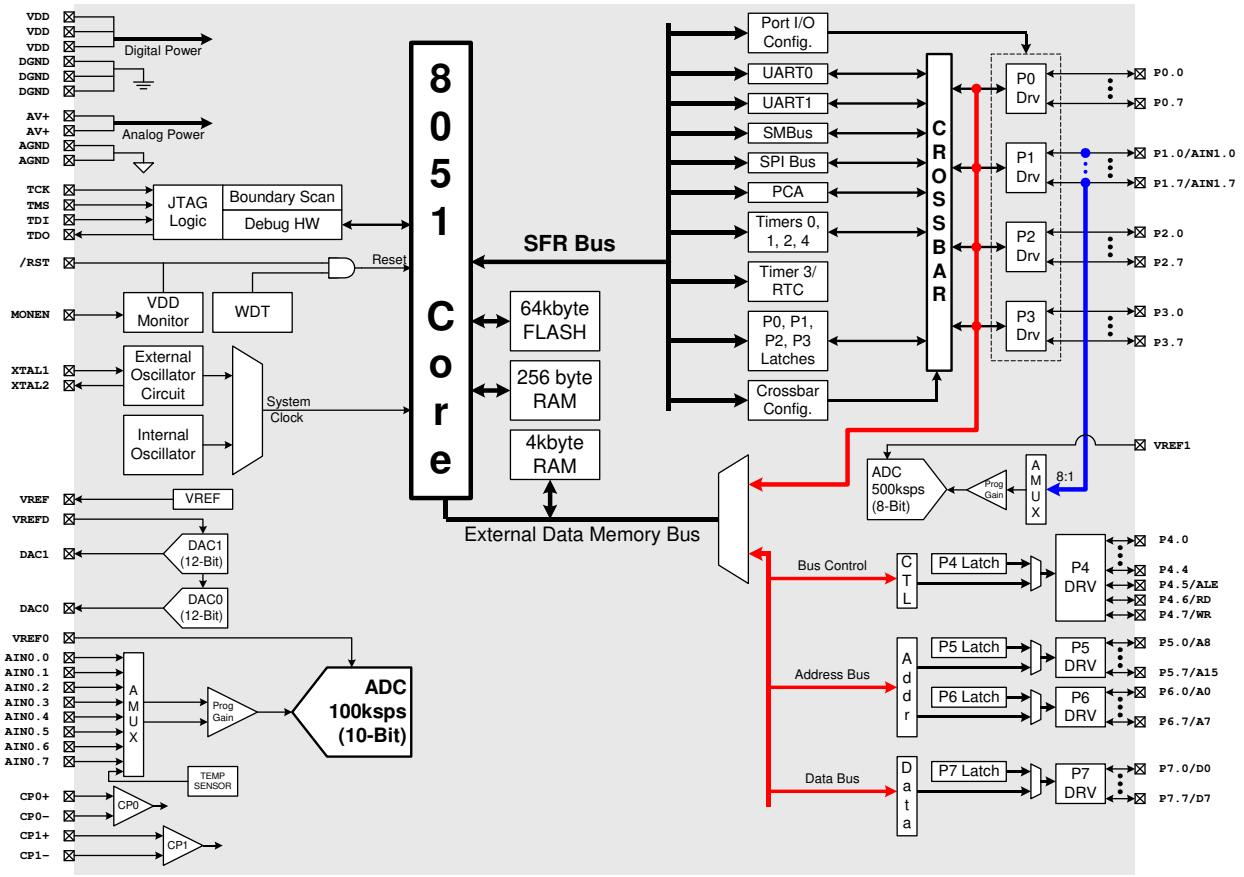
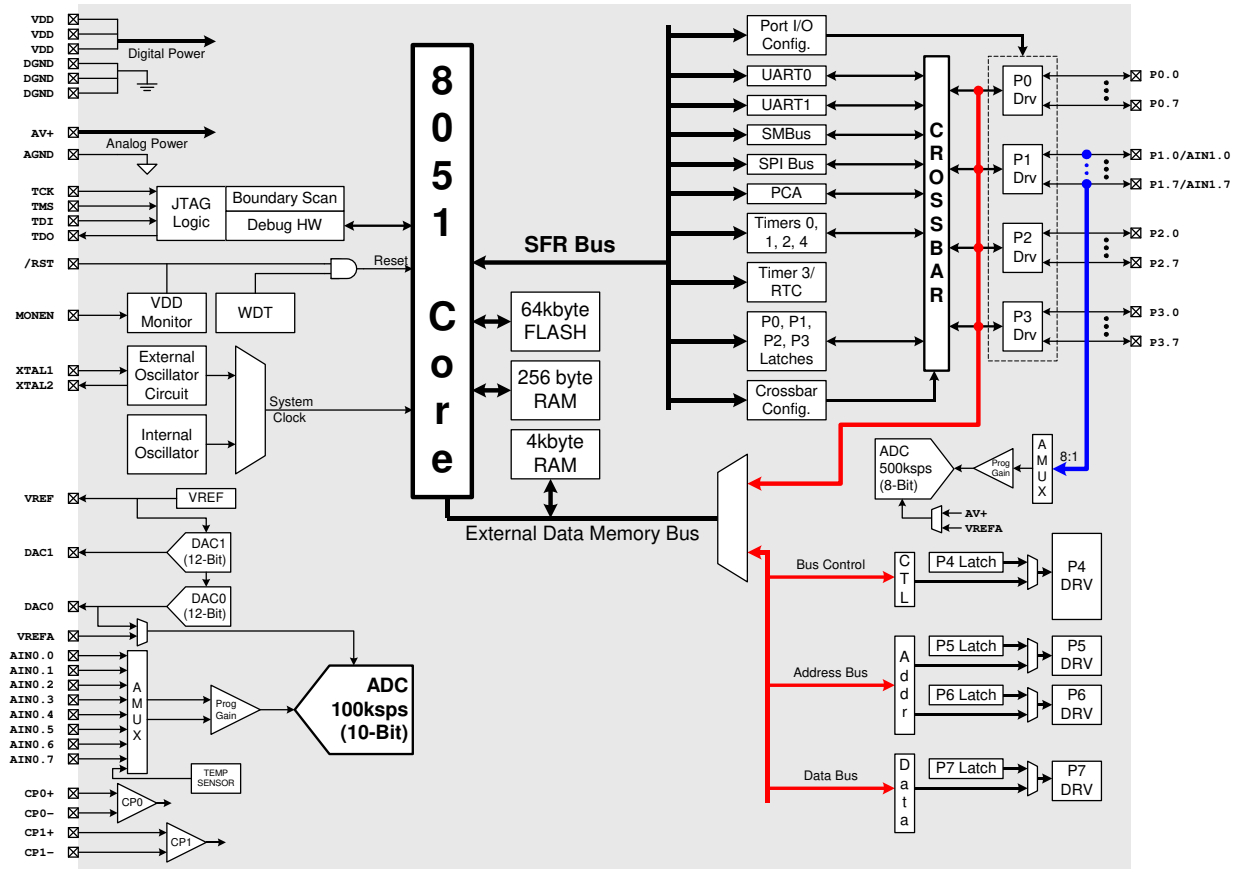


Figure 1.4. C8051F023 Block Diagram



1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F020 family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The core has all the peripherals included with a standard 8052, including five 16-bit counter/timers, two full-duplex UARTs, 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and 8/4 byte-wide I/O Ports.

1.1.2. Improved Throughput

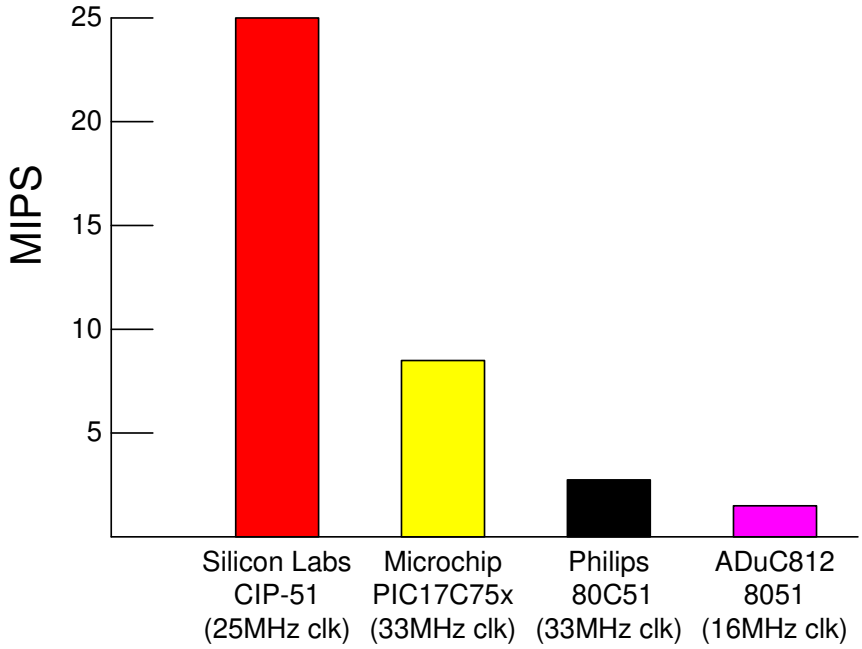
The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

Figure 1.5. Comparison of Peak MCU Execution Speeds



1.1.3. Additional Features

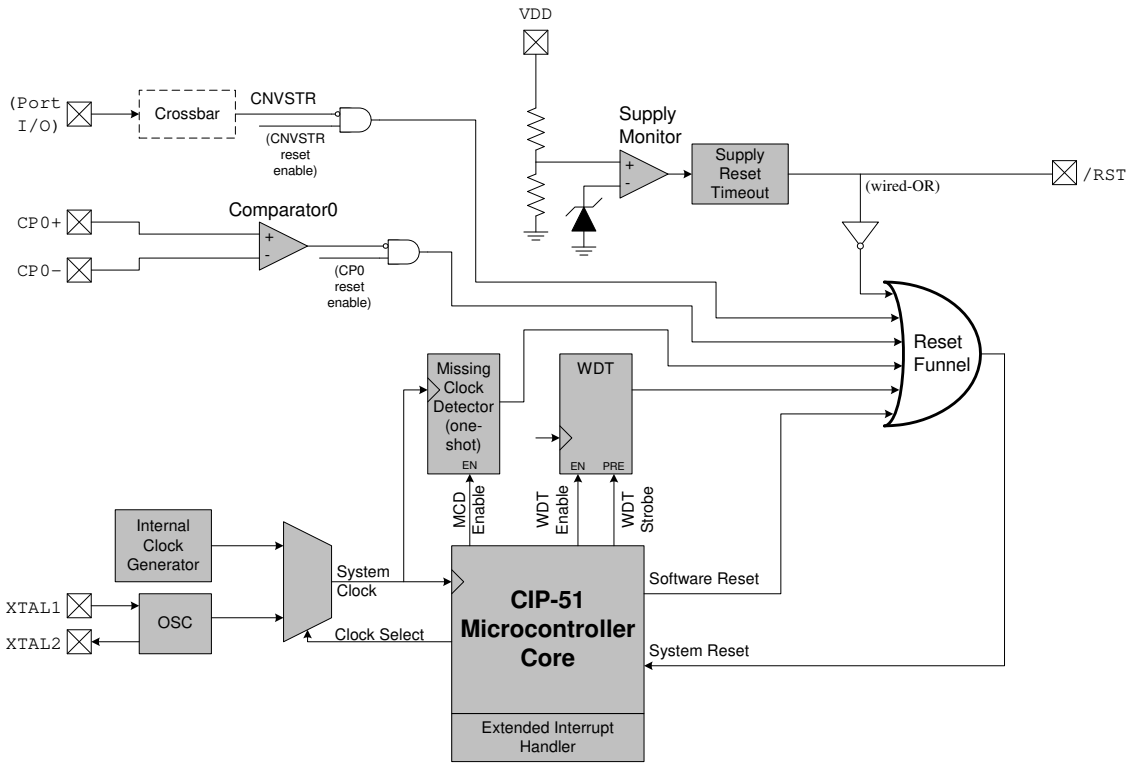
The C8051F020 MCU family includes several key enhancements to the CIP-51 core and peripherals to improve overall performance and ease of use in end applications.

The extended interrupt handler provides 22 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing the numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

There are up to seven reset sources for the MCU: an on-board VDD monitor, a Watchdog Timer, a missing clock detector, a voltage level detection from Comparator0, a forced software reset, the CNVSTR input pin, and the /RST pin. The /RST pin is bi-directional, accommodating an external reset, or allowing the internally generated POR to be output on the /RST pin. Each reset source except for the VDD monitor and Reset Input pin may be disabled by the user in software; the VDD monitor is enabled/disabled via the MONEN pin. The Watchdog Timer may be permanently enabled in software after a power-on reset during MCU initialization.

The MCU has an internal, stand alone clock generator which is used by default as the system clock after any reset. If desired, the clock source may be switched on the fly to the external oscillator, which can use a crystal, ceramic resonator, capacitor, RC, or external clock source to generate the system clock. This can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the fast (up to 16 MHz) internal oscillator as needed.

Figure 1.6. On-Board Clock and Reset



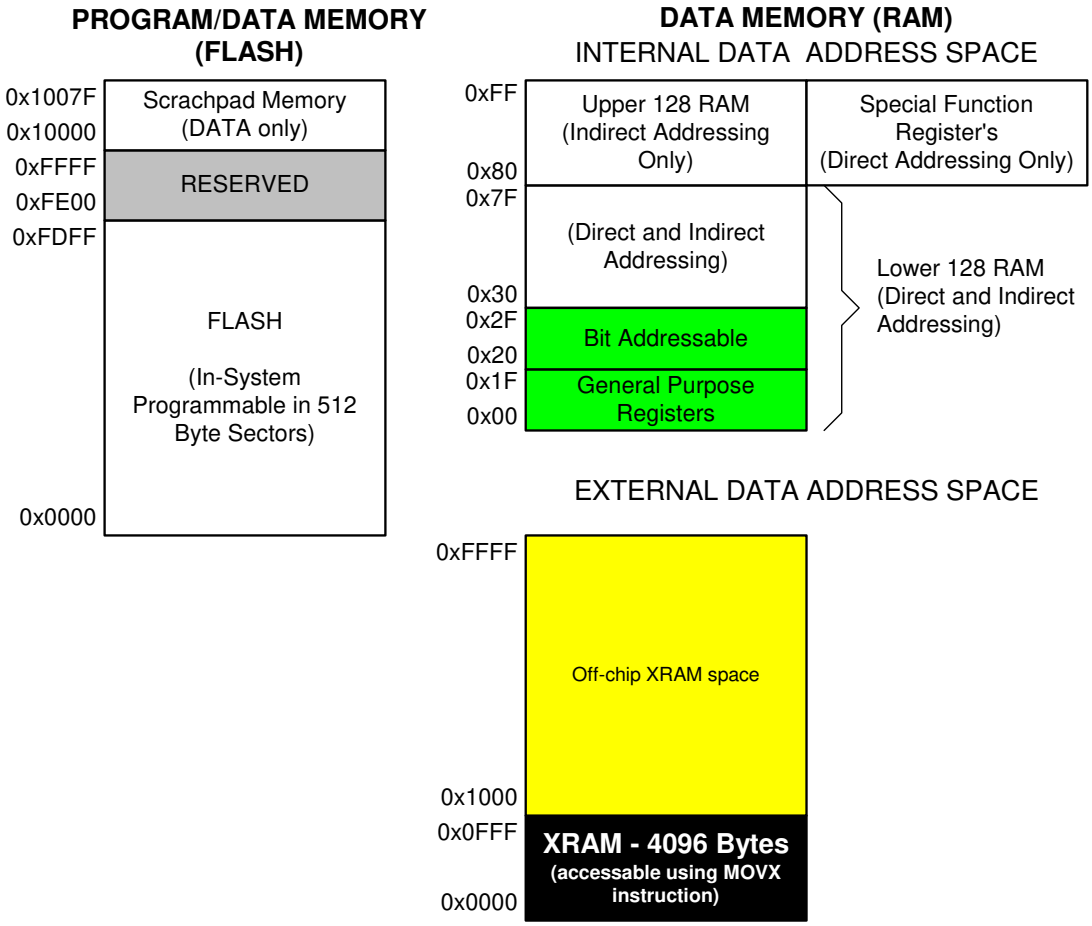
1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The CIP-51 in the C8051F020/1/2/3 MCUs additionally has an on-chip 4k byte RAM block and an external memory interface (EMIF) for accessing off-chip data memory. The on-chip 4k byte block can be addressed over the entire 64k external data memory address range (overlapping 4k boundaries). External data memory address space can be mapped to on-chip memory only, off-chip memory only, or a combination of the two (addresses up to 4k directed to on-chip, above 4k directed to EMIF). The EMIF is also configurable for multiplexed or non-multiplexed address/data lines.

The MCU's program memory consists of 64k bytes of FLASH. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0xFE00 to 0xFFFF are reserved for factory use. There is also a single 128 byte sector at address 0x10000 to 0x1007F, which may be useful as a small table for software constants. See Figure 1.7 for the MCU system memory map.

Figure 1.7. On-Chip Memory Map



1.3. JTAG Debug and Boundary Scan

The C8051F020 family has on-chip JTAG boundary scan and debug circuitry that provides *non-intrusive, full speed, in-circuit debugging using the production part installed in the end application*, via the four-pin JTAG interface. The JTAG port is fully compliant to IEEE 1149.1, providing full boundary scan for test and manufacturing purposes.

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, watchpoints, a stack monitor, and single stepping. No additional target RAM, program memory, timers, or communications channels are required. All the digital and analog peripherals are functional and work correctly while debugging. All the peripherals (except for the ADC and SMBus) are stalled when the MCU is halted, during single stepping, or at a breakpoint in order to keep them synchronized.

The C8051F020DK development kit provides all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8051F020/1/2/3 MCUs. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and an RS-232 to JTAG serial adapter. It also has a target application board with the associated MCU installed, plus the RS-232 and JTAG cables, and wall-mount power supply. The Development Kit requires a Windows 95/98/NT/ME/2000 computer with one available RS-232 serial port. As shown in Figure 1.8, the PC is connected via RS-232 to the Serial Adapter. A six-inch ribbon cable connects the Serial Adapter to the user's application board, picking up the four JTAG pins and VDD and GND. The Serial Adapter takes its power from the application board; it requires roughly 20 mA at 2.7-3.6 V. For applications where there is not sufficient power available from the target system, the provided power supply can be connected directly to the Serial Adapter.

Silicon Labs' debug environment is a vastly superior configuration for developing and debugging embedded applications compared to standard MCU emulators, which use on-board "ICE Chips" and target cables and require the MCU in the application board to be socketed. Silicon Labs' debug environment both increases ease of use and preserves the performance of the precision analog peripherals.

Figure 1.8. Development/In-System Debug Diagram