Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# C8051F040/1/2/3/4/5/6/7

## 8K ISP FLASH MCU Family

### Analog Peripherals
- **10 or 12-Bit SAR ADC**
  - 12-bit (C8051F040/1) or 10-bit (C8051F042/3/4/5/6/7) resolution
  - ± 1 LSB INL, guaranteed no missing codes
  - Programmable throughput up to 100 ksps
  - 13 External Inputs; single-ended or differential
  - SW programmable high voltage difference amplifier
  - Programmable amplifier gain: 16, 8, 4, 2, 1, 0.5
  - Data-dependent windowed interrupt generator
  - Built-in temperature sensor
- **8-bit SAR ADC (C8051F040/1/2/3 only)**
  - Programmable throughput up to 500 ksps
  - 8 External Inputs, single-ended or differential
  - Programmable amplifier gain: 4, 2, 1, 0.5
- **Two 12-bit DACs (C8051F040/1/2/3 only)**
  - Can synchronize outputs to timers for jitter-free waveform generation
- **Three Analog Comparators**
  - Programmable hysteresis/response time
- **Voltage Reference**
- **Precision $V_{DD}$ Monitor/Brown-Out Detector**

### On-Chip JTAG Debug & Boundary Scan
- On-chip debug circuitry facilitates full- speed, non-intrusive in-circuit/in-system debugging
- Provides breakpoints, single-stepping, watchpoints, stack monitor; inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan
- Complete development kit

### High-Speed 8051 µC Core
- Pipelined instruction architecture; executes 70% of instruction set in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- 20 vectored interrupt sources

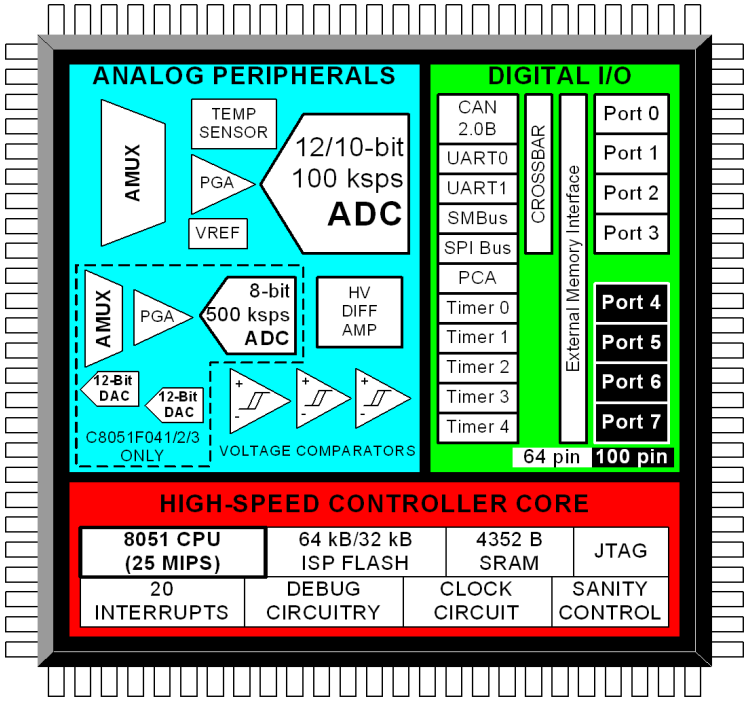
### Memory
- 4352 bytes internal data RAM (4 k + 256)
- 64 kB (C8051F040/1/2/3/4/5) or 32 kB (C8051F046/7) Flash; in-system programmable in 512-byte sectors
- External 64 kB data memory interface (programmable multiplexed or non-multiplexed modes)

### Digital Peripherals
- 8 byte-wide port I/O (C8051F040/2/4/6); 5 V tolerant
- 4 byte-wide port I/O (C8051F041/3/5/7); 5 V tolerant
- Bosch Controller Area Network (CAN 2.0B), hardware SMBus™ ($I^2C$™ Compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with 6 capture/compare modules
- 5 general purpose 16-bit counter/timers
- Dedicated watch-dog timer; bi-directional reset pin

### Clock Sources
- Internal calibrated programmable oscillator: 3 to 24.5 MHz
- External oscillator: crystal, RC, C, or clock
- Real-time clock mode using Timer 2, 3, 4, or PCA

### Supply Voltage: 2.7 to 3.6 V
- Multiple power saving sleep and shutdown modes

### 100-Pin and 64-Pin TQFP Packages Available
- Temperature Range: –40 to +85 °C





Copyright © 2016 by Silicon Laboratories

## Table of Contents


**1. System Overview ..... 19**
1.1. CIP-51™ Microcontroller Core ..... 25
1.1.1. Fully 8051 Compatible ..... 25
1.1.2. Improved Throughput ..... 25
1.1.3. Additional Features ..... 26
1.2. On-Chip Memory ..... 27
1.3. JTAG Debug and Boundary Scan ..... 28
1.4. Programmable Digital I/O and Crossbar ..... 29
1.5. Programmable Counter Array ..... 30
1.6. Controller Area Network ..... 31
1.7. Serial Ports ..... 31
1.8. 12/10-Bit Analog to Digital Converter ..... 32
1.9. 8-Bit Analog to Digital Converter (C8051F040/1/2/3 Only) ..... 33
1.10.Comparators and DACs ..... 34
**2. Absolute Maximum Ratings ..... 35**
**3. Global DC Electrical Characteristic ..... 36**
**4. Pinout and Package Definitions ..... 37**
**5. 12-Bit ADC (ADC0, C8051F040/1 Only) ..... 47**
5.1. Analog Multiplexer and PGA ..... 47
5.1.1. Analog Input Configuration ..... 48
5.2. High-Voltage Difference Amplifier ..... 52
5.3. ADC Modes of Operation ..... 54
5.3.1. Starting a Conversion ..... 54
5.3.2. Tracking Modes ..... 54
5.3.3. Settling Time Requirements ..... 56
5.4. ADC0 Programmable Window Detector ..... 62
**6. 10-Bit ADC (ADC0, C8051F042/3/4/5/6/7 Only) ..... 69**
6.1. Analog Multiplexer and PGA ..... 69
6.1.1. Analog Input Configuration ..... 70
6.2. High-Voltage Difference Amplifier ..... 74
6.3. ADC Modes of Operation ..... 76
6.3.1. Starting a Conversion ..... 76
6.3.2. Tracking Modes ..... 76
6.3.3. Settling Time Requirements ..... 78
6.4. ADC0 Programmable Window Detector ..... 84
**7. 8-Bit ADC (ADC2, C8051F040/1/2/3 Only) ..... 91**
7.1. Analog Multiplexer and PGA ..... 91
7.2. ADC2 Modes of Operation ..... 92
7.2.1. Starting a Conversion ..... 92
7.2.2. Tracking Modes ..... 92
7.2.3. Settling Time Requirements ..... 94
7.3. ADC2 Programmable Window Detector ..... 100
7.3.1. Window Detector in Single-Ended Mode ..... 100

7.3.2. Window Detector in Differential Mode ..... 102
**8. DACs, 12-Bit Voltage Mode (C8051F040/1/2/3 Only) ..... 105**
8.1. DAC Output Scheduling ..... 106
8.1.1. Update Output On-Demand ..... 106
8.1.2. Update Output Based on Timer Overflow ..... 106
8.2. DAC Output Scaling/Justification ..... 106
**9. Voltage Reference (C8051F040/2/4/6) ..... 113**
**10. Voltage Reference (C8051F041/3/5/7) ..... 117**
**11. Comparators ..... 121**
11.1. Comparator Inputs ..... 123
**12. CIP-51 Microcontroller ..... 127**
12.1. Instruction Set ..... 129
12.1.1. Instruction and CPU Timing ..... 129
12.1.2. MOVX Instruction and Program Memory ..... 129
12.2. Memory Organization ..... 133
12.2.1. Program Memory ..... 133
12.2.2. Data Memory ..... 134
12.2.3. General Purpose Registers ..... 134
12.2.4. Bit Addressable Locations ..... 134
12.2.5. Stack ..... 134
12.2.6. Special Function Registers ..... 135
12.2.7. Register Descriptions ..... 150
12.3. Interrupt Handler ..... 153
12.3.1. MCU Interrupt Sources and Vectors ..... 153
12.3.2. External Interrupts ..... 154
12.3.3. Interrupt Priorities ..... 156
12.3.4. Interrupt Latency ..... 156
12.3.5. Interrupt Register Descriptions ..... 156
12.4. Power Management Modes ..... 163
12.4.1. Idle Mode ..... 163
12.4.2. Stop Mode ..... 164
**13. Reset Sources ..... 165**
13.1. Power-On Reset ..... 166
13.2. Power-Fail Reset ..... 166
13.3. External Reset ..... 166
13.4. Missing Clock Detector Reset ..... 167
13.5. Comparator0 Reset ..... 167
13.6. External CNVSTR0 Pin Reset ..... 167
13.7. Watchdog Timer Reset ..... 167
13.7.1. Enable/Reset WDT ..... 168
13.7.2. Disable WDT ..... 168
13.7.3. Disable WDT Lockout ..... 168
13.7.4. Setting WDT Interval ..... 168
**14. Oscillators ..... 173**
14.1. Programmable Internal Oscillator ..... 173

14.2.External Oscillator Drive Circuit ..... 175
14.3.System Clock Selection ..... 175
14.4.External Crystal Example ..... 177
14.5.External RC Example ..... 178
14.6.External Capacitor Example ..... 178
**15. Flash Memory ..... 179**
15.1.Programming The Flash Memory ..... 179
15.2.Non-volatile Data Storage ..... 180
15.3.Security Options ..... 180
15.3.1.Summary of Flash Security Options ..... 183
**16. External Data Memory Interface and On-Chip XRAM ..... 187**
16.1.Accessing XRAM ..... 187
16.1.1.16-Bit MOVX Example ..... 187
16.1.2.8-Bit MOVX Example ..... 187
16.2.Configuring the External Memory Interface ..... 188
16.3.Port Selection and Configuration ..... 188
16.4.Multiplexed and Non-multiplexed Selection ..... 191
16.4.1.Multiplexed Configuration ..... 191
16.4.2.Non-multiplexed Configuration ..... 192
16.5.Memory Mode Selection ..... 193
16.5.1.Internal XRAM Only ..... 193
16.5.2.Split Mode without Bank Select ..... 193
16.5.3.Split Mode with Bank Select ..... 194
16.5.4.External Only ..... 194
16.6.Timing ..... 194
16.6.1.Non-multiplexed Mode ..... 196
16.6.2.Multiplexed Mode ..... 199
**17. Port Input/Output ..... 203**
17.1.Ports 0 through 3 and the Priority Crossbar Decoder ..... 204
17.1.1.Crossbar Pin Assignment and Allocation ..... 205
17.1.2.Configuring the Output Modes of the Port Pins ..... 206
17.1.3.Configuring Port Pins as Digital Inputs ..... 206
17.1.4.Weak Pullups ..... 207
17.1.5.Configuring Port 1, 2, and 3 Pins as Analog Inputs ..... 207
17.1.6.External Memory Interface Pin Assignments ..... 208
17.1.7.Crossbar Pin Assignment Example ..... 210
17.2.Ports 4 through 7 ..... 220
17.2.1.Configuring Ports Which are Not Pinned Out ..... 221
17.2.2.Configuring the Output Modes of the Port Pins ..... 221
17.2.3.Configuring Port Pins as Digital Inputs ..... 221
17.2.4.Weak Pullups ..... 221
17.2.5.External Memory Interface ..... 221
**18. Controller Area Network (CAN0) ..... 227**
18.1.Bosch CAN Controller Operation ..... 228
18.1.1.CAN Controller Timing ..... 229

18.1.2.Example Timing Calculation for 1 Mbit/Sec Communication ..... 229
18.2.CAN Registers ..... 231
18.2.1.CAN Controller Protocol Registers ..... 231
18.2.2.Message Object Interface Registers ..... 231
18.2.3.Message Handler Registers ..... 232
18.2.4.CIP-51 MCU Special Function Registers ..... 232
18.2.5.Using CAN0ADR, CAN0DATH, and CANDATL to Access CAN Registers . 232
18.2.6.CAN0ADR Autoincrement Feature ..... 232
**19. System Management BUS/I2C BUS (SMBUS0) ..... 239**
19.1.Supporting Documents ..... 240
19.2.SMBus Protocol ..... 241
19.2.1.Arbitration ..... 241
19.2.2.Clock Low Extension ..... 242
19.2.3.SCL Low Timeout ..... 242
19.2.4.SCL High (SMBus Free) Timeout ..... 242
19.3.SMBus Transfer Modes ..... 242
19.3.1.Master Transmitter Mode ..... 242
19.3.2.Master Receiver Mode ..... 243
19.3.3.Slave Transmitter Mode ..... 243
19.3.4.Slave Receiver Mode ..... 244
19.4.SMBus Special Function Registers ..... 245
19.4.1.Control Register ..... 245
19.4.2.Clock Rate Register ..... 248
19.4.3.Data Register ..... 249
19.4.4.Address Register ..... 249
19.4.5.Status Register ..... 250
**20. Enhanced Serial Peripheral Interface (SPI0) ..... 255**
20.1.Signal Descriptions ..... 256
20.1.1.Master Out, Slave In (MOSI) ..... 256
20.1.2.Master In, Slave Out (MISO) ..... 256
20.1.3.Serial Clock (SCK) ..... 256
20.1.4.Slave Select (NSS) ..... 256
20.2.SPI0 Master Mode Operation ..... 257
20.3.SPI0 Slave Mode Operation ..... 259
20.4.SPI0 Interrupt Sources ..... 259
20.5.Serial Clock Timing ..... 260
20.6.SPI Special Function Registers ..... 261
**21. UART0 ..... 265**
21.1.UART0 Operational Modes ..... 266
21.1.1.Mode 0: Synchronous Mode ..... 266
21.1.2.Mode 1: 8-Bit UART, Variable Baud Rate ..... 267
21.1.3.Mode 2: 9-Bit UART, Fixed Baud Rate ..... 269
21.1.4.Mode 3: 9-Bit UART, Variable Baud Rate ..... 270
21.2.Multiprocessor Communications ..... 270

21.3.Configuration of a Masked Address ..... 271
21.4.Broadcast Addressing ..... 271
21.5.Frame and Transmission Error Detection..... 272
**22. UART1..... 277**
22.1.Enhanced Baud Rate Generation..... 278
22.2.Operational Modes ..... 279
22.2.1.8-Bit UART ..... 279
22.2.2.9-Bit UART ..... 280
22.3.Multiprocessor Communications ..... 281
**23. Timers..... 289**
23.1.Timer 0 and Timer 1 ..... 289
23.1.1.Mode 0: 13-bit Counter/Timer ..... 289
23.1.2.Mode 1: 16-bit Counter/Timer ..... 290
23.1.3.Mode 2: 8-bit Counter/Timer with Auto-Reload..... 291
23.1.4.Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)..... 292
23.2.Timer 2, Timer 3, and Timer 4 ..... 297
23.2.1.Configuring Timer 2, 3, and 4 to Count Down..... 297
23.2.2.Capture Mode ..... 298
23.2.3.Auto-Reload Mode ..... 299
23.2.4.Toggle Output Mode ..... 300
**24. Programmable Counter Array ..... 305**
24.1.PCA Counter/Timer ..... 306
24.2.Capture/Compare Modules ..... 307
24.2.1.Edge-triggered Capture Mode..... 308
24.2.2.Software Timer (Compare) Mode..... 309
24.2.3.High-Speed Output Mode ..... 310
24.2.4.Frequency Output Mode ..... 311
24.2.5.8-Bit Pulse Width Modulator Mode..... 312
24.2.6.16-Bit Pulse Width Modulator Mode..... 313
24.3.Register Descriptions for PCA0..... 314
**25. JTAG (IEEE 1149.1) ..... 319**
25.1.Boundary Scan ..... 320
25.1.1.EXTEST Instruction..... 321
25.1.2.SAMPLE Instruction ..... 321
25.1.3.BYPASS Instruction ..... 321
25.1.4.IDCODE Instruction..... 321
25.2.Flash Programming Commands..... 323
25.3.Debug Support ..... 326
**Document Change List..... 327**
**Contact Information..... 328**

## NOTES:

## List of Figures

**1. System Overview**
Figure 1.1. C8051F040/2 Block Diagram ..... 21
Figure 1.2. C8051F041/3 Block Diagram ..... 22
Figure 1.3. C8051F044/6 Block Diagram ..... 23
Figure 1.4. C8051F045/7 Block Diagram ..... 24
Figure 1.5. Comparison of Peak MCU Execution Speeds ..... 25
Figure 1.6. On-Board Clock and Reset ..... 26
Figure 1.7. On-Chip Memory Map ..... 27
Figure 1.8. Development/In-System Debug Diagram ..... 28
Figure 1.9. Digital Crossbar Diagram ..... 29
Figure 1.10. PCA Block Diagram ..... 30
Figure 1.11. CAN Controller Diagram ..... 31
Figure 1.12. 10/12-Bit ADC Block Diagram ..... 32
Figure 1.13. 8-Bit ADC Diagram ..... 33
Figure 1.14. Comparator and DAC Diagram ..... 34
**2. Absolute Maximum Ratings**
**3. Global DC Electrical Characteristic**
**4. Pinout and Package Definitions**
Figure 4.1. TQFP-100 Pinout Diagram ..... 43
Figure 4.2. TQFP-100 Package Drawing ..... 44
Figure 4.3. TQFP-64 Pinout Diagram ..... 45
Figure 4.4. TQFP-64 Package Drawing ..... 46
**5. 12-Bit ADC (ADC0, C8051F040/1 Only)**
Figure 5.1. 12-Bit ADC0 Functional Block Diagram ..... 47
Figure 5.2. Analog Input Diagram ..... 48
Figure 5.3. High Voltage Difference Amplifier Functional Diagram ..... 52
Figure 5.4. 12-Bit ADC Track and Conversion Example Timing ..... 55
Figure 5.5. ADC0 Equivalent Input Circuits ..... 56
Figure 5.6. Temperature Sensor Transfer Function ..... 57
Figure 5.7. ADC0 Data Word Example ..... 61
Figure 5.8. 12-Bit ADC0 Window Interrupt Example: Right Justified Single-Ended Data ..... 63
Figure 5.9. 12-Bit ADC0 Window Interrupt Example: Right Justified Differential Data ..... 64
Figure 5.10. 12-Bit ADC0 Window Interrupt Example: Left Justified Single-Ended Data ..... 65
Figure 5.11. 12-Bit ADC0 Window Interrupt Example: Left Justified Differential Data . 66
**6. 10-Bit ADC (ADC0, C8051F042/3/4/5/6/7 Only)**
Figure 6.1. 10-Bit ADC0 Functional Block Diagram ..... 69
Figure 6.2. Analog Input Diagram ..... 70
Figure 6.3. High Voltage Difference Amplifier Functional Diagram ..... 74
Figure 6.4. 10-Bit ADC Track and Conversion Example Timing ..... 77

Figure 6.5. ADC0 Equivalent Input Circuits ..... 78
Figure 6.6. Temperature Sensor Transfer Function ..... 79
Figure 6.7. ADC0 Data Word Example ..... 83
Figure 6.8. 10-Bit ADC0 Window Interrupt Example: Right Justified Single-Ended Data ..... 85
Figure 6.9. 10-Bit ADC0 Window Interrupt Example: Right Justified Differential Data ..... 86
Figure 6.10. 10-Bit ADC0 Window Interrupt Example: Left Justified Single-Ended Data ..... 87
Figure 6.11. 10-Bit ADC0 Window Interrupt Example: Left Justified Differential Data . 88
**7. 8-Bit ADC (ADC2, C8051F040/1/2/3 Only)**
Figure 7.1. ADC2 Functional Block Diagram ..... 91
Figure 7.2. ADC2 Track and Conversion Example Timing ..... 93
Figure 7.3. ADC2 Equivalent Input Circuit ..... 94
Figure 7.4. ADC2 Data Word Example ..... 99
Figure 7.5. ADC Window Compare Examples, Single-Ended Mode ..... 101
Figure 7.6. ADC Window Compare Examples, Differential Mode ..... 102
**8. DACs, 12-Bit Voltage Mode (C8051F040/1/2/3 Only)**
Figure 8.1. DAC Functional Block Diagram ..... 105
**9. Voltage Reference (C8051F040/2/4/6)**
Figure 9.1. Voltage Reference Functional Block Diagram ..... 113
**10. Voltage Reference (C8051F041/3/5/7)**
Figure 10.1. Voltage Reference Functional Block Diagram ..... 117
**11. Comparators**
Figure 11.1. Comparator Functional Block Diagram ..... 121
Figure 11.2. Comparator Hysteresis Plot ..... 122
**12. CIP-51 Microcontroller**
Figure 12.1. CIP-51 Block Diagram ..... 127
Figure 12.2. Memory Map ..... 133
Figure 12.3. SFR Page Stack ..... 136
Figure 12.4. SFR Page Stack While Using SFR Page 0x0F To Access Port 5 ..... 137
Figure 12.5. SFR Page Stack After ADC2 Window Comparator Interrupt Occurs . 138
Figure 12.6. SFR Page Stack Upon PCA Interrupt Occurring During an ADC2 ISR .... 139
Figure 12.7. SFR Page Stack Upon Return From PCA Interrupt ..... 140
Figure 12.8. SFR Page Stack Upon Return From ADC2 Window Interrupt ..... 141
**13. Reset Sources**
Figure 13.1. Reset Sources ..... 165
Figure 13.2. Reset Timing ..... 166
**14. Oscillators**
Figure 14.1. Oscillator Diagram ..... 173
Figure 14.2. 32.768 kHz External Crystal Example ..... 177
**15. Flash Memory**
Figure 15.1. Flash Program Memory Map and Security Bytes ..... 181

**16. External Data Memory Interface and On-Chip XRAM**
Figure 16.1. Multiplexed Configuration Example ... 191
Figure 16.2. Non-multiplexed Configuration Example ... 192
Figure 16.3. EMIF Operating Modes ... 193
Figure 16.4. Non-multiplexed 16-bit MOVX Timing ... 196
Figure 16.5. Non-multiplexed 8-bit MOVX without Bank Select Timing ... 197
Figure 16.6. Non-multiplexed 8-bit MOVX with Bank Select Timing ... 198
Figure 16.7. Multiplexed 16-bit MOVX Timing ... 199
Figure 16.8. Multiplexed 8-bit MOVX without Bank Select Timing ... 200
Figure 16.9. Multiplexed 8-bit MOVX with Bank Select Timing ... 201
**17. Port Input/Output**
Figure 17.1. Port I/O Cell Block Diagram ... 203
Figure 17.2. Port I/O Functional Block Diagram ... 204
Figure 17.3. Priority Crossbar Decode Table ... 205
Figure 17.4. Priority Crossbar Decode Table ... 208
Figure 17.5. Priority Crossbar Decode Table ... 209
Figure 17.6. Crossbar Example: ... 211
**18. Controller Area Network (CAN0)**
Figure 18.1. Typical CAN Bus Configuration ... 227
Figure 18.2. CAN Controller Diagram ... 228
Figure 18.3. Four Segments of a CAN Bit Time ... 229
Figure 18.4. CAN0DATH: CAN Data Access Register High Byte ... 234
**19. System Management BUS/I$^2$C BUS (SMBUS0)**
Figure 19.1. SMBus0 Block Diagram ... 239
Figure 19.2. Typical SMBus Configuration ... 240
Figure 19.3. SMBus Transaction ... 241
Figure 19.4. Typical Master Transmitter Sequence ... 242
Figure 19.5. Typical Master Receiver Sequence ... 243
Figure 19.6. Typical Slave Transmitter Sequence ... 243
Figure 19.7. Typical Slave Receiver Sequence ... 244
**20. Enhanced Serial Peripheral Interface (SPI0)**
Figure 20.1. SPI Block Diagram ... 255
Figure 20.2. Multiple-Master Mode Connection Diagram ... 258
Figure 20.3. 3-Wire Single Master and Slave Mode Connection Diagram ... 258
Figure 20.4. 4-Wire Single Master and Slave Mode Connection Diagram ... 258
Figure 20.5. Data/Clock Timing Diagram ... 260
**21. UART0**
Figure 21.1. UART0 Block Diagram ... 265
Figure 21.2. UART0 Mode 0 Timing Diagram ... 266
Figure 21.3. UART0 Mode 0 Interconnect ... 267
Figure 21.4. UART0 Mode 1 Timing Diagram ... 267
Figure 21.5. UART0 Modes 2 and 3 Timing Diagram ... 269
Figure 21.6. UART0 Modes 1, 2, and 3 Interconnect Diagram ... 269
Figure 21.7. UART Multi-Processor Mode Interconnect Diagram ... 272

**22. UART1**
Figure 22.1. UART1 Block Diagram ..... 277
Figure 22.2. UART1 Baud Rate Logic ..... 278
Figure 22.3. UART Interconnect Diagram ..... 279
Figure 22.4. 8-Bit UART Timing Diagram ..... 279
Figure 22.5. 9-Bit UART Timing Diagram ..... 280
Figure 22.6. UART Multi-Processor Mode Interconnect Diagram ..... 281
**23. Timers**
Figure 23.1. T0 Mode 0 Block Diagram ..... 290
Figure 23.2. T0 Mode 2 Block Diagram ..... 291
Figure 23.3. T0 Mode 3 Block Diagram ..... 292
Figure 23.4. Tn Capture Mode Block Diagram ..... 298
Figure 23.5. Tn Auto-reload Mode and Toggle Mode Block Diagram ..... 299
**24. Programmable Counter Array**
Figure 24.1. PCA Block Diagram ..... 305
Figure 24.2. PCA Counter/Timer Block Diagram ..... 306
Figure 24.3. PCA Interrupt Block Diagram ..... 307
Figure 24.4. PCA Capture Mode Diagram ..... 308
Figure 24.5. PCA Software Timer Mode Diagram ..... 309
Figure 24.6. PCA High-Speed Output Mode Diagram ..... 310
Figure 24.7. PCA Frequency Output Mode ..... 311
Figure 24.8. PCA 8-Bit PWM Mode Diagram ..... 312
Figure 24.9. PCA 16-Bit PWM Mode ..... 313
**25. JTAG (IEEE 1149.1)**

## List of Tables

**1. System Overview**
Table 1.1. Product Selection Guide ..... 20
**2. Absolute Maximum Ratings**
Table 2.1. Absolute Maximum Ratings* ..... 35
**3. Global DC Electrical Characteristic**
Table 3.1. Global DC Electrical Characteristics ..... 36
**4. Pinout and Package Definitions**
Table 4.1. Pin Definitions ..... 37
**5. 12-Bit ADC (ADC0, C8051F040/1 Only)**
Table 5.1. AMUX Selection Chart (AMX0AD3–0 and AMX0CF3–0 bits) ..... 50
Table 5.2. 12-Bit ADC0 Electrical Characteristics ..... 67
Table 5.3. High-Voltage Difference Amplifier Electrical Characteristics ..... 68
**6. 10-Bit ADC (ADC0, C8051F042/3/4/5/6/7 Only)**
Table 6.1. AMUX Selection Chart (AMX0AD3-0 and AMX0CF3-0 bits) ..... 72
Table 6.2. 10-Bit ADC0 Electrical Characteristics ..... 89
Table 6.3. High-Voltage Difference Amplifier Electrical Characteristics ..... 90
**7. 8-Bit ADC (ADC2, C8051F040/1/2/3 Only)**
Table 7.1. AMUX Selection Chart (AMX2AD2-0 and AMX2CF3-0 bits) ..... 96
Table 7.2. ADC2 Electrical Characteristics ..... 103
**8. DACs, 12-Bit Voltage Mode (C8051F040/1/2/3 Only)**
Table 8.1. DAC Electrical Characteristics ..... 111
**9. Voltage Reference (C8051F040/2/4/6)**
Table 9.1. Voltage Reference Electrical Characteristics ..... 115
**10. Voltage Reference (C8051F041/3/5/7)**
Table 10.1. Voltage Reference Electrical Characteristics ..... 119
**11. Comparators**
Table 11.1. Comparator Electrical Characteristics ..... 126
**12. CIP-51 Microcontroller**
Table 12.1. CIP-51 Instruction Set Summary ..... 129
Table 12.2. Special Function Register (SFR) Memory Map ..... 144
Table 12.3. Special Function Registers ..... 146
Table 12.4. Interrupt Summary ..... 154
**13. Reset Sources**
Table 13.1. Reset Electrical Characteristics ..... 171
**14. Oscillators**
Table 14.1. Internal Oscillator Electrical Characteristics ..... 175
**15. Flash Memory**
Table 15.1. Flash Electrical Characteristics ..... 180
**16. External Data Memory Interface and On-Chip XRAM**
Table 16.1. AC Parameters for External Memory Interface ..... 202
**17. Port Input/Output**
Table 17.1. Port I/O DC Electrical Characteristics ..... 203

**18. Controller Area Network (CAN0)**
Table 18.1. Background System Information ..... 229
Table 18.2. CAN Register Index and Reset Values ..... 233
**19. System Management BUS/I2C BUS (SMBUS0)**
Table 19.1. SMB0STA Status Codes and States ..... 252
**20. Enhanced Serial Peripheral Interface (SPI0)**
**21. UART0**
Table 21.1. UART0 Modes ..... 266
Table 21.2. Oscillator Frequencies for Standard Baud Rates ..... 273
**22. UART1**
Table 22.1. Timer Settings for Standard Baud Rates Using the Internal 24.5 MHz Oscillator ..... 284
Table 22.2. Timer Settings for Standard Baud Rates Using an External 25.0 MHz Oscillator ..... 284
Table 22.3. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator ..... 285
Table 22.4. Timer Settings for Standard Baud Rates Using an External 18.432 MHz Oscillator ..... 286
Table 22.5. Timer Settings for Standard Baud Rates Using an External 11.0592 MHz Oscillator ..... 287
Table 22.6. Timer Settings for Standard Baud Rates Using an External 3.6864 MHz Oscillator ..... 288
**23. Timers**
**24. Programmable Counter Array**
Table 24.1. PCA Timebase Input Options ..... 306
Table 24.2. PCA0CPM Register Settings for PCA Capture/Compare Modules .... 307
**25. JTAG (IEEE 1149.1)**
Table 25.1. Boundary Data Register Bit Definitions ..... 320

## List of Registers

SFR Definition 5.1. AMX0CF: AMUX0 Configuration . . . . . 49
SFR Definition 5.2. AMX0SL: AMUX0 Channel Select . . . . . 49
SFR Definition 5.3. AMX0PRT: Port 3 Pin Selection . . . . . 51
SFR Definition 5.4. HVA0CN: High Voltage Difference Amplifier Control . . . . . 53
SFR Definition 5.5. ADC0CF: ADC0 Configuration Register . . . . . 58
SFR Definition 5.6. ADC0CN: ADC0 Control . . . . . 59
SFR Definition 5.7. ADC0H: ADC0 Data Word MSB . . . . . 60
SFR Definition 5.8. ADC0L: ADC0 Data Word LSB . . . . . 60
SFR Definition 5.9. ADC0GTH: ADC0 Greater-Than Data High Byte . . . . . 62
SFR Definition 5.10. ADC0GTL: ADC0 Greater-Than Data Low Byte . . . . . 62
SFR Definition 5.11. ADC0LTH: ADC0 Less-Than Data High Byte . . . . . 62
SFR Definition 5.12. ADC0LTL: ADC0 Less-Than Data Low Byte . . . . . 63
SFR Definition 6.1. AMX0CF: AMUX0 Configuration . . . . . 71
SFR Definition 6.2. AMX0SL: AMUX0 Channel Select . . . . . 71
SFR Definition 6.3. AMX0PRT: Port 3 Pin Selection . . . . . 73
SFR Definition 6.4. HVA0CN: High Voltage Difference Amplifier Control . . . . . 75
SFR Definition 6.5. ADC0CF: ADC0 Configuration . . . . . 80
SFR Definition 6.6. ADC0CN: ADC0 Control . . . . . 81
SFR Definition 6.7. ADC0H: ADC0 Data Word MSB . . . . . 82
SFR Definition 6.8. ADC0L: ADC0 Data Word LSB . . . . . 82
SFR Definition 6.9. ADC0GTH: ADC0 Greater-Than Data High Byte . . . . . 84
SFR Definition 6.10. ADC0GTL: ADC0 Greater-Than Data Low Byte . . . . . 84
SFR Definition 6.11. ADC0LTH: ADC0 Less-Than Data High Byte . . . . . 84
SFR Definition 6.12. ADC0LTL: ADC0 Less-Than Data Low Byte . . . . . 85
SFR Definition 7.1. AMX2CF: AMUX2 Configuration . . . . . 95
SFR Definition 7.2. AMX2SL: AMUX2 Channel Select . . . . . 95
SFR Definition 7.3. ADC2CF: ADC2 Configuration . . . . . 97
SFR Definition 7.4. ADC2CN: ADC2 Control . . . . . 98
SFR Definition 7.5. ADC2: ADC2 Data Word . . . . . 99
SFR Definition 7.6. ADC2GT: ADC2 Greater-Than Data . . . . . 100
SFR Definition 7.7. ADC2LT: ADC2 Less-Than Data . . . . . 100
SFR Definition 8.1. DAC0H: DAC0 High Byte . . . . . 107
SFR Definition 8.2. DAC0L: DAC0 Low Byte . . . . . 107
SFR Definition 8.3. DAC0CN: DAC0 Control . . . . . 108
SFR Definition 8.4. DAC1H: DAC1 High Byte . . . . . 109
SFR Definition 8.5. DAC1L: DAC1 Low Byte . . . . . 109
SFR Definition 8.6. DAC1CN: DAC1 Control . . . . . 110
SFR Definition 9.1. REF0CN: Reference Control . . . . . 114
SFR Definition 10.1. REF0CN: Reference Control . . . . . 118
SFR Definition 11.1. CPTnCN: Comparator 0, 1, and 2 Control . . . . . 124
SFR Definition 11.2. CPTnMD: Comparator Mode Selection . . . . . 125
SFR Definition 12.1. SFR Page Control Register: SFRPGCN . . . . . 142
SFR Definition 12.2. SFR Page Register: SFRPAGE . . . . . 142

SFR Definition 12.3. SFR Next Register: SFRNEXT . . . . . 143
SFR Definition 12.4. SFR Last Register: SFRLAST . . . . . 143
SFR Definition 12.5. SP: Stack Pointer . . . . . 150
SFR Definition 12.6. DPL: Data Pointer Low Byte . . . . . 150
SFR Definition 12.7. DPH: Data Pointer High Byte . . . . . 150
SFR Definition 12.8. PSW: Program Status Word . . . . . 151
SFR Definition 12.9. ACC: Accumulator . . . . . 152
SFR Definition 12.10. B: B Register . . . . . 152
SFR Definition 12.11. IE: Interrupt Enable . . . . . 157
SFR Definition 12.12. IP: Interrupt Priority . . . . . 158
SFR Definition 12.13. EIE1: Extended Interrupt Enable 1 . . . . . 159
SFR Definition 12.14. EIE2: Extended Interrupt Enable 2 . . . . . 160
SFR Definition 12.15. EIP1: Extended Interrupt Priority 1 . . . . . 161
SFR Definition 12.16. EIP2: Extended Interrupt Priority 2 . . . . . 162
SFR Definition 12.18. PCON: Power Control . . . . . 164
SFR Definition 13.1. WDTCN: Watchdog Timer Control . . . . . 169
SFR Definition 13.2. RSTSRC: Reset Source . . . . . 170
SFR Definition 14.1. OSCICL: Internal Oscillator Calibration . . . . . 174
SFR Definition 14.2. OSCICN: Internal Oscillator Control . . . . . 174
SFR Definition 14.3. CLKSEL: Oscillator Clock Selection . . . . . 175
SFR Definition 14.4. OSCXCN: External Oscillator Control . . . . . 176
SFR Definition 15.1. FLACL: Flash Access Limit . . . . . 184
SFR Definition 15.2. FLSCL: Flash Memory Control . . . . . 184
SFR Definition 15.3. PSCTL: Program Store Read/Write Control . . . . . 185
SFR Definition 16.1. EMI0CN: External Memory Interface Control . . . . . 189
SFR Definition 16.2. EMI0CF: External Memory Configuration . . . . . 190
SFR Definition 16.3. EMI0TC: External Memory Timing Control . . . . . 195
SFR Definition 17.1. XBR0: Port I/O Crossbar Register 0 . . . . . 212
SFR Definition 17.2. XBR1: Port I/O Crossbar Register 1 . . . . . 213
SFR Definition 17.3. XBR2: Port I/O Crossbar Register 2 . . . . . 214
SFR Definition 17.4. XBR3: Port I/O Crossbar Register 3 . . . . . 215
SFR Definition 17.5. P0: Port0 Data . . . . . 215
SFR Definition 17.6. P0MDOUT: Port0 Output Mode . . . . . 216
SFR Definition 17.7. P1: Port1 Data . . . . . 216
SFR Definition 17.8. P1MDIN: Port1 Input Mode . . . . . 217
SFR Definition 17.9. P1MDOUT: Port1 Output Mode . . . . . 217
SFR Definition 17.10. P2: Port2 Data . . . . . 218
SFR Definition 17.11. P2MDIN: Port2 Input Mode . . . . . 218
SFR Definition 17.12. P2MDOUT: Port2 Output Mode . . . . . 219
SFR Definition 17.13. P3: Port3 Data . . . . . 219
SFR Definition 17.14. P3MDIN: Port3 Input Mode . . . . . 220
SFR Definition 17.15. P3MDOUT: Port3 Output Mode . . . . . 220
SFR Definition 17.16. P4: Port4 Data . . . . . 222
SFR Definition 17.17. P4MDOUT: Port4 Output Mode . . . . . 222
SFR Definition 17.18. P5: Port5 Data . . . . . 223

SFR Definition 17.19. P5MDOUT: Port5 Output Mode . . . . . 223
SFR Definition 17.20. P6: Port6 Data . . . . . 224
SFR Definition 17.21. P6MDOUT: Port6 Output Mode . . . . . 224
SFR Definition 17.22. P7: Port7 Data . . . . . 225
SFR Definition 17.23. P7MDOUT: Port7 Output Mode . . . . . 225
SFR Definition 18.1. CAN0DATL: CAN Data Access Register Low Byte . . . . . 235
SFR Definition 18.2. CAN0ADR: CAN Address Index . . . . . 235
SFR Definition 18.3. CAN0CN: CAN Control . . . . . 236
SFR Definition 18.4. CAN0TST: CAN Test . . . . . 236
SFR Definition 18.5. CAN0STA: CAN Status . . . . . 237
SFR Definition 19.1. SMB0CN: SMBus0 Control . . . . . 247
SFR Definition 19.2. SMB0CR: SMBus0 Clock Rate . . . . . 248
SFR Definition 19.3. SMB0DAT: SMBus0 Data . . . . . 249
SFR Definition 19.4. SMB0ADR: SMBus0 Address . . . . . 250
SFR Definition 19.5. SMB0STA: SMBus0 Status . . . . . 251
SFR Definition 20.1. SPI0CFG: SPI0 Configuration . . . . . 261
SFR Definition 20.2. SPI0CN: SPI0 Control . . . . . 262
SFR Definition 20.3. SPI0CKR: SPI0 Clock Rate . . . . . 263
SFR Definition 20.4. SPI0DAT: SPI0 Data . . . . . 264
SFR Definition 21.1. SCON0: UART0 Control . . . . . 274
SFR Definition 21.2. SSTA0: UART0 Status and Clock Selection . . . . . 275
SFR Definition 21.3. SBUF0: UART0 Data Buffer . . . . . 276
SFR Definition 21.4. SADDR0: UART0 Slave Address . . . . . 276
SFR Definition 21.5. SADEN0: UART0 Slave Address Enable . . . . . 276
SFR Definition 22.1. SCON1: Serial Port 1 Control . . . . . 282
SFR Definition 22.2. SBUF1: Serial (UART1) Port Data Buffer . . . . . 283
SFR Definition 23.1. TCON: Timer Control . . . . . 293
SFR Definition 23.2. TMOD: Timer Mode . . . . . 294
SFR Definition 23.3. CKCON: Clock Control . . . . . 295
SFR Definition 23.4. TL0: Timer 0 Low Byte . . . . . 295
SFR Definition 23.5. TL1: Timer 1 Low Byte . . . . . 296
SFR Definition 23.6. TH0: Timer 0 High Byte . . . . . 296
SFR Definition 23.7. TH1: Timer 1 High Byte . . . . . 296
SFR Definition 23.8. TMRnCN: Timer n Control . . . . . 301
SFR Definition 23.9. TMRnCF: Timer n Configuration . . . . . 302
SFR Definition 23.10. RCAPnL: Timer n Capture Register Low Byte . . . . . 303
SFR Definition 23.11. RCAPnH: Timer n Capture Register High Byte . . . . . 303
SFR Definition 23.12. TMRnL: Timer n Low Byte . . . . . 303
SFR Definition 23.13. TMRnH Timer n High Byte . . . . . 304
SFR Definition 24.1. PCA0CN: PCA Control . . . . . 314
SFR Definition 24.2. PCA0MD: PCA0 Mode . . . . . 315
SFR Definition 24.3. PCA0CPMn: PCA0 Capture/Compare Mode . . . . . 316
SFR Definition 24.4. PCA0L: PCA0 Counter/Timer Low Byte . . . . . 317
SFR Definition 24.5. PCA0H: PCA0 Counter/Timer High Byte . . . . . 317
SFR Definition 24.6. PCA0CPLn: PCA0 Capture Module Low Byte . . . . . 318

SFR Definition 24.7. PCA0CPHn: PCA0 Capture Module High Byte . . . . . 318
JTAG Register Definition 25.1. IR: JTAG Instruction Register . . . . . 319
JTAG Register Definition 25.2. DEVICEID: JTAG Device ID Register . . . . . 322
JTAG Register Definition 25.3. FLASHCON: JTAG Flash Control Register . . . . . 324
JTAG Register Definition 25.4. FLASHDAT: JTAG Flash Data . . . . . 325
JTAG Register Definition 25.5. FLASHADR: JTAG Flash Address . . . . . 325

# 1. System Overview

The C8051F04x family of devices are fully integrated mixed-signal System-on-a-Chip MCUs with 64 digital I/O pins (C8051F040/2/4/6) or 32 digital I/O pins (C8051F041/3/5/7), and an integrated CAN 2.0B controller. Highlighted features are listed below; refer to Table 1.1 for specific product feature selection.

- High-Speed pipelined 8051-compatible CIP-51 microcontroller core (up to 25 MIPS)
- Controller Area Network (CAN 2.0B) Controller with 32 message objects, each with its own indentifier mask.
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit (C8051F040/1) or 10-bit (C8051F042/3/4/5/6/7) 100 ksps 8-channel ADC with PGA and analog multiplexer
- High Voltage Difference Amplifier input to the 12/10-bit ADC (60 V Peak-to-Peak) with programmable gain.
- True 8-bit 500 ksps 8-channel ADC with PGA and analog multiplexer (C8051F040/1/2/3)
- Two 12-bit DACs with programmable update scheduling (C8051F040/1/2/3)
- 64 kB (C8051F040/1/2/3/4/5) or 32 kB (C8051F046/7) of in-system programmable Flash memory
- 4352 (4096 + 256) bytes of on-chip RAM
- External Data Memory Interface with 64 kB address space
- SPI, SMBus/$I^2C$, and (2) UART serial interfaces implemented in hardware
- Five general purpose 16-bit Timers
- Programmable Counter/Timer Array with six capture/compare modules
- On-chip Watchdog Timer, $V_{DD}$ Monitor, and Temperature Sensor

With on-chip $V_{DD}$ monitor, Watchdog Timer, and clock oscillator, the C8051F04x family of devices are truly stand-alone System-on-a-Chip solutions. All analog and digital peripherals are enabled/disabled and configured by user firmware. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware.

On-board JTAG debug circuitry allows non-intrusive (uses no on-chip resources), full speed, in-circuit programming and debugging using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, Run, and Halt commands. All analog and digital peripherals are fully functional while debugging using JTAG.

Each MCU is specified for 2.7 V to 3.6 V operation over the industrial temperature range (–45 to +85 °C). The Port I/Os, /RST, and JTAG pins are tolerant for input signals up to 5 V. The C8051F040/2/4/6 are available in a 100-pin TQFP and the C8051F041/3/5/7 are available in a 64-pin TQFP.

**Table 1.1. Product Selection Guide**

| Ordering Part Number | MIPS (Peak) | Flash Memory | RAM | External Memory Interface | SMBus/$I^2C$ and SPI | CAN | UARTS | Timers (16-bit) | Programmable Counter Array | Digital Port I/O's | 12-bit 100ksps ADC | 10-bit 100ksps ADC | 8-bit 500 ksps ADC Inputs | High Voltage Diff Amp | Voltage Reference | Temperature Sensor | DAC Resolution (bits) | DAC Outputs | Analog Comparators | Lead-free (RoHS Compliant) | Package |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C8051F040 | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | ✓ | - | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | - | 100TQFP |
| C8051F040-GQ | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | ✓ | - | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | ✓ | 100TQFP |
| C8051F041 | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | ✓ | - | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | - | 64TQFP |
| C8051F041-GQ | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | ✓ | - | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | ✓ | 64TQFP |
| C8051F042 | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | - | ✓ | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | - | 100TQFP |
| C8051F042-GQ | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | - | ✓ | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | ✓ | 100TQFP |
| C8051F043 | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | - | ✓ | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | - | 64TQFP |
| C8051F043-GQ | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | - | ✓ | 8 | ✓ | ✓ | ✓ | 12 | 2 | 3 | ✓ | 64TQFP |
| C8051F044 | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | - | 100TQFP |
| C8051F044-GQ | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | ✓ | 100TQFP |
| C8051F045 | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | - | 64TQFP |
| C8051F045-GQ | 25 | 64 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | ✓ | 64TQFP |
| C8051F046 | 25 | 32 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | - | 100TQFP |
| C8051F046-GQ | 25 | 32 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 64 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | ✓ | 100TQFP |
| C8051F047 | 25 | 32 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | - | 64TQFP |
| C8051F047-GQ | 25 | 32 kB | 4352 | ✓ | ✓ | ✓ | 2 | 5 | ✓ | 32 | - | ✓ | | ✓ | ✓ | ✓ | | | 3 | ✓ | 64TQFP |

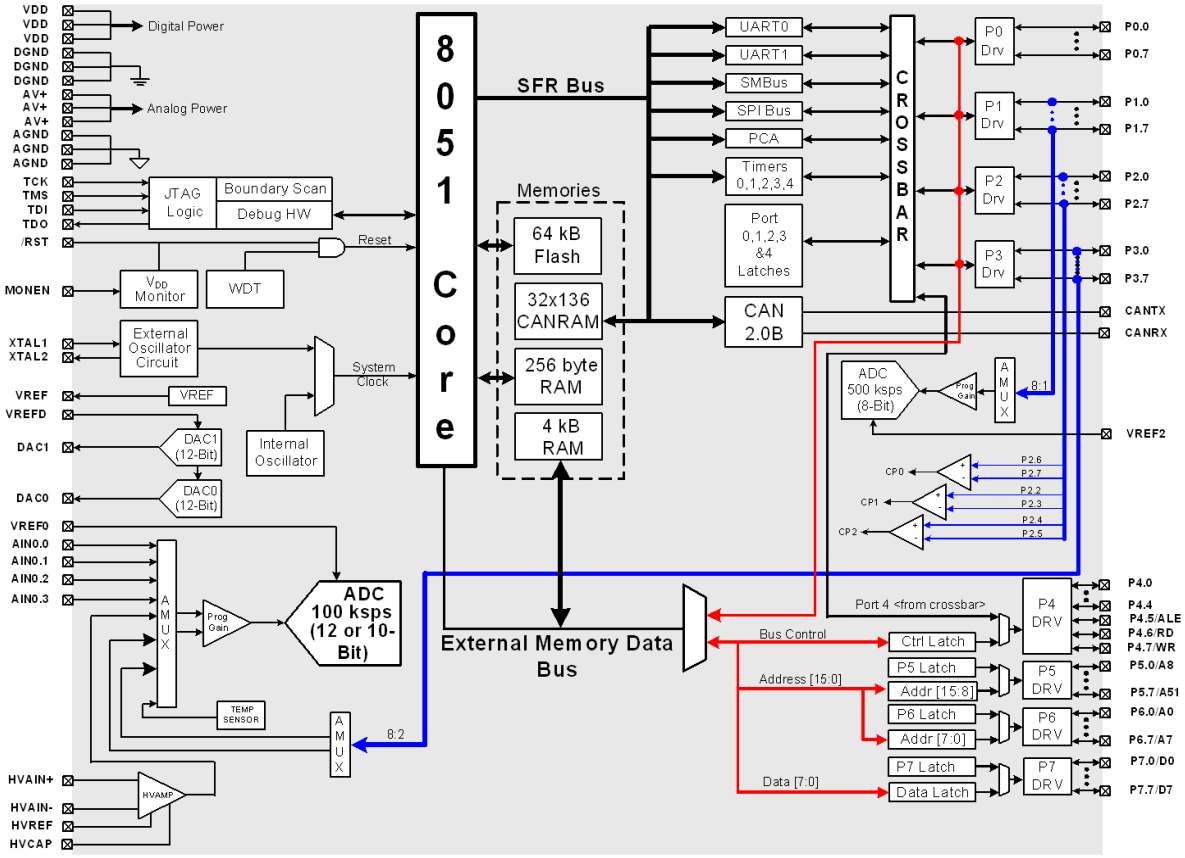



**Figure 1.1. C8051F040/2 Block Diagram**

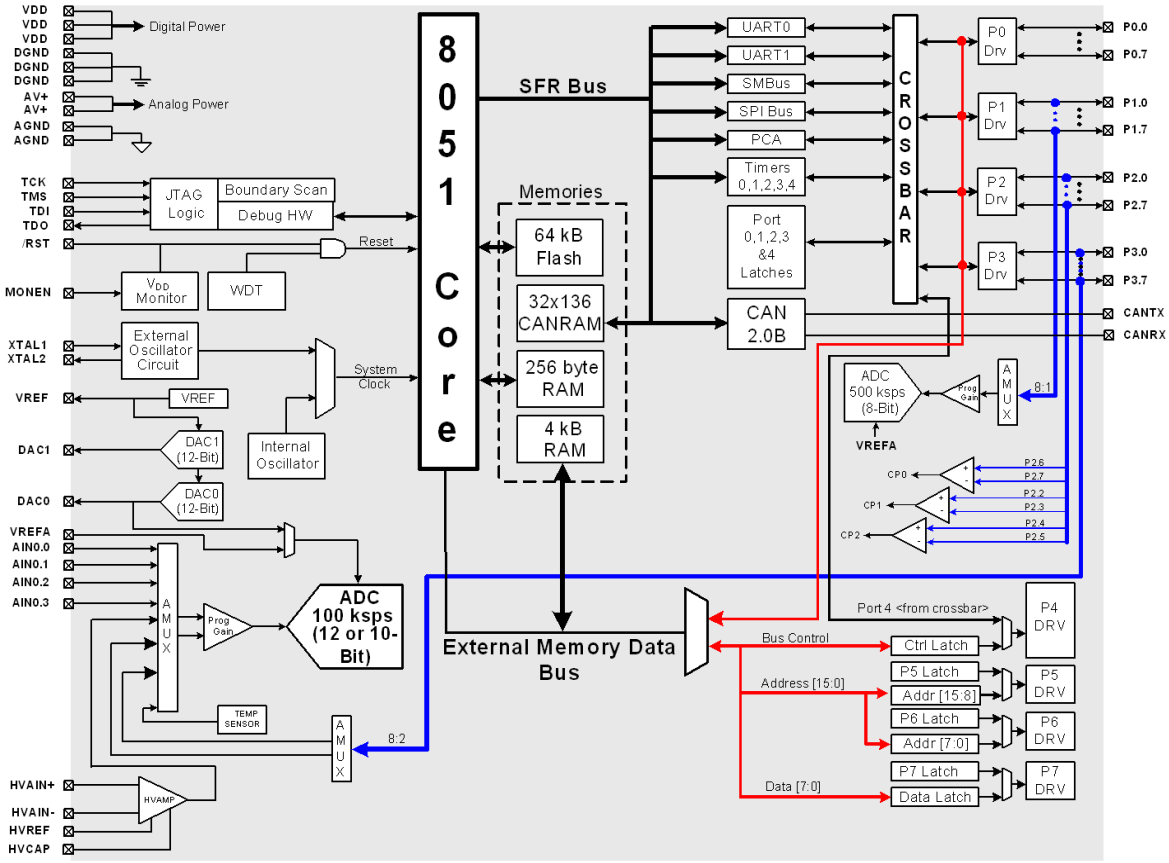



**Figure 1.2. C8051F041/3 Block Diagram**

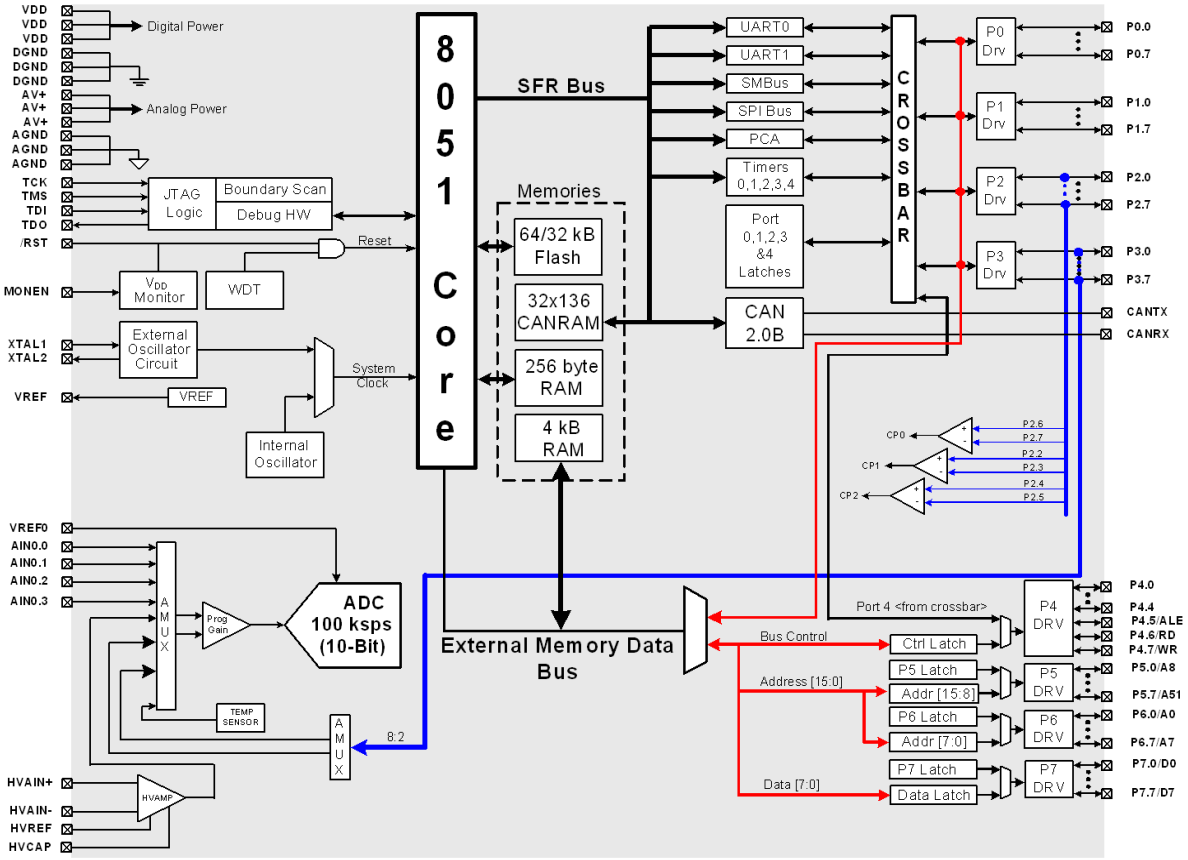



**Figure 1.3. C8051F044/6 Block Diagram**

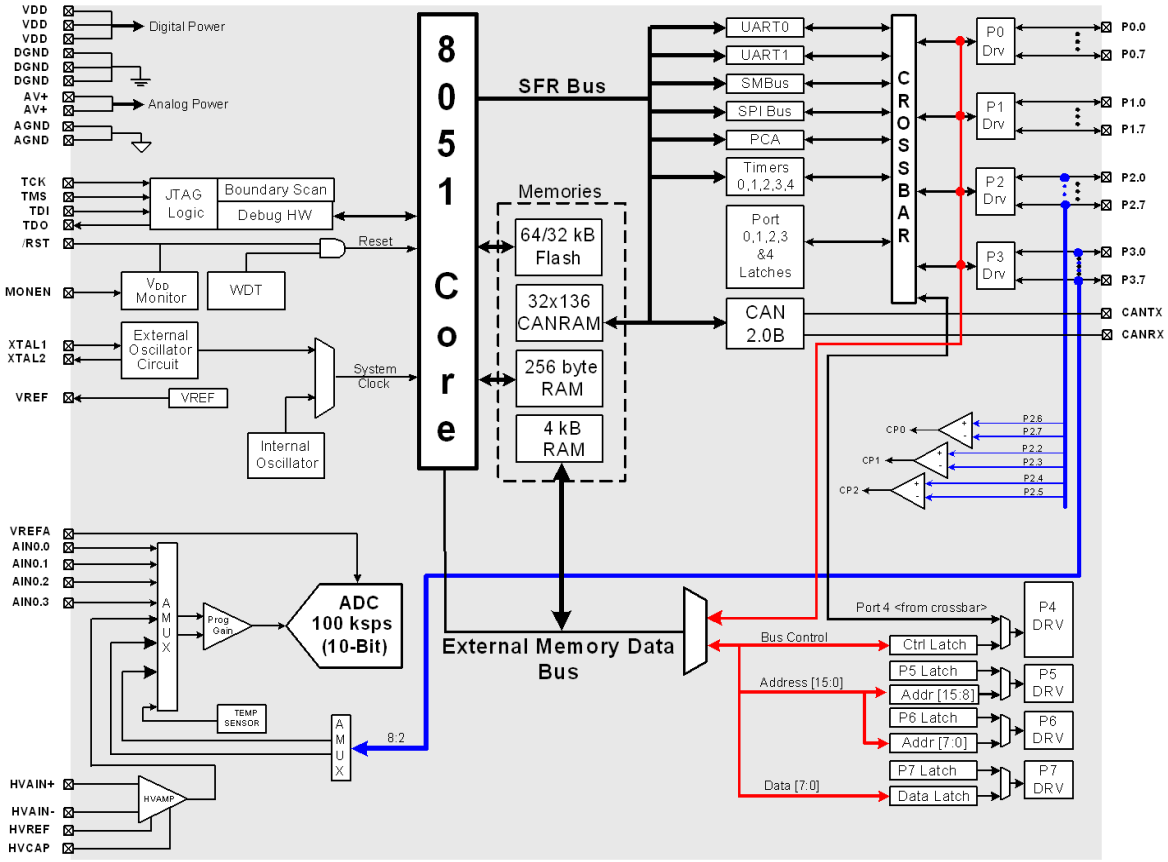



**Figure 1.4. C8051F045/7 Block Diagram**

## 1.1. CIP-51™ Microcontroller Core

### 1.1.1. Fully 8051 Compatible

The C8051F04x family of devices utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The core has all the peripherals included with a standard 8052, including five 16-bit counter/timers, two full-duplex UARTs, 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and up to 8 byte-wide I/O Ports.

### 1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

| Clocks to Execute | 1 | 2 | 2/3 | 3 | 3/4 | 4 | 4/5 | 5 | 8 |
|---|---|---|---|---|---|---|---|---|---|
| Number of Instructions | 26 | 50 | 5 | 14 | 7 | 3 | 1 | 2 | 1 |

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

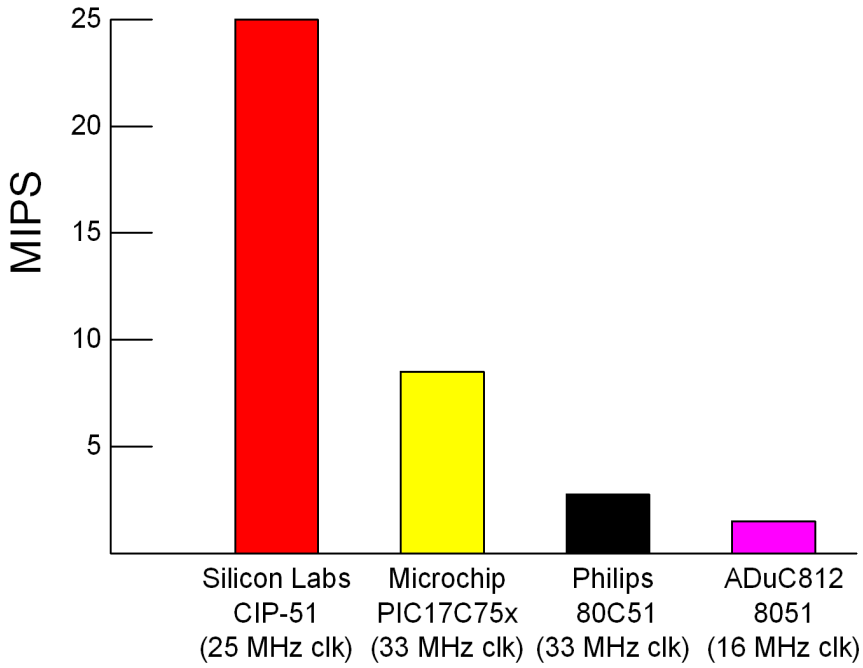



**Figure 1.5. Comparison of Peak MCU Execution Speeds**