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C8051F060/1/2/3/4/5/6/7

8K ISP FLASH MCU Family

Analog Peripherals

- **Two 16-Bit SAR ADCs**
  - 16-bit resolution
  - ±0.75 LSB INL, guaranteed no missing codes
  - Programmable throughput up to 1 Msps
  - Operate as two single-ended or one differential converter
  - Direct memory access; data stored in RAM without software overhead
  - Data-dependent windowed interrupt generator
- **10-bit SAR ADC (C8051F060/1/2/3)**
  - Programmable throughput up to 200 ksps
  - 8 external inputs, single-ended or differential
  - Built-in temperature sensor
- **Two 12-bit DACs (C8051F060/1/2/3)**
  - Can synchronize outputs to timers for jitter-free waveform generation
- **Three Analog Comparators**
  - Programmable hysteresis/response time
- **Voltage Reference**
- **Precision VDD Monitor/Brown-Out Detector**

On-Chip JTAG Debug & Boundary Scan

- On-chip debug circuitry facilitates full-speed, non-intrusive in-circuit/in-system debugging
- Provides breakpoints, single-stepping, watchpoints, stack monitor; inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- IEEE1149.1 compliant boundary scan
- Complete development kit

High Speed 8051 µC Core

- Pipelined instruction architecture; executes 70% of instruction set in 1 or 2 system clocks
- Up to 25 MIPS throughput with 25 MHz clock
- Flexible Interrupt sources

Memory

- 4352 Bytes internal data RAM (4 k + 256)
- 64 kB (C8051F060/1/2/3/4/5), 32 kB (C8051F066/7) Flash; In-system programmable in 512-byte sectors
- External 64 kB data memory interface with multiplexed and non-multiplexed modes (C8051F060/2/4/6)

Digital Peripherals

- 59 general purpose I/O pins (C8051F060/2/4/6)
- 24 general purpose I/O pins (C8051F061/3/5/7)
- Bosch Controller Area Network (CAN 2.0B - C8051F060/1/2/3)
- Hardware SMBus™ (I2C™ Compatible), SPI™, and two UART serial ports available concurrently
- Programmable 16-bit counter/timer array with 6 capture/compare modules
- 5 general purpose 16-bit counter/timers
- Dedicated watchdog timer; bi-directional reset pin

Clock Sources

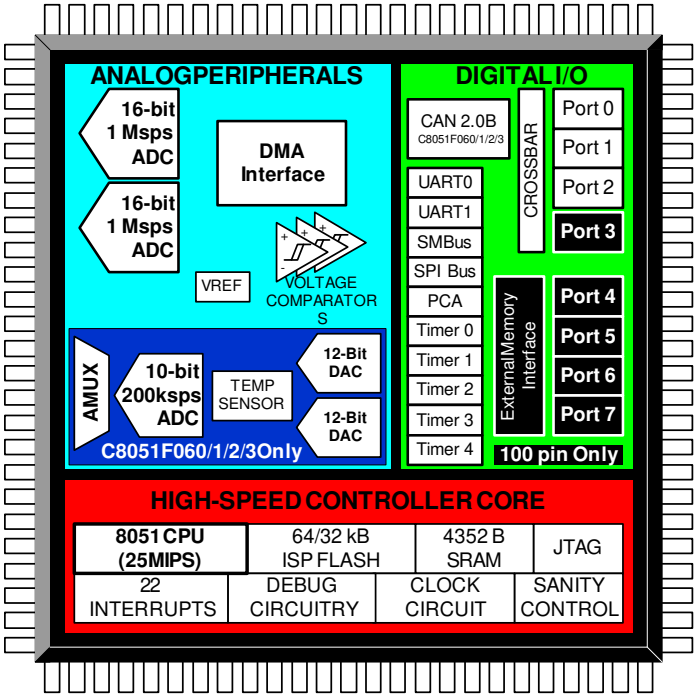
- Internal calibrated precision oscillator: 24.5 MHz
- External oscillator: Crystal, RC, C, or clock

Supply Voltage ..... 2.7 to 3.6 V

- Multiple power saving sleep and shutdown modes

100-Pin and 64-Pin TQFP Packages Available

Temperature Range: -40 to +85 °C



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1. System Overview

The C8051F06x family of devices are fully integrated mixed-signal System-on-a-Chip MCUs with 59 digital I/O pins (C8051F060/2/4/6) or 24 digital I/O pins (C8051F061/3/5/7), and two integrated 16-bit 1 Msps ADCs. Highlighted features are listed below; refer to Table 1.1 for specific product feature selection.

- High-Speed pipelined 8051-compatible CIP-51 microcontroller core (up to 25 MIPS)
- Two 16-bit 1 Msps ADCs with a Direct Memory Access controller
- Controller Area Network (CAN 2.0B) Controller with 32 message objects, each with its own indentifier mask (C8051F060/1/2/3)
- In-system, full-speed, non-intrusive debug interface on-chip
- 10-bit 200 ksps ADC with PGA and 8-channel analog multiplexer (C8051F060/1/2/3)
- Two 12-bit DACs with programmable update scheduling (C8051F060/1/2/3)
- 64 kB (C8051F060/1/2/3/4/5) or 32 kB (C8051F066/7) of in-system programmable Flash memory
- 4352 (4096 + 256) bytes of on-chip RAM
- External Data Memory Interface with 64 kB direct address space (C8051F060/2/4/6)
- SPI, SMBus/I2C, and (2) UART serial interfaces implemented in hardware
- Five general purpose 16-bit Timers
- Programmable Counter/Timer Array with six capture/compare modules
- On-chip Watchdog Timer, VDD Monitor, and Temperature Sensor

With on-chip VDD monitor, Watchdog Timer, and clock oscillator, the C8051F06x family of devices are truly stand-alone System-on-a-Chip solutions. All analog and digital peripherals are enabled/disabled and configured by user firmware. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware.

On-board JTAG debug circuitry allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, Run and Halt commands. All analog and digital peripherals are fully functional while debugging using JTAG.

Each MCU is specified for 2.7 to 3.6 V operation over the industrial temperature range (-45 to +85 °C). The C8051F060/2/4/6 are available in a 100-pin TQFP package and the C8051F061/3/5/7 are available in a 64-pin TQFP package (see block diagrams in Figure 1.1, Figure 1.2, Figure 1.3 and Figure 1.4).

Table 1.1. Product Selection Guide

	MIPS (Peak)	Flash Memory	RAM	External Memory Interface	SMBus/I2C and SPI	CAN	UARTS	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	16-bit 1 Msps ADC Typical INL (LSBs)	10-bit 200 ksps ADC Inputs	Voltage Reference	Temperature Sensor	DAC Resolution (bits)	DAC Outputs	Analog Comparators	Package
C8051F060	25	64 k	4352	✓	✓	✓	2	5	✓	59	±0.75	8	✓	✓	12	2	3	100 TQFP
C8051F061	25	64 k	4352	-	✓	✓	2	5	✓	24	±0.75	8	✓	✓	12	2	3	64 TQFP
C8051F062	25	64 k	4352	✓	✓	✓	2	5	✓	59	±1.5	8	✓	✓	12	2	3	100 TQFP
C8051F063	25	64 k	4352	-	✓	✓	2	5	✓	24	±1.5	8	✓	✓	12	2	3	64 TQFP
C8051F064	25	64 k	4352	✓	✓	-	2	5	✓	59	±0.75	-	✓	-	-	-	3	100 TQFP
C8051F065	25	64 k	4352	-	✓	-	2	5	✓	24	±0.75	-	✓	-	-	-	3	64 TQFP
C8051F066	25	32 k	4352	✓	✓	-	2	5	✓	59	±0.75	-	✓	-	-	-	3	100 TQFP
C8051F067	25	32 k	4352	-	✓	-	2	5	✓	24	±0.75	-	✓	-	-	-	3	64 TQFP

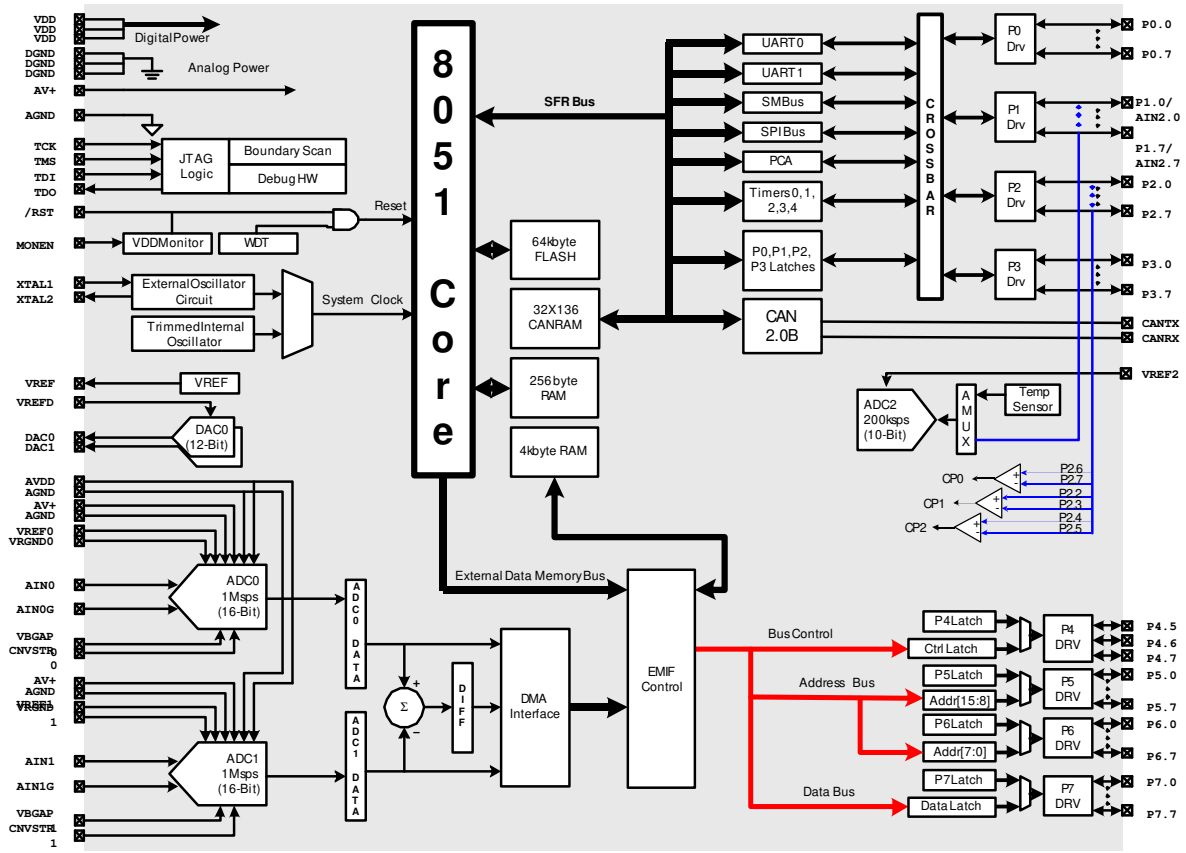

Figure 1.1. C8051F060 / C8051F062 Block Diagram

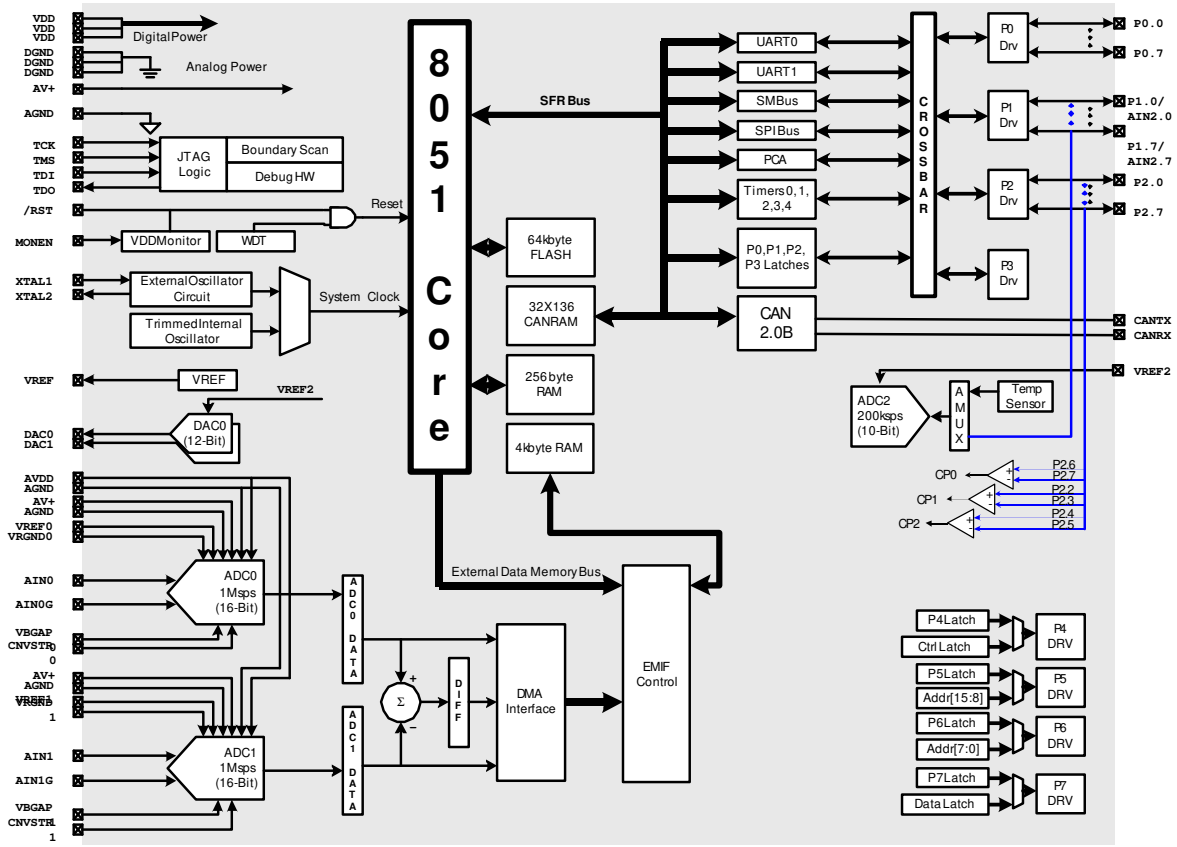

Figure 1.2. C8051F061 / C8051F063 Block Diagram

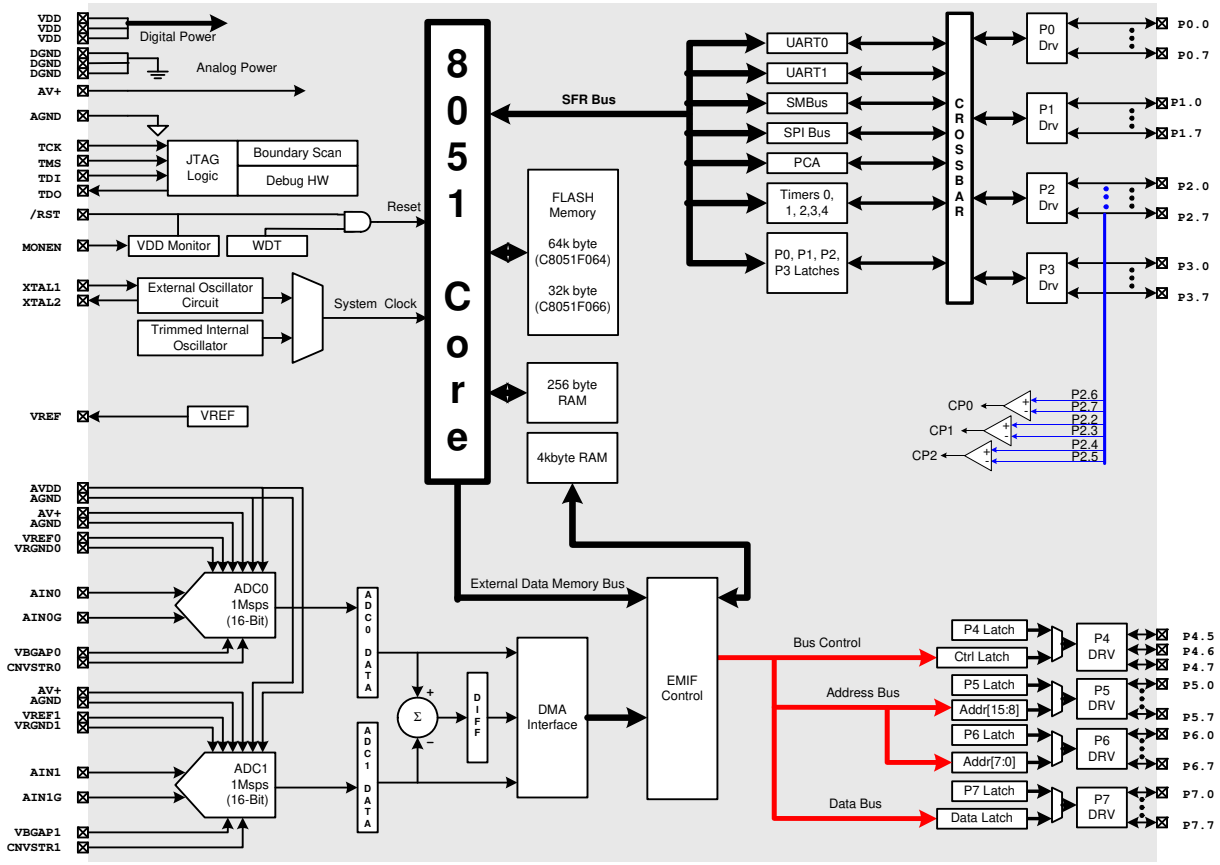

Figure 1.3. C8051F064 / C8051F066 Block Diagram

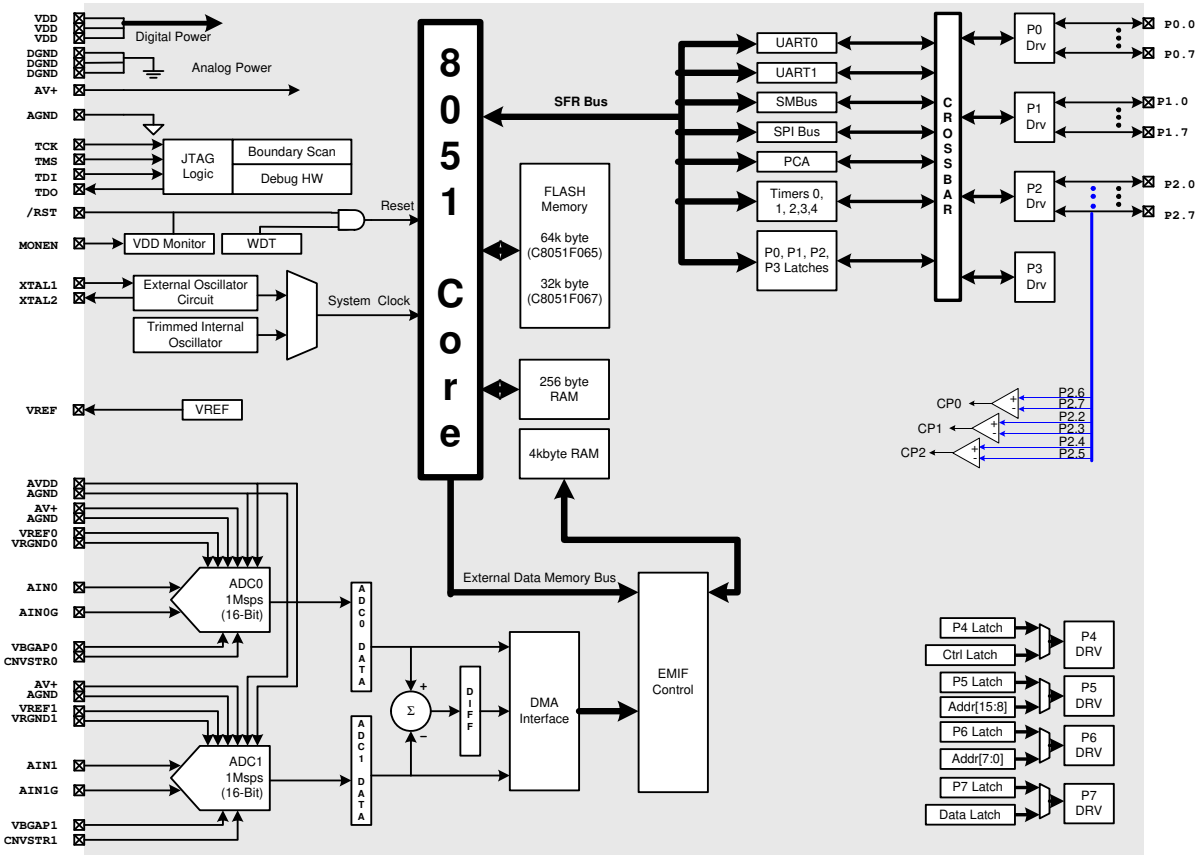

Figure 1.4. C8051F065 / C8051F067 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F06x family of devices utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The core has all the peripherals included with a standard 8052, including five 16-bit counter/timers, two full-duplex UARTs, 256 bytes of internal RAM, 128 byte Special Function Register (SFR) address space, and bit-addressable I/O Ports.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12-to-24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

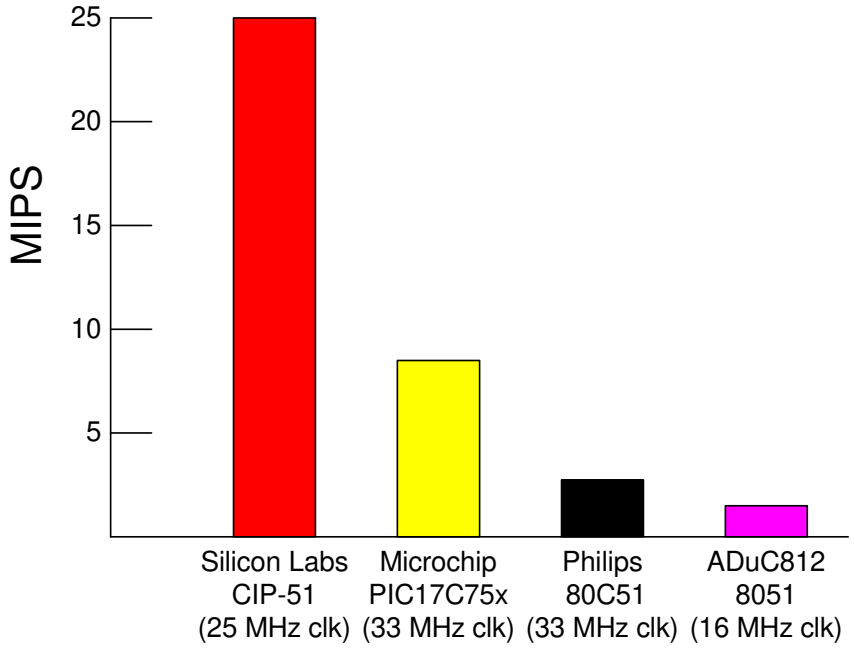

Figure 1.5. Comparison of Peak MCU Execution Speeds