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C8051F2xx

8K ISP FLASH MCU Family

Analog Peripherals
- SAR ADC
  - 12-bit resolution ('F206)
  - 8-bit resolution ('F220/1/6)
  - ±1/4 LSB INL (8-bit) and ±2 LSB INL (12-bit)
  - Up to 100 ksps
  - Up to 32 channel input multiplexer; each port I/O pin can be an ADC input
- Two Comparators
  - 16 programmable hysteresis states
  - Configurable to generate interrupts or reset
- V_{DD} monitor and brown-out detector

On-Chip JTAG Debug
- On-chip debug circuitry facilitates full speed, non-intrusive in-system debug (No emulator required)
- Provides breakpoints, single-stepping, watchpoints, stack monitor
- Inspect/modify memory and registers
- Superior performance to emulation systems using ICE-chips, target pods, and sockets
- Complete, low cost development kit

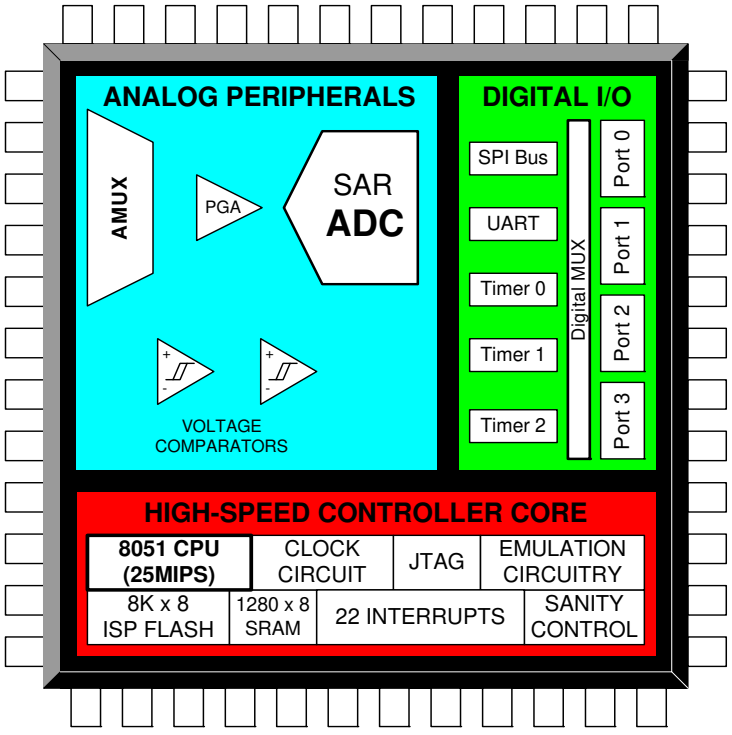
High Speed
- 8051 mC Core
- Pipelined Instruction Architecture; Executes 70% of Instructions in 1 or 2 System Clocks
- Up to 25MIPS Throughput with 25MHz Clock
- Expanded Interrupt Handler

Memory
- 256 bytes internal data RAM
- 1024 bytes XRAM (available on 'F206/226/236)
- 8 kB Flash; In-system programmable in 512 byte sectors

Digital Peripherals
- Four byte wide Port I/O; All are 5 V tolerant
- Hardware UART and SPI bus
- 3 general purpose 16-bit counter/timers
- Dedicated watch-dog timer
- Bi-directional reset
- System clock: internal programmable oscillator, external crystal, external RC, or external clock

Supply Voltage 2.7 to 3.6 V
- Typical operating current: 10 mA @ 25 MHz
- Multiple power saving sleep and shutdown modes

(48-Pin TQFP and 32-Pin LQFP Version Available)
Temperature Range: –40 to +85 °C



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1. System Overview

The C8051F2xx is a family of fully integrated, mixed-signal System on a Chip MCU's available with a true 12-bit ('F206) multi-channel ADC, 8-bit multi-channel ADC ('F220/1/6 and 'F206), or without an ADC ('F230/1/6). Each model features an 8051-compatible microcontroller core with 8 kB of Flash memory. There are also UART and SPI serial interfaces implemented in hardware (not "bit-banged" in user software). Products in this family feature 22 or 32 general purpose I/O pins, some of which can be used for assigned digital peripheral interface. Any pins may be configured for use as analog input to the analog-to-digital converter ('F220/1/6 and 'F206 only). (See the Product Selection Guide in Table 1.1 for a quick reference of each MCUs' feature set.)

Other features include an on-board V_{DD} monitor, WDT, and clock oscillator. On-board Flash memory can be reprogrammed in-circuit, and may also be used for non-volatile data storage. Integrated peripherals can also individually shut down any or all of the peripherals to conserve power. All parts have 256 bytes of SRAM. Also, an additional 1024 bytes of RAM is available in the 'F206/226/236.

On-board JTAG debug support allows non-intrusive (uses no on-chip resources), full speed, in-circuit debug using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional when emulating using JTAG.

Each MCU is specified for 2.7 to 3.6 V operation over the industrial temperature range (–45 to +85 °C) and is available in the 48-pin TFQP and 32-pin LFQP. The Port I/Os are tolerant for input signals up to 5 V.

Table 1.1. Product Selection Guide

	MIPS (Peak)	Flash Memory	RAM	SPI	UART	Timers (16-bit)	Digital Port I/O's	ADC Resolution (bits)	ADC Max Speed (ksps)	ADC Inputs	Voltage Comparators	Package
C8051F206	25	8 k	1280	✓	✓	3	32	12	100	32	2	48TQFP
C8051F220	25	8 k	256	✓	✓	3	32	8	100	32	2	48TQFP
C8051F221	25	8 k	256	✓	✓	3	22	8	100	22	2	32LQFP
C8051F226	25	8 k	1280	✓	✓	3	32	8	100	32	2	48TQFP
C8051F230	25	8 k	256	✓	✓	3	32	—	—	—	2	48TQFP
C8051F231	25	8 k	256	✓	✓	3	22	—	—	—	2	32LQFP
C8051F236	25	8 k	1280	✓	✓	3	32	—	—	—	2	48TQFP

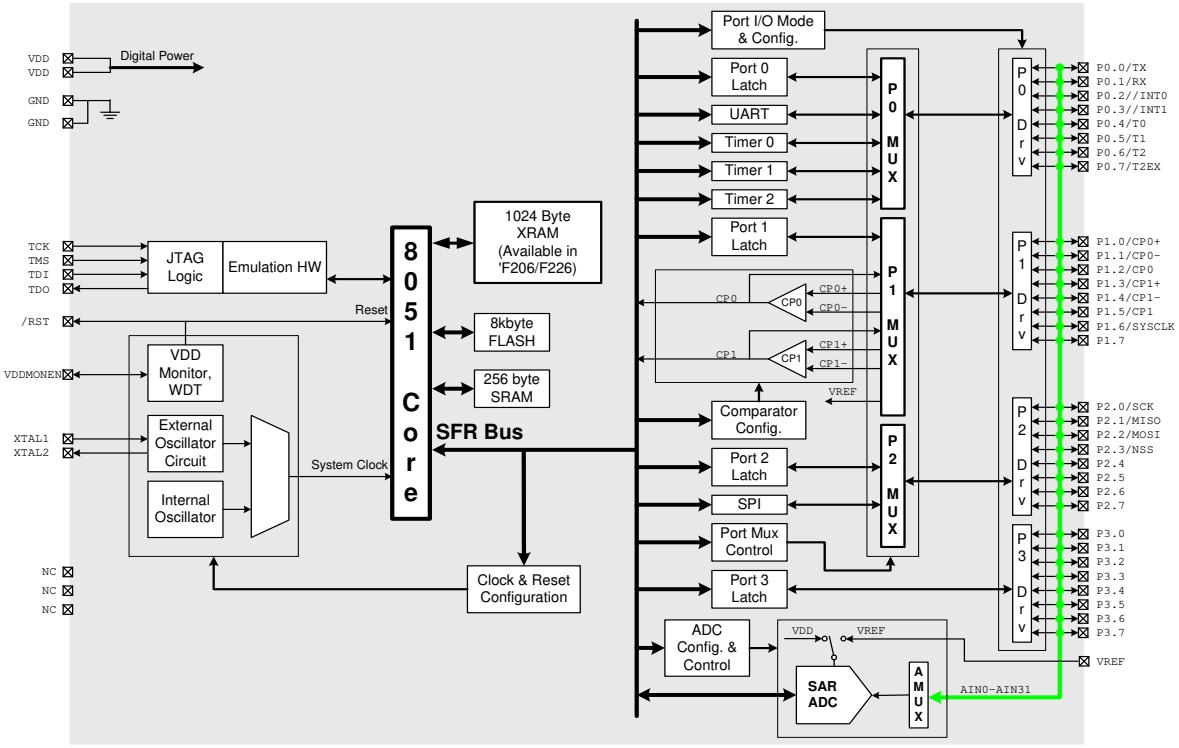

Figure 1.1. C8051F206, C8051F220 and C8051F226 Block Diagram (48 TQFP)

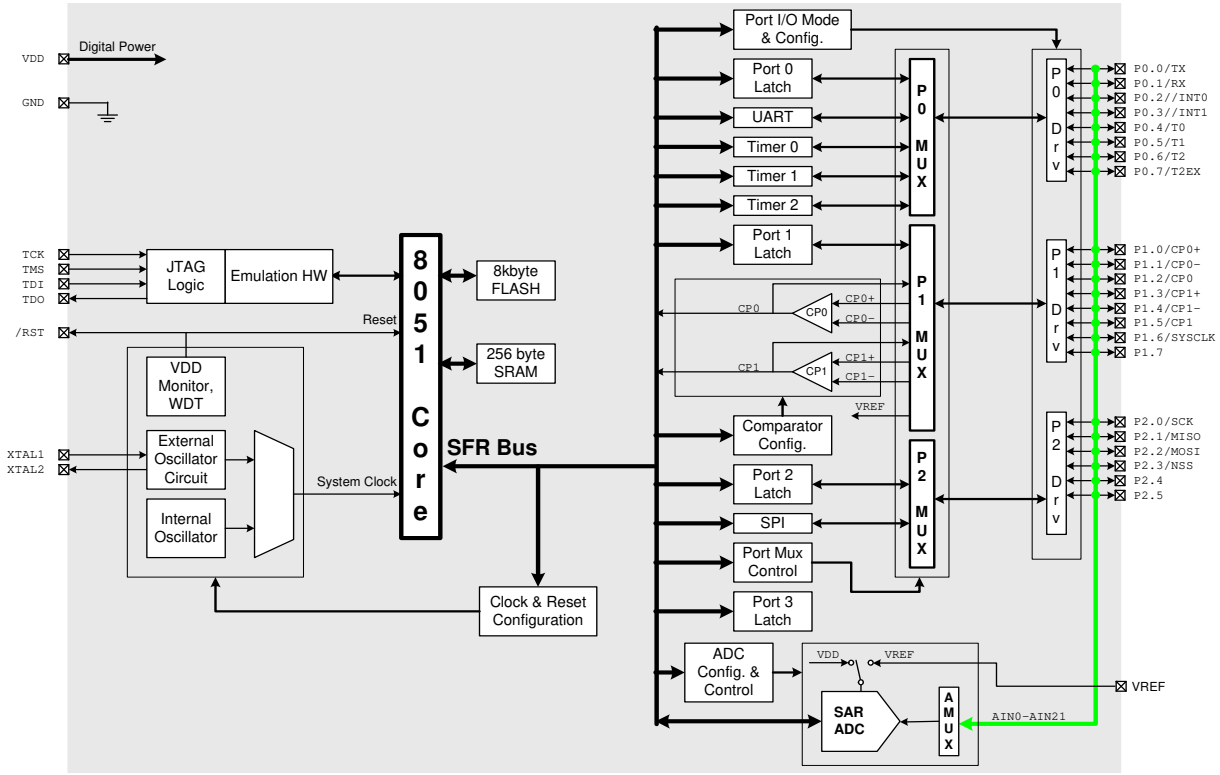

Figure 1.2. C8051F221 Block Diagram (32 LQFP)

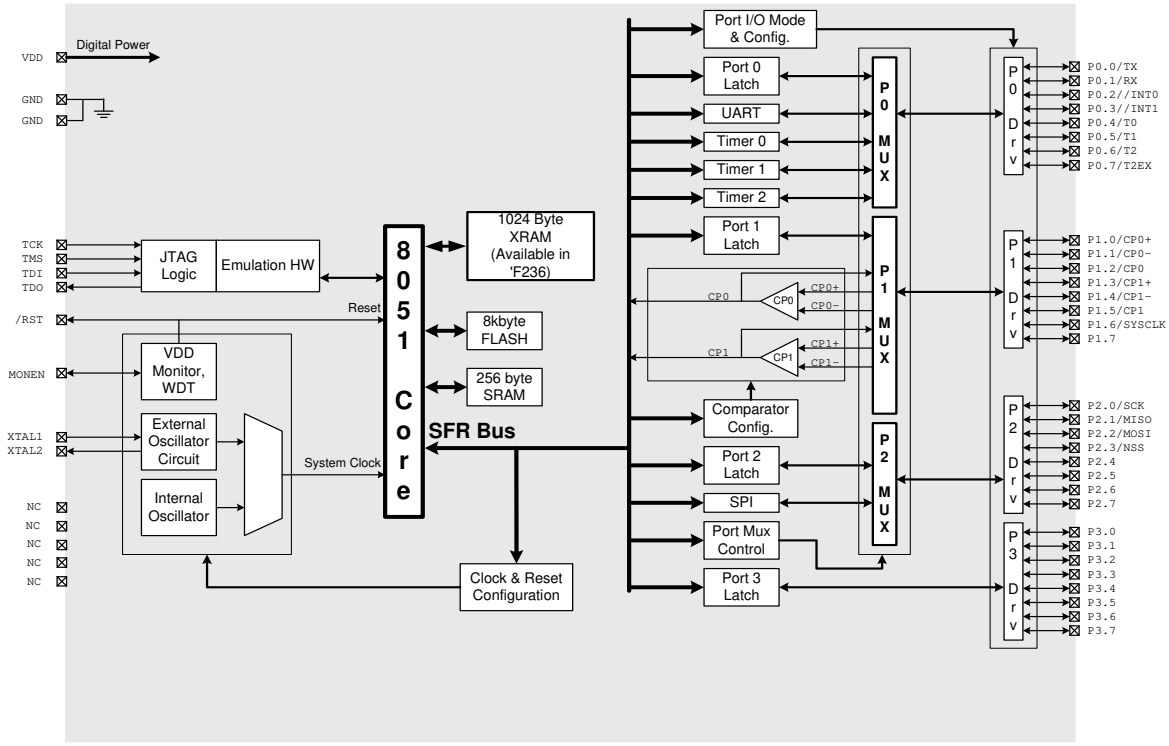

Figure 1.3. C8051F230 and C8051F236 Block Diagram (48 TQFP)

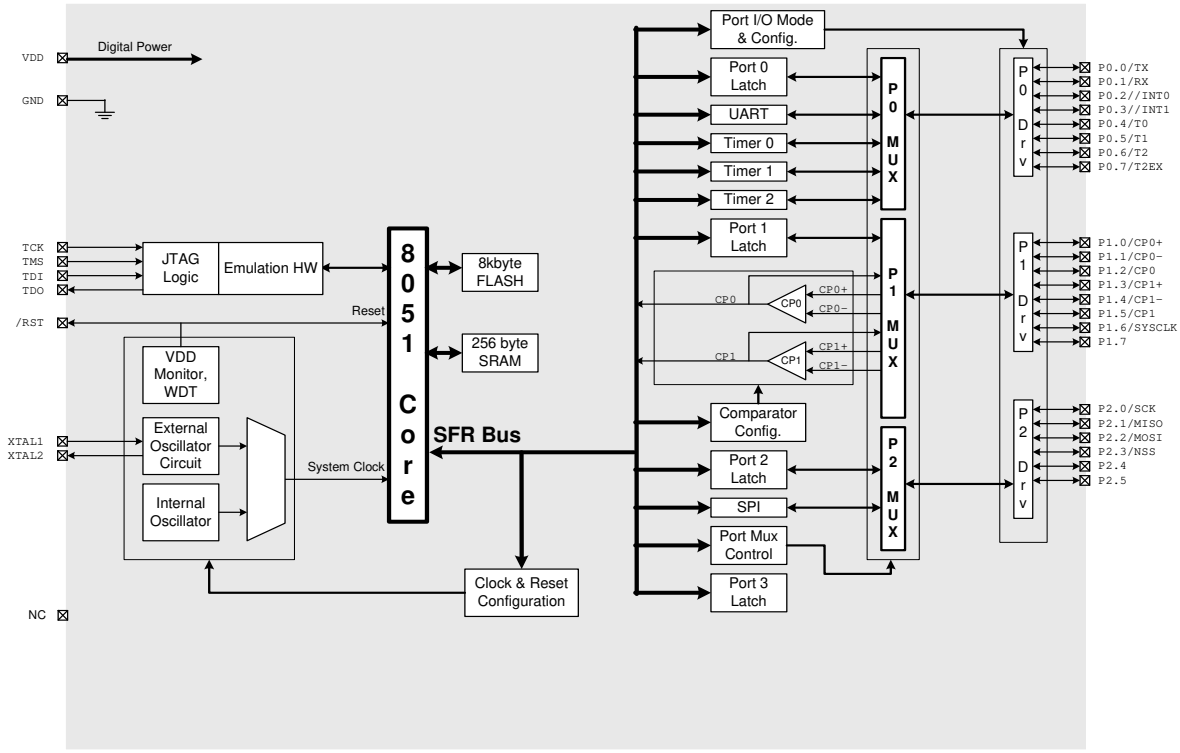

Figure 1.4. C8051F231 Block Diagram (32 LQFP)

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F206, C8051F220/1/6 and C8051F230/1/6 utilize Silcon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The core contains the peripherals included with a standard 8052, including three 16-bit counter/timers, a full-duplex UART, 256 bytes of internal RAM, an optional 1024 bytes of XRAM, 128 byte Special Function Register (SFR) address space, and four byte-wide I/O Ports.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The number of instructions versus the system clock cycles to execute them is as follows:

Instructions	26	50	5	14	7	3	1	2	1
Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

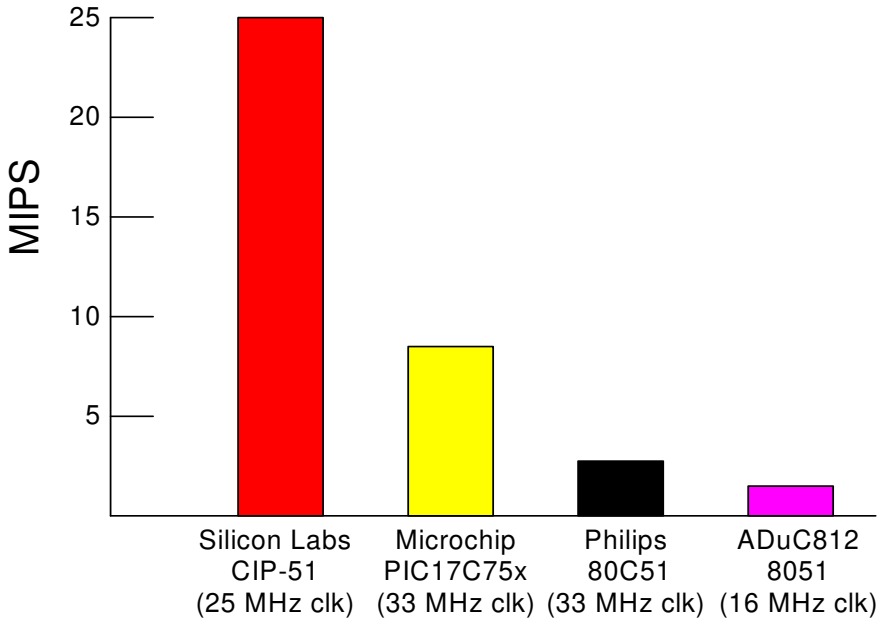

Figure 1.5. Comparison of Peak MCU Throughputs

1.1.3. Additional Features

The C8051F206, C8051F220/1/6 and C8051F230/1/6 have several key enhancements both inside and outside the CIP-51 core to improve overall performance and ease of use in end applications.

The extended interrupt handler provides 22 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing the numerous analog and digital peripherals to interrupt the controller. (An interrupt driven system requires less intervention by the MCU, giving it more effective throughput.) The extra interrupt sources are very useful when building multi-tasking, real-time systems.

There are up to six reset sources for the MCU: an on-board V_{DD} monitor, a Watchdog Timer, a missing clock detector, a voltage level detection from Comparator 0, a forced software reset, and an external reset pin. The $\overline{\text{RST}}$ pin is bi-directional, accommodating an external reset, or allowing the internally generated reset to be output on the $\overline{\text{RST}}$ pin. The on-board V_{DD} monitor is enabled by pulling the MONEN pin high (digital 1). The user may disable each reset source except for the V_{DD} monitor and Reset Input Pin from software. The watchdog timer may be permanently enabled in software after a power-on reset during MCU initialization.

The MCU has an internal, stand-alone clock generator that is used by default as the system clock after reset. If desired, the clock source may be switched "on the fly" to the external oscillator, which can use a crystal, ceramic resonator, capacitor, RC, or external clock source to generate the system clock. This can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the fast (up to 16MHz) internal oscillator as needed.

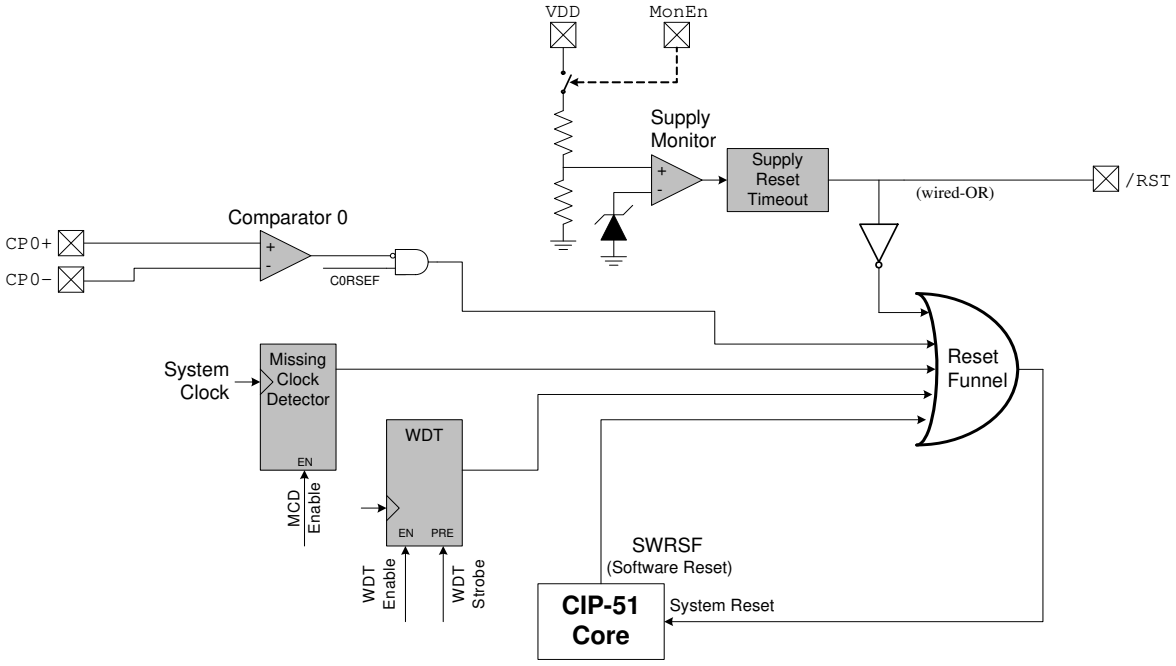

Figure 1.6. Comparison of Peak MCU Throughputs

1.2. On-Board Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. An optional 1024 bytes of XRAM is available on the 'F206, 'F226 and 'F236. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128-byte SFR address space. The lower 128 bytes of RAM are accessible via direct or indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

The MCU's program memory consists of 8 k + 128 bytes of Flash. This memory may be reprogrammed in-system in 512 byte sectors, and requires no special off-chip programming voltage. The 512 bytes from addresses 0x1E00 to 0x1FFF are reserved for factory use. There is also a user programmable 128-byte sector at address 0x2000 to 0x207F, which may be useful as a table for storing software constants, nonvolatile configuration information, or as additional program space. See Figure 1.7 for the MCU system memory map.

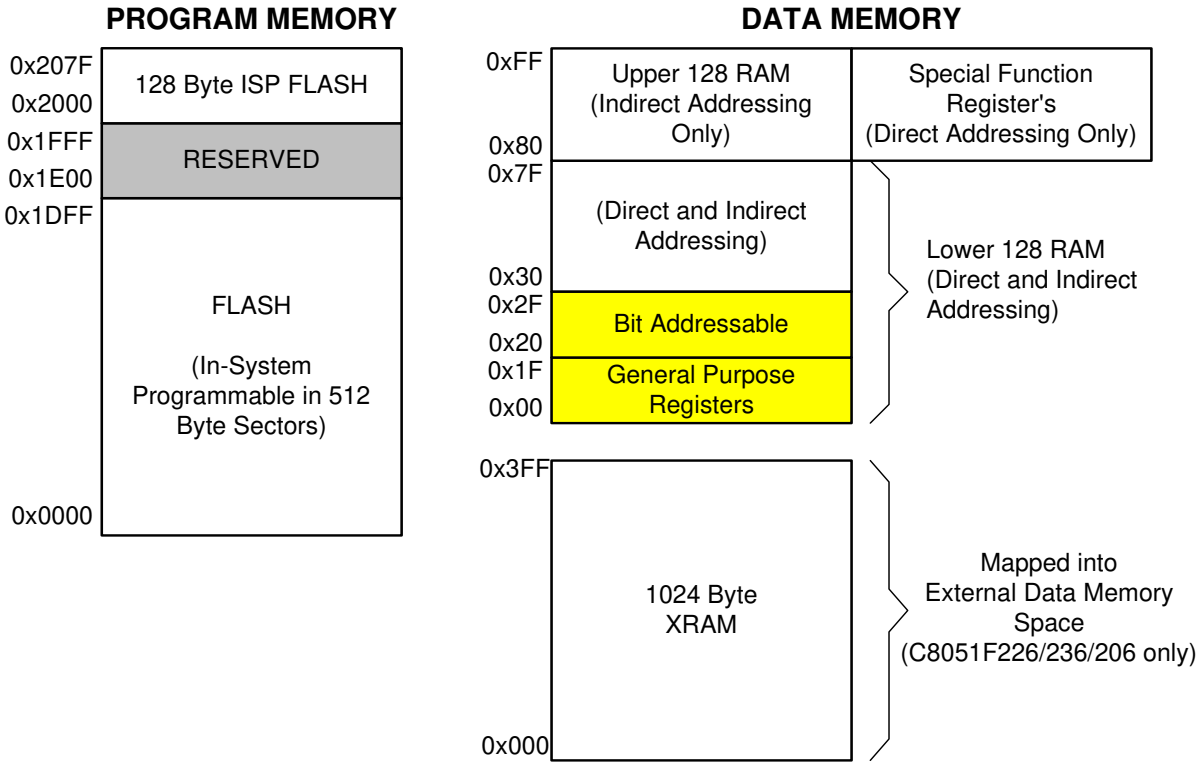

Figure 1.7. On-Board Memory Map

1.3. JTAG

The C8051F2xx have on-chip JTAG and debug logic that provide non-intrusive, full speed, in-circuit debug using the production part installed in the end application using the four-pin JTAG I/F. The C8051F2xxDK is a development kit with all the hardware and software necessary to develop application code and perform in-circuit debug with the C8051F2xx. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and an RS-232 to JTAG interface module referred to as the EC. It also has a target application board with a C8051F2xx installed and large prototyping area, plus the RS-232 and JTAG cables, and wall-mount power supply. The Development Kit requires a Windows OS (Windows 95 or later) computer with one available RS-232 serial port. As shown in Figure 1.8, the PC is connected via RS-232 to the EC. A six-inch ribbon cable connects the EC to the user's application board, picking up the four JTAG pins and V_{DD} and GND. The EC takes its power from the application board. It requires roughly 20 mA at 2.7–3.6 V. For applications where there is not sufficient power available from the target board, the provided power supply can be connected directly to the EC.

This is a vastly superior configuration for developing and debugging embedded applications compared to standard MCU Emulators, which use on-board "ICE Chips" and target cables and require the MCU in the application board to be socketed. Silicon Labs' debug environment both increases ease of use, and preserves the performance of the precision analog peripherals.

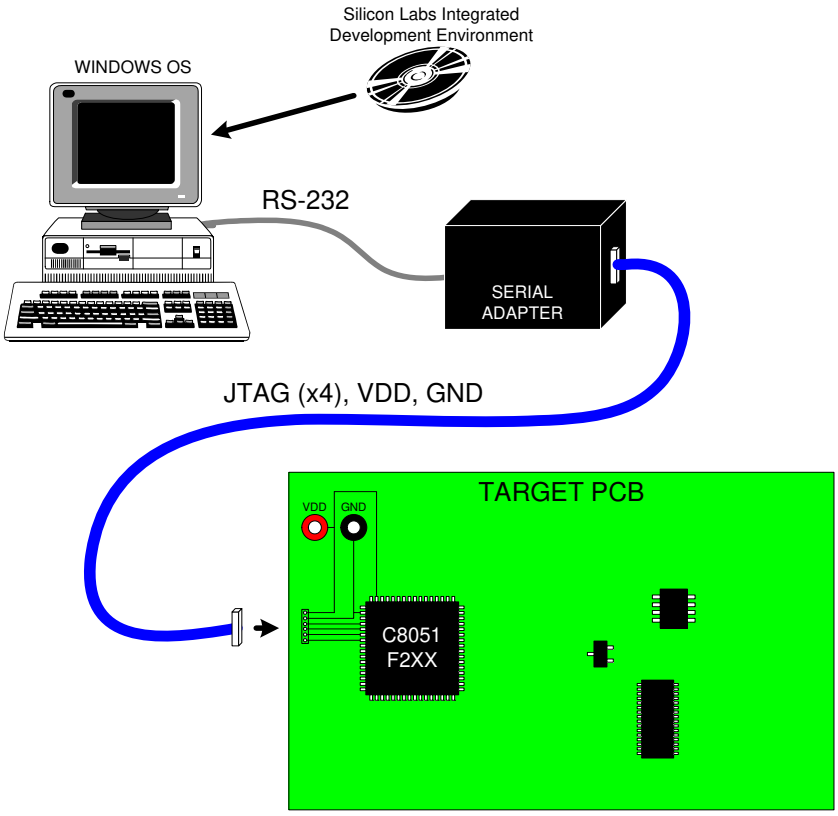

Figure 1.8. Degub Environment Diagram

1.4. Digital/Analog Configurable I/O

The standard 8051 Ports (0, 1, 2, and 3) are available on the device. The ports behave like standard 8051 ports with a few enhancements.

Each port pin can be configured as either a push-pull or open-drain output. Any input that is configured as an analog input will have its corresponding weak pull-up turned off.

Digital resources (timers, SPI, UART, system clock, and comparators) are routed to corresponding I/O pins by configuring the port multiplexer. Port multiplexers are programmed by setting bits in SFR's (please see Section 14). Any of the 32 external port pins may be configured as either analog inputs or digital I/O (See Figure 1.9), so effectively, all port pins are dual function.

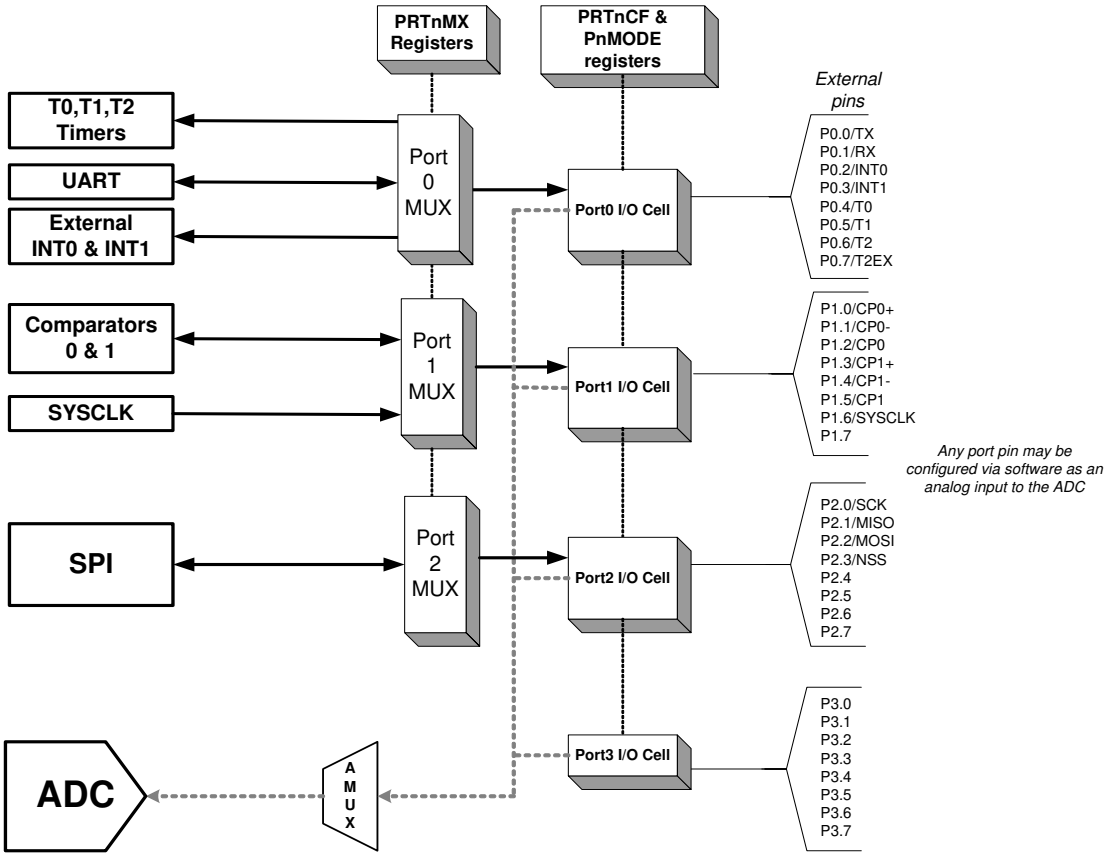

Figure 1.9. Port I/O Functional Block Diagram

1.5. Serial Ports

The C8051F206, C8051F220/1/6 and C8051F230/1/6 include a Full-Duplex UART and SPI Bus. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little intervention by the CPU. The serial buses do not have to "share" resources such as timers, interrupts, or Port I/O, so both of the serial buses may be used simultaneously. (You may use Timer1, Timer 2, or SYSCLK to generate baud rates for UART).

1.6. Analog to Digital Converter

The C8051F220/1/6 has an on-chip 8-bit SAR ADC and the C8051F206 has a 12-bit SAR ADC with a programmable gain amplifier. With a maximum throughput of 100ksps, the ADC offers true 8-bit with an INL of ±1/4 LSB, and or 12-bit accuracy with ±2 LSB. The voltage reference can be the power supply (V_{DD}), or an external reference voltage (VREF). Also, the system controller can place the ADC into a power-saving shutdown mode when not in use. A programmable gain amplifier follows the analog multiplexer. The gain can be set in software from 0.5 to 16 in powers of 2.

Conversions can be initiated in two ways; a software command or an overflow on Timer 2. This flexibility allows the start of conversion to be triggered by software events, or convert continuously. A completed conversion causes an interrupt, or a status bit can be polled in software to determine the end of conversion. The resulting 8-bit data word is latched into an SFR upon completion of a conversion.

ADC data is continuously monitored by a programmable window detector, which interrupts the CPU when data is within the user-programmed window. This allows the ADC to monitor key system voltages in background mode, without the use of CPU resources.

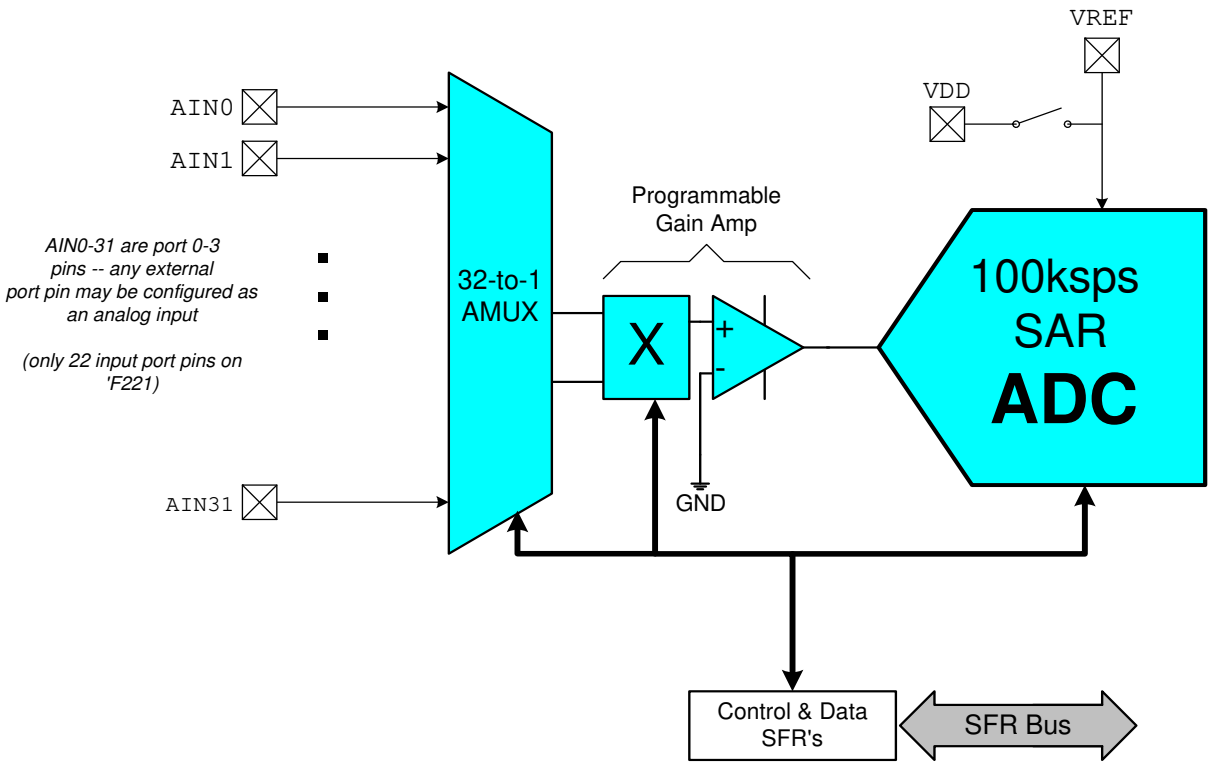

Figure 1.10. ADC Diagram

1.7. Comparators

The MCU's have two on-chip voltage comparators. The inputs of the comparators are available at package pins as illustrated in Figure 1.11. Each comparator's hysteresis is software programmable via special function registers (SFR's). Both voltage level and positive/negative going symmetry can be easily programmed by the user. Additionally, comparator interrupts can be implemented on either rising or falling-edge output transitions. Please see 8.‘Comparators” on page 52 for details.

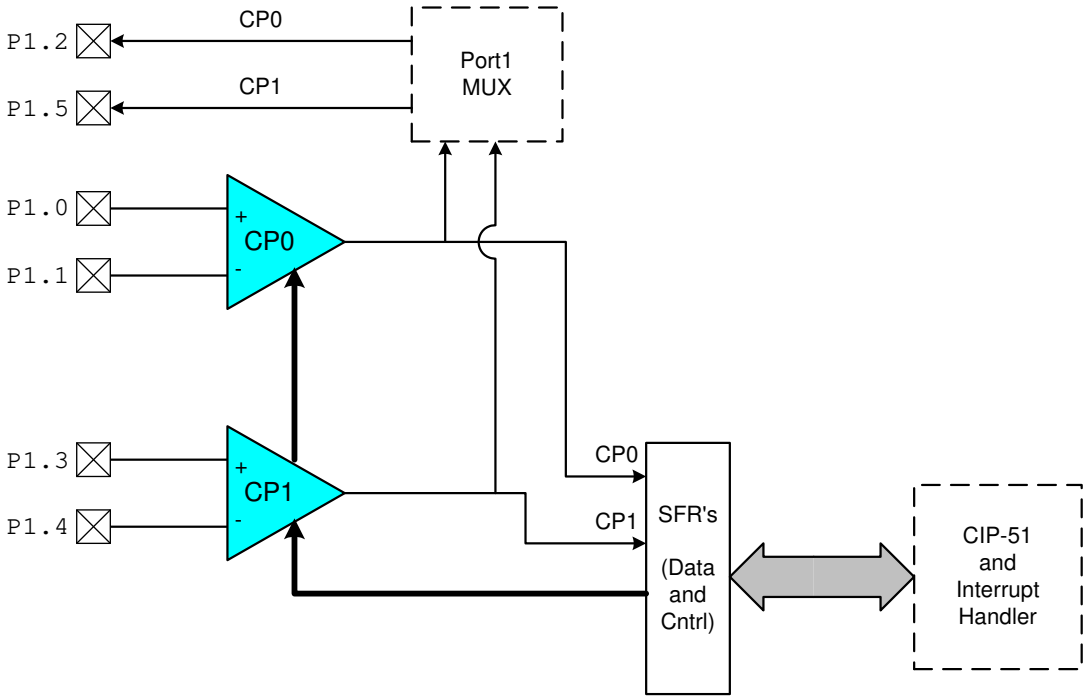

Figure 1.11. Comparator Diagram

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient Temperature under Bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Pin (except V_{DD} and Port I/O) with respect to DGND		–0.3	—	V_{DD} + 0.3	V
Voltage on any Port I/O Pin or $\overline{RST}$ pins with respect to DGND		–0.3	—	5.8	V
Voltage on V_{DD} with respect to DGND		–0.3		4.2	V
Total Power Dissipation		—	1.0	800	W
Maximum Output Current Sunk by any Port pin		—	—	200	mA
Maximum Output Current Sunk by any other I/O pin		—	—	25	mA
Maximum Output Current Sourced by any Port pin		—	—	200	mA
Maximum Output Current Sourced by any other I/O pin		—	—	25	mA

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

3. Global DC Electrical Characteristics

Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage[1]		2.7	3.0	3.6	V
V_{DD} supply current with ADC and comparators active, and CPU active	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	13 1.5 300	—	mA mA µA
V_{DD} supply current with ADC and comparators active, and CPU inactive (Idle Mode)	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	9 1.8 275	—	mA mA µA
V_{DD} supply current with ADC and comparators inactive, and CPU active	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	12.5 1.0 25	—	mA mA µA
Digital Supply Current with CPU inactive (Idle Mode)	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	8.5 1.4 25	—	mA mA µA
Digital Supply Current (Stop Mode), V_{DD} monitor enabled	Oscillator not running	—	10	—	µA
Digital Supply Current (Stop Mode), V_{DD} monitor disabled	Oscillator not running	—	0.1	—	µA
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
Specified Operating Temperature Range		–40	—	+85	°C
SYSCLK (system clock frequency)[2]		0	—	25	MHz
Tsysl (SYSCLK low time)		18	—	—	ns
Tsysh (SYSCLK high time)		18	—	—	ns

Notes:
1. Analog Supply AV+ must be greater than 1 V for V_{DD} monitor to operate.
2. SYSCLK must be at least 32 kHz to enable debugging.

4. Pinout and Package Definitions

Table 4.1. Pin Definitions

Name	'F206, F220, 226, 230, 236	'F221, 231	Type	Description
	48-Pin	32-Pin		
V_{DD}	11,31	8		Digital Voltage Supply.
GND	5,6,8, 13,32	9		Ground. (**Note:** Pins 5,6, and 8 on the 48-pin package are not connected (NC), but it is recommended that they be connected to ground.)
MONEN	12		D In	Monitor Enable (on 48 pin package ONLY). Enables reset voltage monitor function when pulled high (logic "1").
TCK	25	17	D In	JTAG Test Clock with internal pull-up.
TMS	26	18	D In	JTAG Test-Mode Select with internal pull-up.
TDI	28	20	D In	JTAG Test Data Input with internal pull-up. TDI is latched on a rising edge of TCK.
TDO	27	19	D Out	JTAG Test Data Output. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
XTAL1	9	6	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL2	10	7	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
$\overline{RST}$	14	10	D I/O	Chip Reset. Open-drain output of internal Voltage Supply monitor. Is driven low when V_{DD} is < 2.7V and MONEN=1, or when a '1'is written to PORSF. An external source can force a system reset by driving this pin low.
VREF	7	5	A I/O	Voltage Reference. When configured as an input, this pin is the voltage reference for the ADC. Otherwise, V_{DD} will be the reference. NOTE: this pin is Not Connected (NC) on 'F230/1/6.
CP0+	4	4	A In	Comparator 0 Non-Inverting Input.
CP0-	3	3	A In	Comparator 0 Inverting Input.
CP0	2	2	D Out	Comparator 0 Output
CP1+	1	1	A In	Comparator 1 Non-Inverting Input.
CP1-	48	32	A In	Comparator 1 Inverting Input.
CP1	47	31	D Out	Comparator 1 Output
P0.0/TX	40	28	D I/O A In	Port0 Bit0. (See the Port I/O Sub-System section for complete description).
P0.1/RX	39	27	D I/O A In	Port0 Bit1. (See the Port I/O Sub-System section for complete description).
P0.2/INT0	38	26	D I/O A In	Port0 Bit2. (See the Port I/O Sub-System section for complete description).